Am2901B/Am2901C

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- **Two-address architecture –**
  Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU –**
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Expandable –**
  Connect any number of Am2901s together for longer word lengths.
- **Left/right shift independent of ALU –**
  Add and shift operations take only one cycle.
- **Four status flags –**
  Carry, overflow, zero, and negative.
- **Flexible data source selection –**
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.

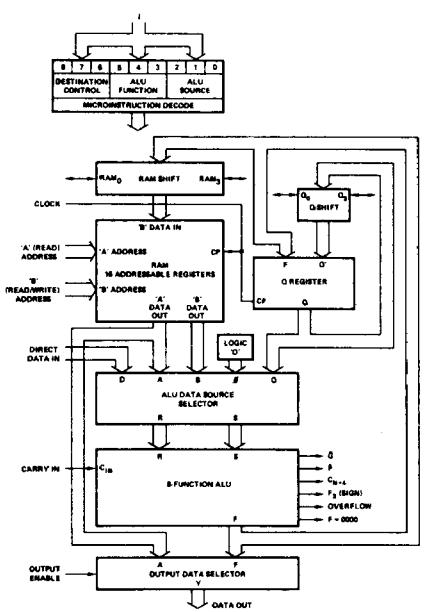
GENERAL DESCRIPTION

The Am2901 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the Am2901 permits efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. AMD's ion-implanted micro-oxide (IMOX) processing is used to fabricate the 40-lead LSI chip.

The Am2901C is a plug-in replacement for the Am2901B, but is 33% faster than the Am2901B.

MICROPROCESSOR SLICE BLOCK DIAGRAM



BD002120

IMOX is a trademark of Advanced Micro Devices.

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Refer to Page 13-1 for Essential Information on Military Devices

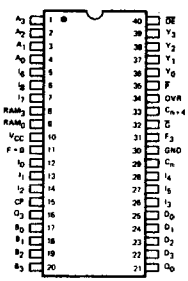
RELATED PRODUCTS

Part No.	Description
Am2902	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am27S35	Registered PROM

For applications information see Chapters III and IV of
Bit Slice Microprocessor Design,
by Mick and Brick, McGraw Hill Publishers.

CONNECTION DIAGRAM
Top View

P-40, D-40



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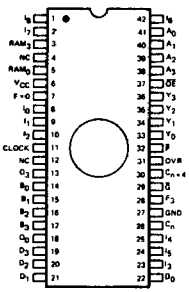

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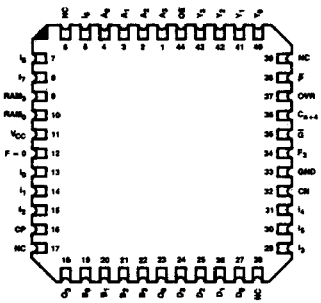

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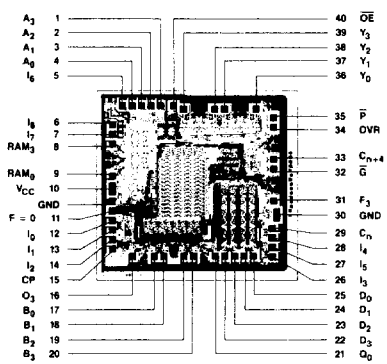
Note: Pin 1 is marked for orientation

Figure 1.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.130" x 0.123"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2901B
Am2901C

D — Package
- D – 40-pin CERDIP
- F – 42-pin flatpak
- L – 44-pin leadless chip carrier
- P – 40-pin plastic DIP
- X – Dice

C — Temperature (See Operating Range)
- C – Commercial (0°C to +70°C)
- M – Military (–55°C to +125°C)

B — Screening Option
- Blank – Standard processing
- B – Burn-in

Device type
Four-Bit Microprocessor Slice

Valid Combinations	
Am2901B	PC DC, DCB, DMB FMB XC, XM
Am2901C	PC DC, DCB, DMB FMB LC, LMB XC, XM

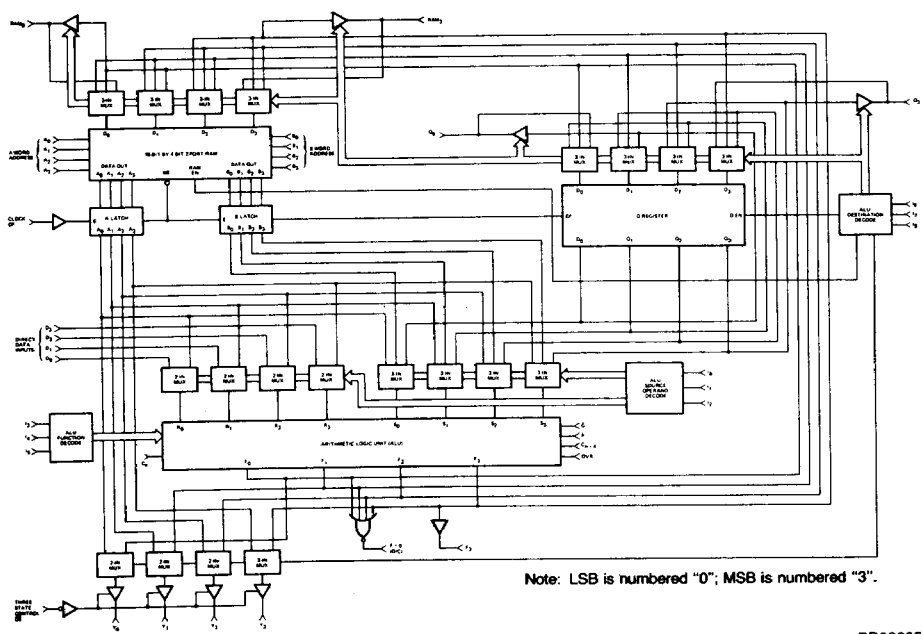
Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 3, 2, 1	A_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.
17, 18 19, 20	B_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.
	I_{0-8}	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).
16	Q_3 RAM_3	I/O	A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are electrically OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).
21, 9	Q_0 RAM_0	I/O	Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.
25, 24 23, 22	D_{0-3}	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.
36, 37 38, 39	Y_{0-3}	O	The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.
40	$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).
32, 35	$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.
34	OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
11	F = 0	O	This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.
31	F_3	O	The most significant ALU output bit.
29	C_n	I	The carry-in to the internal ALU.
33	C_{n+4}	O	The carry-out of the internal ALU.
15	CP	I	The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

DETAILED Am2901C MICROPROCESSOR BLOCK DIAGRAM



Note: LSB is numbered "0"; MSB is numbered "3".

BD002050

Figure 2.

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Refer to Page 13-1 for Essential Information on Military Devices

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 2, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 3. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 4. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 5.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 12 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 5.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 5.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 3. ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \triangledown S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Figure 4. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 5. ALU Destination Control.

OCTAL I_{543}	ALU Function	I_{210}OCTAL							
		0	1	2	3	4	5	6	7
		ALU Source							
		A,Q	A,B	0,Q	0,B	O,A	D,A	D,Q	D,0
0	$C_n = L$ R Plus S $C_n = H$	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	$C_n = L$ S Minus R $C_n = H$	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	−D − 1 −D
2	$C_n = L$ R Minus S $C_n = H$	A − Q − 1 A − Q	A − B − 1 A − B	−Q − 1 −Q	−B − 1 −B	−A − 1 −A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \triangledown Q$	$A \triangledown B$	Q	B	A	$D \triangledown A$	$D \triangledown Q$	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∇ = EX-OR

Figure 6. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 6 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 7 defines the various logic operations that the Am2901 can perform and Figure 8 shows the arithmetic functions of the device. Both carry-in LOW ($C_n = 0$) and carry-in HIGH ($C_n = 1$) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	AvQ
3 1		AvB
3 5		DvA
3 6		DvQ
6 0	EX-OR	A∇Q
6 1		A∇B
6 5		D∇A
6 6		D∇Q
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 7. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp)	Q - A - 1	Subtract (2's Comp)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Figure 8. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 3.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \nabla C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R∨S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R∧S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$∧S	LOW	← Same as R∧S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R∇S	← Same as $R \nabla S$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \nabla S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$	See note

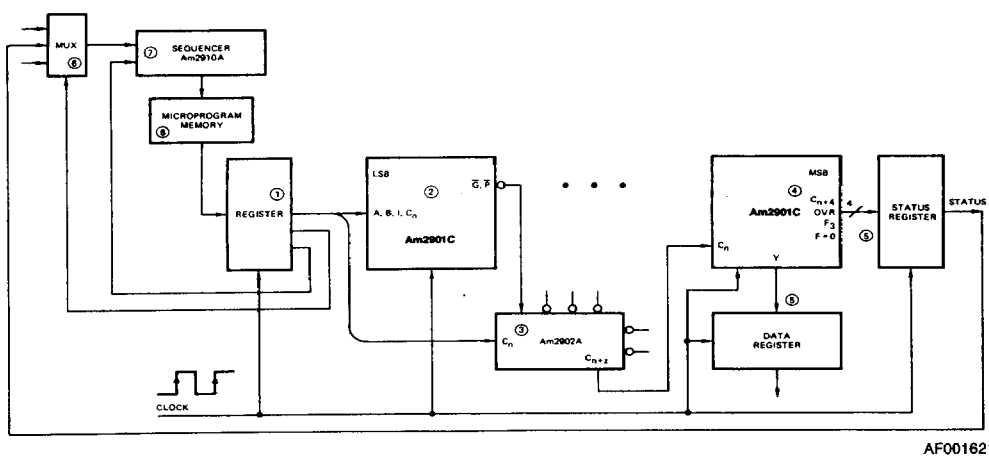
Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \nabla$
$[\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

+ = OR

Figure 9.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901C are representative for available MSI parts.



AF001621

Pipelined System. Add without Simultaneous Shift.

DATA LOOP

①Register	Clock to Output	9
+ ②2901C	A, B to $\overline{G}$, $\overline{P}$	37
+ ③2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7
+ ④2901C	C_n to C_{n+4}, OVR, F_3, F = 0, Y	25
+ ⑤Register	Setup Time	2
		80ns

CONTROL LOOP

①Register	Clock to Output	9
+ ⑥MUX	Select to Output	13
+ ⑦2910A	CC to Output	30
+ ⑧PROM	Access Time	40
+ ①Register	Setup Time	2
		94ns

Minimum clock period = 94ns

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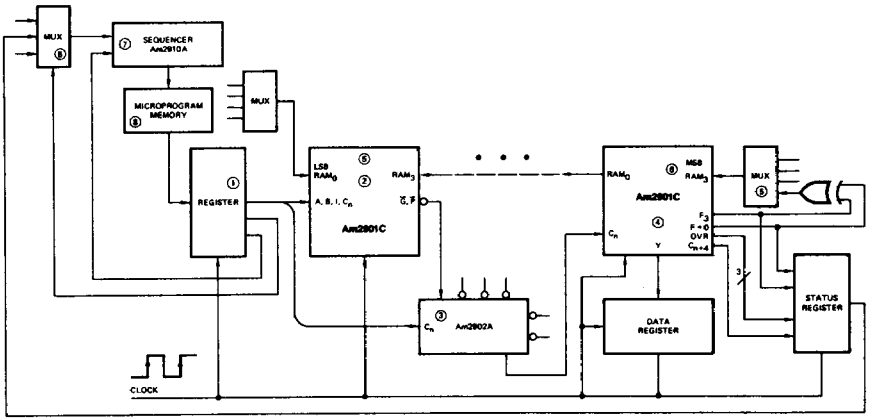
Refer to Page 13-1 for Essential Information on Military Devices



AF001631

Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP		
①Register	Clock to Output	9
+ ②2901C	A, B to $\overline{G}$,$\overline{P}$	37
+ ③2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7
+ ④2901C	C_n to F_3, OVR	22
+ ⑤XOR and MUX		21
+ ⑥2901C	RAM_3 Setup	12
		108ns

CONTROL LOOP		
①Register	Clock to Output	9
+ ⑧MUX	Select to Output	13
+ ⑦2910A	CC to Output	30
+ ⑥PROM	Access Time	40
+ ①Register	Setup Time	2
		94ns

Minimum clock period = 108ns

Figure 10.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0 Y_1, Y_2, Y_3	2.4		Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4		
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4		
				I_{OH} = −600μA, F_3	2.4		
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4		
				I_{OH} = −1.6mA, $\overline{G}$	2.4		
I_{CEX}	Output Leakage Current For F = 0 Output	V_{CC} = MIN, V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L) (Note 4)		0.5	
				I_{OL} = 16mA (MIL) (Note 4)		0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA		0.5	
			C_{n+4}	I_{OL} = 10mA		0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA		0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		Clock, $\overline{OE}$		−0.36	mA
				A_0, A_1, A_2, A_3		−0.36	
				B_0, B_1, B_2, B_3		−0.36	
				D_0, D_1, D_2, D_3		−0.72	
				I_0, I_1, I_2, I_6, I_8		−0.36	
				I_3, I_4, I_5, I_7		−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 3)		−0.8	
				C_n		−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		Clock, $\overline{OE}$		20	μA
				A_0, A_1, A_2, A_3		20	
				B_0, B_1, B_2, B_3		20	
				D_0, D_1, D_2, D_3		40	
				I_0, I_1, I_2, I_6, I_8		20	
				I_3, I_4, I_5, I_7		40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 3)		100	
				C_n		200	

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters	Description	Test Conditions (Note 1)				Min	Max	Units
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX		Y_0, Y_1, Y_2, Y_3	V_O = 2.4V		50	µA
					V_O = 0.5V		−50	
				$RAM_{0, 3}$ $Q_{0, 3}$	V_O = 2.4V (Note 3)		100	
					V_O = 0.5V (Note 3)		−800	
I_{OS}	Output Short Circuit Current (Note 2)	V_{CC} = MAX + 0.5V, V_O = 0.5V		Y_0, Y_1, Y_2, Y_3, $\overline{G}$		−30	−85	mA
				C_{n+4}		−30	−85	
				OVR, $\overline{P}$		−30	−85	
				F_3		−30	−85	
				$RAM_{0, 3}$, $Q_{0, 3}$		−30	−85	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	COM'L Only (Note 4)	T_A = 0°C to +70°C			265	mA
				T_A = +70°C			220	
			MIL Only (Note 4)	T_C = −55°C to+ 125°C			280	
				T_C = +125°C			198	

Note:
1. V_{CC} conditions shown as MIN or MAX, refer to the military (±10%) or commercial (±5%) V_{CC} limits.
2. Not more than one output should be stored at a time. Duration of the short circuit test should not exceed one second.
3. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
4. "MIL" = Am2901CXM, DM, FM, LM, "COM'L" = Am2901CXC, PC, DC, LC.
5. Worst case I_{CC} is measured at the lowest temperature in the specified operating range.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment, (not functionally tested).

I. Am2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns. with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC Am2901BDC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle. I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	35	35
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ⎍	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change (Note 2)		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It indicates all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

II. Am2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	88ns
Maximum Clock Frequency to shift Q (50% duty cycle. I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	65	55	58	–
I345	58	58	58	48	64	56	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ⎍	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	CP: **Set-up Time Before H →L**	**Hold Time After H →L**	**Set-up Time Before L →H**	**Hold Time After L →H**
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change (Note 2)		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	62	0
I678	14	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	40	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

III. Am2901C Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901C over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CPC
Am2901CDC
Am2901CLC

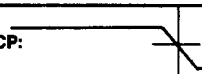
A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	31ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	31ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	40	40	40	37	40	40	40	–
D	30	30	30	30	38	30	30	–
Cn	22	22	20	–	25	22	25	–
I012	35	35	35	37	37	35	35	–
I345	35	35	35	35	38	35	35	–
I678	25	–	–	–	–	–	26	26
A Bypass ALU (I = 2XX)	35	–	–	–	–	–	–	–
Clock ⎍	35	35	35	35	35	35	35	28

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	CP:  **Set-up Time Before H →L**	**Hold Time After H →L**	**Set-up Time Before L →H**	**Hold Time After L →H**
A, B Source Address	15	1 (Note 3)	30, 15 + T_{PWL} (Note 4)	1
B Destination Address	15	Do Not Change (Note 2)		1
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	12	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	23	23

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

IV. Am2901C Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901C over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CDM
Am2901CFM
Am2901CLM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	32ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	32ns

B. Combinational Propagation Delays. (Note 1)
C_L = 50pF

	To Output							
From Input	**Y**	**F3**	**Cn+4**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM0 RAM3**	**Q0 Q3**
A, B Address	48	48	48	44	48	48	48	–
D	37	37	37	34	40	37	37	–
Cn	25	25	21	–	28	25	28	–
I012	40	40	40	44	44	40	40	–
I345	40	40	40	40	40	40	40	–
I678	29	–	–	–	–	–	29	29
A Bypass ALU (I = 2XX)	40	–	–	–	–	–	–	–
Clock ⌐	40	40	40	40	40	40	40	33

C. Set-up and Hold Times Relative to Clock (CP) Input. (Note 1)

Input	CP: **Set-up Time Before H → L**	**Hold Time After H → L**	**Set-up Time Before L → H**	**Hold Time After L → H**
A, B Source Address	15	2 (Note 3)	30, 15 + T_{PWL} (Note 4)	2
B Destination Address	15	Do Not Change (Note 2)		2
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change (Note 2)		0
RAM0, 3, Q0, 3	–	–	12	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y	25	25

NOTES:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

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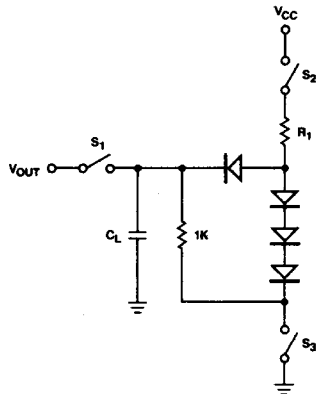
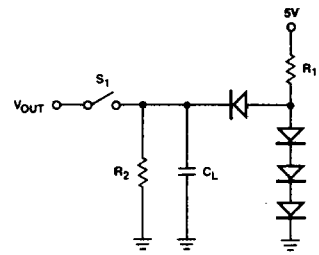
SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



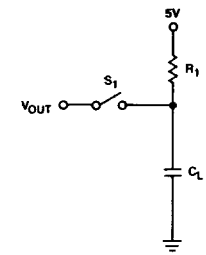
TC001100

B. NORMAL OUTPUTS



TC001080

C. OPEN-COLLECTOR OUTPUTS



TC001090

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

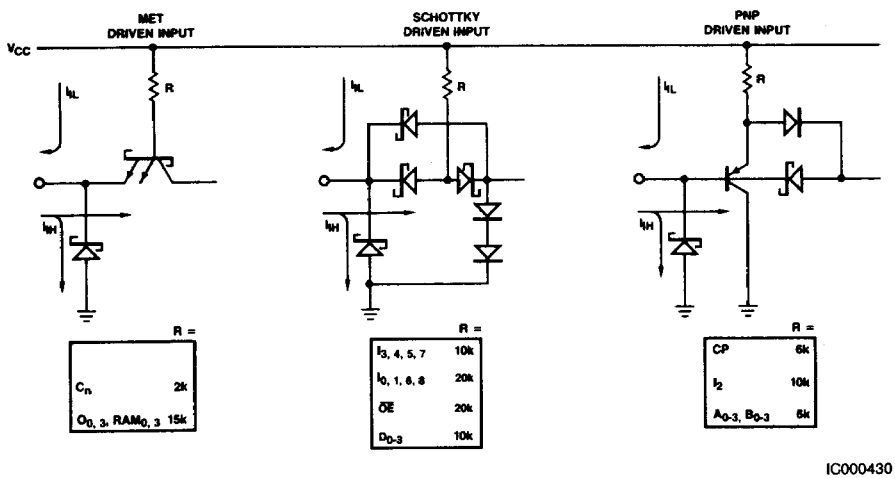
$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L=5.0pF for output disable tests.

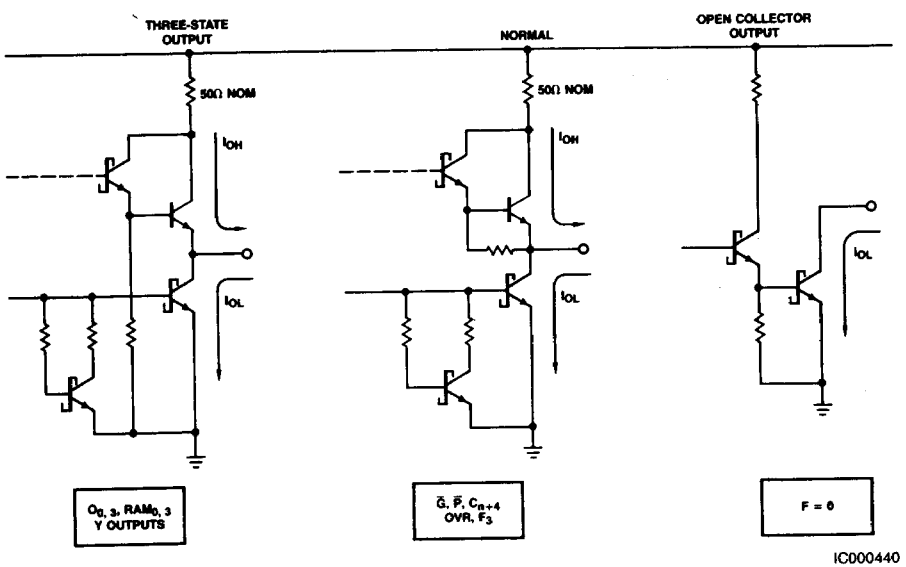
TEST OUTPUT LOADS FOR Am2901C (DIP)

Pin #	Pin Label	Test Circuit	R_1	R_2
8	RAM_3	A	560	1K
9	RAM_0	A	560	1K
11	F = 0	C	270	–
16	Q_3	A	560	1K
21	Q_0	A	560	1K
31	F_3	B	620	3.9K
32	G	B	220	1.5K
33	C_{n+4}	B	360	2.4K
34	OVR	B	470	3K
35	P	B	470	3K
36-39	Y_{0-3}	A	220	1K

TTL INPUT/OUTPUT CURRENT INTERFACES



$C_I \cong 5.0pF$, all inputs



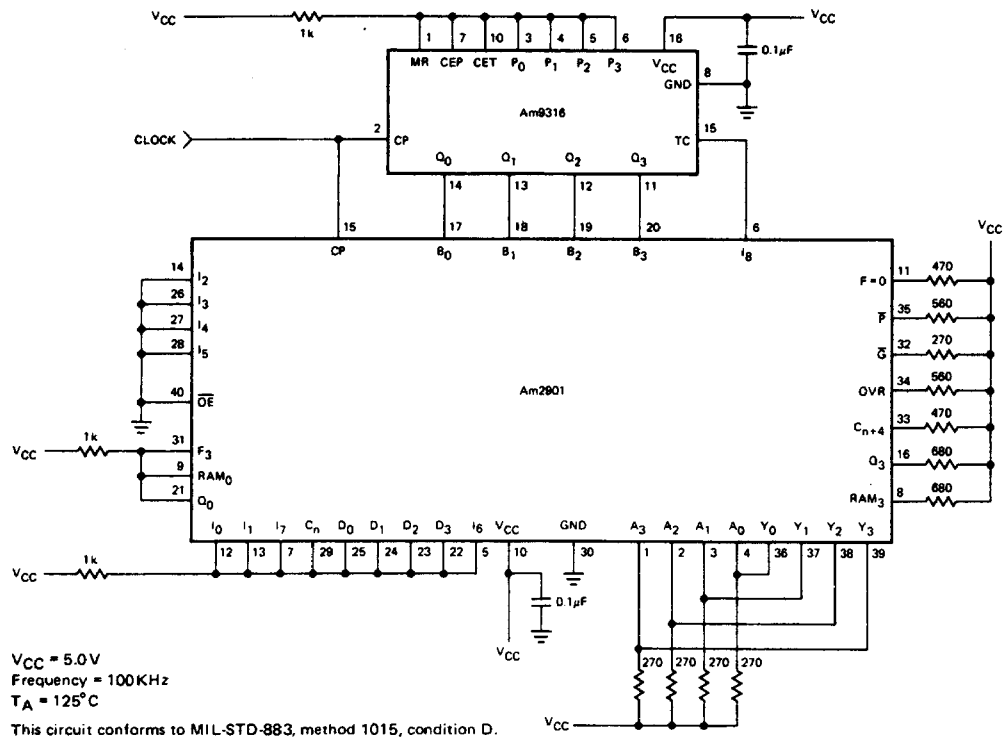
$C_O \cong 5.0pF$, all outputs

Figure 11.

01656B

Refer to Page 13-1 for Essential Information on Military Devices

LIFE TEST AND BURN-IN CIRCUIT FOR MILITARY CLASS B PARTS.



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(Contact Factory for Commercial Burn-in Conditions)

Figure 12.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

For additional information on testing, see section
"Guidelines on Testing Am2900 Family Devices"
in the Bipolar Microprocessor Logic and Interface Data Book.