AM26C31-EP
QUADRUPLE DIFFERENTIAL LINE DRIVER

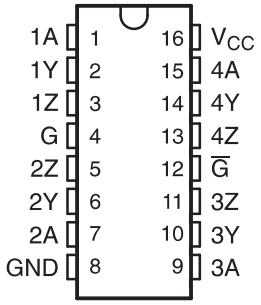
SLLS871–NOVEMBER 2007

FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Meets or Exceeds the Requirements of TIA/EIA-422-B and ITU Recommendation V.11**
- **Low Power, I_{CC} = 100 μA Typ**
- **Operates From a Single 5 V Supply**
- **High Speed, $t_{PLH} = t_{PHL}$ = 7 ns Typ**
- **Low Pulse Distortion, $t_{sk(p)}$ = 0.5 ns Typ**
- **High Output Impedance in Power-Off Conditions**
- **Improved Replacement for AM26LS31**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

AM26C31... D PACKAGE



DESCRIPTION/ORDERING INFORMATION

The AM26C31 is a differential line driver with complementary outputs, designed to meet the requirements of TIA/EIA -422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable functions are common to all four drivers and offer the choice of an active-high (G) or active-low ($\overline{G}$) enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

The AM26C31 is characterized for operation over extended temperature range of –55°C to 125°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	AM26C31MDREP	26C31EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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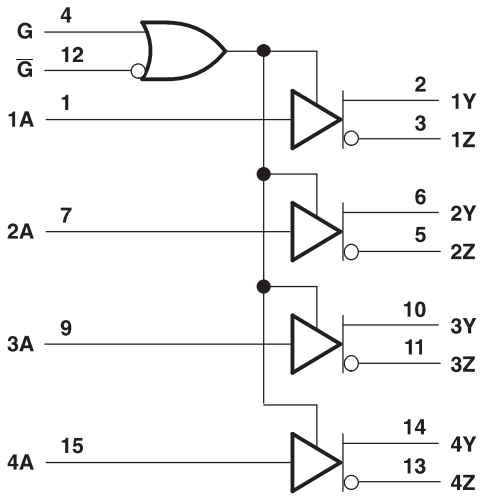
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

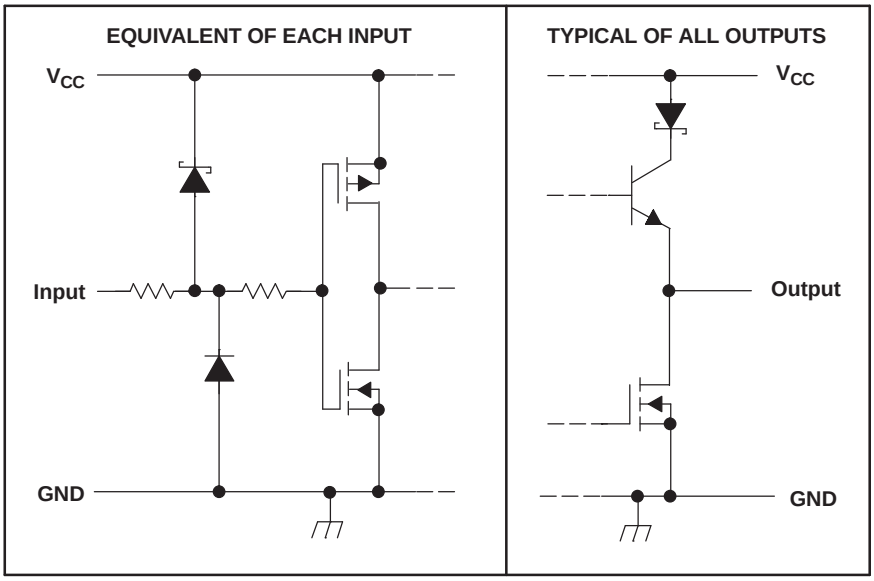
FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUT	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS AND OUTPUTS



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)	–0.5	7	V
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
V_{ID}	Differential input voltage range	–14	14	V
V_O	Output voltage range	–0.5	7	V
I_{IK} or I_{OK}	Input or output clamp current		±20	mA
I_O	Output current		±150	mA
	V_{CC} current		200	mA
	GND current		–200	mA
θ_{JA}	Package thermal impedance(3)(4)		73	°C/W
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage (V_{OD}), are with respect to the network ground terminal.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{ID}	Differential input voltage		±7		V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–20	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	–55		125	°C

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ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_O = –20 mA		2.2	3.4		V
V_{OL}	Low-level output voltage	I_O = 20 mA			0.2	0.4	V
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 1		2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(2)	R_L = 100 Ω, See Figure 1				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω, See Figure 1				3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)	R_L = 100 Ω, See Figure 1				±0.4	V
I_I	Input current	V_I = V_{CC} or GND				±1	µA
$I_{O(off)}$	Driver output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = –0.25 V			–100	
I_{OS}	Driver output short-circuit current	V_O = 0				–170	mA
I_{OZ}	High-impedance off-state output current	V_O = 2.5 V				20	µA
		V_O = 0.5 V				–20	
I_{CC}	Quiescent supply current	I_O = 0	V_I = 0 V or 5 V			100	µA
		I_O = 0	V_I = 2.4 V or 0.5 V(3)			3.2	mA
C_I	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) This parameter is measured per input. All other inputs are at 0 V or 5 V.

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2		7	12	ns
t_{PHL}	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2		6.5	12	ns
$t_{sk(p)}$	Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)	S1 is open,	See Figure 2		0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
t_{PZH}	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level	S1 is closed,	See Figure 4		10	19	ns
t_{PHZ}	Output disable time from high level	S1 is closed,	See Figure 4		7	16	ns
t_{PLZ}	Output disable time from low level	S1 is closed,	See Figure 4		7	16	ns
C_{pd}	Power dissipation capacitance (each driver)(2)	S1 is open,	See Figure 2		100		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}^2 \times f$, where f is the switching frequency.

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PARAMETER MEASUREMENT INFORMATION

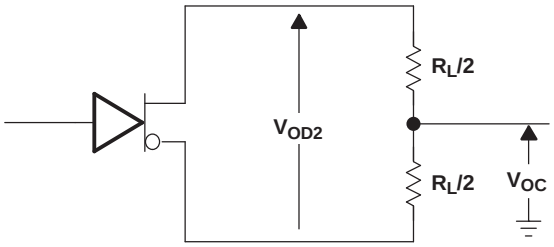
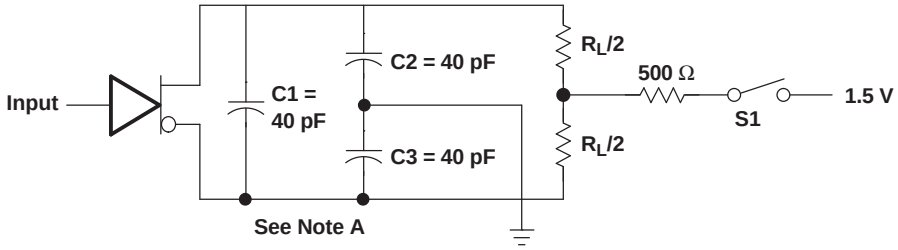
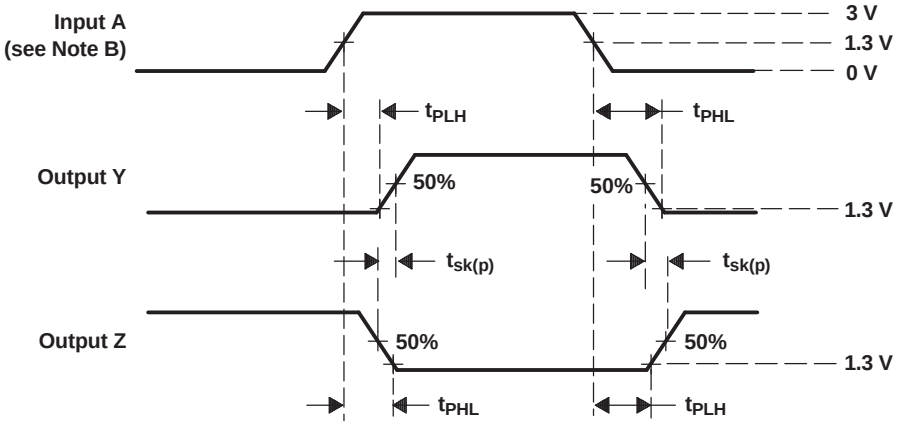


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT



A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6 ns.

Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit

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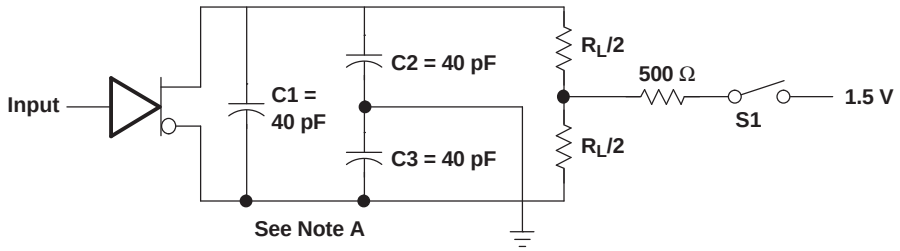
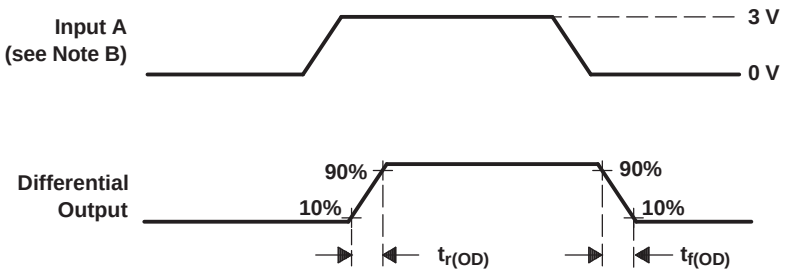
PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6 ns.

Figure 3. Differential Output Rise and Fall Time Waveforms and Test Circuit

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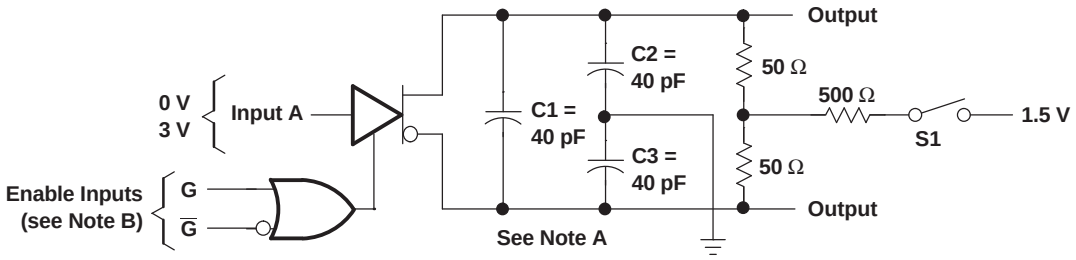
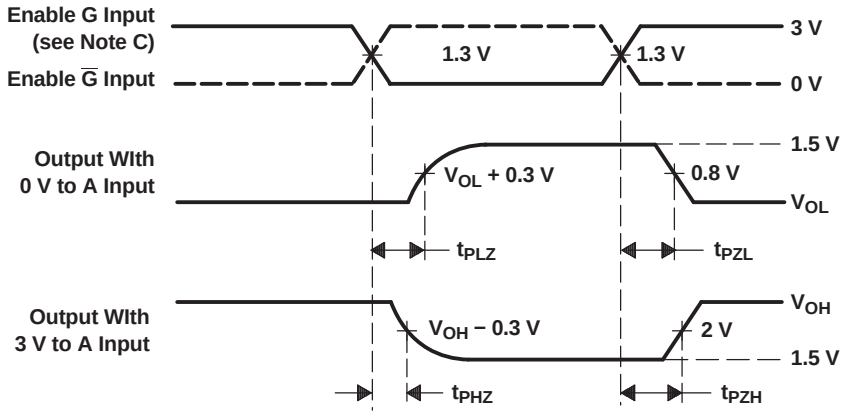
PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r < 6 ns, and t_f < 6 ns.

C. Each enable is tested separately.

Figure 4. Output Enable and Disable Time Waveforms and Test Circuit

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TYPICAL CHARACTERISTICS

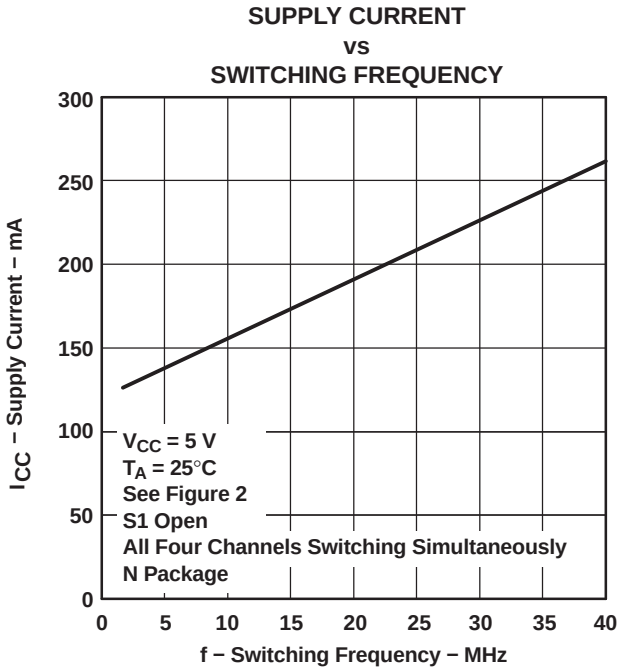

Figure 5.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
AM26C31MDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP	Samples
V62/07647-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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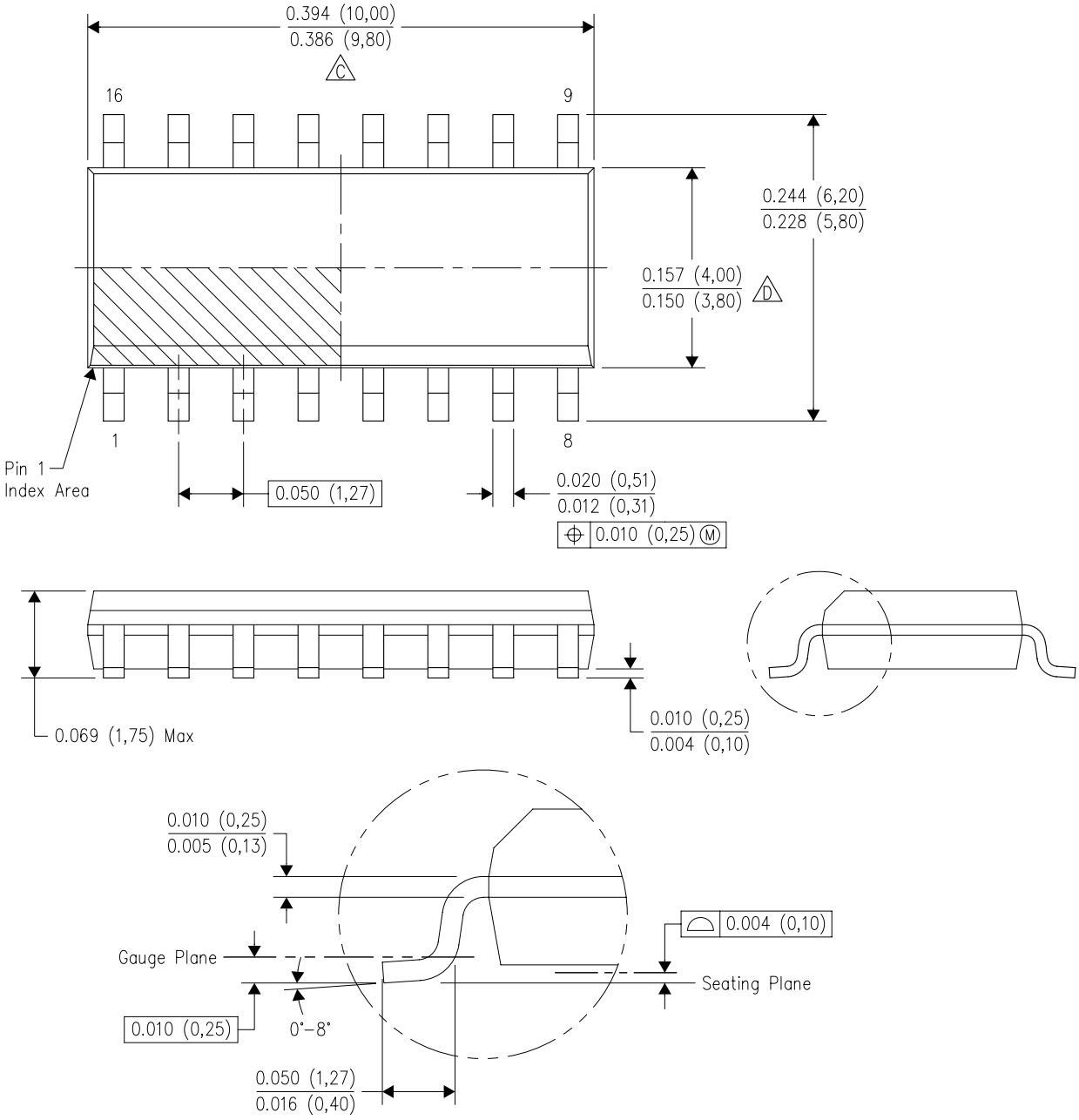
OTHER QUALIFIED VERSIONS OF AM26C31-EP :

- Catalog: AM26C31
- Military: AM26C31M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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