ALM-42316

(3.3 – 5)V Linear Wireless Data Power Amplifier for (3.3 - 3.8)GHz Operation

Data Sheet

Description

Avago Technologies' ALM-42316 is a fully-matched Power amplifier module for use in the (3.3-3.8)GHz band. High linear output power at 3.3V is achieved through the use of Avago Technologies' proprietary 0.25um GaAs Enhancement-mode pHEMT process. It is housed in a miniature 5.0 x 5.0 x 1.1mm MCOB module. It includes shutdown and switchable gain functions. A detector is also included on-chip. The compact footprint and low profile coupled with high gain and high efficiency make the ALM-42316 an ideal choice as a power amplifier for IEEE 802.16 (Wimax) and WLL applications.

Applications

- High linearity amplifier for IEEE 802.16 mobile and fixed terminal amplifier
- WLL amplifier

Component Image

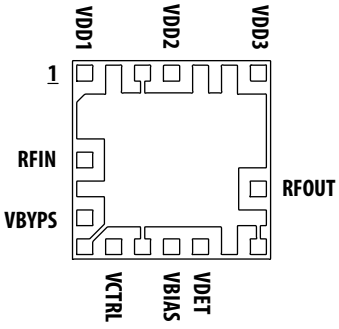
5.0 x 5.0 x 1.1 mm^3 MCOB



TOP VIEW

Notes:
Package marking provides orientation and identification
"42316" = Device Part Number
"WWYY" = Work week and Year
"XXXX" = Assembly lot number

Pin Configuration



TOP VIEW

Features

- High Efficiency of 14.5% at low 3.3V supply voltage
- High gain : 30dB
- High linearity performance : 23dBm at 2.5% EVM (64 QAM ¾ FEC rate OFDMA).
- Broadband Fully-matched 50 Ohm input and output impedances
- 45dBc 2nd harmonic attenuation
- Built-in detector and shutdown switches
- Switchable gain : 18 dB attenuation using one single CMOS compatible switch pin
- GaAs E-pHEMT Technology[1]
- Low cost small package size: 5.0 x 5.0 x 1.1 mm^3
- Useable at 5V supplies for higher output power

Specifications

3.5GHz; 3.3V, Iqtotal=240 mA (typ)

- 30 dB Gain
- 23dBm linear Pout (2.5% EVM, 64QAM OFDMA)
- 24.5dBm linear Pout (2.5% EVM, 64QAM OFDMA) @ Vdd=5V
- P1dB : 30.5dBm
- Detector range : 10dB (0.3V – 2.0V)
- 18 dB switchable gain attenuation
- Shutdown current : < 20uA

Notes:
1. Enhancement mode technology employs positive Vgs, thereby eliminating the need of negative gate voltage associated with conventional depletion mode devices.



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 40 V
ESD Human Body Model = 250 V
Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

Absolute Maximum Rating [1] T_A=25°C

Symbol	Parameter	Units	Absolute Max.
Vdd, Vddbias	Supply voltages, bias supply voltage	V	5.5
Vc	Control Voltage	V	(Vdd)
$P_{in,max}$	CW RF Input Power	dBm	+12
P_{diss}	Total Power Dissipation [3]	W	4.4
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance [2,3] (V_{dd} = 3.3V, Id=240mA), θjc = 28 °C/W

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. Board temperature (TB) is 25 °C , for TB >25 °C derate the device power at 30mW per °C rise in Board (package belly) temperature.

Electrical Specifications

T_A = 25 °C, Vdd =3.3V, Iqtotal = 240mA, RF performance at 3.5 GHz, IEEE 802.16e 64-QAM, ¾ rate FEC, OFDMA operation unless otherwise stated. Vbyp = 0V.

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
Vdd	Supply Voltage			3.3	
Iqtotal	Quiescent Supply Current (normal high gain mode) [5]	mA		240	
	Quiescent Supply Current (bypass mode, Vbyp = 3.3V)	mA		200	
freq	Input Frequency Range	GHz	3.3		3.8
Vc	Control voltage required for Iqtotal=240mA	V	1.6	2	2.5
Gain	Gain	dB	27.5	29.7	
OP1dB	Output Power at 1dB Gain Compression	dBm		30.5	
Plin	Linear Output power at 2.5%EVM (normal gain mode)	dBm	21.5	23	
Ilintotal	Total current draw at Plin level [4]	mA		417	490
S11	Input Return Loss, 50Ω source	dB		-15	
S22	Output Return Loss, 50Ω load	dB		-11	
S12	Reverse Isolation	dB		45	
2Fc	Second harmonic attenuation	dBc		45	
Atten	Gain attenuation in bypass mode	dB		18	
Vdet	Detector output DC voltage at Plin	V		1.6	
DetR	Detector RF dynamic range	dB		10	
S	Stability under load VSWR of 6:1 (all phase)	dBc			-55

Notes:
4. Current is measured during ON portion of amplifier using 50% downlink ratio, IEEE 802.16e modulation.
5. Iq(total) is defined as the sum of all quiescent currents flowing into pins Vdd1, Vdd2, Vdd3, Vddbias.

Product Consistency Distribution Charts [1]

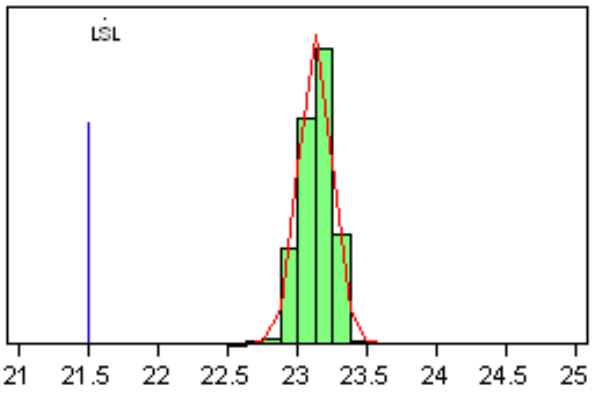


Figure 1a. Linear Pout Distribution (normal gain mode)

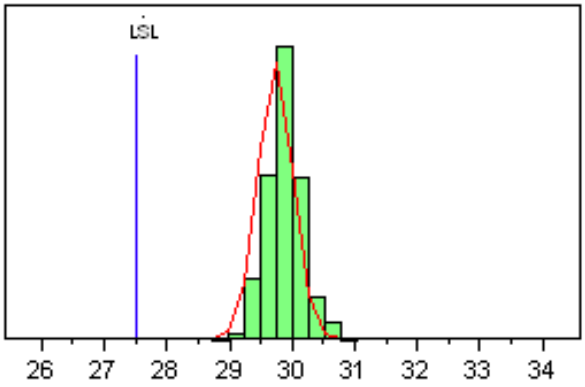


Figure 1b . Gain Distribution (normal gain mode)

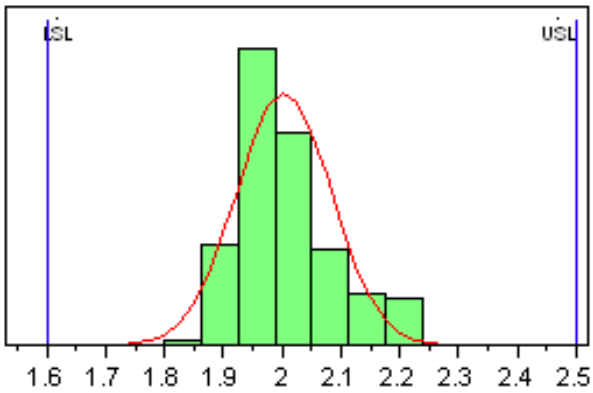


Figure 1c. Vc Distribution for Iq(total)=240mA

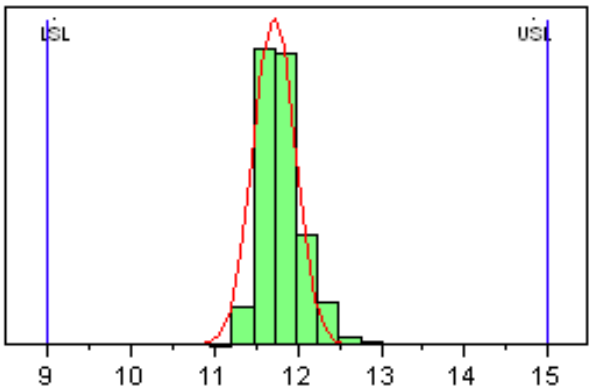


Figure 1d. Gain Distribution (bypass mode)

Notes:

1. Distribution data sample size are 500 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.

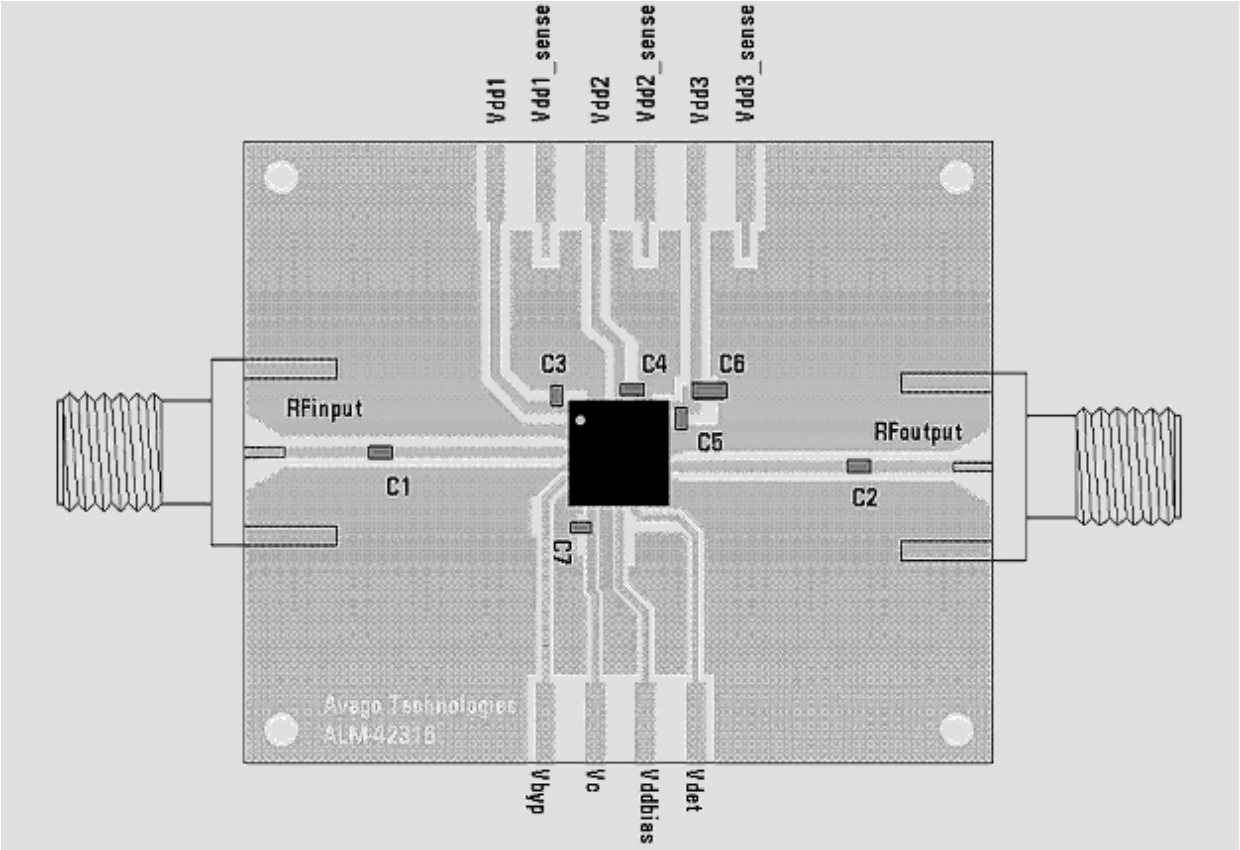


Figure 2. Demo board circuit for ALM-42316 module

Notes:
C1, C2, C7 : 3.9 pF, 0402 ceramic chip capacitor
C3, C4 : 0.1uF 0402 ceramic chip capacitor
C5 : 100pF 0402 ceramic chip capacitor
C6 : 2.2 uF 0805 ceramic chip capacitor

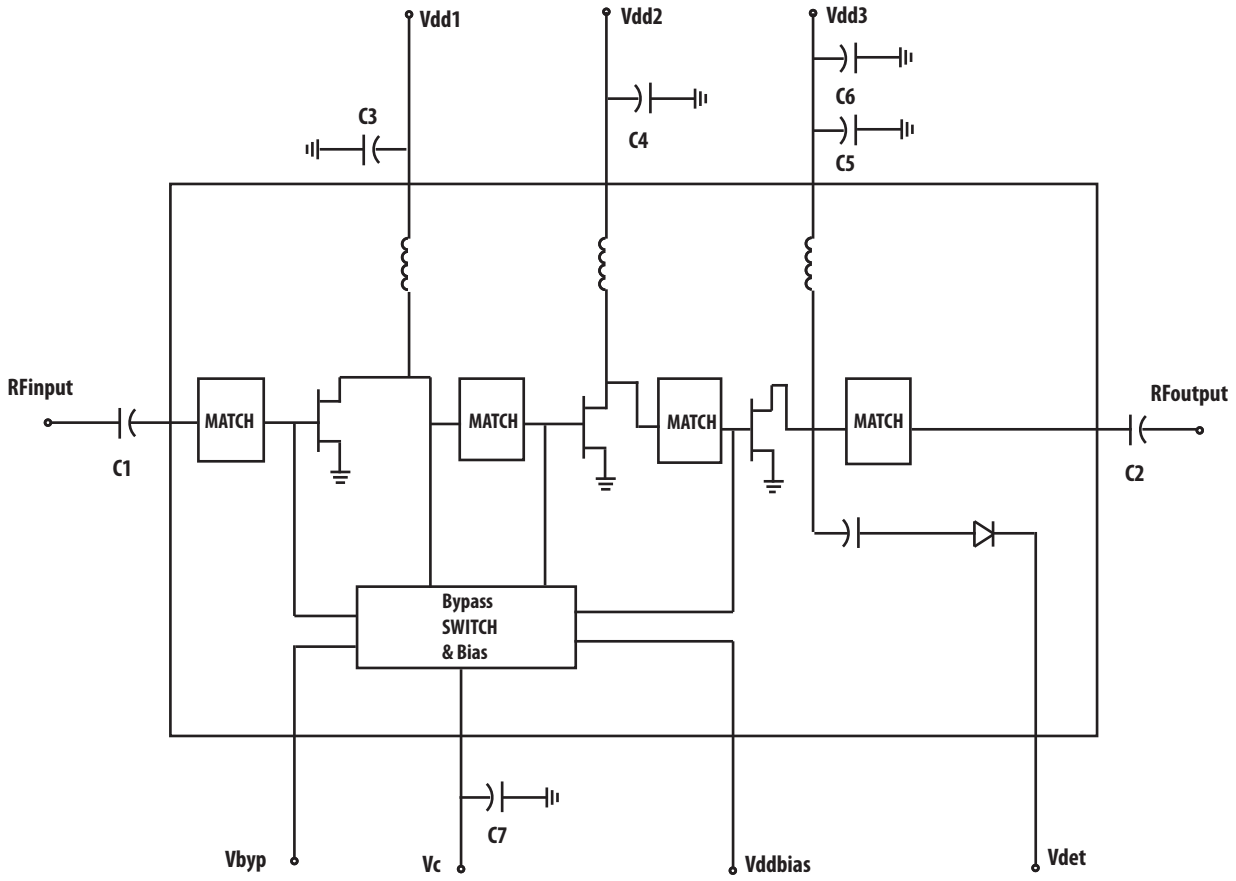


Figure 3. Application circuit in demoboard

Notes:

1. In normal gain mode operation, Vbyp = 0V. Vc is a bias pin that is used to set the bias conditions to the 3 internal gain stages of the PA.
2. Typical quiescent current distribution with Vdd1=Vdd2=Vdd3 = 3.3V, Vbyp = 0V, Vc = 2.0V is :
   a. Idd1 = 40 mA
   b. Idd2 = 118 mA
   c. Idd3 = 65 mA
   d. I_Vddbias = 17mA
3. Bypass mode is enabled by setting Vbyp pin to 3.3V. This condition overrides the normal high gain mode operation and bypasses the first gain stage, regardless of the voltage at Vc1 pin. The first gain stage is also shut down to reduce current consumption in this mode.
4. Modulated signal measurements are made with Agilent 89600 VSA and Agilent ESG4438C signal generator with IEEE 802.16e option using the following test conditions :
   - Signal format : IEEE 802.16e OFDMA, ¾ rate FEC
   - Modulation : 64-QAM
   - Numher of Subcarriers : 840
   - Modulation bandwidth : 10 MHz
   - Downlink ratio : 50%

   Residual distortion of signal generator : (0.6-0.8)%. This distortion is included in the overall EVM data in the datasheet.
5. Typical operating voltages and currents : -
   a. Normal gain mode : Vdd1 = Vdd2 = Vdd3 = Vddbias = 3.3V. Vc = 2.0V. Vbyp = 0V. Iq(total) = 240 mA.
   b. Bypass mode : Vdd1 = Vdd2 = Vdd3 = Vddbias = 3.3V. Vc = 2.0V. Vbyp = 3.3V. Iq(total) = 200 mA.

Unless otherwise stated, all measurements are made at Vdd=+3.3V, Iq(total)=240mA. Vc (typ) = 2.0V

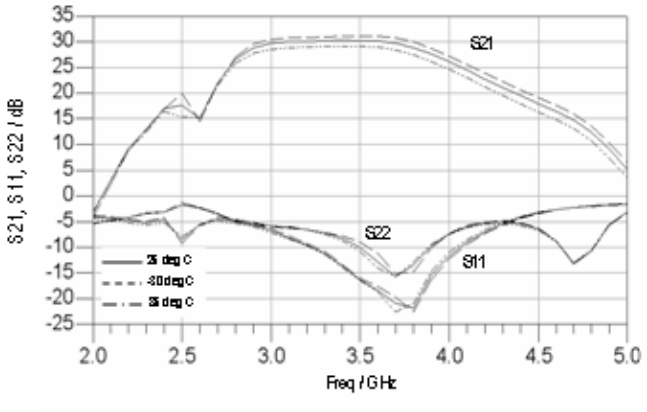


Figure 4. Small-signal performance in high-gain mode, Vdd = 3.3V

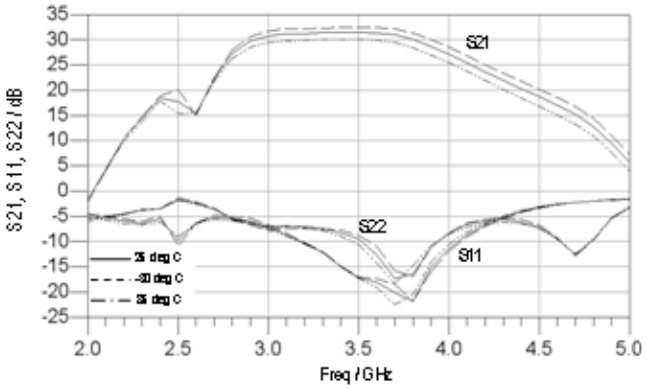


Figure 5. Small-signal performance in high-gain mode, Vdd = 5V)

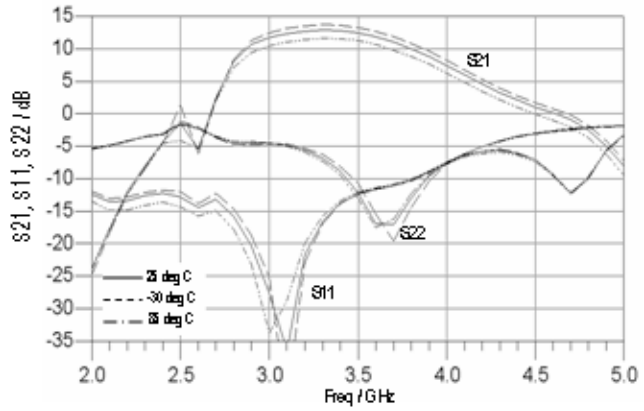


Figure 6. Small-signal performance in bypass mode, Vdd = 3.3V

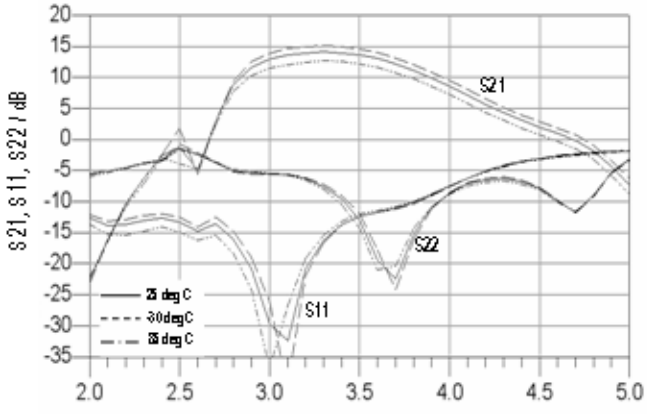


Figure 7. Small-signal performance in bypass mode, Vdd = 5V

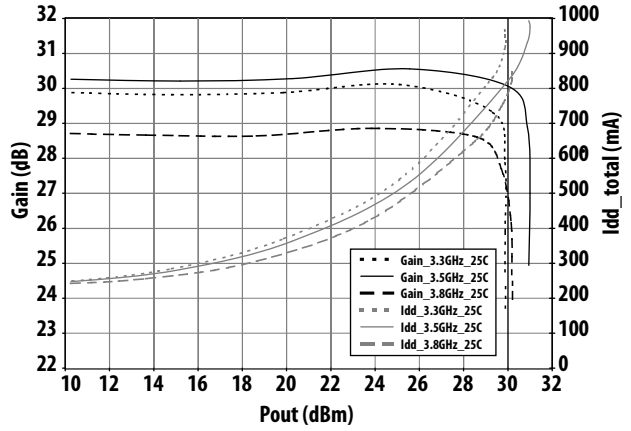


Figure 8 .CW Gain vs Pout @ 25°C, high-gain mode, Vdd = 3.3V

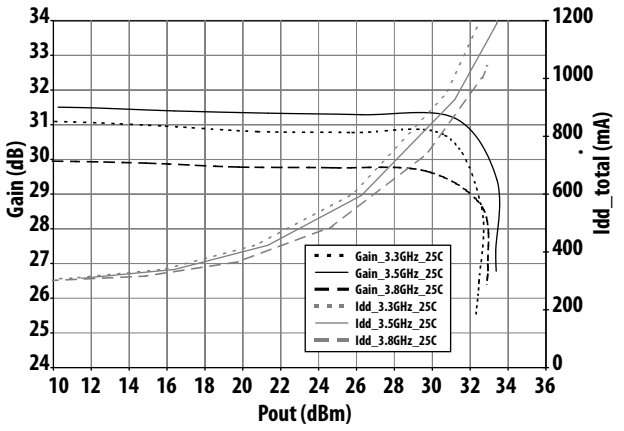


Figure 9. CW Gain vs Pout @ 25°C, high-gain mode, Vdd = 5V

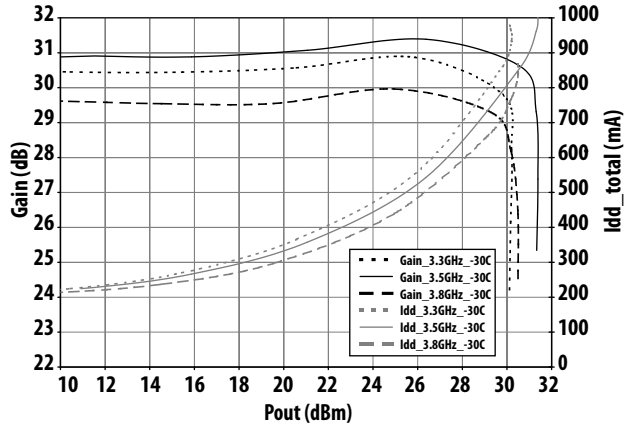


Figure 10. CW Gain vs Pout @ -30°C, high-gain mode, Vdd = 3.3V

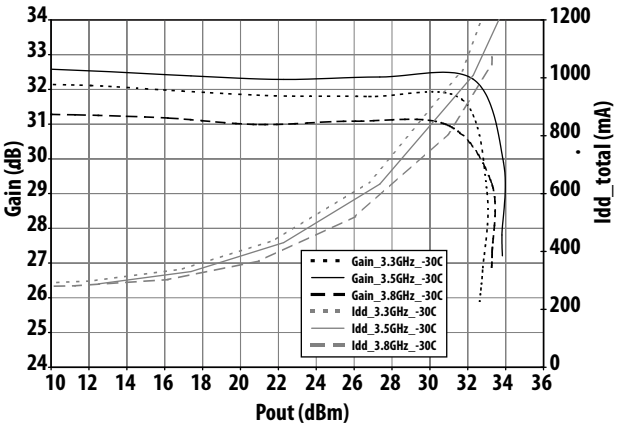


Figure 11. CW Gain vs Pout @ -30°C, high-gain mode, Vdd = 5 V

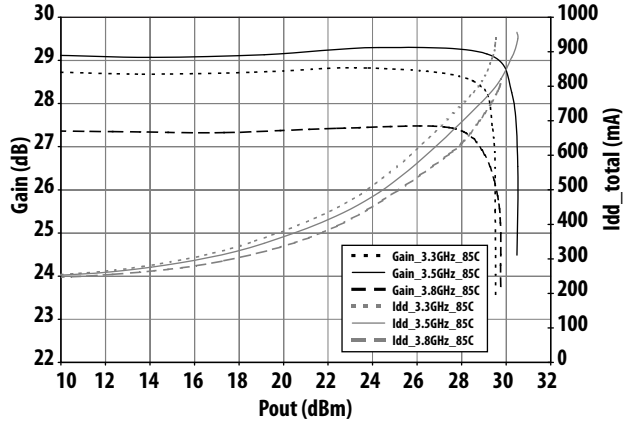


Figure 12. CW Gain vs Pout @ 85°C, high-gain mode, Vdd = 3.3V

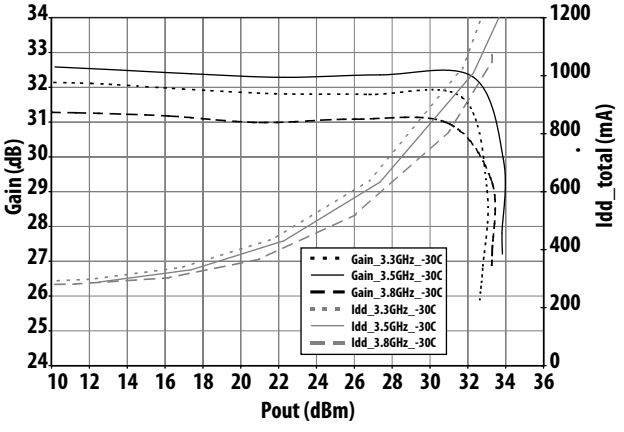


Figure 13. CW Gain vs Pout @ 85°C, high-gain mode, Vdd = 5V

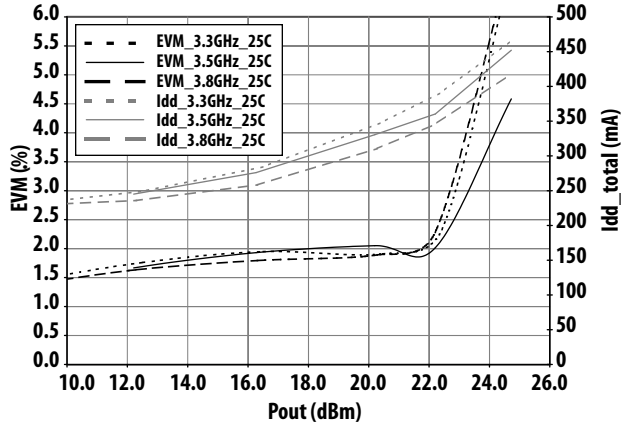


Figure 14. EVM vs Pout @ 25°C, High-gain mode, Vdd = 3.3V

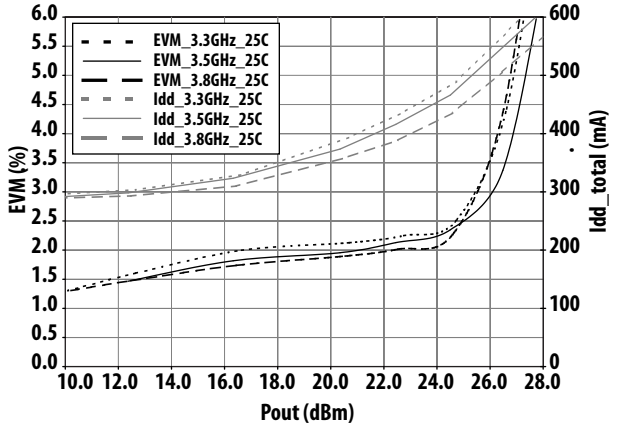


Figure 15. EVM vs Pout @ 25°C, High-gain mode, Vdd = 5V

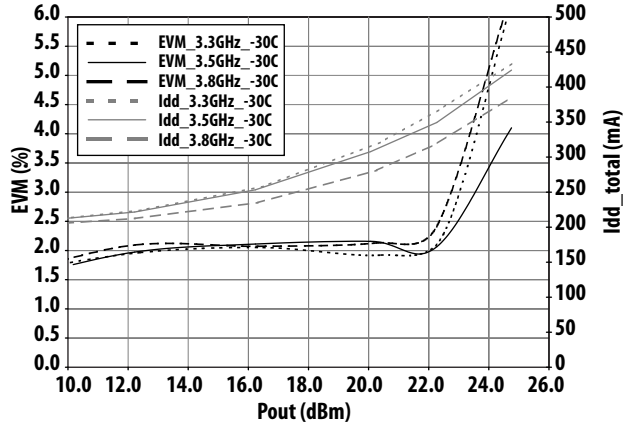


Figure 16. EVM vs Pout @ -30°C, High-gain mode, Vdd = 3.3V

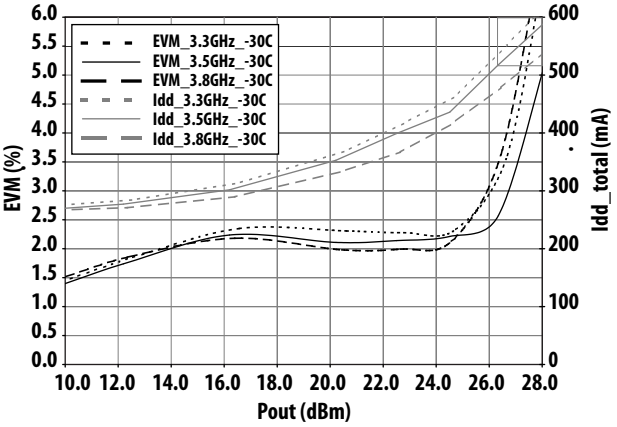


Figure 17. EVM vs Pout @ -30°C, High-gain mode, Vdd = 5V

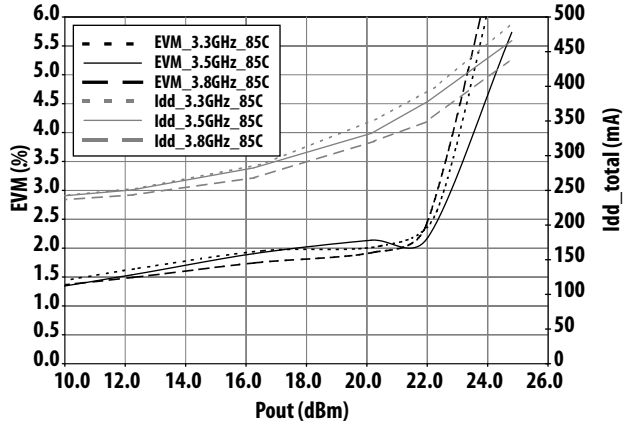


Figure 18. EVM vs Pout @ 85°C, High-gain mode, Vdd = 3.3

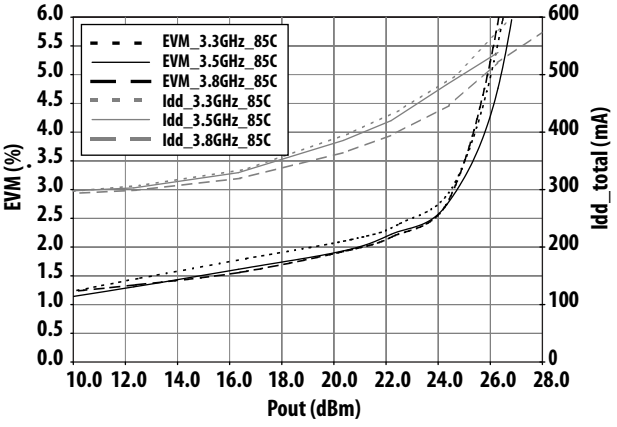


Figure 19. EVM vs Pout @ 85°C, High-gain mode, Vdd = 5V

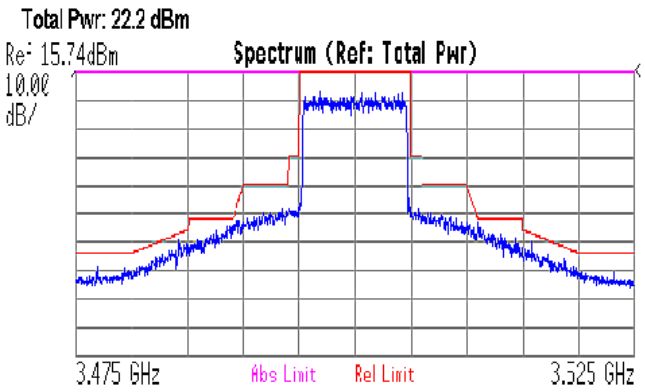


Figure 20. Spectral mask at Pout = 22.2 dBm, Freq= 3.5GHz, normal gain mode, Vdd = 3.3V, Temperature = 25°C

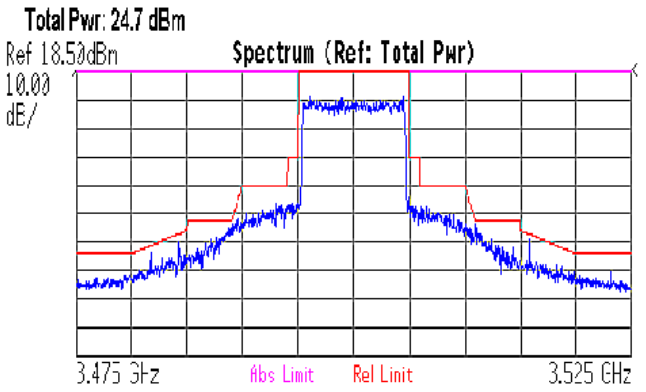


Fig 21. Spectral mask at Pout = 24.7 dBm meeting specs, Freq=3.5GHz, normal gain mode, Vdd = 5V, Temperature = 25°C

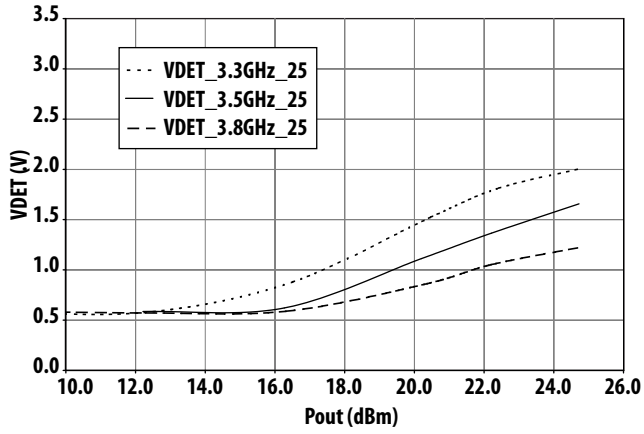


Figure 22. Detector vs Pout, normal gain mode, Vdd = 3.3V, Temperature = 25°C

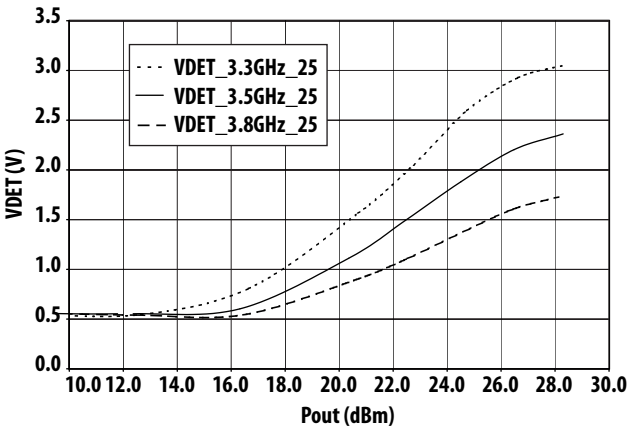


Figure 23. Detector vs Pout, normal gain mode, Vdd = 5V, Temperature = 25°C

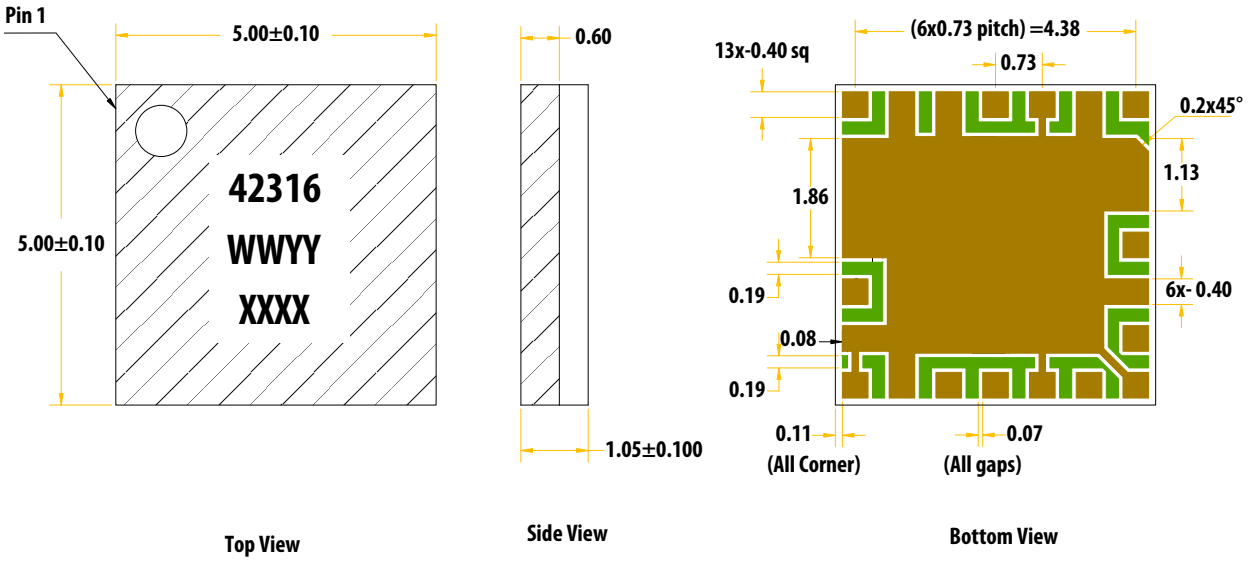
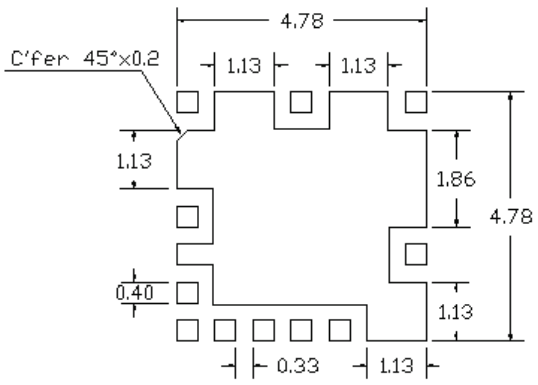
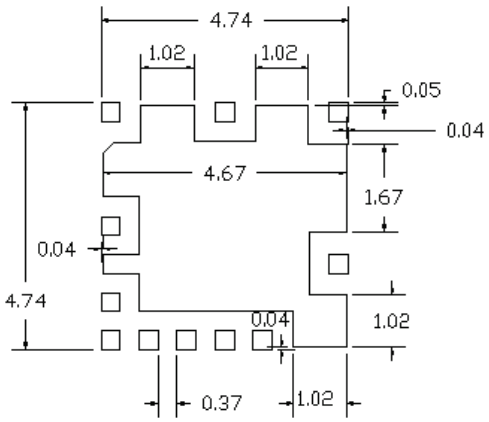


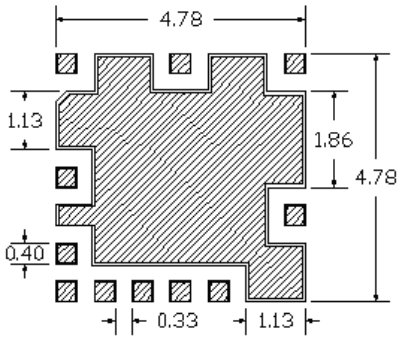
Figure 24. Package Drawing dimensions



PCB Land Pateern (Top View)



Stencil Outline

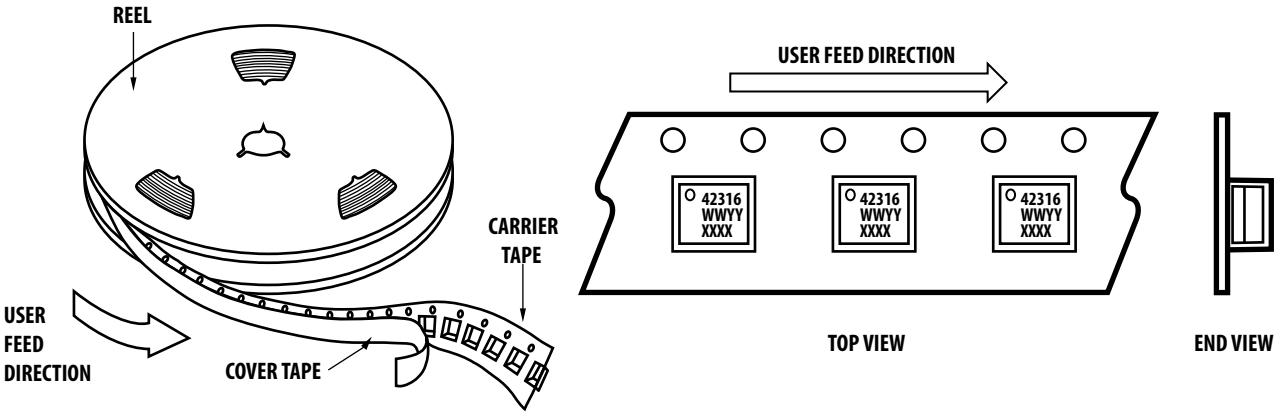


Combined PCB and Stencil Layout

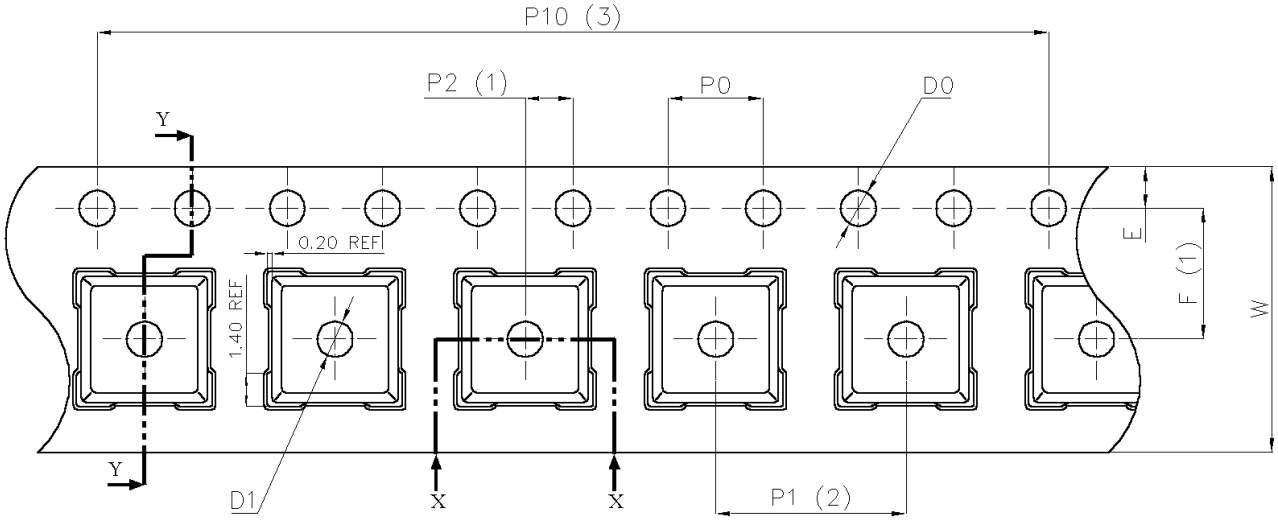
All Dimensions are in mm

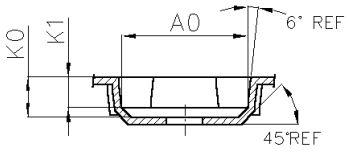
Figure 25. PC board and stencil design

Device Orientation

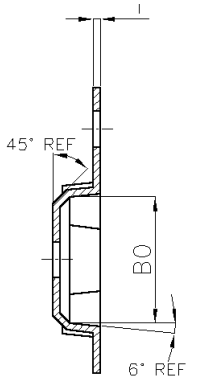


Tape Dimensions





SECTION X - X



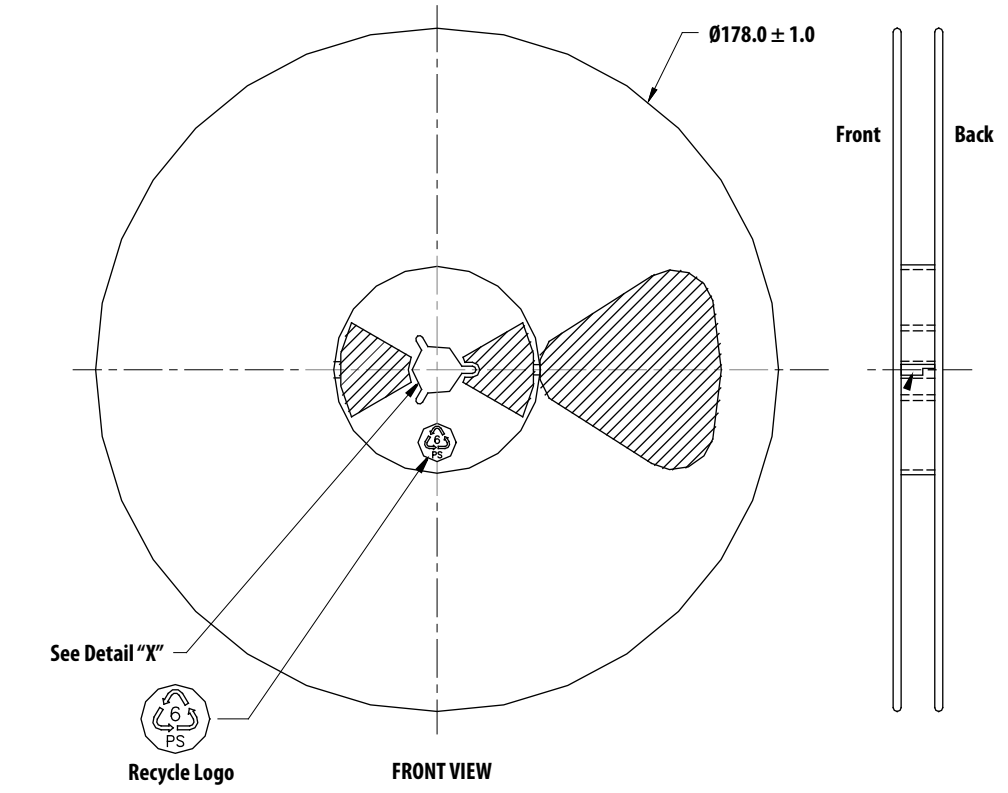
SECTION Y - Y

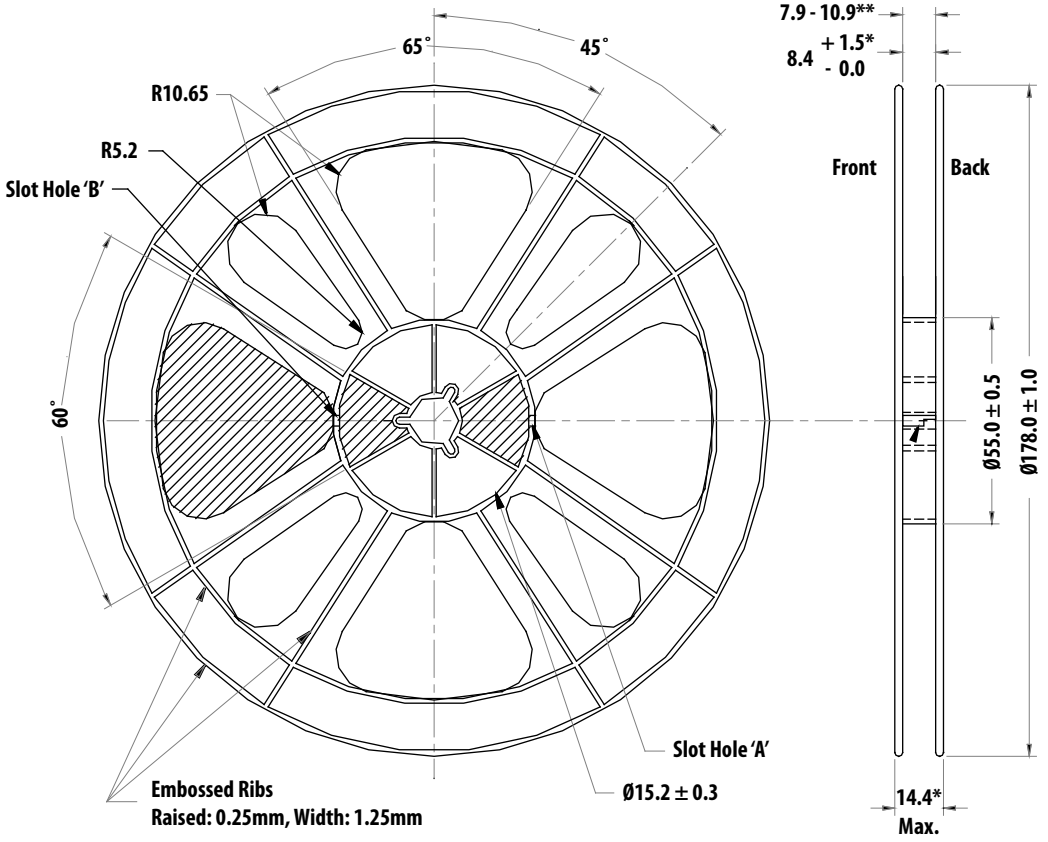
Dimension List			
Annote	Milimeter	Annote	Milimeter
A0	5.40±0.10	P0	4.00±0.10
B0	5.40±0.10	P2	2.00±0.10
D0	$1.50^{+0.10}_{-0}$	P10	40.00±0.20
D1	1.60±0.10	E	1.75±0.10
K0	1.90±0.10	F	5.50±0.10
K1	1.50±0.10	T	0.30±0.03
P1	8.00±0.10	W	12.00±0.30

Part Number Ordering Information

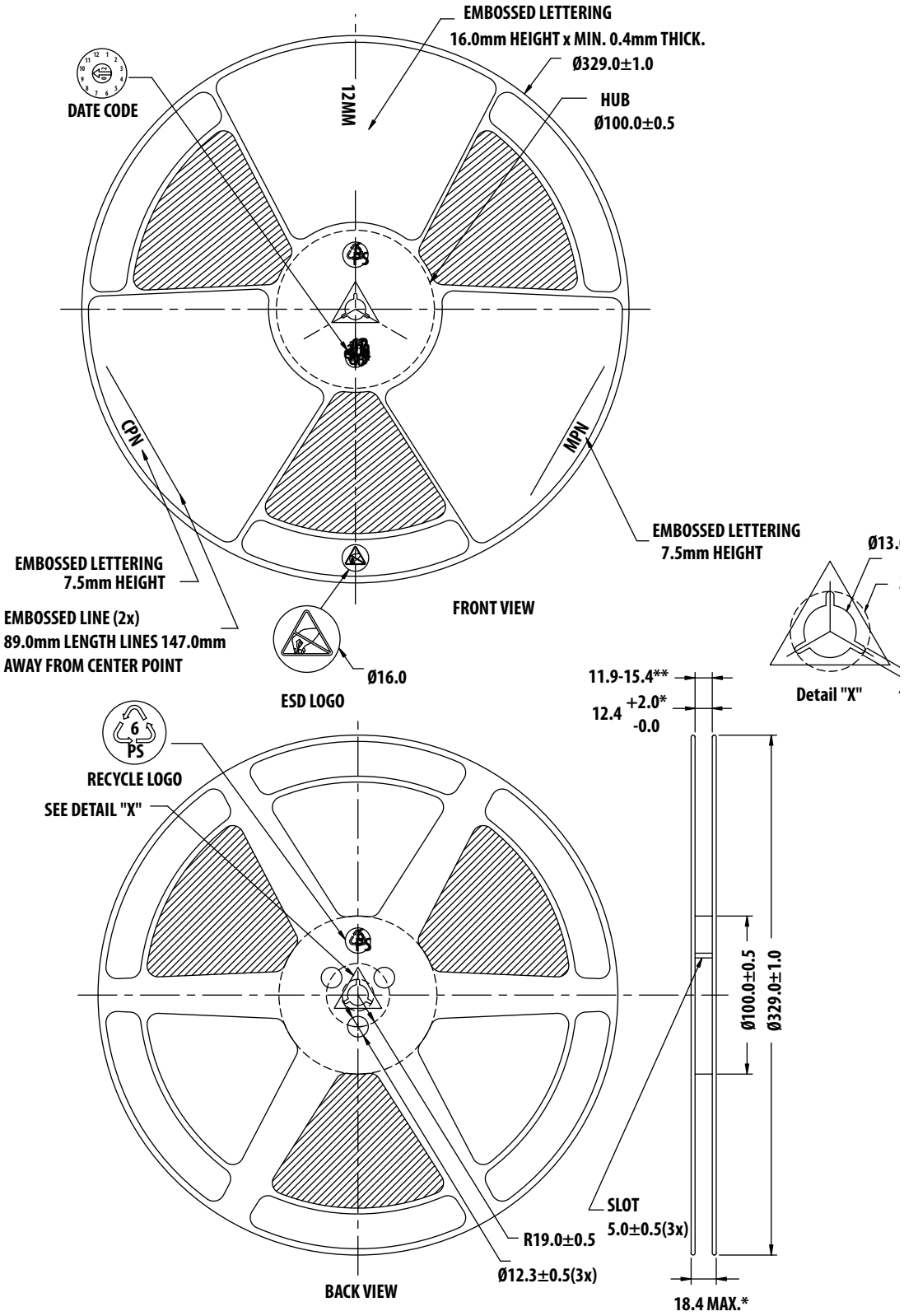
Part Number	No. of Devices	Container
ALM-42316-BLKG	100	Antistatic Bag
ALM-42316-TR1G	1000	7″ Reel
ALM-42316-TR2G	3000	13″ Reel

Reel Dimensions - 7 Inch





Reel Dimensions - 13 Inch



For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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AV02-1111EN - May 5, 2008