DUAL RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD2704A/ALD2704B/ALD2704 is a dual monolithic operational amplifier with MOSFET input that has rail-to-rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be beyond positive power supply voltage V^+ or the negative power supply voltage V^- by up to 300mV. The output voltage swings to within 60mV of either positive or negative power supply voltages at rated load.

With high impedance load, the output voltage of the ALD2704A/ALD2704B/ALD2704 approaches within 1mV of the power supply rails. This device is designed as an alternative to the popular J-FET input operational amplifier in applications where lower operating voltages, such as 9V battery or ±3.25V to ±5V power supplies are being used. The ALD2704A/ALD2704B/ALD2704 offers high slew rate of 5V/μs. It is designed and manufactured with Advanced Linear Devices' standard enhanced ACMOS silicon gate CMOS process, and it offers low unit cost and exceptional reliability.

The rail-to-rail input and output feature of the ALD2704A/ALD2704B/ALD2704 expands signal voltage range for a given operating supply voltage and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10mA into 400pF capacitive and 1.5KΩ resistive loads at unity gain and up to 4000pF at a gain of 5. Short circuit protection to either ground or the power supply rails is at approximately 15mA clamp current. Due to complementary output stage design, the output can source and sink 10mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

For each of the operational amplifier, the offset voltage is trimmed on-chip to eliminate the need for external nulling in many applications. For precision applications, the output is designed to settle to 0.1% in 2μs. In large signal buffer applications, the operational amplifier can function as an ultrahigh input impedance voltage follower /buffer that allows input and output voltage swings from positive to negative supply voltages. This feature is intended to greatly simplify systems design and eliminate higher voltage power supplies in many applications. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to 125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD2704ASAL	ALD2704APAL	ALD2704ADA
ALD2704BSAL	ALD2704BPAL	ALD2704BDA
ALD2704SAL	ALD2704PAL	ALD2704DA

* Contact factory for leaded (non-RoHS) or high temperature versions.

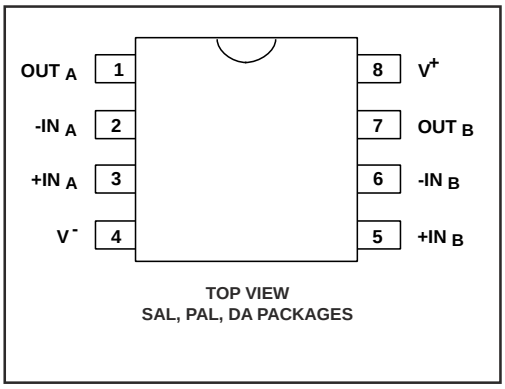
FEATURES

- Rail-to-rail input and output voltage ranges
- Symmetrical push-pull output drives
- Output settles to 2mV of supply rails
- 5.0V/μs slew rate
- High capacitive load capability -- up to 4000pF
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- <1.0pA typical (20pA max.)
- Ideal for high source impedance applications
- High voltage gain -- typically 100V/mV
- Output short circuit protected
- Unity gain bandwidth of 2.1MHz
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter
- Coaxial cable driver
- Capacitive sensor amplifier
- Piezoelectric transducer amplifier

PIN CONFIGURATION



TOP VIEW
SAL, PAL, DA PACKAGES

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+ referenced to V^- ——— -0.3V to V^++10.6V
Supply voltage, V_S referenced to V^- ——— ±5.3V
Differential input voltage range ——— -0.3V to V^+ +0.3V
Power dissipation ——— 600 mW
Operating tempurature range SAL, PAL packages ——— 0°C to +70°C
DA package ——— -55°C to +125°C
Storage tempurature range ——— -65°C to +150°C
Lead tempurature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±5.0V unless otherwise specified

		2704A			2704B			2704				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Supply Voltage	V_S V^+	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	V V	Dual Supply Single Supply
Input Offset Voltage	V_{OS}			1.0 1.5			2.0 3.0			5.0 6.0	mV mV	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Input Offset Current	I_{OS}		1.0	15 240		1.0	15 240		1.0	15 240	pA pA	T_A = 25°C $0°C \le T_A \le +70°C$
Input Bias Current	I_B		1.0	20 300		1.0	20 300		1.0	20 300	pA pA	T_A = 25°C $0°C \le T_A \le +70°C$
Input Voltage Range	V_{IR}	-5.3		5.3	-5.3		5.3	-5.3		5.3	V	
Input Resistance	R_{IN}		10^{12}			10^{12}			10^{12}		Ω	
Input Offset Voltage Drift	TCV_{OS}		5			5			5		µV/°C	$R_S \le 100K\Omega$
Power Supply Rejection Ratio	PSRR	65	80		65	80		60	80		dB	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Common Mode Rejection Ratio	CMRR	65	83		65	83		60	83		dB	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Large Signal Voltage Gain	A_V	15 28 100			15 28 100			10 28 100			V/mV V/mV	R_L = 100KΩ $R_L \ge 1M\Omega$
Output Voltage Range	V_O low V_O high	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	V	$R_L \ge 10K\Omega$ $0°C \le T_A \le +70°C$
	V_O low V_O high	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	V	R_L = 1MΩ $0°C \le T_A \le +70°C$
Output Short Circuit Current	I_{SC}		15			15			15		mA	
Supply Current	I_S		5.0	6.5		5.0	6.5		5.0	6.5	mA	V_{IN} = -5V No Load
Power Dissipation	P_D			65			65			65	mW	Both amplifiers, No Load V_S = ±5.0V
Input Capacitance	C_{IN}		1			1			1		pF	
Bandwidth	B_W		2.1			2.1			2.1		MHz	
Slew Rate	S_R		5.0			5.0			5.0		V/µs	A_V = +1 R_L = 2.0KΩ
Rise time	t_r		0.1			0.1			0.1		µs	R_L = 2.0KΩ
Overshoot Factor			15			15			15		%	R_L = 2.0KΩ C_L = 100pF

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	2704A			2704B			2704			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Load Capacitance	C_L		400 4000			400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Input Noise Voltage	e_n		26			26			26		nV/√Hz	f =1KHz
Input Current Noise	i_n		0.6			0.6			0.6		fA/√Hz	f =10Hz
Settling Time	t_s		5.0 2.0			5.0 2.0			5.0 2.0		µs µs	0.01% 0.1% A_V = 1 R_L = 5KΩ C_L= 50pF

V_S = ±5.0V -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Symbol	2704ADA			2704BDA			2704DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			2.0			4.0			7.0	mV	R_S ≤ 100KΩ
Input Offset Current	I_{OS}			8.0			8.0			8.0	nA	
Input Bias Current	I_B			10.0			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		60	75		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	AV	10	25		10	25		10	25		V/mV	R_L = 10KΩ
Output Voltage Range	V_O low V_O high	4.8	-4.9 4.9	-4.8	4.8	-4.9 4.9	-4.8	4.8	-4.9 4.9	-4.8	V	R_L = 10KΩ

Design & Operating Notes:

1. The ALD2704A/ALD2704B/ALD2704 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. The ALD2704A/ALD2704B/ALD2704 is internally compensated for unity gain stability using a novel scheme. This design produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD2704A/ALD2704B/ALD2704 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD2704A/ALD2704B/ALD2704 is much more resistant to parasitic oscillations.

2. The ALD2704A/ALD2704B/ALD2704 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. With the common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. As offset voltage trimming on the ALD2704A/ALD2704B/ALD2704 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain greater than 2 (10V operation), where the common mode voltage does not make excursions below this switching point.

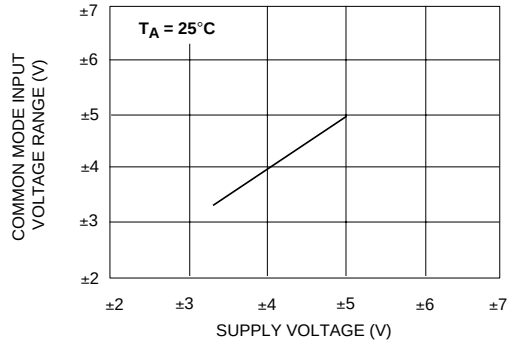
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. The voltage follower configuration, the oscillation and resistant with the rail-to-rail input and output feature, makes the ALD2704A/ALD2704B/ALD2704 an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

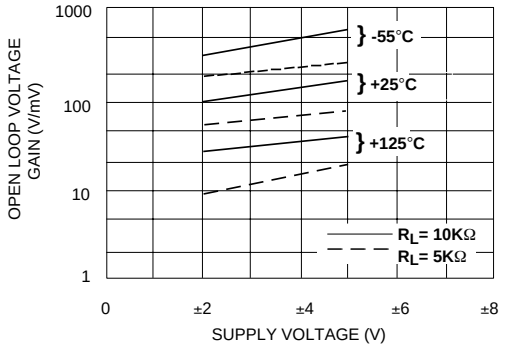
5. The ALD2704A/ALD2704B/ALD2704 operational amplifier has been designed to provide static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels. Alternatively, a 100KΩ or higher value resistor at the input terminals will limit input currents to acceptable levels while causing very small or negligible accuracy effects.

TYPICAL PERFORMANCE CHARACTERISTICS

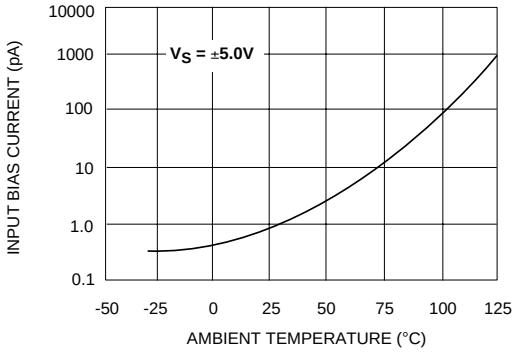
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



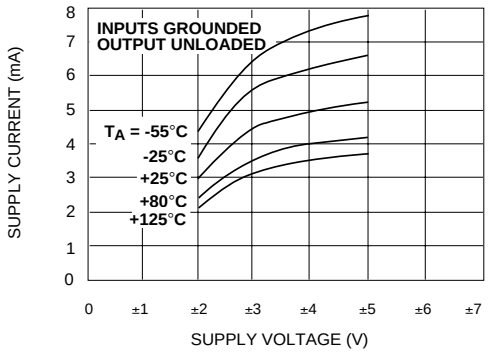
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

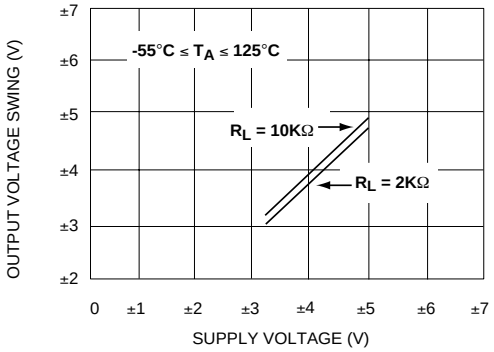


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

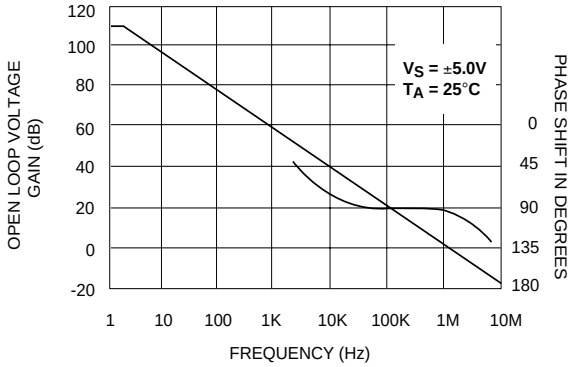


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

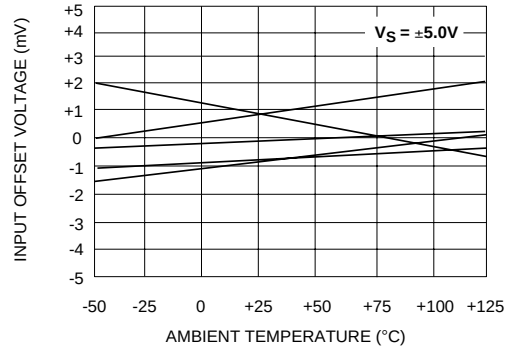
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



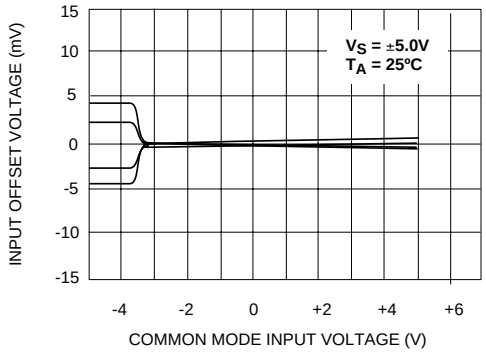
OPEN LOOP VOLTAGE AS A FUNCTION OF FREQUENCY



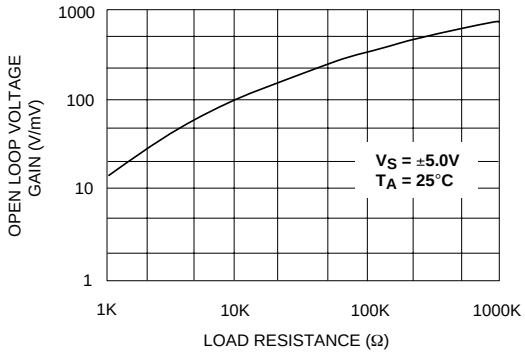
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS



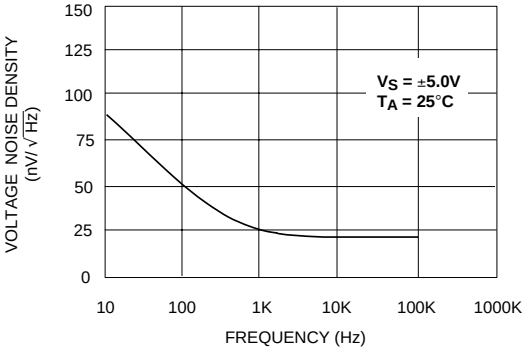
INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



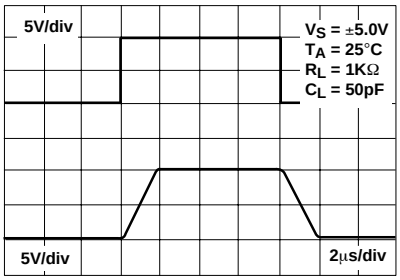
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



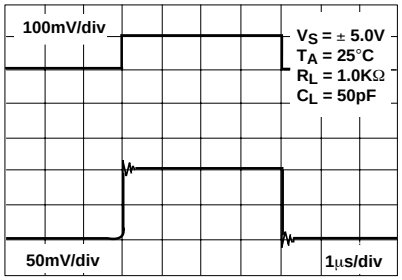
VOLTAGE NOISE DENSITY AS A FUNCTION OF FREQUENCY



LARGE - SIGNAL TRANSIENT RESPONSE

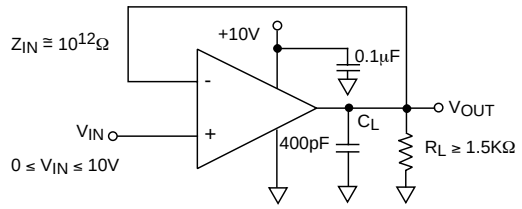


SMALL - SIGNAL TRANSIENT RESPONSE

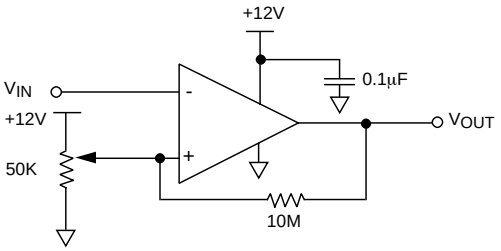


TYPICAL APPLICATIONS

RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER



RAIL-TO-RAIL VOLTAGE COMPARATOR



LOW OFFSET SUMMING AMPLIFIER

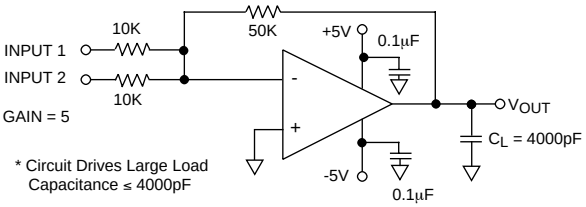
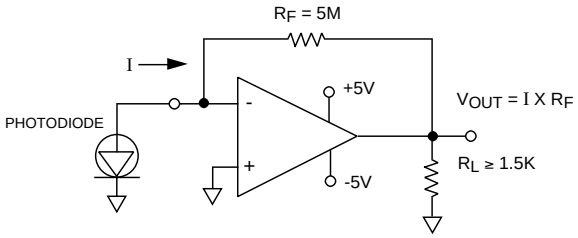
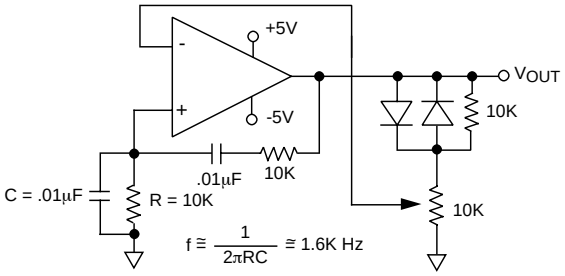


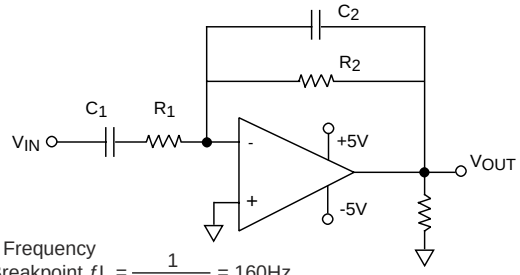
PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



WIEN BRIDGE OSCILLATOR (RAIL-TO -RAIL) SINE WAVE GENERATOR



BANDPASS NETWORK

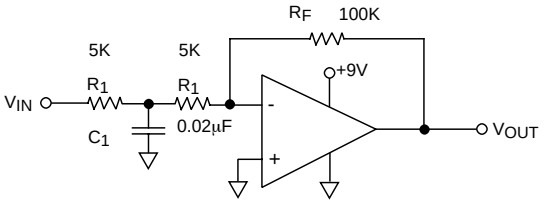


Low Frequency Breakpoint $fL = \frac{1}{2\pi R1C1} = 160Hz$

High Frequency Cutoff $fH = \frac{1}{2\pi R2C2} = 32KHz$

R_1 = 10K C_1 = 100nF
R_2 = 10K C_2 = 500pF

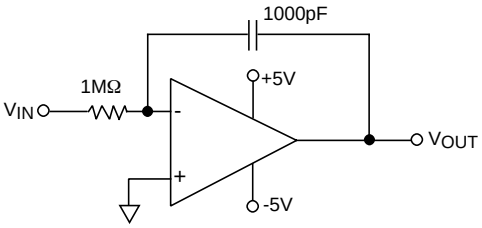
LOW PASS FILTER (RFI FILTER)



Cutoff frequency = $\frac{1}{\pi R1C1}$ = 3.2kHz

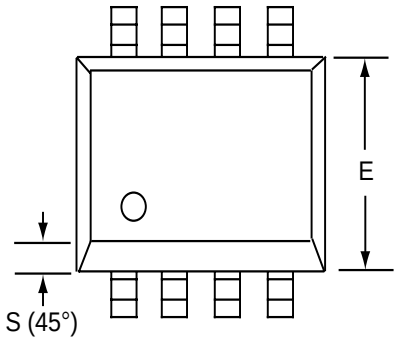
Gain = 10 Frequency roll-off 20dB/decade

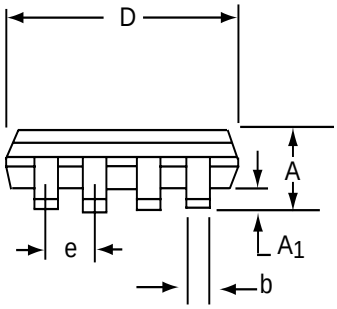
PRECISION CHARGE INTEGRATOR

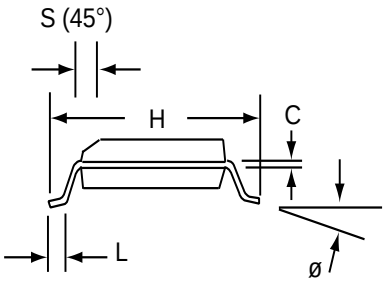


SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package



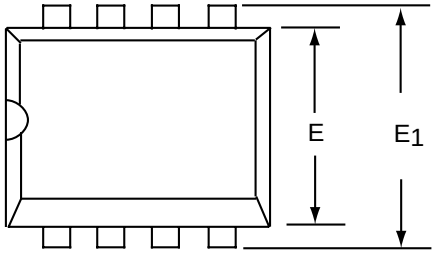


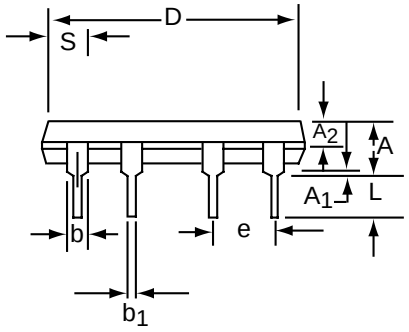


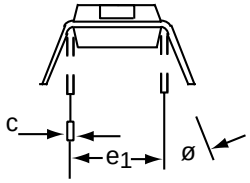
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



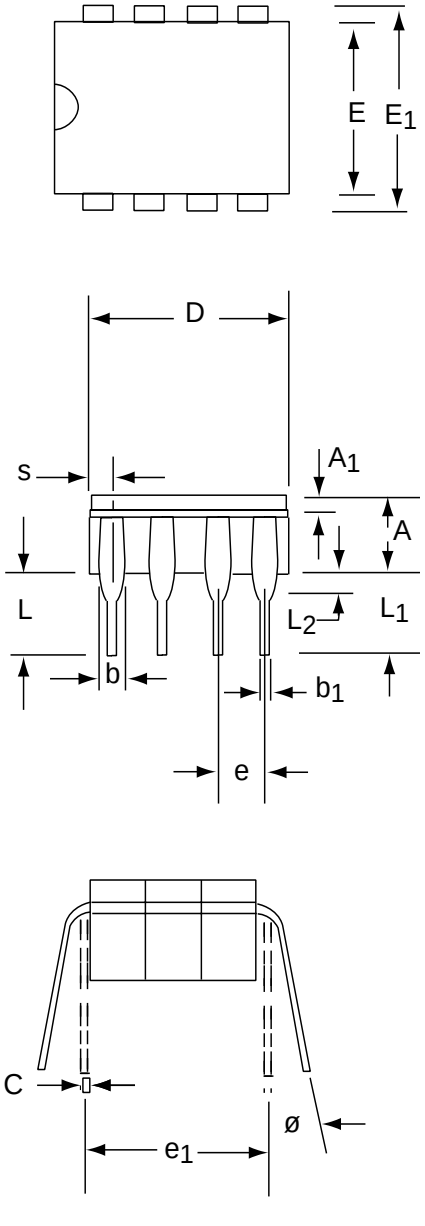




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°