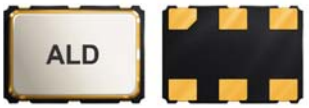
CERAMIC SMD CRYSTAL CLOCK OSCILLATOR



5.08 x 7.0 x 1.8mm

ALD SERIES : PRELIMINARY

FEATURES:

- Based on a proprietary digital multiplier
- Tri-State Output
- Low Phase Jitter
- 2.5V to 3.3V +/- 5% operation
- Ceramic SMD, low profile package
- 156.25MHz, 187.5MHz, and 212.5MHz applications

APPLICATIONS:

- SONET, xDSL
- SDH, CPE
- STB

STANDARD SPECIFICATIONS:

PARAMETERS	
Frequency Range	750 KHz to 800 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	- 40°C to + 85°C
Overall Frequency Stability	± 50 ppm max. (see options)
Supply Voltage (Vdd)	2.5V to 3.3 Vdc ± 5%
Linearity	5% typ, 10% max.
Jitter (12KHz - 20MHz)	RMS phase jitter 3pS typ. < 5pS max. period jitter < 35pS peak to peak
Phase Noise	-109 dBc/Hz @ 1kHz Offset from 622.08MHz -110 dBc/Hz @ 10kHz Offset from 622.08MHz -109 dBc/Hz @ 100kHz Offset from 622.08MHz
Tri-State Function	"1" ($V_{IH} \geq 0.7*V_{DD}$) or open: Oscillation/ "0" ($V_{IH} > 0.3*V_{DD}$) No Oscillation/Hi Z
PECL	
Supply Current (I_{DD})	80mA (Fo < 155.52MHz), 100mA (Fo < 155.52MHz)
Symmetry (Duty Cycle)	45% min, 50% typical, 55% max.
Output Logic High	V_{DD} -1.025V min, V_{DD} -0.880V max.
Output Logic Low	V_{DD} -1.810V min, V_{DD} -1.620V max.
Clock Rise time (t_r) @ 20/80%	1.5ns max, 0.6nSec typical
Clock Fall time (t_f) @ 80/20%	1.5ns max, 0.6nSec typical
CMOS	
Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]	1.6ns max, 1.2ns typical
Output Clock Duty Cycle [Measured @ 50% VDD]	45% min, 50% typical, 55% max
LVDS	
Supply Current (I_{DD}) [Fout = 212.50MHz]	60mA max, 55mA typical.
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V_{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV_{OD})	-50mV min, 50mV max
Output High Voltage	V_{OH} = 1.6V max, 1.4V typical
Output Low Voltage	V_{OL} = 0.9V min, 1.1V typical
Offset Voltage [R_L = 100Ω]	V_{OS} = 1.125V min, 1.2V typical, 1.375V max
Offset Magnitude Voltage[RL = 100Ω]	ΔV_{OS} = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V]	±10µA max, ±1µA typical
Differential Clock Rise Time (t_r) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max
Differential Clock Fall Time (t_f) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max

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5.08 x 7.0 x 1.8mm

ALD SERIES : PRELIMINARY

PIN ASSIGNMENTS:

PIN #	NAME	DESCRIPTION
1	Tri-state or VC	Tri-state or Voltage Control
2	Tri-state or NC	Tri-state or No Connect
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output
5	Q	Complimentary PECL,LVDS, or NC
6	V_{DD}	VDD Connection

TRI-STATE PIN OPERATION:

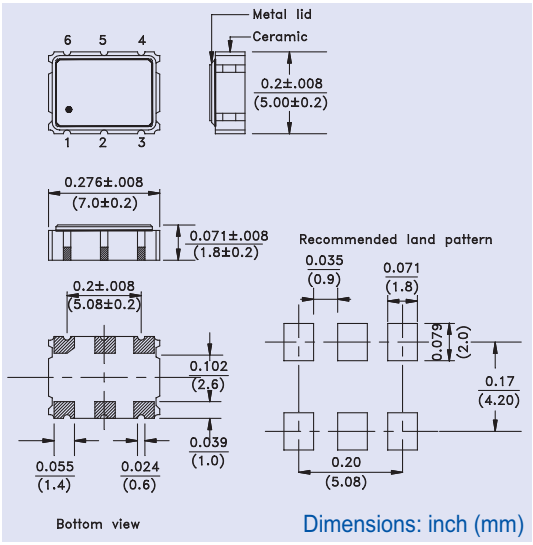
OUTPUT TYPE	PIN 1 LOGIC LEVEL*	OUTPUT STATE
PECL (P)	0 (Default)	Enabled
	1	Tri-state
LVDS & CMOS (L, C)	0	Tri-state
	1(Default)	Enabled
PECL1 (P1)	0	Tri-state
	1(Default)	Enabled

*Connect to VDD from logic level "1", connect to ground for logic level "0".

MARKING:

- TUH (Frequency: T=First “”10” digit of frequency, U=First “unit” of frequency, H=First “tenth” of frequency, Ex: 100 for 10.0MHz)
- ALD ZYX (Z: Month, A to L; Y: Year, 5 for 2005; X: Traceability Code)

OUTLINE DRAWING:



OPTIONS AND PART IDENTIFICATION (Left blank if standard):

ALD - Frequency - Temperature - Frequency Stability - Output - Packaging

Temperature:
D for -10°C to +60°C
E for -20°C to +70°C
F for -30°C to +70°C
N for -30°C to +85°C
L for -40°C to +85°C

Stability options:
R for ± 25 ppm
K for ± 30 ppm
H for ± 35 ppm

Output options:
P = PECL
L = LVDS
C = CMOS
P1 = PECL1

Tri-State option: **A** for Pin 1 = NC, Pin 2 = Tristate

Packaging option: **T** for Tape and Reel (1,000pcs/reel)

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