AK4340

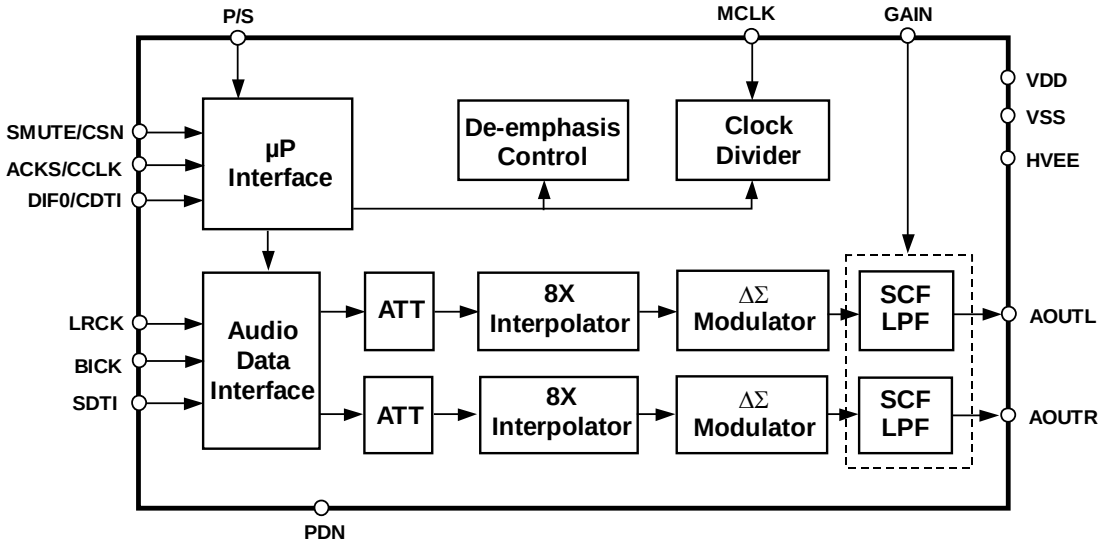
192kHz 24-Bit Stereo ΔΣ DAC with 2Vrms Output

GENERAL DESCRIPTION

The AK4340 offers the ideal features for consumer systems that require a 2Vrms audio output. Using AKM's multi bit architecture for its modulator the AK4340 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4340 integrates the Switched Capacitor Filter (SCF) increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications including Set-top-box, DVD-Audio. The AK4340 is offered in a space saving 16pin TSSOP package.

FEATURES

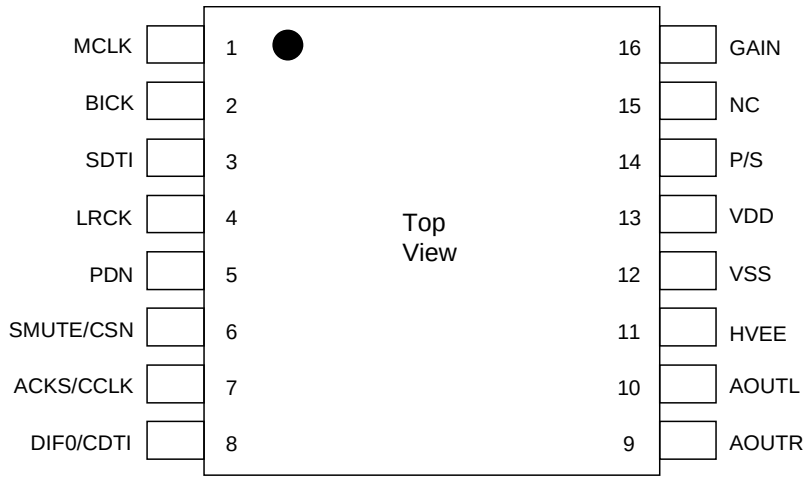
- **Sampling Rate Ranging from 8kHz to 192kHz**
- **128 times Oversampling (Normal Speed Mode)**
- **64 times Oversampling (Double Speed Mode)**
- **32 times Oversampling (Quad Speed Mode)**
- **24-Bit 8 times FIR Digital Filter**
- **Switched Capacitor Filter with High Tolerance to Clock Jitter**
- **On chip Buffer with 2Vrms Single-ended output**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz or 48kHz**
- **Soft Mute Function**
- **Digital Attenuator (Linear 256 Step)**
- **Audio interface format: 24Bit MSB justified, 24/20/16 LSB justified or I^2S compatible**
- **Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)**
  128fs, 192fs, 256fs or 512fs (Double Speed Mode)
  128fs or 192fs (Quad Speed Mode)
- **THD+N: -90dB**
- **Dynamic Range: 106dB**
- **Power supply: +4.5V to +5.5V (DAC), - 4.5V to - 13.2V (Output Buffer)**
- **Ta = - 20 to 85 °C**
- **Package: 16pin TSSOP (6.4mm x 5.0mm)**



■ Ordering Guide

AK4340ET	-20 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4340	Evaluation board for AK4340	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4340 is in the power-down mode and is held in reset. The AK4340 must be reset once upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel control mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial control mode
7	ACKS	I	Auto Setting Mode Pin in parallel control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial control mode
8	DIF0	I	Audio Data Interface Format Pin in parallel control mode
	CDTI	I	Control Data Input Pin in serial control mode
9	AOUTR	O	Rch Analog Output Pin
10	AOUTL	O	Lch Analog Output Pin
11	HVEE	-	Output Buffer Negative Power Supply Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
12	VSS	-	Ground Pin
13	VDD	-	DAC Power Supply Pin
14	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
15	NC	-	No connect No internal banding (Note)
16	GAIN	I	Output Gain Select Pin "L": 0dB, "H": +1.94dB

Note: Do not allow digital input pins except pull-up pin to float.
Note: Pin No.15 (NC) has no internal bonding and can be left Open, connected GND or VDD.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	DAC	VDD	-0.3	+6.0	V
	Output Buffer	HVEE	-14.0	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Input Voltage		VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	DAC	VDD	+4.5	+5.0	+5.5	V
	Output Buffer	HVEE	-13.2	-5.0	-4.5	V

Note 1. All voltages with respect to ground.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=+5.0VV; HVEE=-5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; $R_L \geq 5k\Omega$; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 2)						
THD+N	fs=44.1kHz	0dBFS		-90	-84	dB
	BW=20kHz	-60dBFS		-42	-	dB
	fs=96kHz	0dBFS		-90	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
	fs=192kHz	0dBFS		-90	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
Dynamic Range (-60dBFS with A-weighted) (Note 3)			100	106		dB
S/N (A-weighted) (Note 4)			100	106		dB
Interchannel Isolation (1kHz)			90	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage (Note 5)		GAIN pin = "L"	1.85	2	2.15	Vrms
		GAIN pin = "H"	2.35	2.5	2.65	Vrms
Load Capacitance (Note 6)					25	pF
Load Resistance			5			kΩ
Power Supplies						
Power Supply Current: (Note 7)						
Normal Operation (PDN pin = "H", fs≤96kHz)						
VDD				22	30	mA
HVEE				6	9	mA
Normal Operation (PDN pin = "H", fs=192kHz)						
VDD				25	33	mA
HVEE				6	9	mA
Power-Down Mode (PDN pin = "L") (Note 8)						
VDD				10	100	μA
HVEE				10	100	μA

Note 2. Measured by Audio Precision (System Two). GAIN pin = "L". Refer to the evaluation board manual regarding the measurement results.

Note 3. 98dB at 16bit data

Note 4. S/N ration does not depend on the input data length

Note 5. Full-scale voltage (0dB). Output voltage is proportional to VDD voltage.
AOUT (typ.@ 0dB, GAIN = 0dB) = 2Vrms × VDD/5.

Note 6. When the output pin drives a capacitive load, a resistor should be added in series between output pin and capacitive load.

Note 7. These values are supplied to VDD pin or HVEE pin.

Note 8. P/S pin is tied to VDD and the other all digital inputs including clock pins (MCLK, BICK and LRCK) are tied to VDD or VSS.

FILTER CHARACTERISTICS

(Ta = 25°C; VDD = +4.5 ~ +5.5V, HVEE = -13.2 ~ -4.5V; fs = 44.1kHz, DEM = OFF)

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband ±0.05dB (Note 9)			PB	0		20.0	kHz
-6.0dB				-	22.05	-	kHz
Stopband (Note 9)			SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay (Note 10)			GD	-	19.3	-	1/fs
Digital Filter + LPF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.05	-	dB
	40.0kHz	fs=96kHz	FR	-	± 0.05	-	dB
	80.0kHz	fs=192kHz	FR	-	± 0.05	-	dB

Note 9. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 10. Delay time caused by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VDD = +4.5 ~ +5.5V, HVEE = -13.2 ~ -4.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Input Leakage Current (Note 11)	Iin	-	-	± 10	µA

Note 11. P/S pin is pulled-up internally. (typ. 100kΩ)

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD = +4.5 ~ +5.5V, HVEE = -13.2 ~ -4.5V)

Parameter		Symbol	min	typ	max	Units
Master Clock Frequency		fCLK	2.048	11.2896	36.864	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency						
Normal Speed Mode		fsn	8		48	kHz
Double Speed Mode		fsd	60		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/64fsd			ns
Quad Speed Mode		tBCK	1/64fsq			ns
BICK Pulse Width Low		tBCKL	30			ns
Pulse Width High		tBCKH	30			ns
BICK rising to LRCK Edge	(Note 12)	tBLR	20			ns
LRCK Edge to BICK rising	(Note 12)	tLRB	20			ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 13)	tPD	150			ns

Note 12. BICK rising edge must not occur at the same time as LRCK edge.
Note 13. The AK4340 can be reset by bringing PDN pin = "L".

■ Timing Diagram

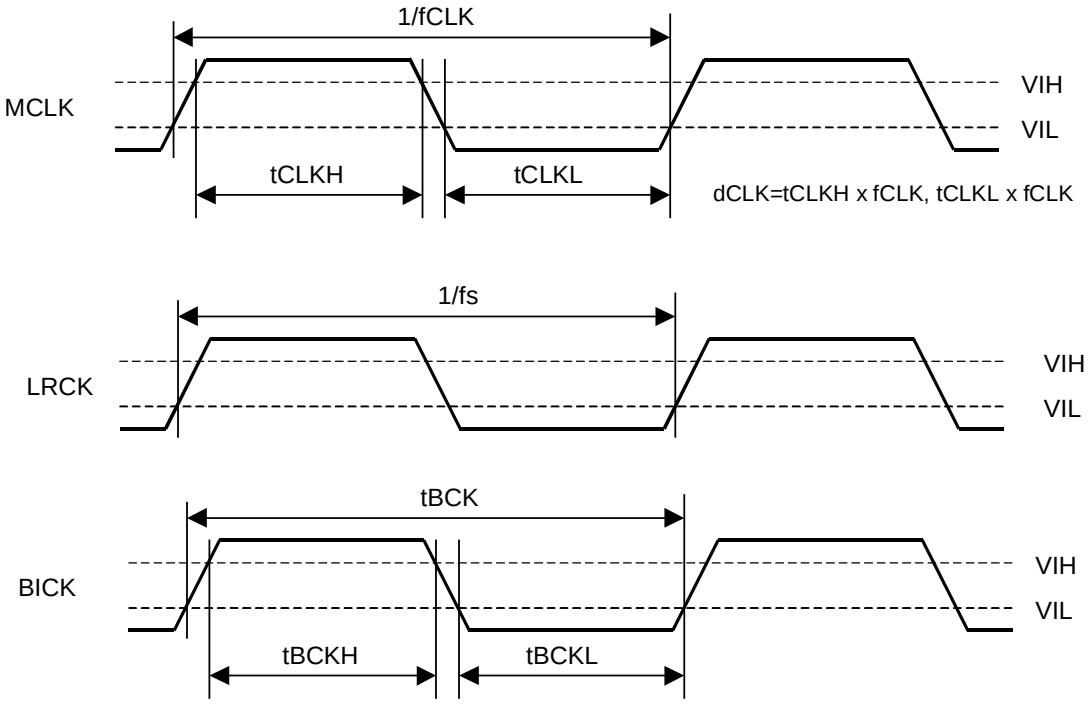


Figure 1. Clock Timing

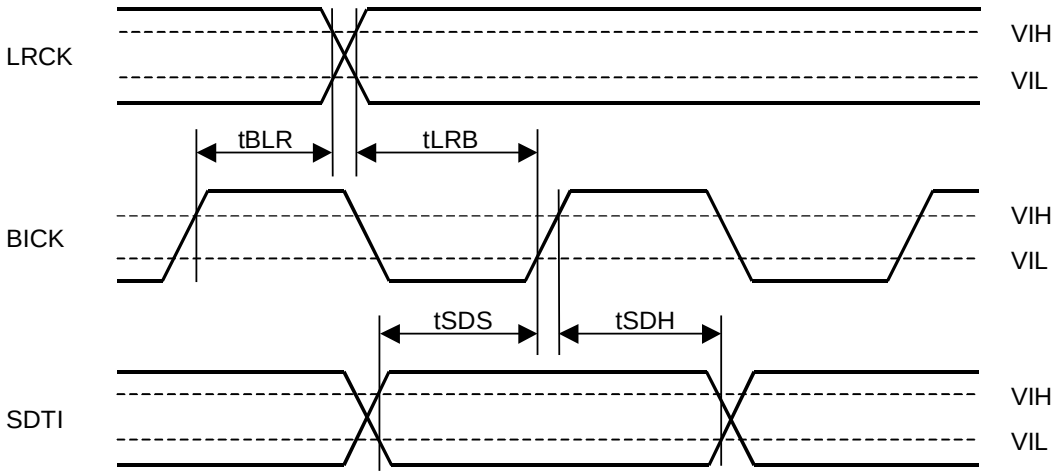


Figure 2. Serial Interface Timing

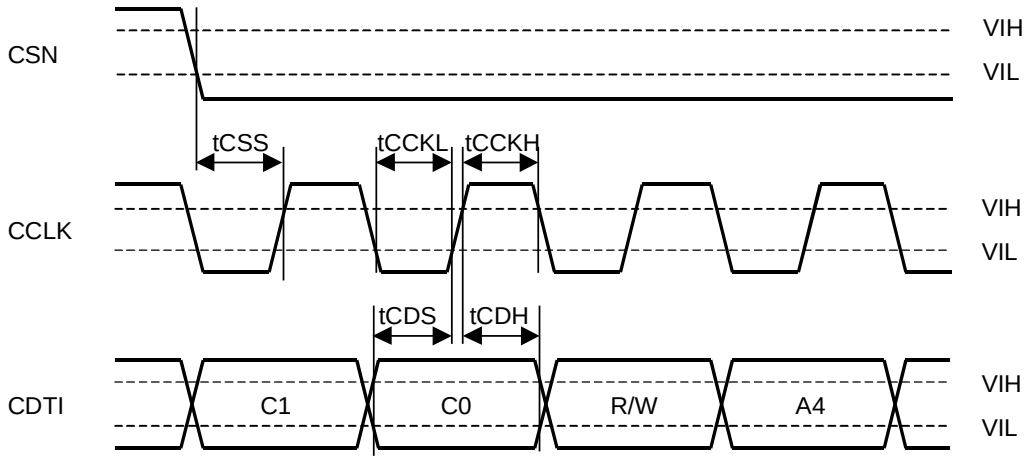


Figure 3. WRITE Command Input Timing

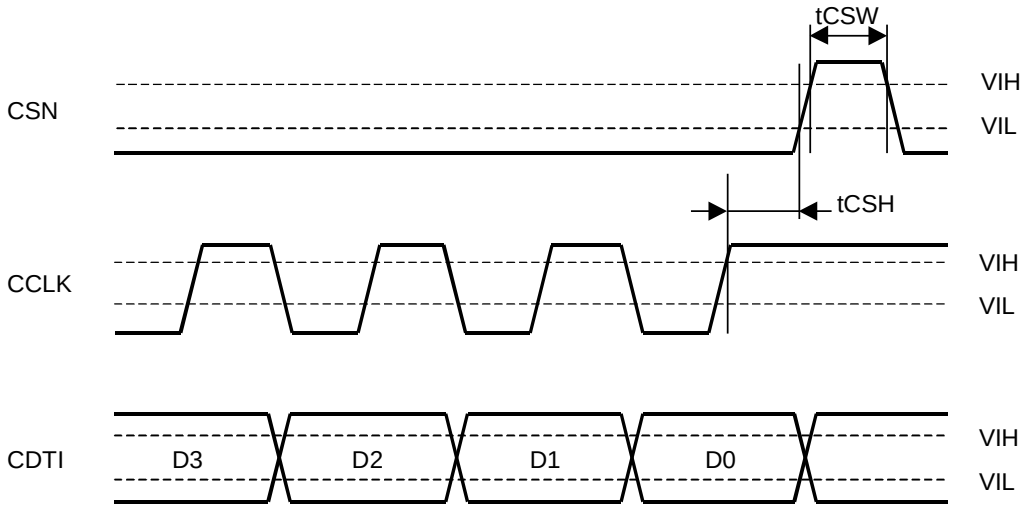


Figure 4. WRITE Data Input Timing

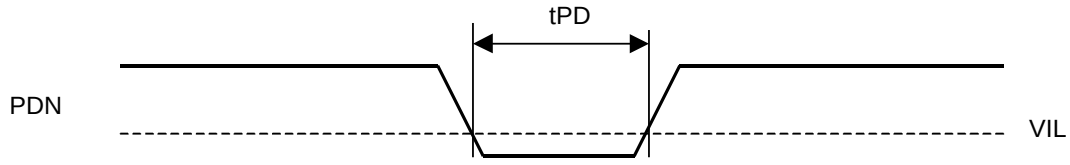


Figure 5. Power-down Timing

OPERATION OVERVIEW

■ System Clock

The AK4340 requires MCLK, BICK and LRCK external clocks. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2) After exiting reset (PDN pin = "↑"), the AK4340 is in Auto Setting Mode. In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 3), and the internal master clock becomes the appropriate frequency (Table 4), it is not necessary to set DFS0/1.

In parallel control mode, the sampling speed can be set by only ACKS pin. The internal DFS0 and DFS1 bits are fixed to "0". Therefore, when ACKS pin is "L", the AK4340 operates in Normal Speed Mode. The AK4340 operates in Auto Setting Mode at ACKS pin = "H". In parallel control mode, the AK4340 does not support 128fs and 192fs of Double Speed Mode.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4340 is in the normal operation mode (PDN pin = "H"). If these clocks are not provided, the AK4340 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. The AK4340 should be reset by PDN pin = "L" after these clocks are provided. If the external clocks are not present, the AK4340 should be in the power-down mode (PDN pin = "L"). After exiting reset at power-up etc., the AK4340 is in the power-down mode until MCLK and LRCK are input.

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	Default
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

DFS1	DFS0	Sampling Speed	LRCK (kHz)	MCLK(MHz)							BICK (MHz)
			fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
0	0	Normal	32.0	-	-	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480
0	0		44.1	-	-	11.2896	16.9344	22.5792	33.8688	-	2.8224
0	0		48.0	-	-	12.2880	18.4320	24.5760	36.8640	-	3.0720
0	1	Double	88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	5.6448
0	1		96.0	12.2880	18.4320	24.5760	36.8640	-	-	-	6.1440
1	0	Quad	176.4	22.5792	33.8688	-	-	-	-	-	11.2896
1	0		192.0	24.5760	36.8640	-	-	-	-	-	12.2880

Table 2. System Clock Example (Manual Setting Mode)

MCLK		Sampling Speed
1152fs		Normal (fs=32kHz Only)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 3. Sampling Speed (Auto Setting Mode: Default at Serial control mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 4. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. In serial control mode, five serial data mode can be selected by DIF2-0 bits. (See Table 5). In parallel control mode, two serial data mode can be selected by DIF0 pin. (See Table 6) In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure	
0	0	0	0	16bit LSB Justified	≥32fs	Figure 6	
1	0	0	1	20bit LSB Justified	≥40fs	Figure 7	
2	0	1	0	24bit MSB Justified	≥48fs	Figure 8	Default
3	0	1	1	24bit I^2S Compatible	≥48fs	Figure 9	
4	1	0	0	24bit LSB Justified	≥48fs	Figure 7	

Table 5. Audio Data Format in Serial control mode

Mode	DIF0	SDTI Format	BICK	Figure
2	0	24bit MSB Justified	≥48fs	Figure 8
3	1	24bit I^2S Compatible	≥48fs	Figure 9

Table 6. Audio Data Format in Parallel control mode

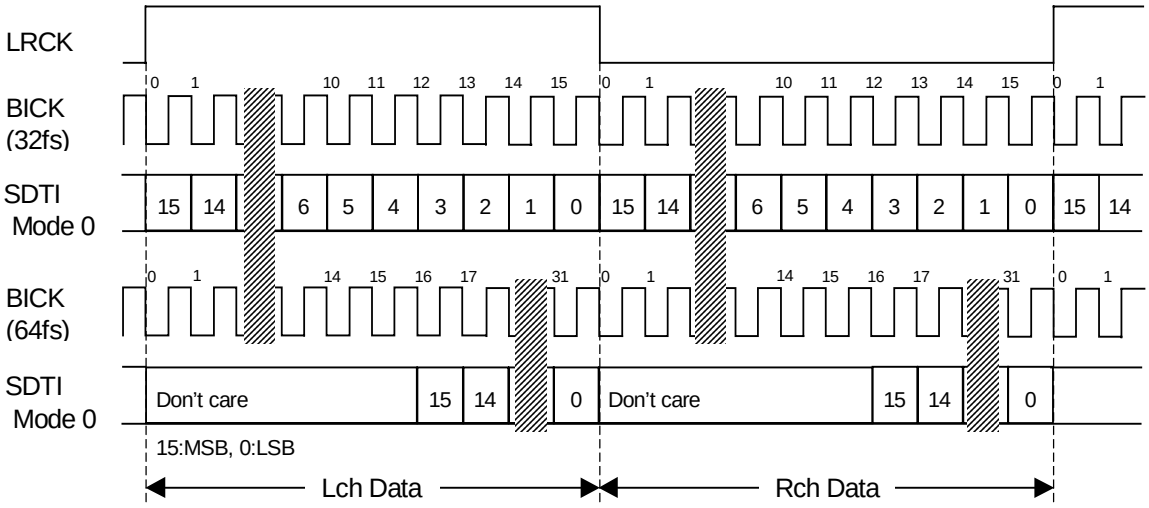


Figure 6. Mode 0 Timing

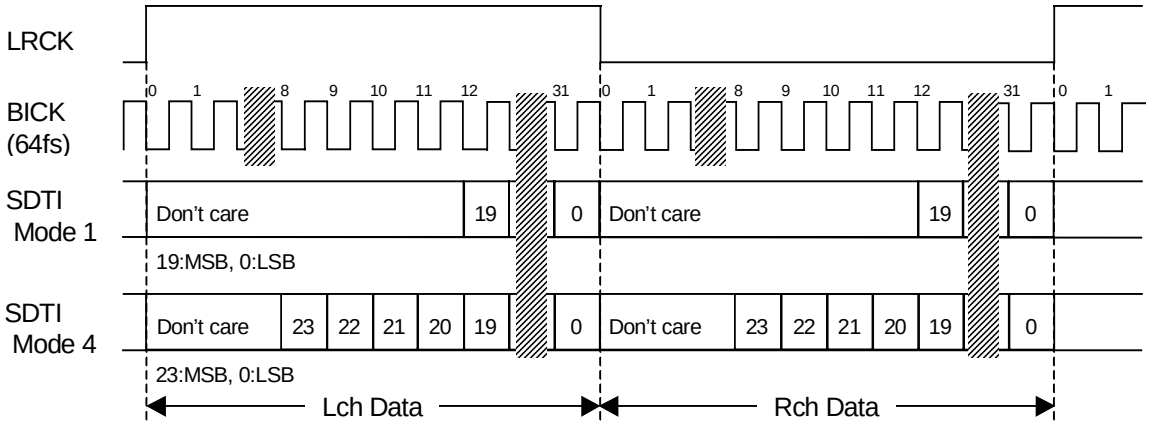


Figure 7. Mode 1,4 Timing

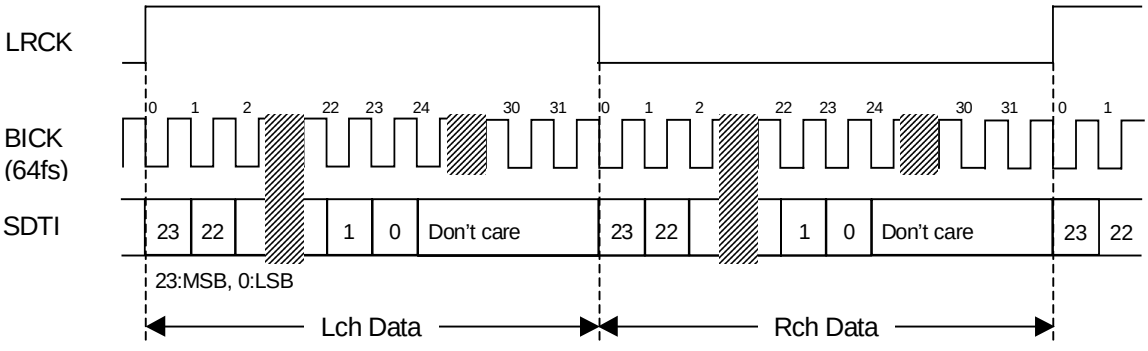


Figure 8. Mode 2 Timing

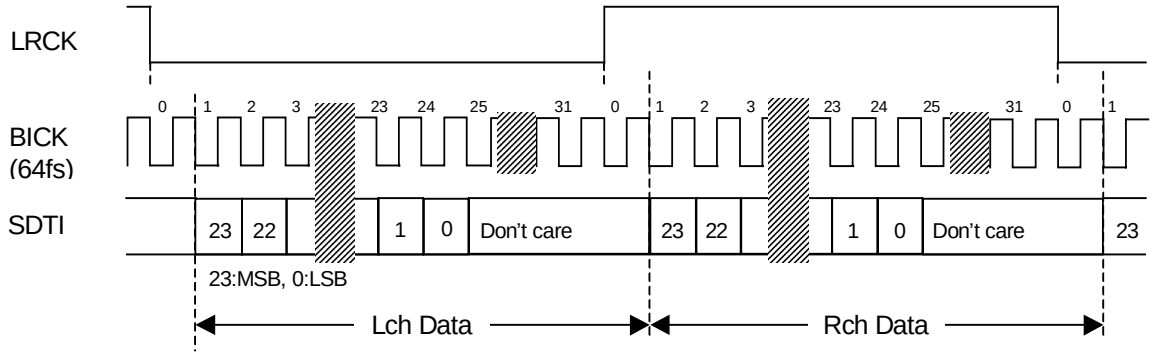


Figure 9. Mode 3 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always OFF.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 7. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4340 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 8.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 8. ATT Transition Time

■ Output Gain Setting

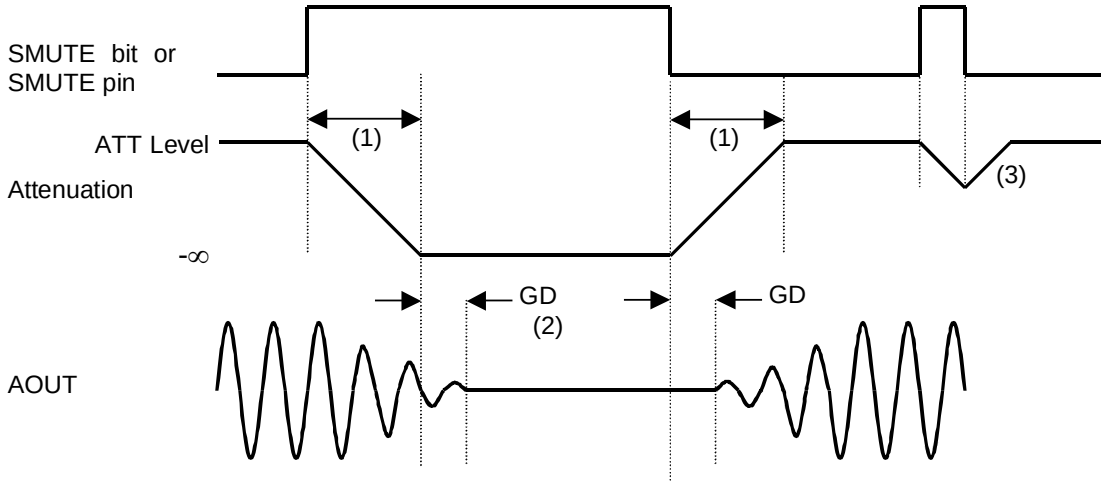
Outputs level of AOUTL/AOUTR pin can be selected by GAIN pin.

GAIN pin	GAIN	Output Level (VDD=5V)
L	0dB	2Vrms (typ)
H	+1.94dB	2.5Vrms (typ)

Figure 10. Output Level Setting

■ Soft Mute Operation

Soft mute operation is performed in digital domain. When the SMUTE bit (SMUTE pin) goes to "1"("H"), the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 8) from the current ATT level. When the SMUTE bit (SMUTE pin) is returned to "0" ("L"), the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 8). For example, in Normal Speed Mode, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

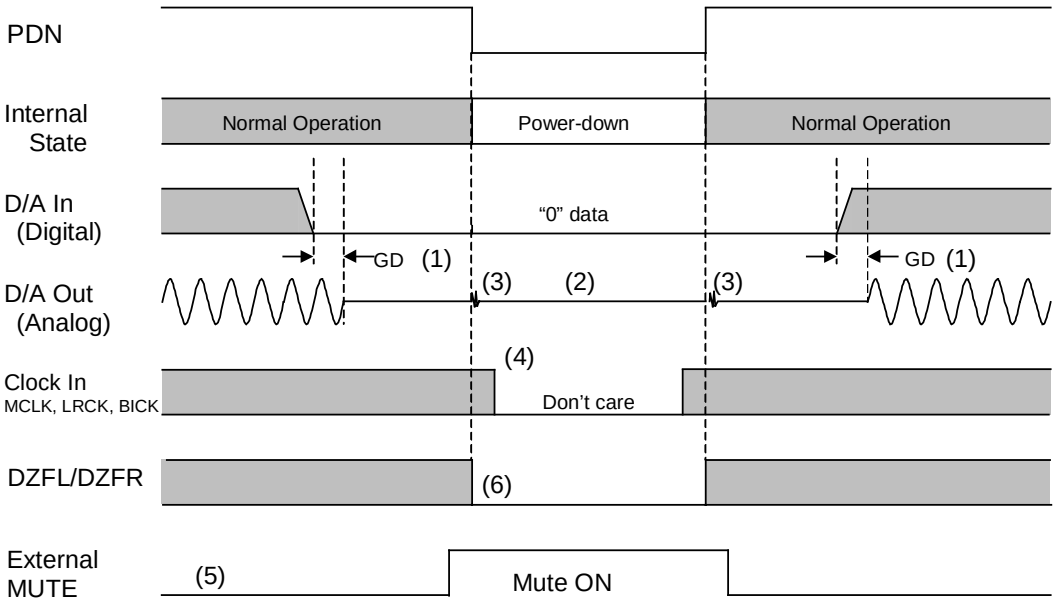
Figure 11. Soft Mute function

■ System Reset

The AK4340 should be reset once by bringing PDN pin = "L" upon power-up. The AK4340 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4340 is in the power-down mode until MCLK and LRCK are input.

■ Power-down

The AK4340 is placed in the power-down mode by bringing PDN pin "L" and the analog outputs are GND. Figure 6 shows an example of the system timing at the power-down and power-up.



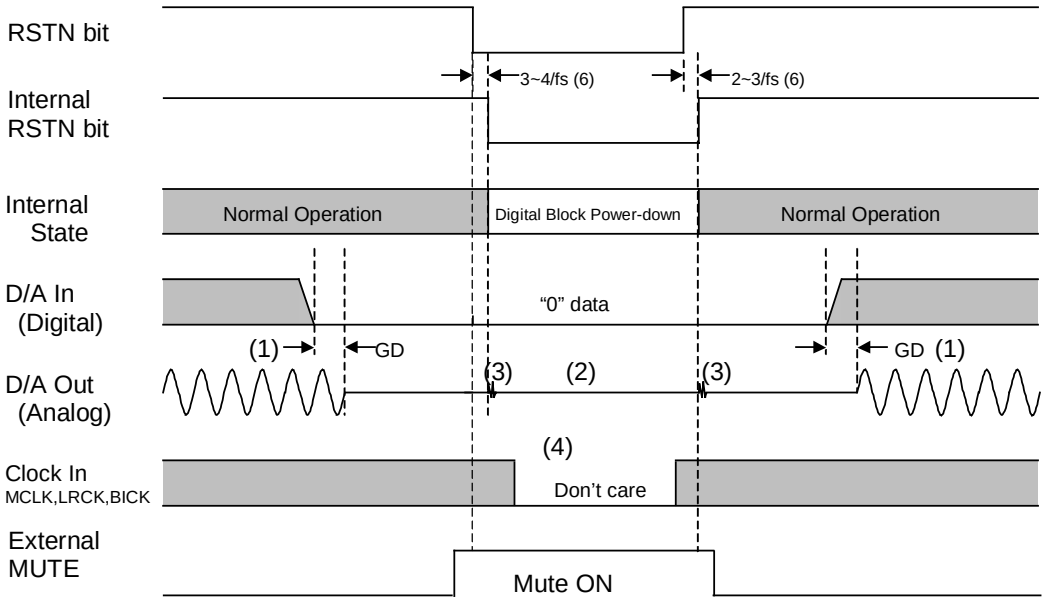
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.

Figure 12. Power-down/up Sequence Example

■ Reset Function

When RSTN=0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZF pin goes to "H". Figure 7 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage (VDD/2).
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN "1".

Figure 13. Reset Sequence Example

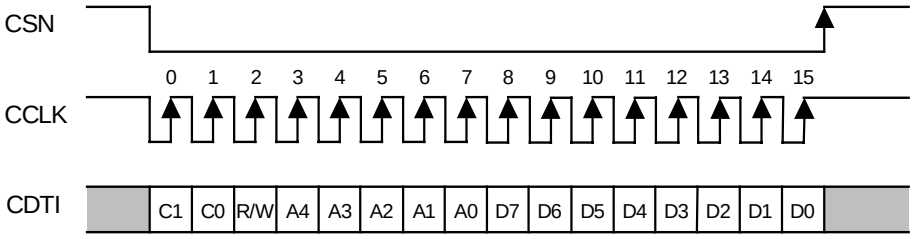
■ Mode Control Interface

Some function of the AK4340 can be controlled by pins (parallel control mode) shown in Table 11. The serial control interface is enabled by the P/S pin = "L". Internal registers may be written to 3-wire µP interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4340 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel control mode	Serial control mode
Double sampling mode at 128/192fs	X	O
De-emphasis	X	O
SMUTE	O	O
16/20/24bit LSB justified format	X	O

Table 11. Function list (O: available, X: not available)

PDN pin = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4340 should be reset by PDN pin = "L". The internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 14. Control I/F Timing

*The AK4340 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4340 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	0	0	0	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	0	INVL	INVR	0	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

For addresses from 05H to 1FH, data must not be written.

When PDN pin goes "L", the registers are initialized to their default values.

When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values. All data can be written to the register even if PW or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
default		1	0	0	0	1	0	1	1

RSTN: Internal timing reset control
0: Reset. All registers are not initialized.
1: Normal Operation
When MCLK frequency or DFS changes, the click noise can be reduced by RSTN bit.

PW: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation

DIF2-0: Audio data interface formats (see Table 5)
Initial: "010", Mode 2

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the settings of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	DFS1	DFS0	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (see Table 7)
Initial: "01", OFF

DFS1-0: Sampling speed control
00: Normal Speed Mode
01: Double Speed Mode
10: Quad Speed Mode
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	0	INVL	INVR	0	0	0
default		0	0	0	0	0	0	0	0

INVR: Inverting Lch Output Polarity
0: Normal Output
1: Inverted Output

INVL: Inverting Rch Output Polarity
0: Normal Output
1: Inverted Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
default		1	1	1	1	1	1	1	1

$ATT = 20 \log_{10} (ATT_DATA / 255)$ [dB]
00H: Mute

SYSTEM DESIGN

Figure 15and Figure 16 show the system connection diagram. An evaluation board (AKD4340) is available in order to allow an easy study on the layout of a surround circuit.

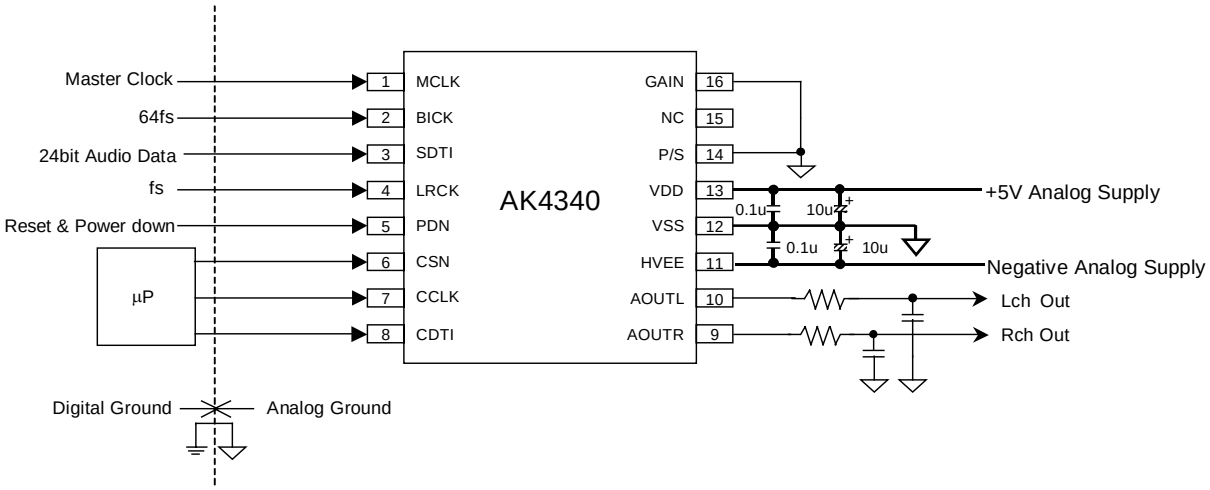


Figure 15. Typical Connection Diagram (Serial Control Mode, GAIN=0dB)

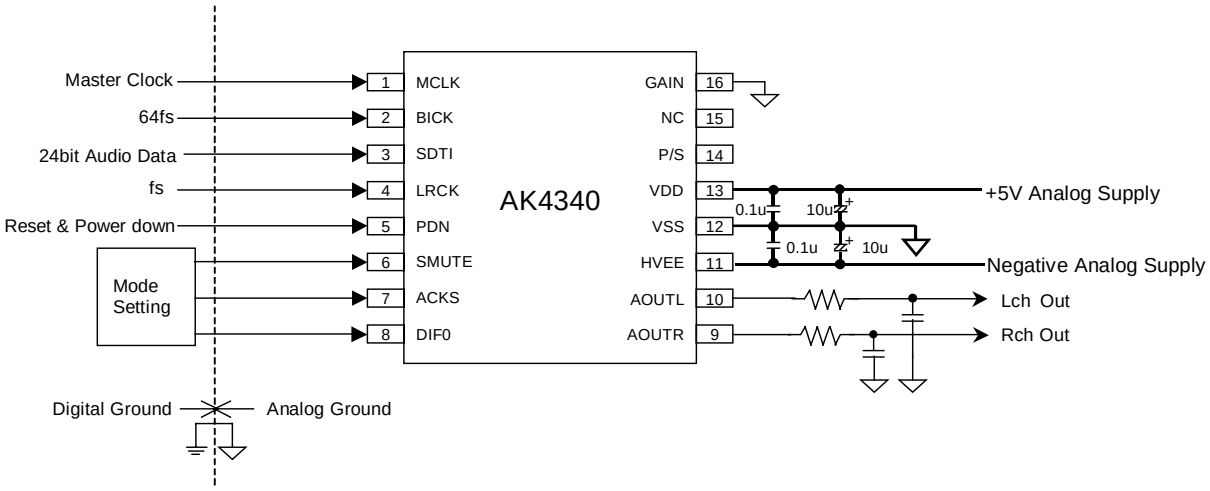


Figure 16. Typical Connection Diagram (Parallel Control Mode, GAIN=0dB)

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except for pull-up pin must not be left floating.

1. Grounding and Power Supply Decoupling

VDD, HVEE and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD and HVEE as possible. The differential Voltage between VDD and VSS pins set the analog output range.

Power-up sequence between VDD and HVEE is not critical.

2. Analog Outputs

The analog outputs are single-ended and centered around the ground (VSS). The output signal range is typically 2Vrms (@VDD=5V & GAIN pin = "L"). The phase of the analog outputs can be inverted channel independently by INVL/INVR bits. The internal switched capacitor filter (SCF) and continuous time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the 1st order filter is required. (See Figure 17)

The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is 0V(VSS) for 000000H (@24bit).

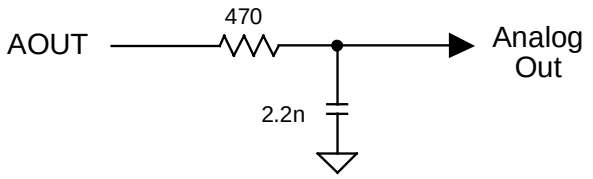
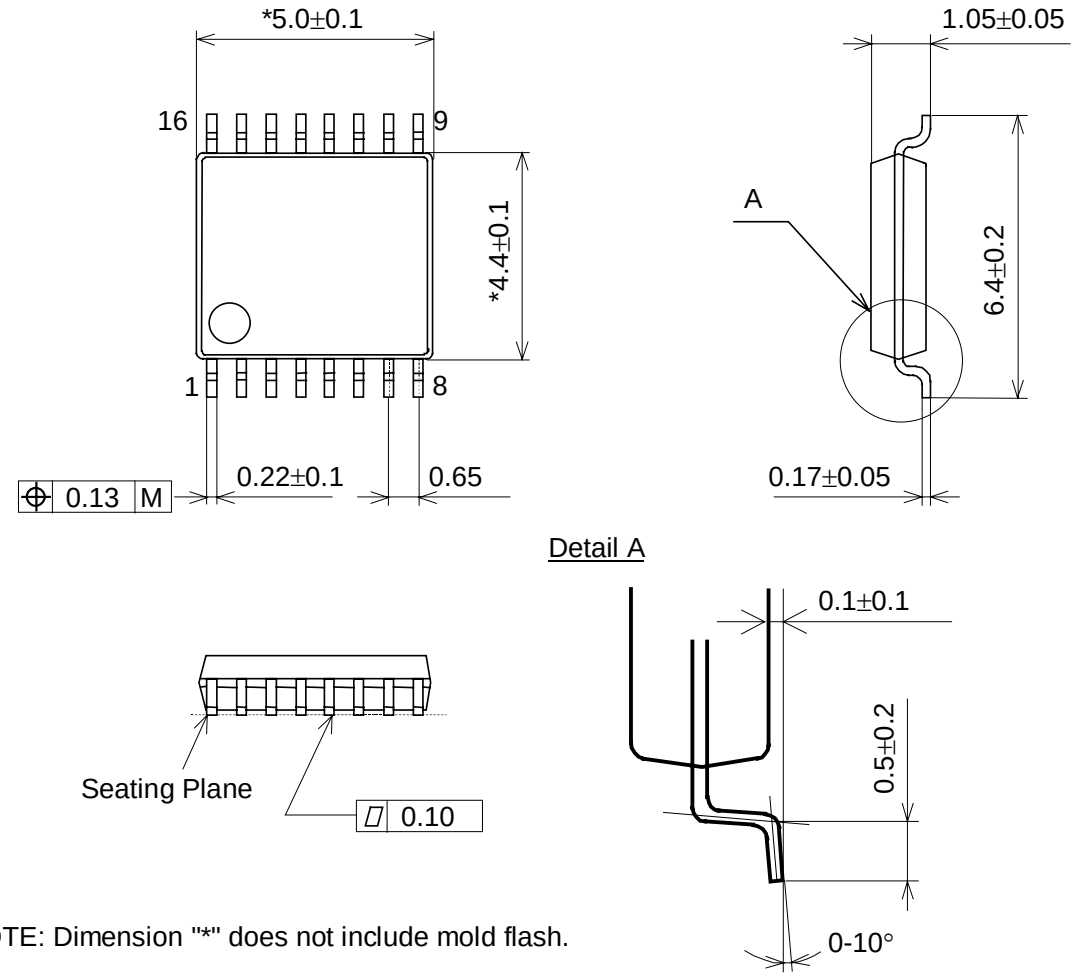


Figure 17. External 1st order LPF Circuit Example
(fc = 154kHz, gain = -0.28dB @ 40kHz, gain = -1.04dB @ 80kHz)

PACKAGE

16pin TSSOP (Unit: mm)

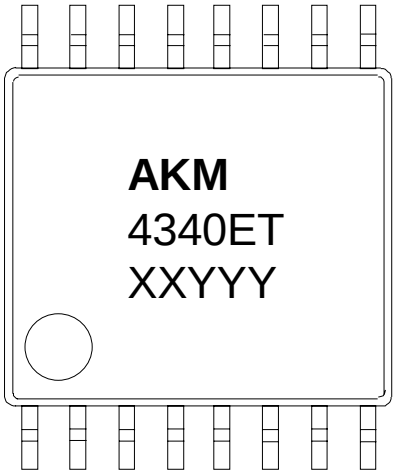


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4340ET
4) Asahi Kasei Logo

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/04/24	00	First Edition		

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