AKD4126-A
AK4126 Evaluation Board Rev.2

GENERAL DESCRIPTION

The AKD4126-A is an evaluation board for the AK4126, the digital sample rate converter. The AKD4126-A has the digital audio interface and can achieve the interface with digital audio system via opt-connector.

■ **Ordering guide**

AKD4126-A --- AK4126 Evaluation Board

FUNCTION

- **DIR/DIT with optical input/output**
- **10pin Header for AKM AD/DA evaluation board**

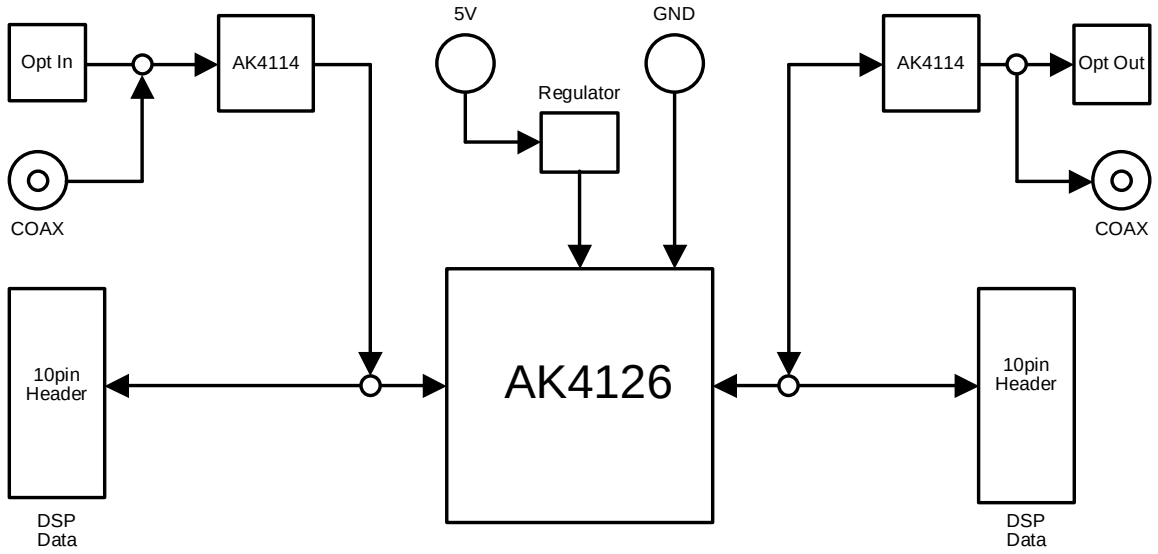


Figure 1. AKD4126-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

[1] Set up lines of power supply

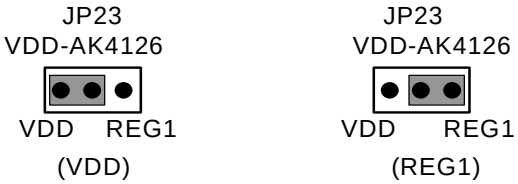
[VDD] (Red) = +5[V]
(Power supply for regulator REG1 and REG2. REG1 and REG2 supplies 3.3V to the AKD4126-A.)
[GND] (Black) = 0[V]

[2] Set up jumper pins of power supply

(1). Set up AVDD1 and DVDD1 (Set up AVDD and DVDD of the AK4126)

Power supply source of AVDD1 and DVDD1 is selected by JP23.

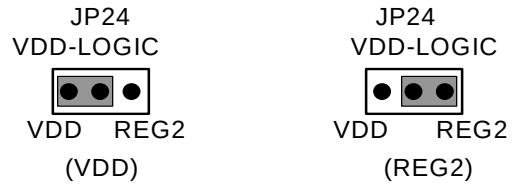
(a) From VDD terminal (b) From REG1



(2). Set up VDD1 and VDD2 (Set up AVDD, DVDD and TVDD of the AK4114, VDD of logic IC and others)

Power supply source of VDD1 and VDD2 is selected by JP24.

(a) From VDD terminal (b) From REG2



[3] Evaluation modes

(1). Input PORT

(1)-1. DIR functions of the AK4114 (U2) are used. (Default)

(1)-2. External equipments are connected via 10-pin connector (PORT2).

(2). Output PORT

(2)-1. DIT functions of the AK4114 (U3) are used. (Default)

(2)-2. External equipments are connected via 10-pin connector (PORT4).

[4] Set up jumper pins and DIP-switches of evaluation modes. (Refer to the following.)

[5] Power on.

Power down reset of the AK4126 (U1), the AK4114 (U2) and the AK4114 (U3) should be done once after power on. Method of power down reset of them is that after once put them on power-down bringing toggle switches SW6 and SW8 to “L”, release them from power-down bringing toggle switches SW6 and SW8 to “H”.

■ Set up jumper pins and DIP-switches of evaluation modes

(1). Set up jumper pins and DIP-switches of input PORT

(1)-1. DIR functions of the AK4114 (U2) are used. (Default)

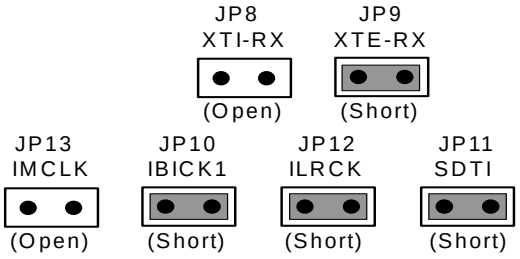
(1)-1-1. Set up RX

Select input connector of RX by JP7 (RX).

(a) RX is input from PORT1 (OPT) (b) RX is input from J1 (COAX)

(1)-1-2. Set up IBICK, ILRCK and SDTI

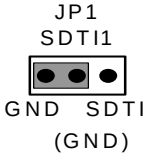
Clocks (IBICK and ILRCK) and data (SDTI) of the AK4126 (U1) are supplied from the AK4114 (U2).
As 10-pin connector: PORT2 (INPUT) is not used, please don't connect anything.



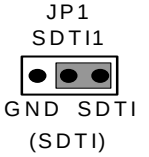
(1)-1-3. Set up SDTI1, SDTI2 and SDTI3

Select input data to SDTI1, SDTI2 and SDTI3 of the AK4126 (U1). When these jumper pins are set to SDTI side, SDTO of the AK4114 (U2) is input to SDTI1, SDTI2 and SDTI3. When these jumper pins are set to GND side, "0" data is input to SDTI1, SDTI2 and SDTI3.

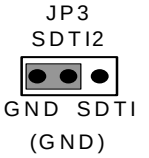
(a) "0" data is input to SDTI1



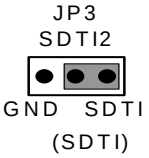
(b) SDTO of the AK4114 (U2) is input to SDTI1



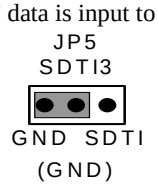
(a) "0" data is input to SDTI2



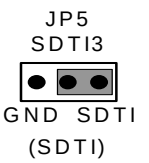
(b) SDTO of the AK4114 (U2) is input to SDTI2



(a) "0" data is input to SDTI3



(b) SDTO of the AK4114 (U2) is input to SDTI3



(1)-1-4. Set up PLL Mode and Input Audio Interface Format of the AK4126 (U1)

Set up PLL Mode and Input Audio Interface Format of the AK4126 (U1) by SW1. About setting of default, please refer to Table1. About setting except default, please refer to Table2 and Table3.

(1)-1-5. Set up Output Audio Interface Format, Clock Mode and Master Clock Frequency of the AK4114 (U2)

Set up Output Audio Interface Format, Clock Mode and Master Clock Frequency of theAK4114 (U2) by SW4. About setting of default, please refer to Table4. About setting except default, please refer to Table5, Table6, and Table7.

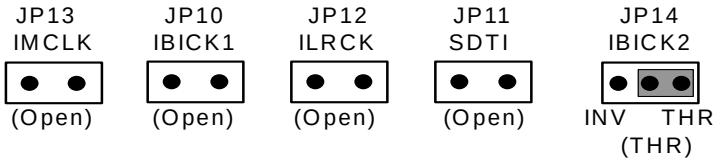
(1)-2. External equipments are connected via 10-pin connector (PORT2).

(1)-2-1. Set up RX

As Optical connector: PORT1 (OPT) and BNC connector: J1 (COAX) are not used, please don't connect anything.

(1)-2-2. Set up IBICK, ILRCK and SDTI

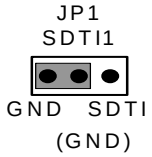
Clocks (IBICK and ILRCK) and data (SDTI) of AK4126 (U1) are supplied from external equipments via 10-pin connector: PORT2 (INPUT).



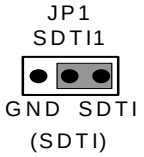
(1)-2-3. Set up SDTI1, SDTI2 and SDTI3

Select input data to SDTI1, SDTI2 and SDTI3 of the AK4126 (U1). When these jumper pins are set to SDTI side, output data of external equipment is input to SDTI1, SDTI2 and SDTI3 via 10-pin connector: PORT2 (INPUT). When these jumper pins are set to GND side, "0" data is input to SDTI1, SDTI2 and SDTI3.

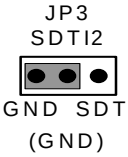
(a) "0" data is input to SDTI1



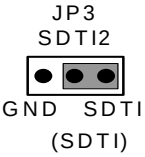
(b) Output data of external equipment is input to SDTI1



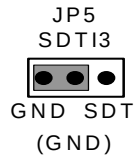
(a) "0" data is input to SDTI2



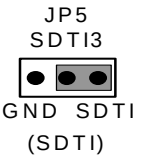
(b) Output data of external equipment is input to SDTI2



(a) "0" data is input to SDTI3



(b) Output data of external equipment is input to SDTI3



(1)-2-4. Set up PLL Mode and Input Audio Interface Format of the AK4126 (U1)

Set up PLL Mode and Input Audio Interface Format of the AK4126 (U1) by SW1. About setting of default, please refer to Table1. About setting except default, please refer to Table2 and Table3.

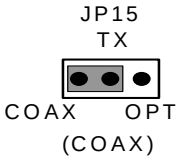
(2). Set up jumper pins and DIP-switches of output PORT

(2)-1. DIT functions of AK4114 (U3) are used. (Default)

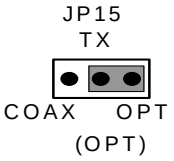
(2)-1-1. Set up TX

Select output connector of TX by JP15 (TX).

(a) TX is output from J3 (COAX)



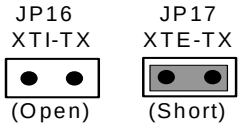
(b) TX is output from PORT3 (OPT)



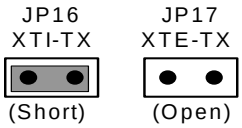
(2)-1-2. Set up XTI

Clock source of XTI of the AK4114 (U3) is selected by JP16 (XTI-TX) and JP17 (XTE-TX). When X'tal: X2 is selected, and OBICK frequency and OLRCK frequency are changed, the value of X'tal: X2 should be changed.

(a) XTI is supplied from X'tal: X2



(b) XTI is supplied from J4 (XTI-TX)



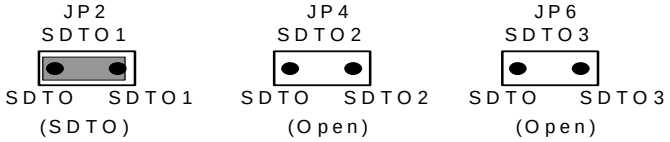
(2)-1-3. Set up OBICK, OLRCK and SDTO

Clocks (OBICK and OLRCK) of the AK4126 (U1) are supplied from the AK4114 (U3), and data (SDTO) of the AK4126 (U1) is output to the AK4114 (U3). As 10-pin connector: PORT4 (OUTPUT) is not used, please don't connect anything.

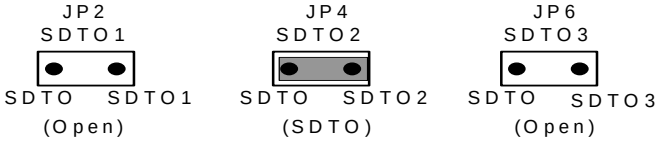
(2)-1-4. Set up SDTO1, SDTO2 and SDTO3

A data selected among SDTO1, SDTO2 and SDTO3 of the AK4126 (U1), is input to DAUX of the AK4114 (U3). SDTO1, SDTO2 and SDTO3 cannot be selected at same time.

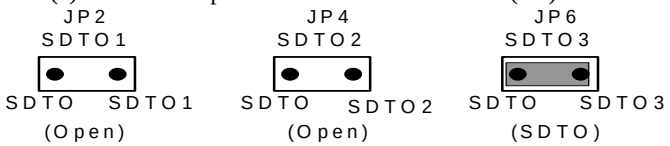
(a) SDTO1 is input to DAUX of the AK4114 (U3).



(b) SDTO2 is input to DAUX of the AK4114 (U3).



(c) SDTO3 is input to DAUX of the AK4114 (U3).



(2)-1-5. Set up Output Audio Interface Format 2 and Output Audio Interface Format 1 of the AK4126 (U1)

Set up Output Audio Interface Format 2 and Output Audio Interface Format 1 of the AK4126 (U1) by SW2. About setting of default, please refer to Table8. About setting except default, please refer to Table9, Table11.

(2)-1-6. Set up Input Audio Interface Format, Clock Mode and Master Clock Frequency of the AK4114 (U3)

Set up Input Audio Interface Format, Clock Mode and Master Clock Frequency of the AK4114 (U3) by SW5. About setting of default, please refer to Table12. About setting except default, please refer to Table13, Table14, and Table15.

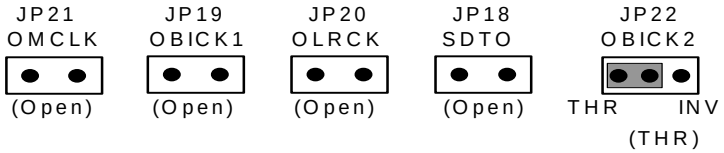
(2)-2. External equipments are connected via 10-pin connector (PORT4).

(2)-2-1. Set up TX

As Optical connector: PORT3 (OPT) and BNC connector: J3 (COAX) are not used, please don't connect anything.

(2)-2-2. Set up OBICK, OLRCK and SDTO

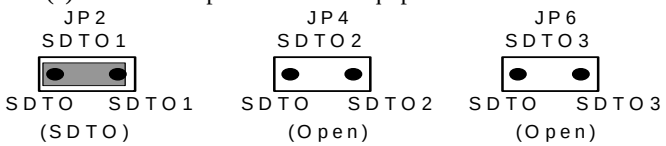
Clocks (OBICK and OLRCK) of the AK4126 (U1) are supplied from external equipment via 10-pin connector: PORT4 (OUTPUT), and output data (SDTO) of the AK4126 (U1) is output to external equipment via 10-pin connector: PORT4 (OUTPUT).



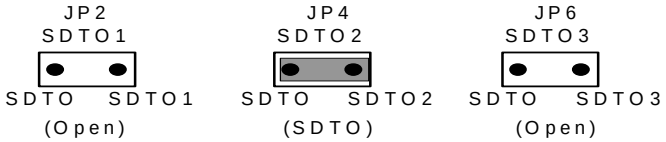
(2)-2-3. Set up SDTO1, SDTO2 and SDTO3

A data selected among SDTO1, SDTO2 and SDTO3 of the AK4126 (U1), is input to external equipment via 10-pin connector: PORT4 (OUTPUT). SDTO1, SDTO2 and SDTO3 cannot be selected at same time.

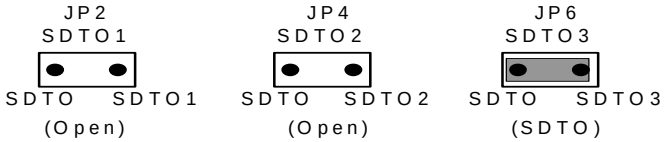
(a) SDTO1 is input to external equipment



(b) SDTO2 is input to external equipment



(c) SDTO3 is input to external equipment



(2)-2-4. Set up Output Audio Interface Format 2 and Output Audio Interface Format 1 of the AK4126 (U1)

Set up Output Audio Interface Format 2 and Output Audio Interface Format 1 of the AK4126 (U1) by SW2. About setting of default, please refer to Table8. About setting except default, please refer to Table9 and Table11.

(3). Set up other modes

(3)-1. Set up TEST Pin, Soft Mute Cycle Mode, De-emphasis Filter Mode and Channel Mode of the AK4126 (U1)

Set up TEST Pin, Soft Mute Cycle Mode, De-emphasis Filter Mode and Channel Mode of the AK4126 (U1) by SW3. About setting of default, please refer to Table16. About setting except default, please refer to Table17, Table18, and Table19.

- **Set up SW3**

ON is "H", and OFF is "L".
Setting of default is as follows. (Please refer to Table 16.)

SW3 No.	Name	ON ("H")	OFF ("L")	Default
1	TI2	AK4126 TEST Pin Fixed to "L".		L
2	TI1			L
3	TI0			L
4	SMT1	AK4126 Soft Mute Cycle Mode Setting (On Manual Mode) Please refer to Table 17.		L
5	SMT0			L
6	DEM1	AK4126 De-emphasis Filter Mode Setting Please refer to Table 18.		L
7	DEM0			H
8	PM	AK4126 Channel Mode Setting Please refer to Table 19.		L

Table 16. SW3 Setting

Mode	SMT1 pin	SMT0 pin	Period	Soft Mute Cycle			
				fso=48kHz	fso=96kHz	fso=192kHz	
0	L	L	1024/fso	21.3ms	10.7ms	5.3ms	(Default)
1	L	H	2048/fso	42.7ms	21.3ms	10.7ms	
2	H	L	4096/fso	85.3ms	42.7ms	21.3ms	
3	H	H	8192/fso	170.7ms	85.3ms	42.7ms	

Table 17. AK4126 Soft Mute Cycle Mode Setting (On Manual Mode)

Mode	DEM1 pin	DEM0 pin	De-emphasis Filter	
0	L	L	44.1kHz	
1	L	H	OFF	(Default)
2	H	L	48kHz	
3	H	H	32kHz	

Table 18. AK4126 De-emphasis Filter Mode Setting

Mode	PM pin	Channel Mode	
0	L	6-channel	(Default)
1	H	4-channel	

Table 19. AK4126 Channel Mode Setting

■ Set up DIP-switches

(1). Set up input mode

(1)-1. Set up the AK4126 (U1)

- **Set up SW1**

ON is "H", and OFF is "L".
Setting of default (Slave Mode, 24bit MSB justified, IBICK lock mode (64fsi), IBICK=Input, ILRCK=Input) is as follows. (Please refer to Table 1.)

SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	PLL2	AK4126 PLL Mode Setting Please refer to Table 2.		H
2	PLL1			L
3	PLL0			H
4	IDIF2	AK4126 Input Audio Interface Format Setting Please refer to Table 3.		L
5	IDIF1			H
6	IDIF0			L

Table 1. SW1 Setting

Mode	PLL2 pin	PLL1 pin	PLL0 pin	ILRCK Freq	IBICK Freq	SMUTE	
0	L	L	L	8k ~ 96kHz	Depending on IDIF2-0	Manual (Note 4)	
1	L	L	H	8k ~ 192kHz			
2	L	H	L	16k ~ 192kHz (Note 1)		Semi-Auto (Note 5)	
3	L	H	H	Reserved			
4	H	L	L	8k ~ 192kHz (Note 2)	32fsi (Note 3)	Manual (Note 4)	(Default)
5	H	L	H		64fsi		
6	H	H	L		128fsi		
7	H	H	H		64fsi	Semi-Auto (Note 5)	

Table2. AK4126 PLL Mode Setting (Input PORT)

(Note 1) PLL lock range is changed by values of R and C connected by FILT pin. For more further details, please refer to datasheet: "PLL Loop Filter".
(Note 2) IBICK should be always and continuously supplied, except when clocks are changed.
(Note 3) IBICK = 32fsi is applied to only two audio data formats of 16bit LSB justified and 16bit I^2S Compatible.
(Note 4) Please refer to datasheet: "Soft Mute Operation": "Manual mode".
(Note 5) Please refer to datasheet: "Soft Mute Operation ": "Semi-Auto mode".

Mode	IDIF2 pin	IDIF1 pin	IDIF0 pin	SDTI Format	IBICK Freq	
0	L	L	L	16bit, LSB justified	≥ 32fsi	
1	L	L	H	20bit, LSB justified	≥ 40fsi	
2	L	H	L	24/20bit, MSB justified	≥ 48fsi	(Default)
3	L	H	H	24/16bit, I2S Compatible	≥ 48fsi or 32fsi	
4	H	L	L	24bit, LSB justified	≥ 48fsi	
5	H	L	H	Reserved		
6	H	H	L	Reserved		
7	H	H	H	Reserved		

Table 3. AK4126 Input Audio Interface Format Setting (Input PORT)

(1)-2. Set up the AK4114 (U2)

- **Set up SW4**

ON is "H", and OFF is "L".
Setting of default (Master mode, 24bit Left justified) is as follows. (Please refer to Table 4.)

SW4 No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Output Audio Interface Format Setting Please refer to Table 5.		H
2	DIF1			L
3	DIF0			L
4	CM1	AK4114 Clock Mode Setting Fixed to "L".		L
5	CM0			L
6	OCKS1	AK4114 Master Clock Frequency Setting Please refer to Table 7.		H
7	OCKS0			L

Table 4. SW4 Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	SDTO Format	LRCK		BICK		
						I/O		I/O	
0	L	L	L	16bit, Right justified	H/L	O	64fs	O	
1	L	L	H	18bit, Right justified	H/L	O	64fs	O	
2	L	H	L	20bit, Right justified	H/L	O	64fs	O	
3	L	H	H	24bit, Right justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	H/L	O	64fs	O	(Default)
5	H	L	H	24bit, I^2S Compatible	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit, I^2S Compatible	L/H	I	64-128fs	I	

Table 5. AK4114 Output Audio Interface Format Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	MCKO2	X'tal	fs (max)	
0	L	L	256fs	256fs	256fs	96 kHz	
1	L	H	256fs	128fs	256fs	96 kHz	
2	H	L	512fs	256fs	512fs	48 kHz	(Default)
3	H	H	128fs	64fs	128fs	192 kHz	

Table 7. AK4114 Master Clock Frequency Setting

(2). Set up output mode

(2)-1. Set up the AK4126 (U1)

- **Set up SW2**

  ON is "H", and OFF is "L".
  Setting of default (Slave Mode, 24bit MSB justified, OLRCK=Input, OBICK=Input, fso=8K~192KHz) is as follows. (Please refer to Table 8.)

SW2 No.	Name	ON ("H")	OFF ("L")	Default
1	DITHER	Dither ON	Dither OFF	L
2	OBIT1	AK4126 Output Audio Interface Format 2 Setting		H
3	OBIT0	Please refer to Table 9.		H
4	TEST1	AK4126 TEST Pin. Fixed to "H".		H
5	TEST2	AK4126 TEST Pin. Fixed to "L".		L
6	TEST3			L
7	ODIF1	AK4126 Output Audio Interface Format 1 Setting		H
8	ODIF0	Please refer to Table 11.		L

Table 8. SW2 Setting

Mode	OBIT1 pin	OBIT0 pin	SDTO	OBICK Frequency	
				MSB justified, I2S Compatible	LSB justified
0	L	L	16bit	≥ 32fso	64fso
1	L	H	18bit	≥ 36fso	
2	H	L	20bit	≥ 40fso	
3	H	H	24bit	≥ 48fso	

(Default)

Table 9. AK4126 Output Audio Interface Format 2 Setting (Output PORT)

Mode	ODIF1 pin	ODIF0 pin	SDTO Format
0	L	L	LSB justified
1	L	H	(Reserved)
2	H	L	MSB justified
3	H	H	I^2S Compatible

(Default)

Table 11. AK4126 Output Audio Interface Format 1 Setting (Output PORT)

(2)-2. Set up the AK4114 (U3)

- **Set up SW5**

ON is "H", and OFF is "L".
Setting of default (Master mode, 24bit Left justified) is as follows. (Please refer to Table 12.)

SW5 No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Input Audio Interface Format Setting Please refer to Table 13.		H
2	DIF1			L
3	DIF0			L
4	CM1	AK4114 Clock Mode Setting Fixed to "L".		L
5	CM0	AK4114 Clock Mode Setting Fixed to "H".		H
6	OCKS1	AK4114 Master Clock Frequency Setting Please refer to Table 15.		L
7	OCKS0			L

Table 12. SW5 Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	DAUX Format	LRCK		BICK		
						I/O		I/O	
0	L	L	L	24bit, Left justified	H/L	O	64fs	O	
1	L	L	H	24bit, Left justified	H/L	O	64fs	O	
2	L	H	L	24bit, Left justified	H/L	O	64fs	O	
3	L	H	H	24bit, Left justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	H/L	O	64fs	O	(Default)
5	H	L	H	24bit, I^2S Compatible	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit, I^2S Compatible	L/H	I	64-128fs	I	

Table 13. AK4114 Input Audio Interface Format Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	MCKO2	X'tal	fs (max)	
0	L	L	256fs	256fs	256fs	96 kHz	(Default)
1	L	H	256fs	128fs	256fs	96 kHz	
2	H	L	512fs	256fs	512fs	48 kHz	
3	H	H	128fs	64fs	128fs	192 kHz	

Table 15. AK4114 Master Clock Frequency Setting

■ Toggle Switch Operation

Upper side is “H” and lower side is “L”.

[SW6] (PDN-AK4126): Power down switch of the AK4126 (U1).
The AK4126 (U1) should be reset once by bringing to “L” upon power-up.
Keep “H” during normal operation.

[SW7] (SMUTE-AK4126): Soft mute switch of the AK4126 (U1).
Output of the AK4126 (U1) is soft-muted by bringing to “H”.

[SW8] (PDN-AK4114-RX/TX): Power down switch of the AK4114 (U2) and the AK4114 (U3).
The AK4114 (U2) and the AK4114 (U3) should be reset once by bringing to “L” upon power-up.
Keep “H” during normal operation.

■ LED Indication

[LED1] (UNLOCK): Output of UNLOCK pin of the AK4126 (U1).
Turns on when PLL of the AK4126 (U1) is unlocked.

[LED2] (INT0): Output of INT0 pin of the AK4114 (U2).
Turns on when the AK4114 (U2) is unlocked.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- Power Supply : AVDD=DVDD=3.3V
- Band width : 20Hz ~ FSO/2
- Temperature : Room

[Measurement Result]

SRC Characteristics	SDTO1 Lch	SDTO1 Rch	SDTO2 Lch	SDTO2 Rch	SDTO3 Lch	SDTO3 Rch	Unit
THD+N							
(Input = 1kHz, 0dBFS)							
FSO/FSI = 44.1kHz/48kHz	130.2	130.2	130.2	130.2	130.2	130.2	dB
FSO/FSI = 48kHz/44.1kHz	124.9	124.9	124.9	124.9	124.9	124.9	dB
FSO/FSI = 48kHz/192kHz	136.2	136.2	136.2	136.2	136.2	136.2	dB
FSO/FSI = 192kHz/48kHz	124.9	124.9	124.9	124.9	124.9	124.9	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)	96.1	96.1	96.1	96.1	96.1	96.1	dB
Dynamic Range							
(Input = 1kHz, –60dBFS)							
FSO/FSI = 44.1kHz/48kHz	136.2	136.2	136.2	136.2	136.2	136.2	dB
FSO/FSI = 48kHz/44.1kHz	136.4	136.4	136.4	136.4	136.4	136.4	dB
FSO/FSI = 48kHz/192kHz	136.2	136.2	136.2	136.2	136.2	136.2	dB
FSO/FSI = 192kHz/48kHz	135.6	135.6	135.6	135.6	135.6	135.6	dB
FSO/FSI = 48kHz/32kHz	137.3	137.3	137.3	137.3	137.3	137.3	dB
Dynamic Range							
(Input = 1kHz, –60dBFS, A-weighted)							
FSO/FSI = 44.1kHz/48kHz	139.6	139.6	139.6	139.6	139.6	139.6	dB

[Plot]

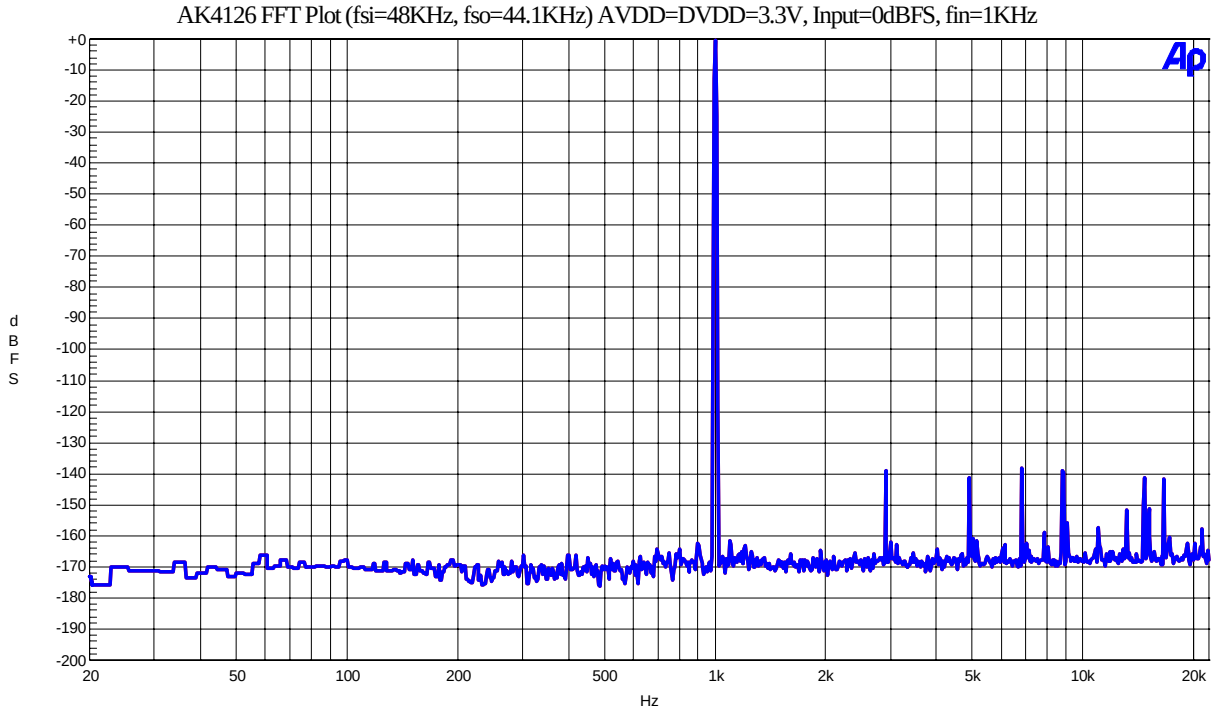


Fig 6. FFT Plot (Input = 0dBFS)

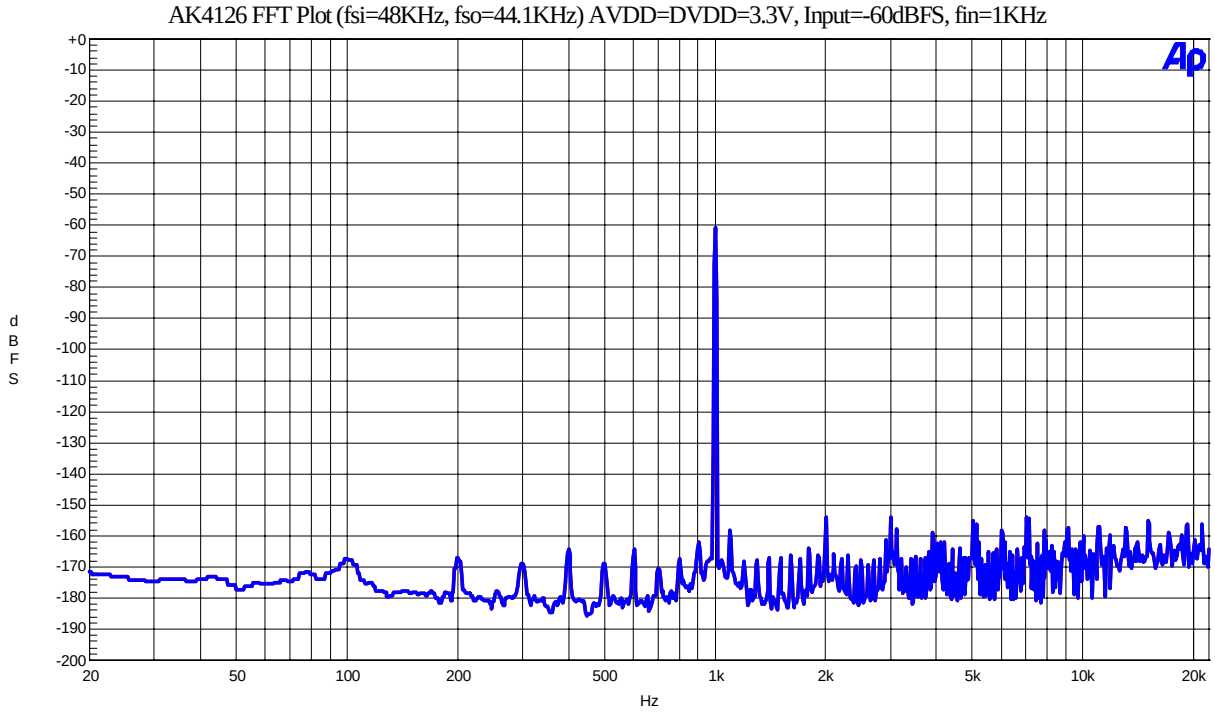


Fig 7. FFT Plot (Input = -60dBFS)

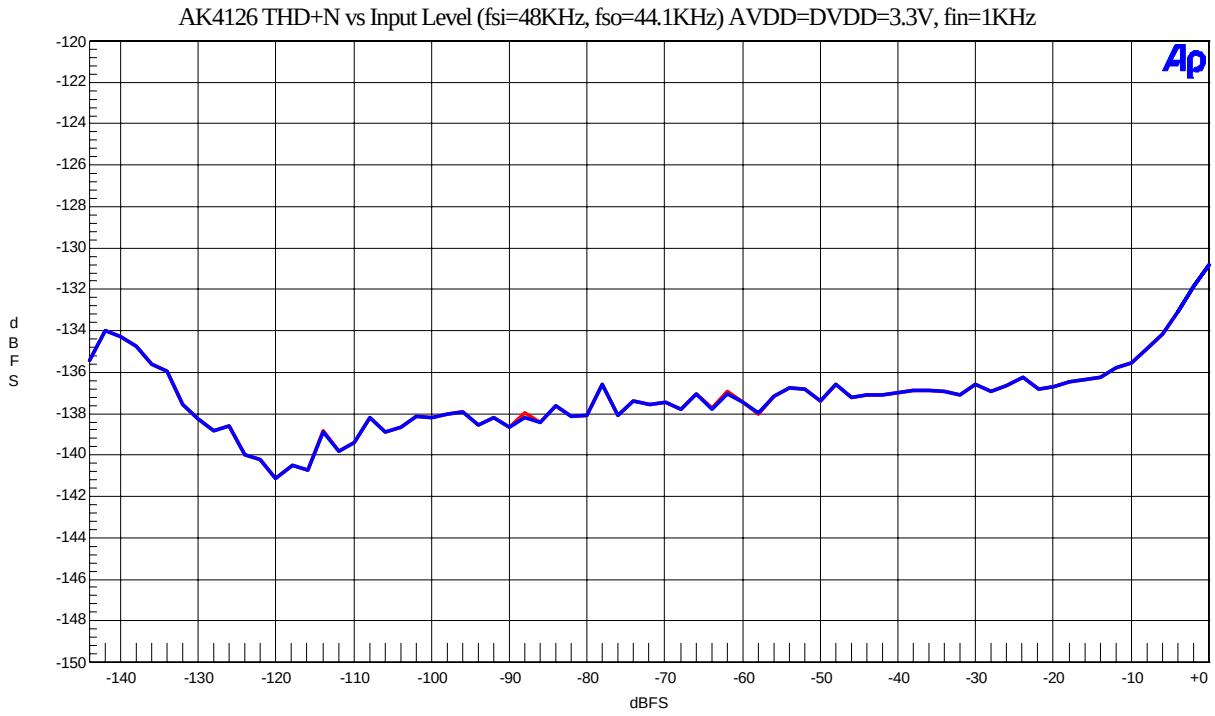


Fig 1. THD+N vs. Input Level

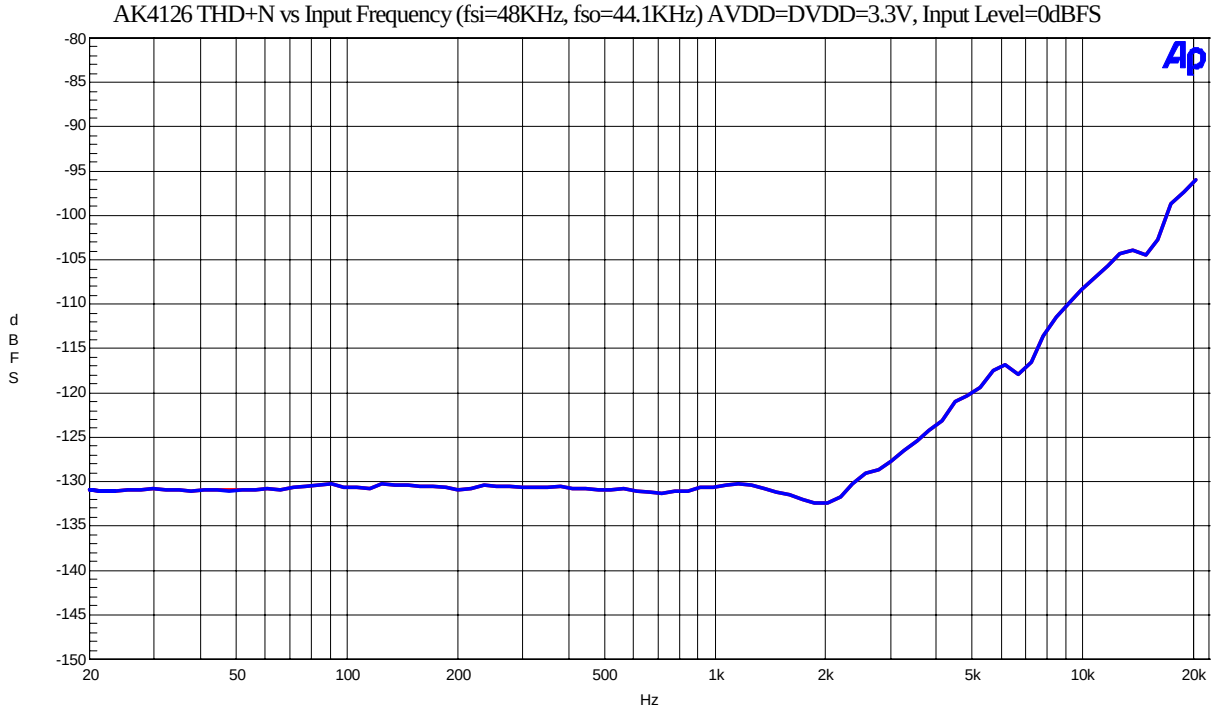


Fig 2. THD+N vs. Input Frequency (Input = 0dBFS)

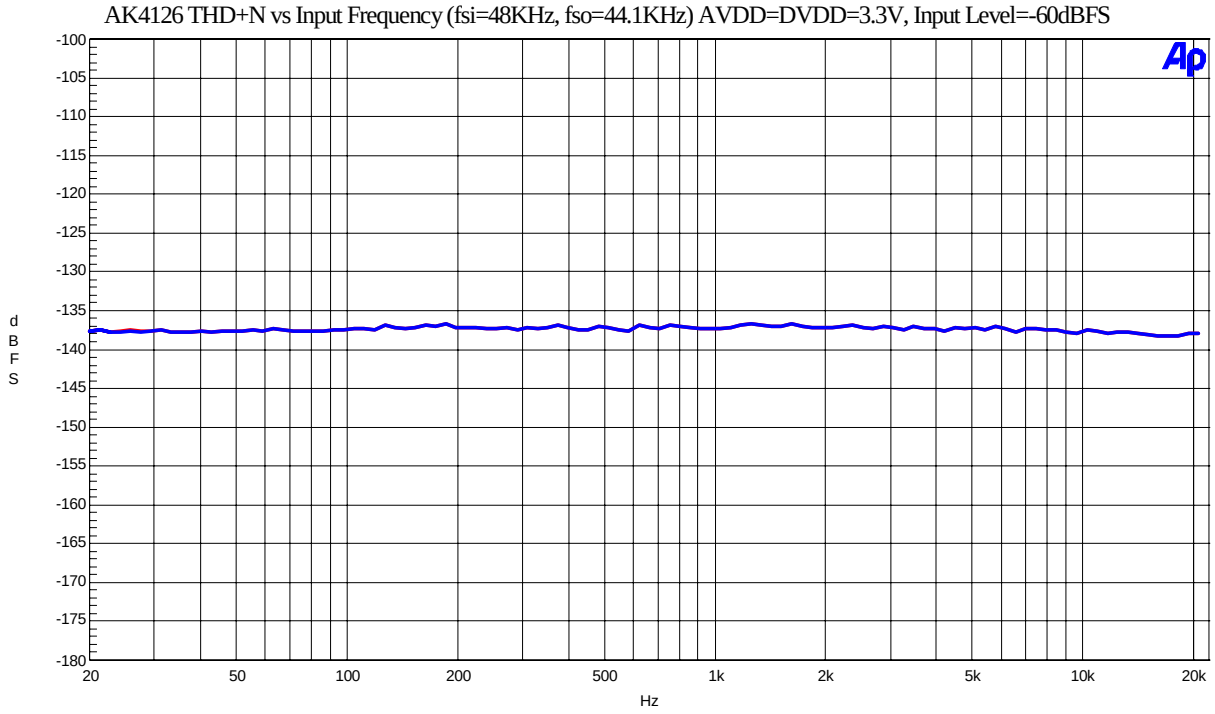


Fig 3. THD+N vs. Input Frequency (Input = -60dBFS)

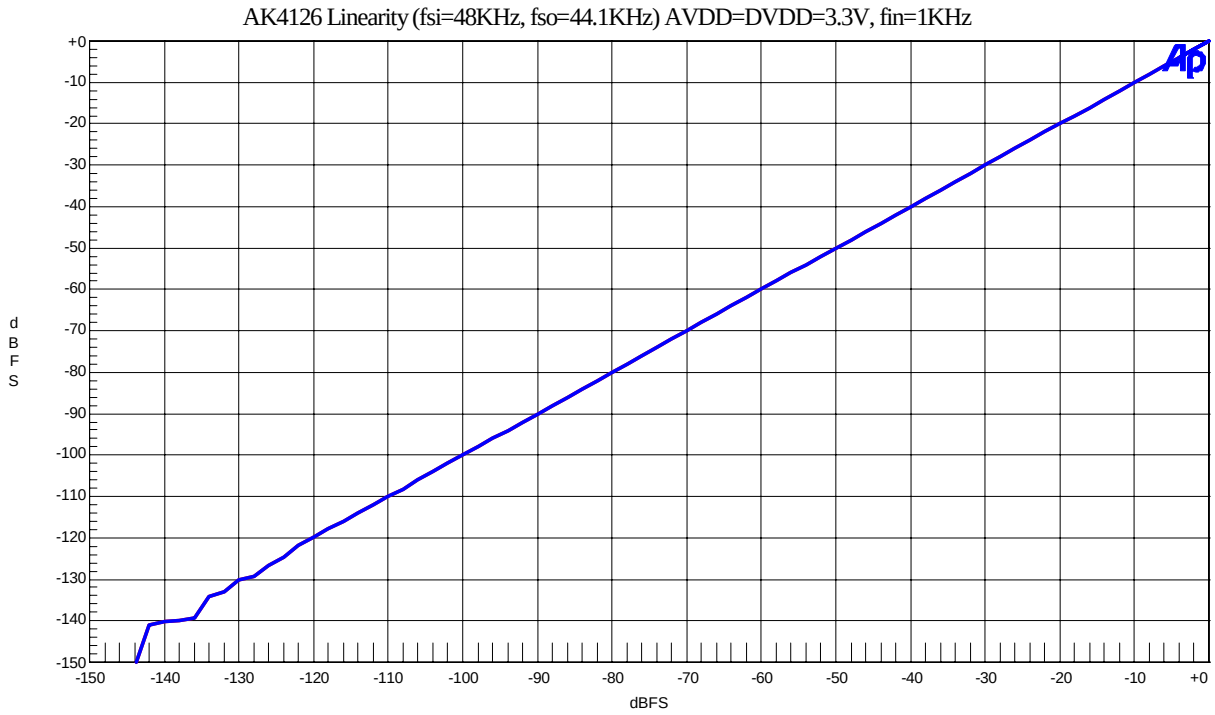


Fig 4. Linearity

AK4126 Frequency Response (fsi=48KHz, fso=44.1KHz) AVDD=DVDD=3.3V, Input Level=0dBFS

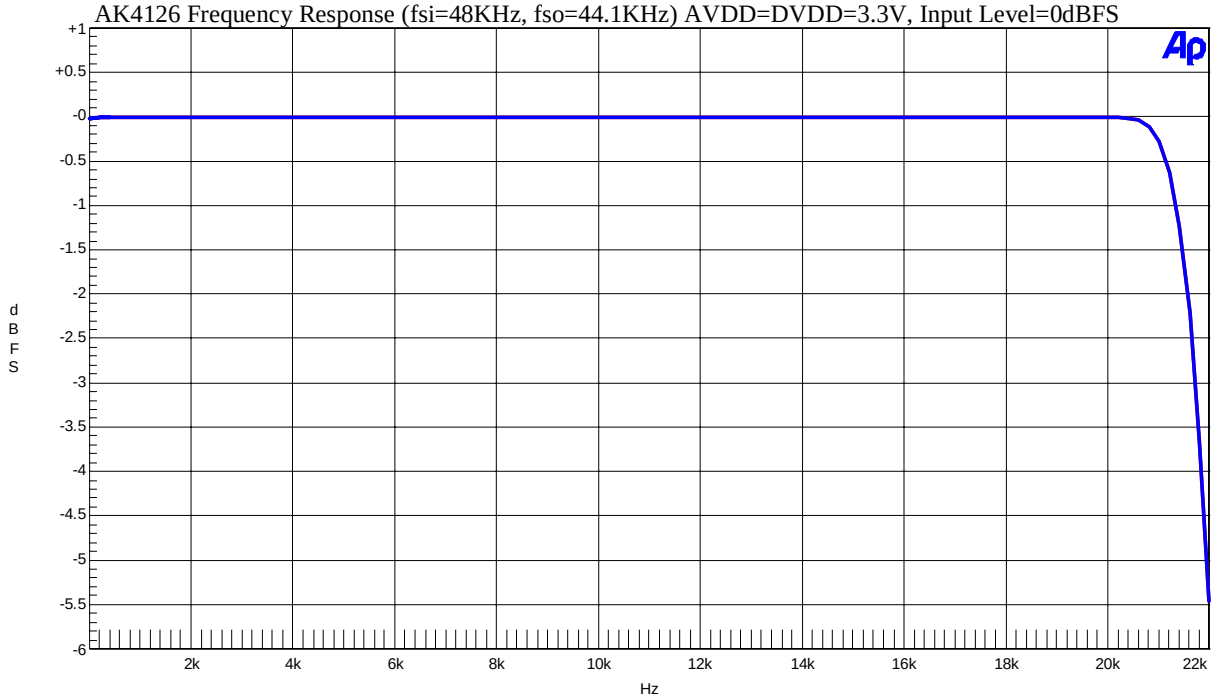


Fig 5. Frequency Response

AK4126 Frequency Response (Blue: fsi=48KHz, Red: fsi=96KHz, Green: fsi=192KHz), fso=48KHz
AVDD=DVDD=3.3V, Input Level=0dBFS

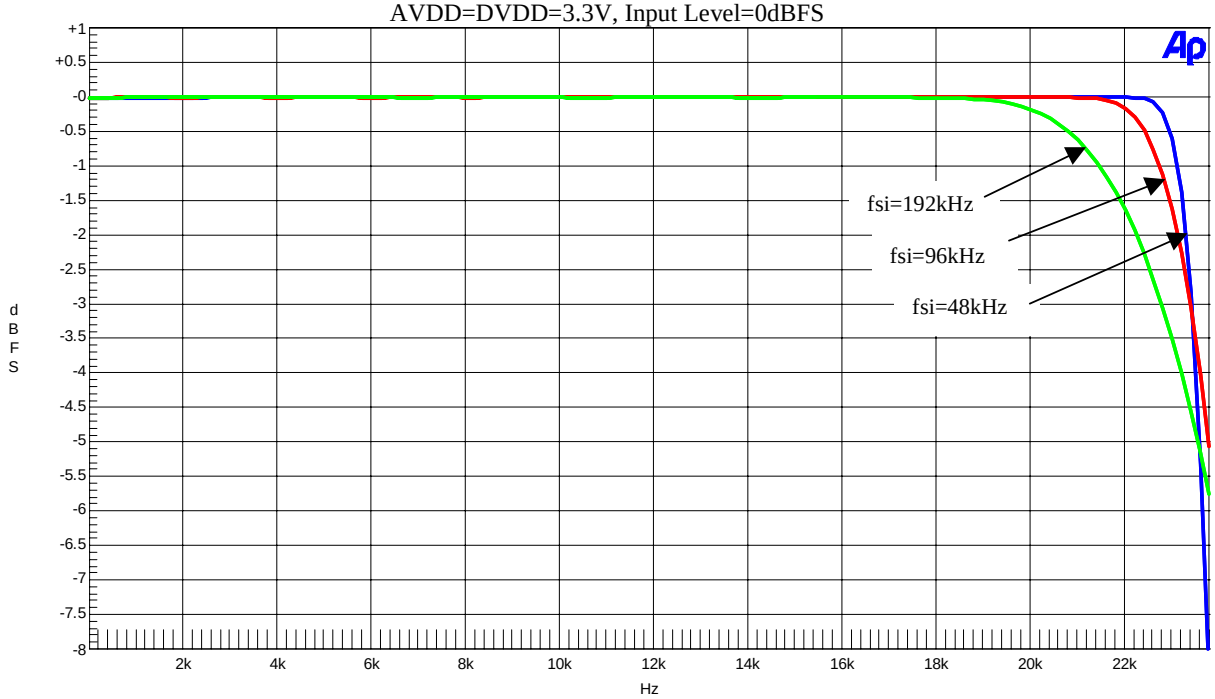


Fig 8. Frequency Response

AK4126 Frequency Response (Yellow: fsi=44.1KHz, Blue: fsi=48KHz, Red: fsi=96KHz, Green: fsi=192KHz),
fso=44.1KHz
AVDD=DVDD=3.3V, Input Level=0dBFS

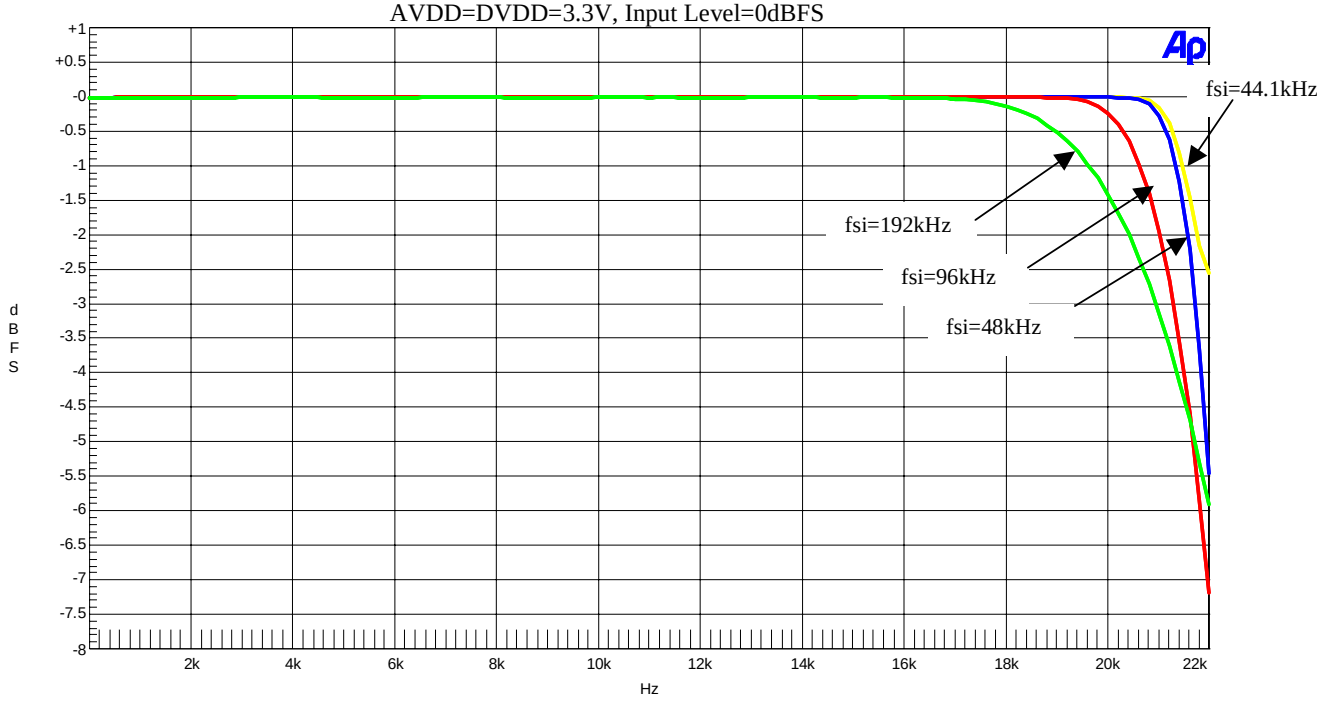
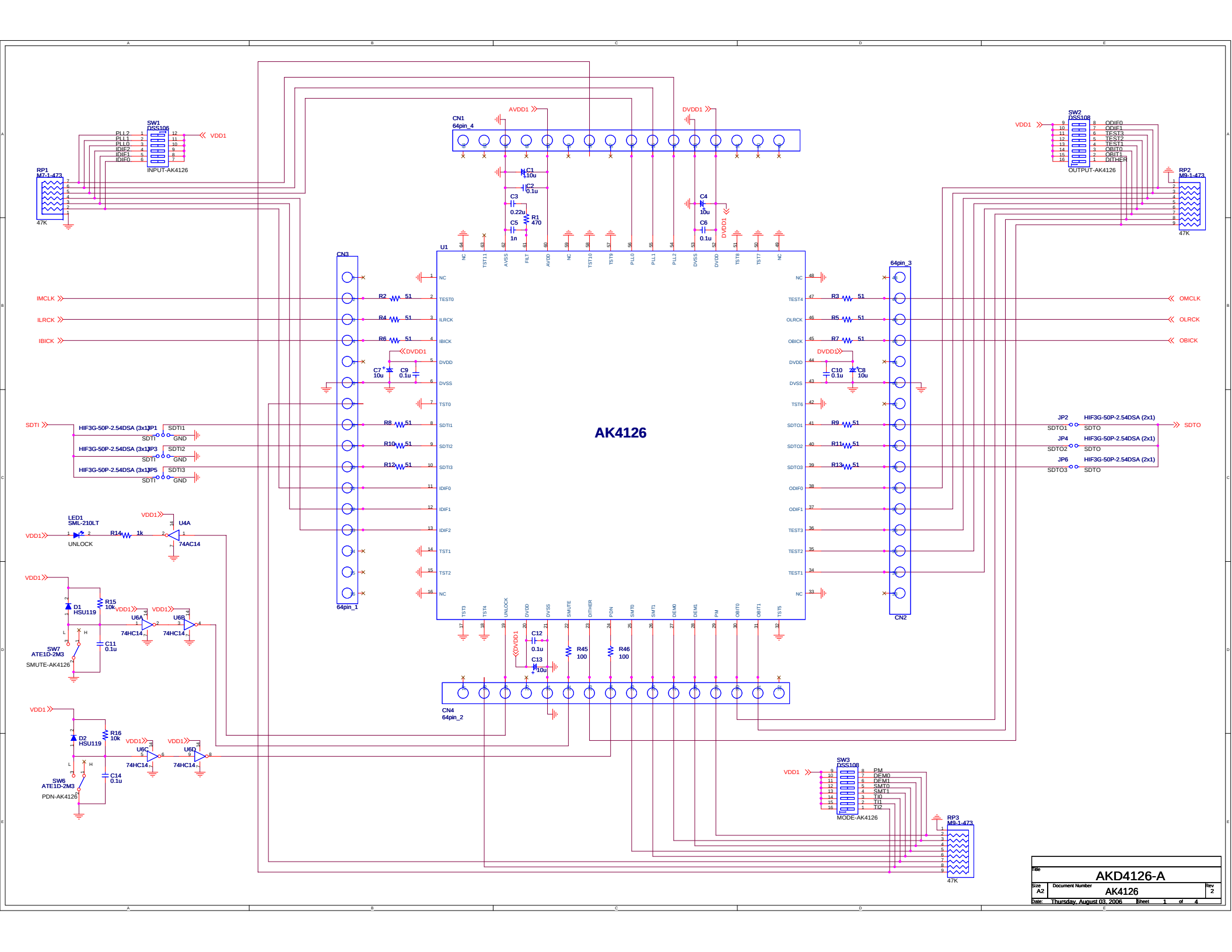


Fig 9. Frequency Response

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/01/09	KM083203	2	First Edition	



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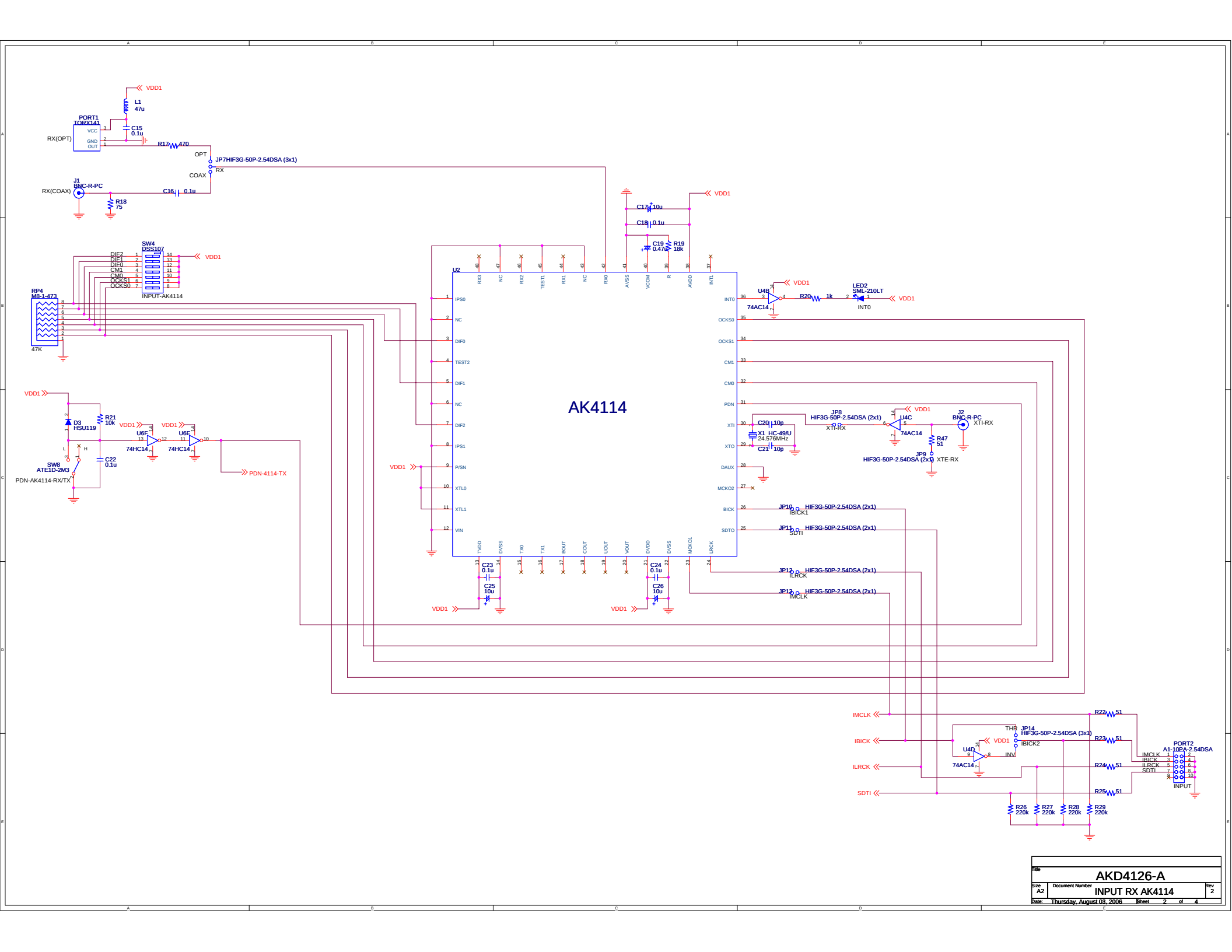
Size A2	Document Number AK4126		Rev 2
Date: Thursday, August 03, 2006	Sheet 1 of 4		



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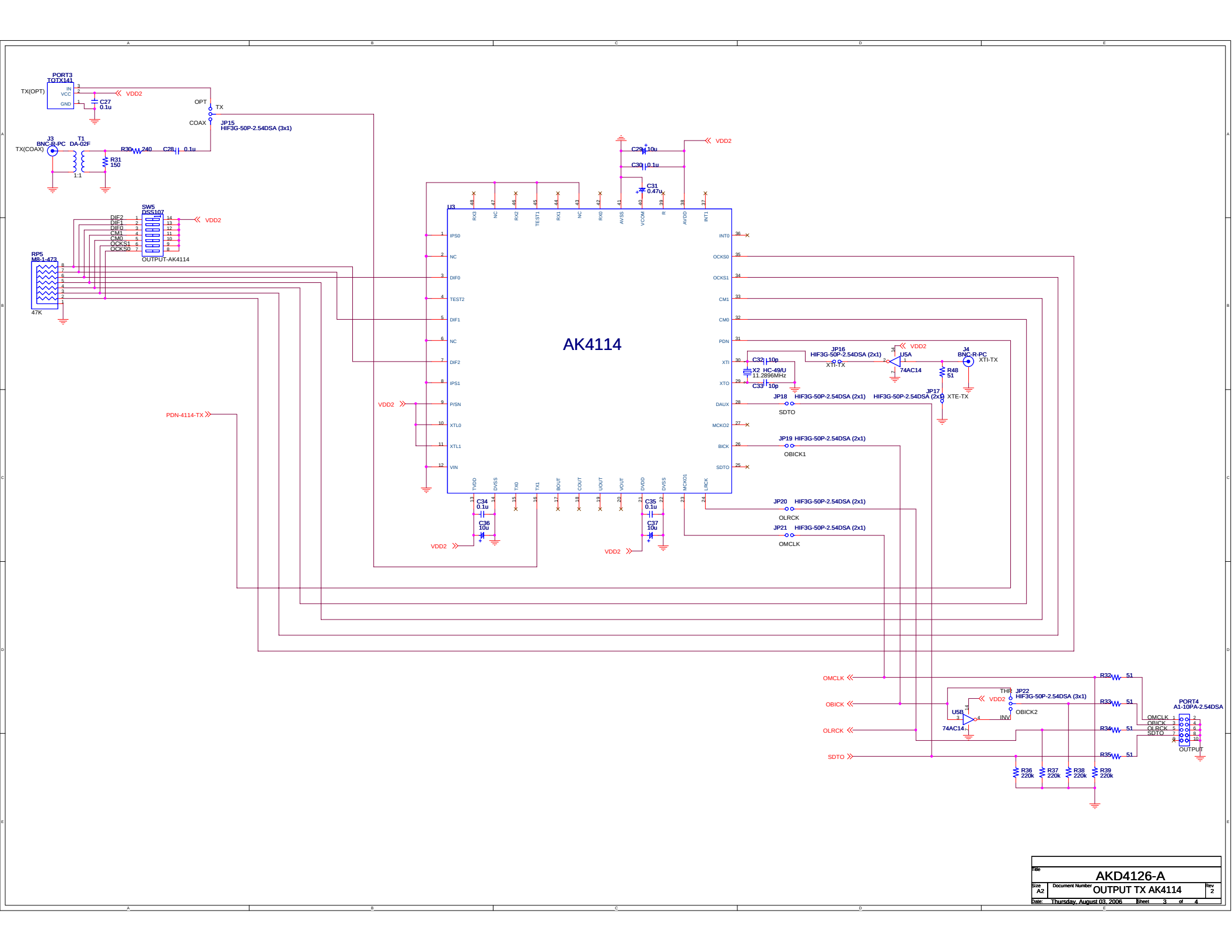
Size A2	Document Number INPUT RX AK4114	Rev 2
Date: Thursday, August 03, 2006	Sheet 2 of 4	



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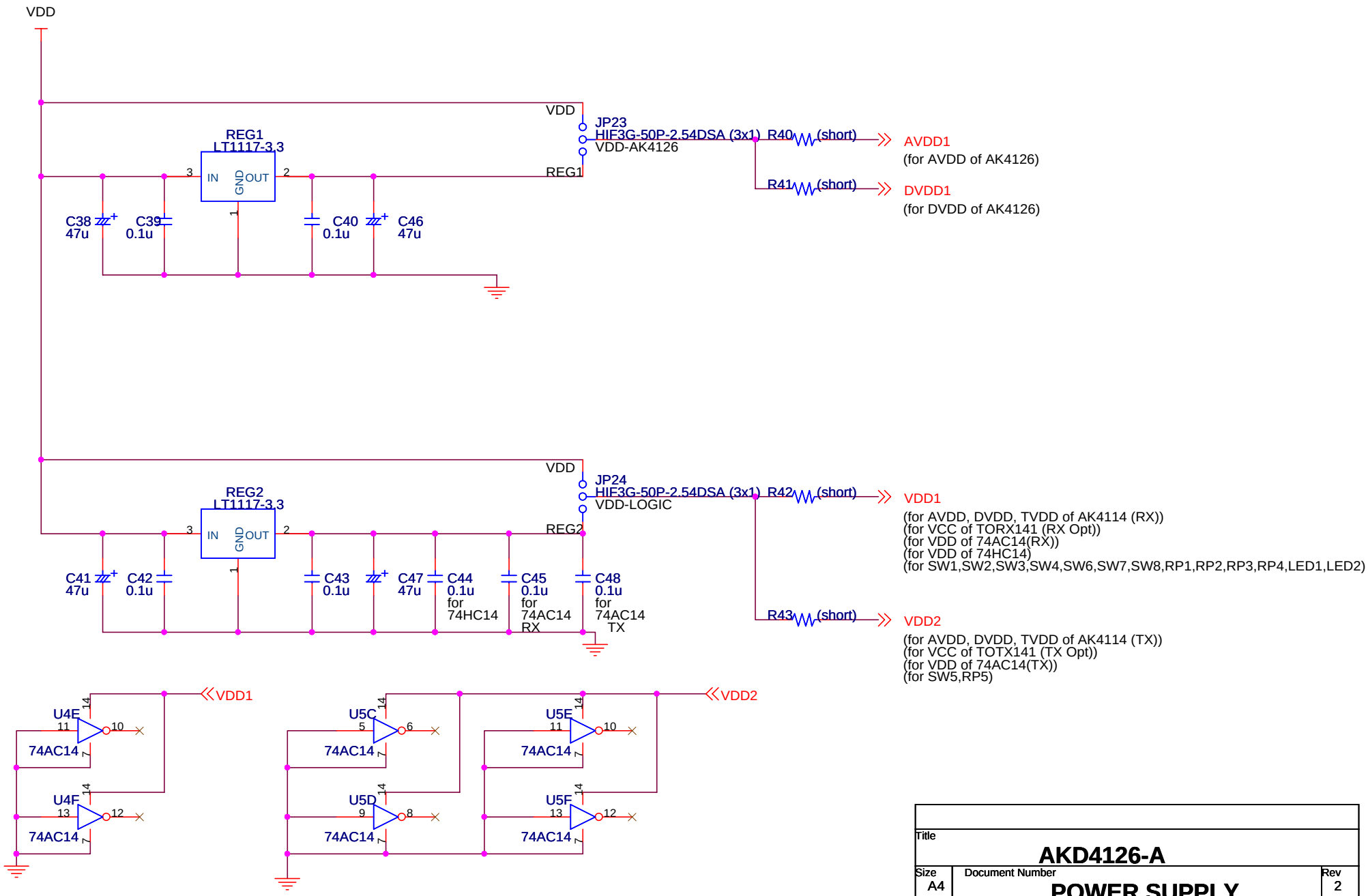
Size A2	Document Number OUTPUT TX AK4114		Rev 2
Date: Thursday, August 03, 2006	Sheet 3 of 4		



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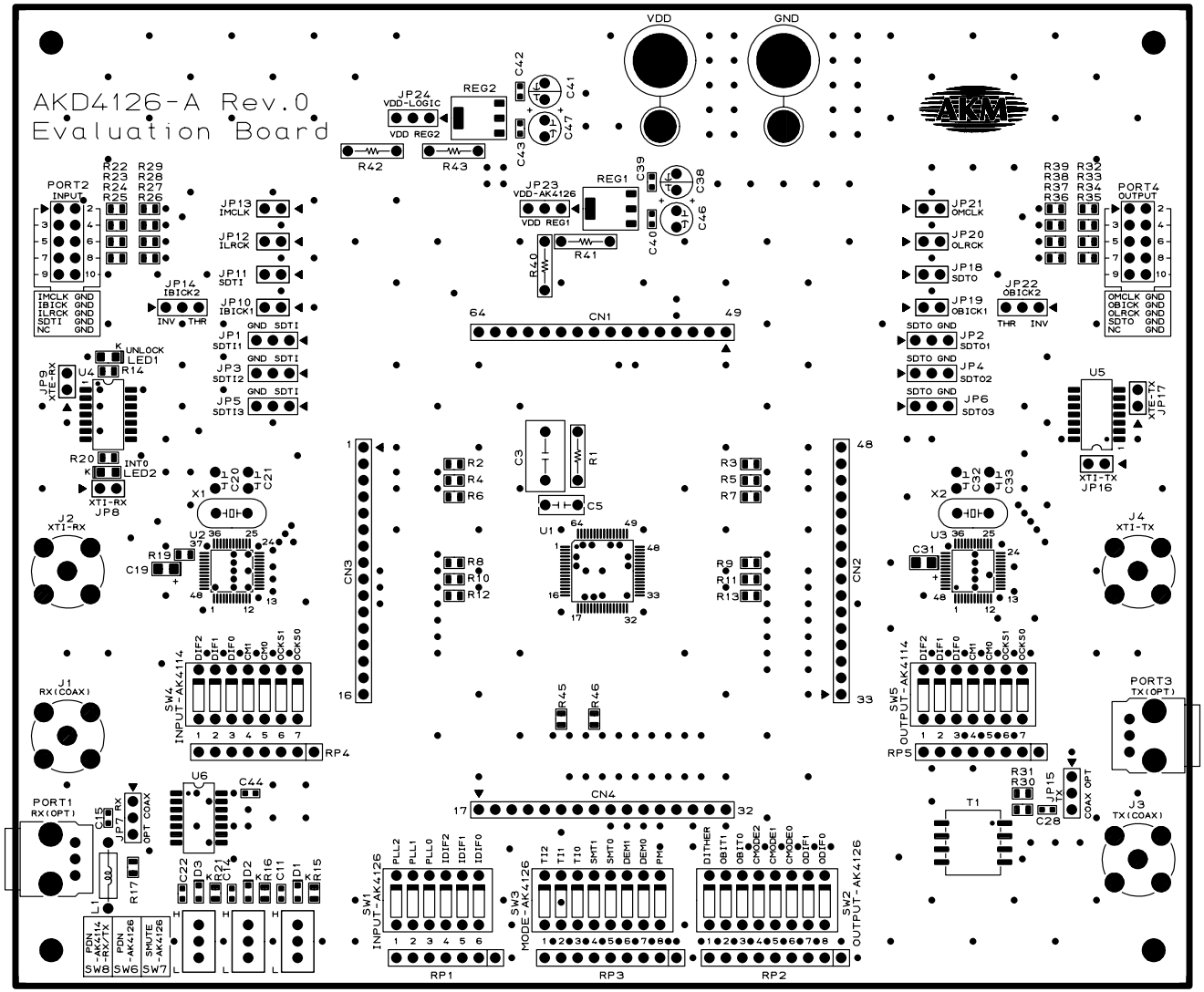
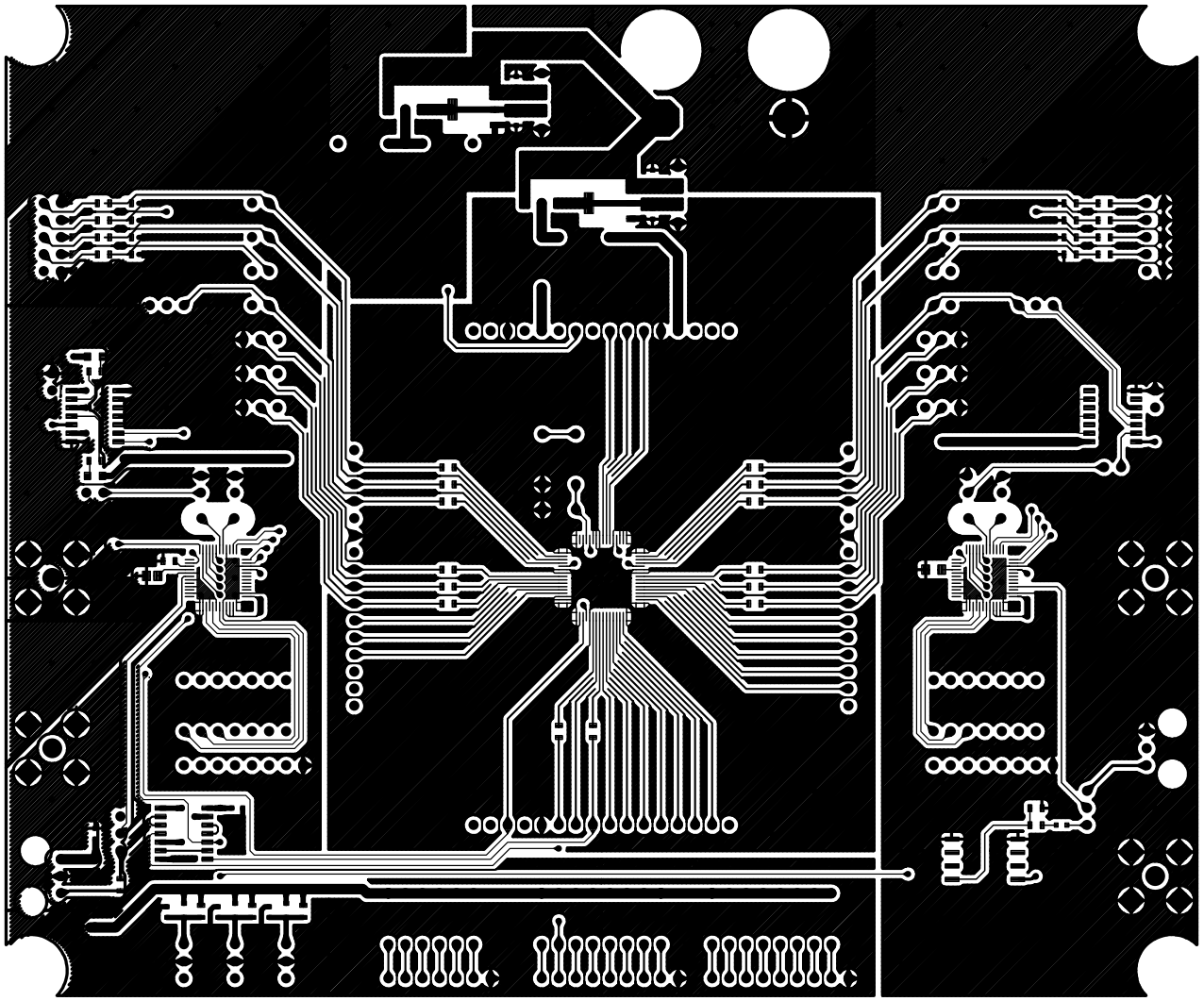


AKD4126-A L1 SILK

AKD4126-A L2 SILK



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AKD4126-A L2