Preliminary

AK8851

NTSC/PAL/SECAM Digital Video Decoder

General Description

The AK8851 is an integrated chip that decodes NTSC, PAL, SECAM composite and S Video signals..

The digital output of the AK8851 is in Y, Cb, Cr signal format which compliances with ITU-R BT.601 and ITU-R BT.656* specifications.

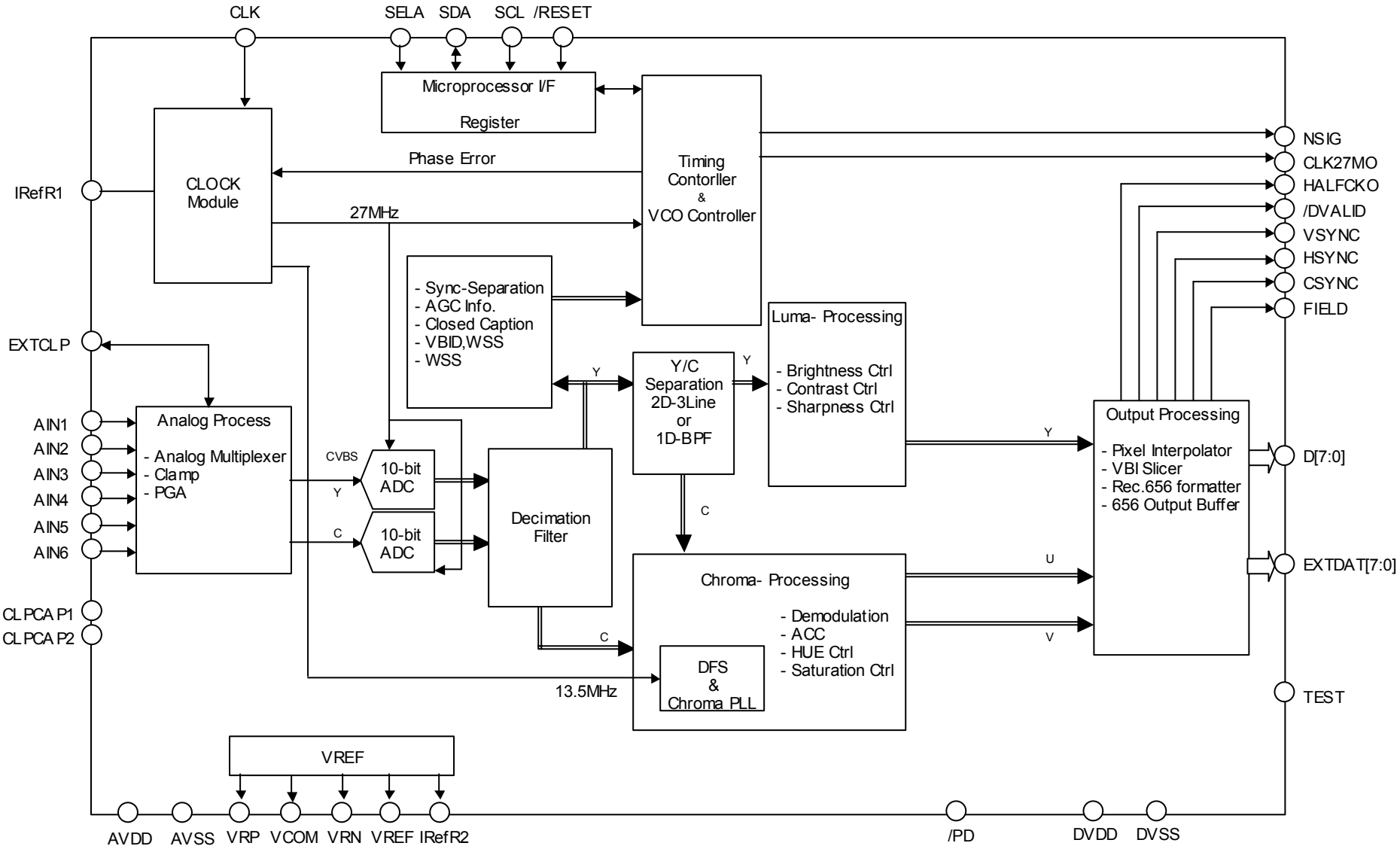
An internally generated pixel clock is synchronized with an input signal. The clock rate is 27 MHz.
When Closed Caption, VBID or WSS information are encoded on input Video signal, they are externally accessible.

Features

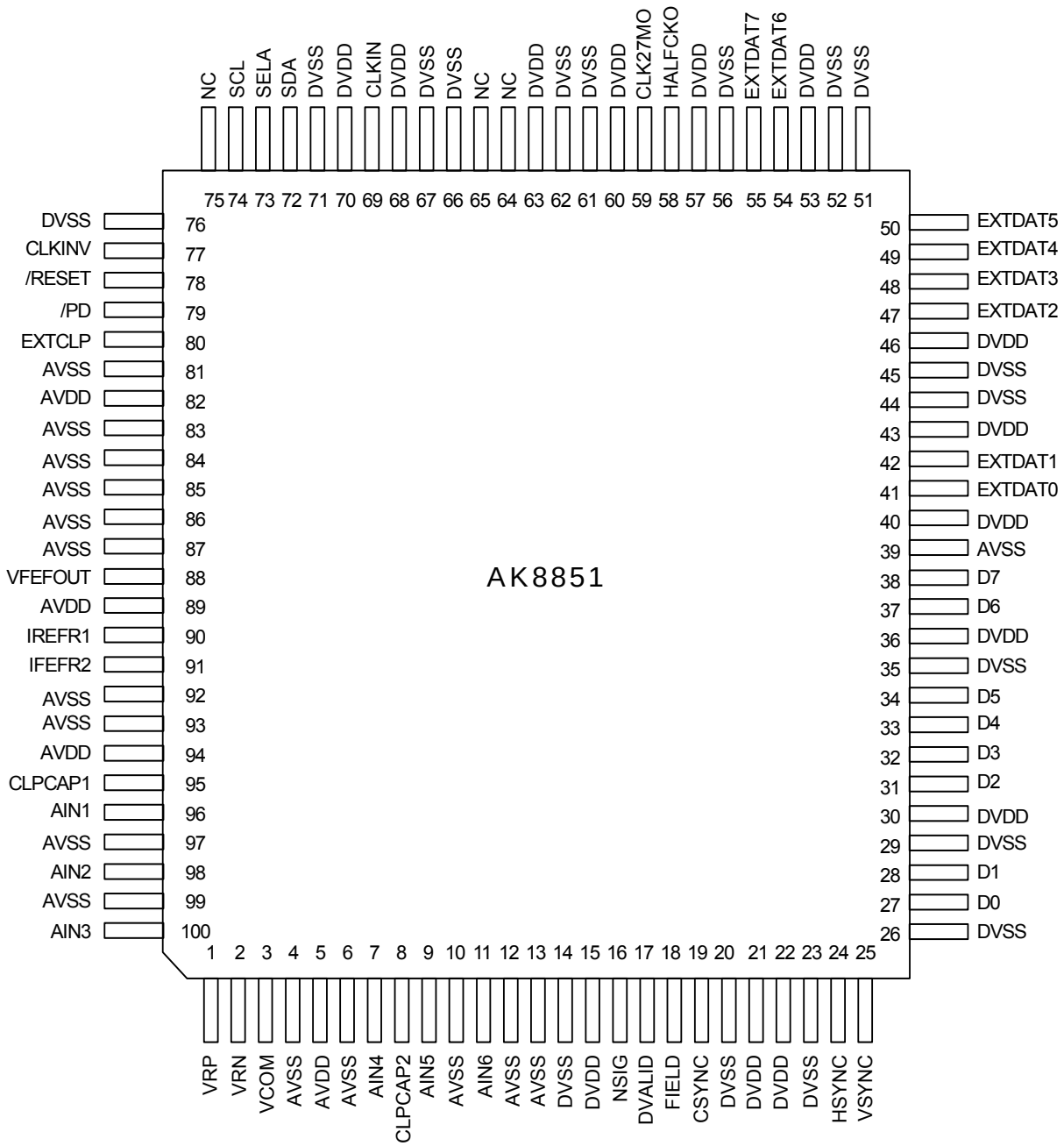
- NTSC-M, NTSC-4.43/PAL-B, D, G, H, I, N, Nc, M, 60/SECAM Composite signals and S Video signal decoding function
- On-chip dual 10 Bit ADCs (27 MHz operation)
- Built-in PLLs for input-signal-synchronized clock generation (Line-locked PLL and Frame-locked PLL)
- On-chip Programmable Gain Amp (PGA), ranging from 0 dB to 12 dB
- Auto Color Control (ACC)
- Auto Gain Control (AGC)
- Automatic input signal distinction function
- Adaptive 3-/5-line (NTSC/PAL) YC Separation
- Phase compensation function for PAL signal decoding
- ITU-R BT.656 format output (4:2:2 8 Bit parallel output with EAV / SAV)/ 16-Bit output is also available
- NTSC Closed Caption signal decoding function
- VBID (CGM-A) Program condition decoding function (CRCC decode)
- WSS Program condition decoding function
- VBI slicer function
- Macrovision Certification
- Power down function
- 6 – channel Analog inputs
- I2C Control
- 3.3 V +/- 10 % CMOS
- 100 Pin LQFP package

Note: * ITU-R BT.656 spec compatibility requires appropriate input signal quality.

1.Functional Block Diagram



2. Pin Assignment



3. Pin Functional Description

PIN#	Symbol	I/O	Function
1	VRP	O	Internal reference positive Voltage for AD Converter
2	VRN	O	Internal reference negative Voltage for AD Converter
3	VCOM	O	Common voltage for AD Converter
4	AVSS	G	Ground pin for Analog
5	AVDD	P	Analog supply voltage (3.3V)
6	AVSS	G	Ground pin for Analog
7	AIN4	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor.
8	CLPCAP2	O	Capacitor for clamp. Connect 0.1uF ceramic capacitor between AVSS
9	AIN5	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor.
10	AVSS	G	Ground pin for Analog
11	AIN6	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor.
12	AVSS	G	Ground pin for Analog
13	AVSS	G	Ground pin for Analog
14	DVSS	G	Ground pin for Digital
15	DVDD	P	Digital supply voltage (3.3V)
16	NSIG	O	No-signal indicator. H: No input video Signal L: Video Signal Input
17	DVALID	O	Active video data (720pixel) indicator
18	FIELD	O	Timing signal for FIELD
19	CSYNC	O	Timing signal for CSYNC
20	DVSS	G	Ground pin for Digital
21	DVDD	P	Digital supply voltage (3.3V)
22	DVDD	P	Digital supply voltage (3.3V)
23	DVSS	G	Ground pin for Digital
24	HSYNC	O	Timing signal for HSYNC
25	VSYNC	O	Timing signal for VSYNC
26	DVSS	G	Ground pin for Digital
27	D0	O	Decoded Data output pin (LSB)
28	D1	O	Decoded Data output pin
29	DVSS	G	Ground pin for Digital
30	DVDD	P	Digital supply voltage (3.3V)
31	D2	O	Decoded Data output pin
32	D3	O	Decoded Data output pin
33	D4	O	Decoded Data output pin
34	D5	O	Decoded Data output pin
35	DVSS	G	Ground pin for Digital
36	DVDD	P	Digital supply voltage (3.3V)
37	D6	O	Decoded Data output pin
38	D7	O	Decoded Data output pin (MSB)
39	AVSS	G	Ground pin for Analog
40	DVDD	P	Digital supply voltage (3.3V)
41	EXTDAT0	O	Cb/Cr data output pin for 16-bit output mode (LSB) Open this pin for 8-bit output mode
42	EXTDAT1	O	Cb/Cr data output pin for 16-bit output mode Open this pin for 8-bit output mode
43	DVDD	P	Digital supply voltage (3.3V)
44	DVSS	G	Ground pin for Digital
45	DVSS	G	Ground pin for Digital
46	DVDD	P	Digital supply voltage (3.3V)
47	EXTDAT2	O	Cb/Cr data output pin for 16-bit output mode Open this pin for 8-bit output mode
48	EXTDAT3	O	
49	EXTDAT4	O	
50	EXTDAT5	O	
51	DVSS	G	Ground pin for Digital
52	DVSS	G	Ground pin for Digital
53	DVDD	P	Digital supply voltage (3.3V)
54	EXTDAT6	O	Cb/Cr data output pin for 16-bit output mode Open this pin for 8-bit output mode
55	EXTDAT7	O	Cb/Cr data output pin for 16-bit output mode (MSB) Open this pin for 8-bit output mode

56	DVSS	G	Ground pin for Digital
57	DVDD	P	Digital supply voltage (3.3V)
58	HALFCKO	O	Indicator for Y Data and Cb/Cr Data in 8-bit output mode (Indicator transition rate is 13.5MHz)
59	CLK27MO	O	27MHz Clock output
60	DVDD	P	Digital supply voltage (3.3V)
61	DVSS	G	Ground pin for Digital
62	DVSS	G	Ground pin for Digital
63	DVDD	P	Digital supply voltage (3.3V)
64	NC		
65	NC		
66	DVSS	G	Ground pin for Digital
67	DVSS	G	Ground pin for Digital
68	DVDD	P	Digital supply voltage (3.3V)
69	CLK	I	Clock input pin (24.576MHz)
70	DVDD	P	Digital supply voltage (3.3V)
71	DVSS	G	Ground pin for Digital
72	SDA	I/O	I^2C bus Data
73	SELA	I	I^2C bus address select
74	SCL	I	I^2C bus clock
75	NC		
76	DVSS	G	Ground pin for Digital
77	CLKINV	I	CLK27MO output polarization is determined by this pin
78	/RESET	I	Reset signal input pin (Low Active) Reset sequence needs 24.576MHz Clock
79	/PD	I	Power down control pin. L: Power down H: Active Reset sequence is necessary when Power Down signal after High All output pins become Low while Power down pin is Low.
80	EXTCLP	I/O	Monitor pin for internal clamp timing pulse. External clamp timing pulse can be input on this pin by setting a register Open this pin when not using
81	AVSS	G	Ground pin for Analog
82	AVDD	P	Analog supply voltage (3.3V)
83	AVSS	G	Ground pin for Analog
84	AVSS	G	Ground pin for Analog
85	AVSS	G	Ground pin for Analog
86	AVSS	G	Ground pin for Analog
87	AVSS	G	Ground pin for Analog
88	VREFOUT	O	Internal Vref Output pin Connect ceramic capacitor (0.1uF -) between Analog Ground
89	AVDD	G	Analog supply voltage (3.3V)
90	IREFR1	O	Connect 12kΩ(1%) Register between Analog ground
91	IREFR2	O	Connect 4.7kΩ(1%) Register between Analog ground
92	AVSS	G	Ground pin for Analog
93	AVSS	G	Ground pin for Analog
94	AVDD	P	Analog supply voltage (3.3V)
95	CLPCAP1	O	Capacitor for clamp. Connect 0.1uF ceramic capacitor between AVSS
96	AIN1	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor.
97	AVSS	G	Ground pin for Analog
98	AIN2	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor.
99	AVSS	G	Ground pin for Analog
100	AIN3	I	Analog Video Signal Input pin. Input –6dB analog video signal via 0.1uF capacitor
	AVDD	P	Analog supply voltage (3.3V)
	AVSS	G	Ground pin for Analog
	DVDD	P	Digital supply voltage (3.3V)
	DVSS	G	Ground pin for Digital

* Recommendation: Perform a “power on reset” prior to using the device, as applying voltage to the AK8851 cannot ensure proper device initialization. Only a reset sequence can ensure this.

4.Electrical Specifications

(1) Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage* (VDD) DVDD, AVDD	-0.3	4.5	V
Input Pin Voltage (Vin)	-0.3	VDD + 0.3	V
Input Pin Current (Iin)	-10	10	mA
Storage Temperature	-40	125	°C

Note) power supply voltages are referenced to each ground pin (DVSS, AVSS) which is equal to 0 V (voltage reference).

(2) Recommended Operating Conditions

Parameter		Min.	Typ.	Max	Units
Supply Voltage *	AVDD	3.0	3.3	3.6	V
	DVDD	3.0	3.3	3.6	V
Operating Temperature		-20		85	°C

Note) power supply voltages are referenced to each ground pin (DVSS, AVSS) which is equal to 0 V (voltage reference).

(3) DC Characteristics (DVDD=3.0 ~ 3.6 V at –20 ~+85 degree C)

Parameter	Symbol	Min	Typ.	Max.	Units	Condition
Digital Input High Voltage	VIH	0.7DVDD			V	
Digital Input Low Voltage	VIL			0.3DVDD	V	
Digital Input Leak Current	IIL			+/- 10	uA	
Digital Output High Voltage	VOH	2.4			V	IOH = -400uA
Digital Output High Voltage	VOL			0.4	V	IOL = 1.2mA
I^2C Input High Voltage I^2C (SDA, SCL)	VIHC	0.7VDD			V	
I^2C Input Low Voltage I^2C (SDA, SCL)	VILC			0.3VDD	V	
I^2C (SDA) Output Low Voltage	VOLC			0.4	V	IOLC = 3mA

Note) The following are Digital Output pins:,
CLK27MO/D[7:0]/NSIG/DVALID/FIELD/CSYNC/HSYNC/VSYNC/HALFCKO/EXTDAT[7:0].
Digital output pins, excluding CLK27MO, are shown as Digital Data pins.
SDA pin is separated from Digital output pins and its characteristics are described in other terms.

(4) AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Digital Maximum Load Capacitance	CL	15		40	pF	

(5) Analog Characteristics and Power Dissipation (AVDD =3.3 V at room temperature)

Selector Clamp

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Input Range	VIMX			1.20	V_{PP}	PGA Gain 0dB
Clamp Level (Composite / Y Video Signal)	VYCP		0.65		V	
C Signal Clamp Level	VCCP		1.29		V	
Clamp Current	CLPI		+/-150		uA	
Isolation between Each Channels			-60		dB	5.5MHz

PGA

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolutions			7		bit	
Gain offset	GOF		0.65		dB	Gain 0dB (Reg0x0A, 0x0B = 0x00)
Minimum Gain	GMN		0		dB	
Maximum Gain	GMX		12		dB	
Gain Step	GST		0.094		dB	

AD Converter

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolutions	RES		10		bits	
Operation Clock	FS		27		MHz	
ADC Range	AIN		1.6		Vpp	(VRP-VRN) x 2
INL	INL		+/-2.5	+/-5.0	LSB	fs=27MHz (*1)
DNL	DNL		+/-0.8	+/-2.0	LSB	fs=27MHz (*1)
S/N	SN		54		dB	fin=1MHz Ain= -1dB fs=27MHz (*2)
S/(N+D)	SND		51		dB	fin=1MHz Ain= -1dB fs=27MHz (*2)
ADC Internal Common Voltage	VCOM		1.2		V	
ADC Internal VREF+	VRP		1.6		V	
ADC Internal VREF-	VRN		0.8		V	

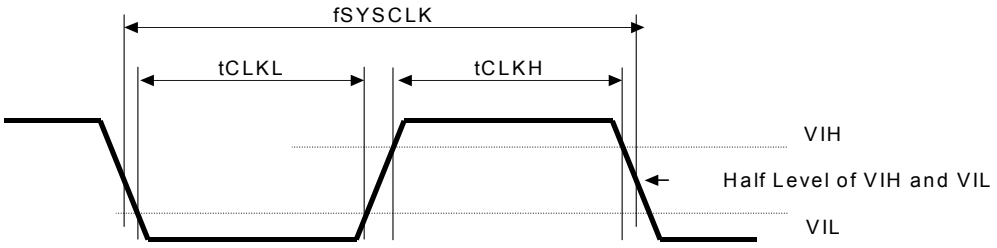
(*1) Full scale input range: VI=1.2Vpp, When PGA Gain Control Register 0x0A/0x0B is set to 0x0E.
(*2) VI=1.2Vpp PGA Gain Control Register 0x0A/0x0B = 0x06

Power Dissipation

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Active Mode						
Digital + Analog			142	185	mA	2ch operation (YCmode)
Analog			(129)		mA	(1ch operation (CVBS))
			44		mA	2ch operation (YC mode)
			(30)			(1ch operation (CVBS))
Digital			98			25pF Load 100% Color Bar Input
Power Down Current						Mode 1: AFE Control Register INSEL[2:0]=111
Mode 1						
Digital + Analog			81	105	mA	Analog ADC Path Power Down
Analog			16		mA	(PLL block is not powered down.)
Digital			85		mA	
Mode 2						Mode 2: PD pin Low
Digital + Analog			10	200	uA	When PD pin changes Low to High, the AK8851 requires a Reset sequence.
Analog			1		uA	
Digital			9		uA	

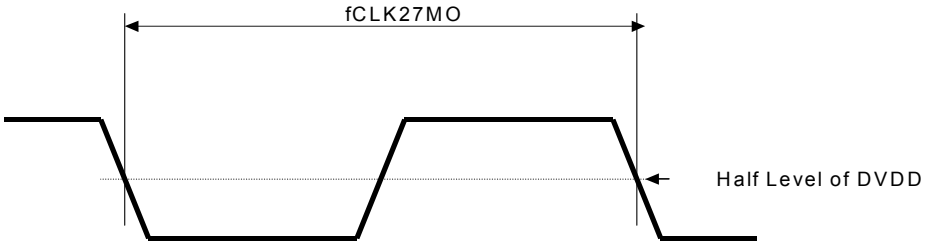
5. AC Timing (DVDD=3.0 ~ 3.6 V at 25 deg. C)

(1) Clock Input



Parameter	Symbol	Min.	Typ.	Max.	Units
CLK	fSYSCLK		24.576		MHz
CLK Pulse width H	tCLKH	16			nsec
CLK Pulse width L	tCLKL	16			nsec
Frequency stability				+/-100	ppm

(2)CLK27MO output

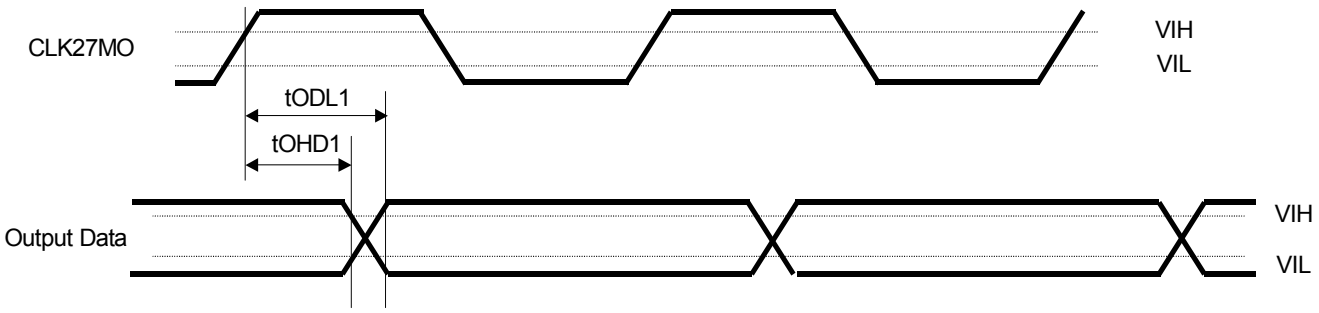


Parameter	Symbol	Min.	Typ.	Max.	Units
CLK27MO	fCLK27MO		27		MHz

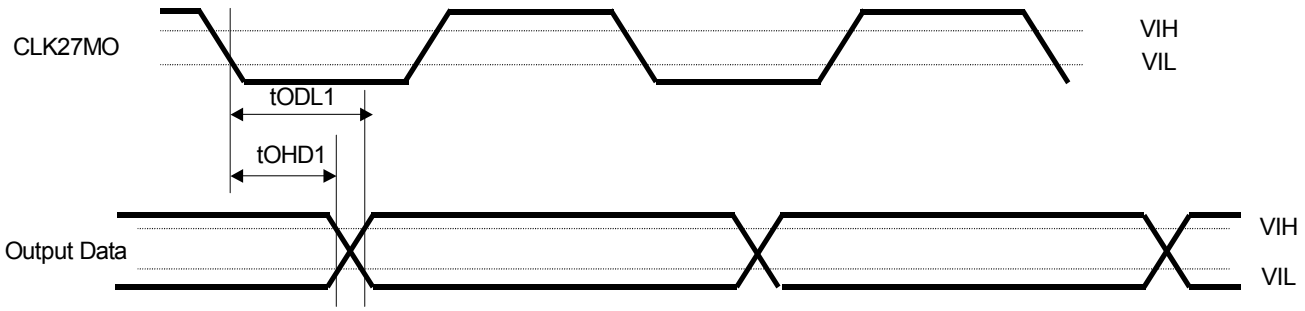
(3) Output Data Timing

(3-1) Output Data Timing (except for D[7:0] and EXTDAT[7:0] in 16-Bit output mode and NSIG output)

CLKINV=Low

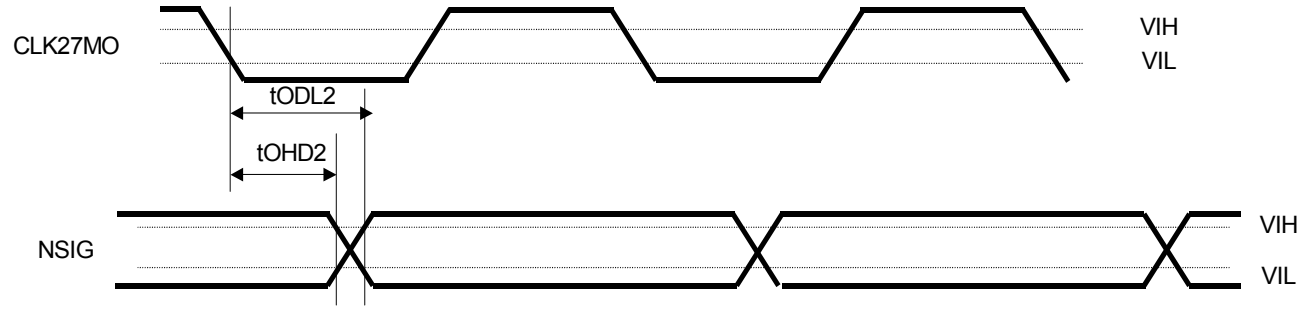


CLKINV=High



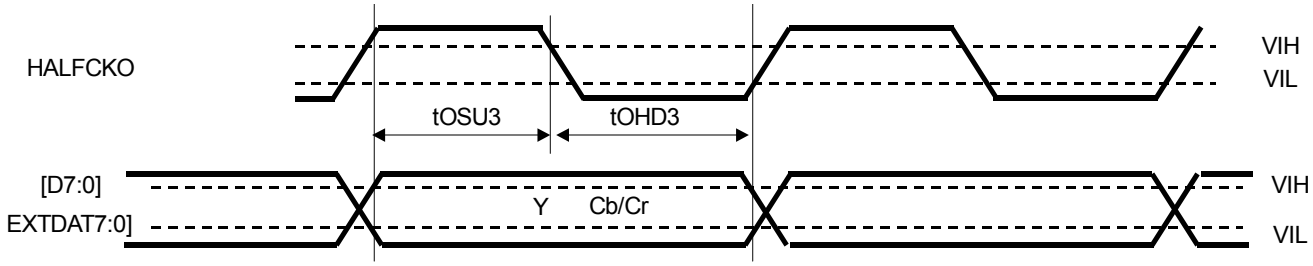
Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
Output Data Delay Time	tODL1			25	nsec	CL_{Clk} 25pF
Output Data Hold Time	tOHD1	3				CL_{Data} 25pF

CLKINV=High



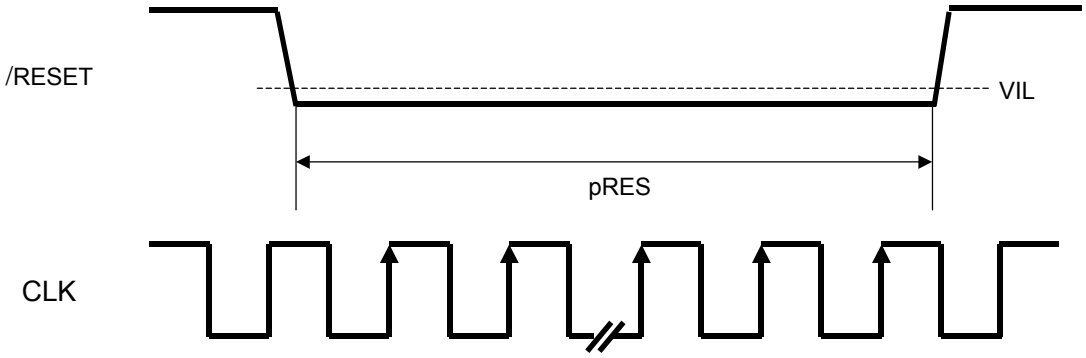
Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
Output Data Delay Time	tODL2			35	nsec	CL_{Clk} 25pF
Output Data Hold Time	tOHD2	3				CL_{Data} 25pF

(3-2) 16-Bit Output Data Timing ([D7:D0] and [EXTDAT7:EXTDAT0])



Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
Output Data Setup Time	tOSU3	10			nsec	CL_{Clk} 25pF
Output Data Hold Time	tOHD3	20			nsec	CL_{Data} 25pF

(4) Reset Timing



Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
/RESET Pulse width	pRES	10			CLK	Clock Rising Edge

Note) a 24.576 MHz clock is required for reset operation.

After application of clock, the /RESET pin should be pulled low. This power-on RESET is recommended whenever power is applied or removed from the AK8851, until as applying voltage to the AK8851 cannot ensure proper device initialization. Only a reset sequence can ensure this.

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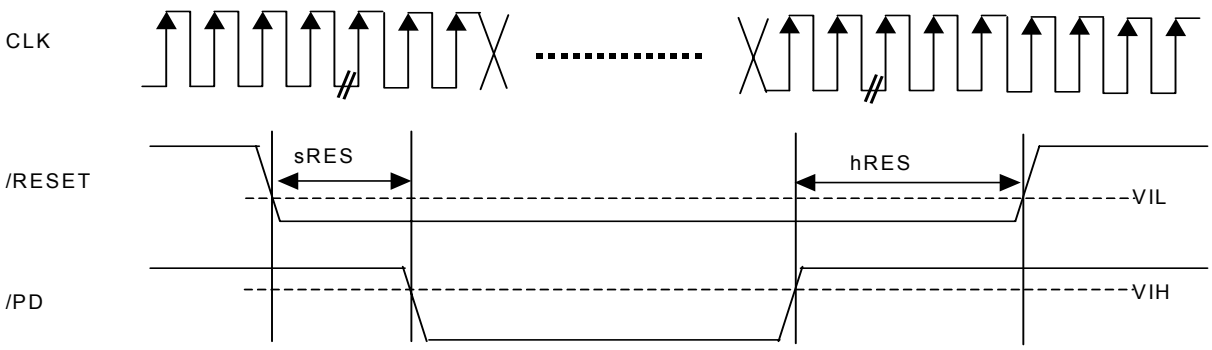
Output pins except for CLK27MO pin become low during the reset sequence.

(5) /PD pin release reset

Before setting /PD pin to Low, at least 100 clock cycles must be applied to the device..

After releasing /PD pin to high, the /RESET pin must be kept low until the analog reference voltage and current are stabilized.



Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
Set /PD RESET width	sRES	100			CLK	Clock Rising Edge
Release /PD Reset width	hRES	10			msec	

Note) a 24.576 MHz clock is required for reset operation.

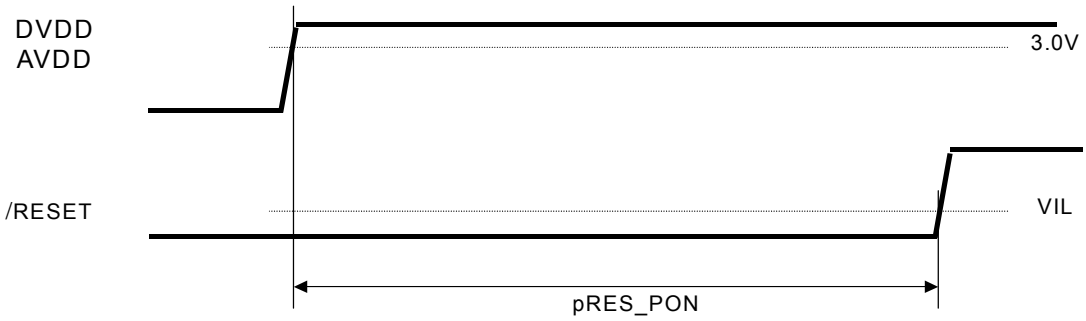
After application of clock, the /RESET pin should be pulled low. This power-on RESET is recommended whenever power is applied or removed from the AK8851, as applying voltage to the AK8851 cannot ensure proper device initialization. Only a reset sequence can ensure this.

until.

Output pins except for CLK27MO pin become low during the reset sequence.

(6) Power-On-Reset

At power-on, /RESET pin must be kept low until the analog reference voltage and current are stabilized.



Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
/RESET pulse width	pRES_PON	10			msec	

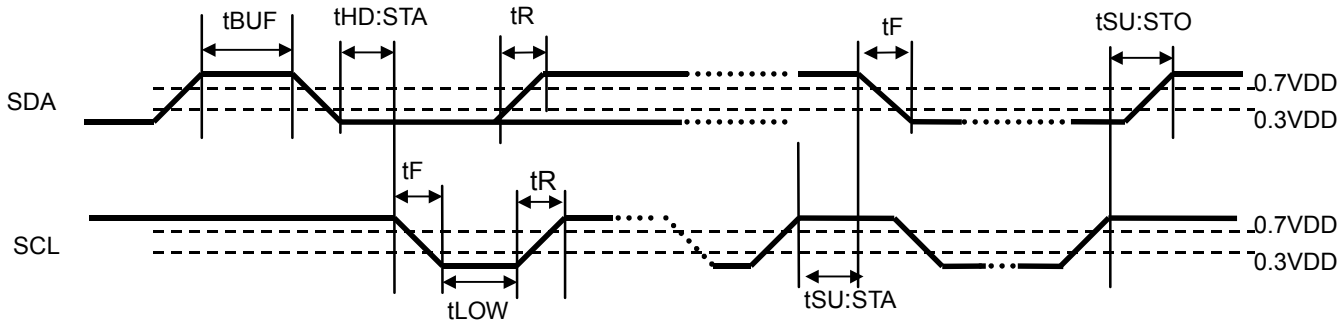
Note) For reset operation, a 24.576 MHz clock is required.

System control pins (SELA,CLKINV,/PD) must be kept valid until the 10-clock time after the rising edge of reset pulse.

Output pins except for CLK27MO pin become low during the reset sequence.

(7) I2C bus Input and Output Timing

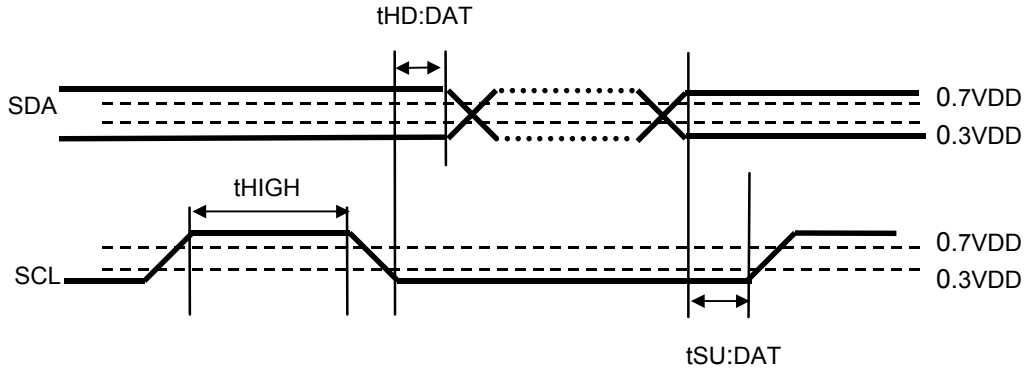
(7-1) Timing 1



Item	Symbol	Min	Max	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

All the figures shown above are restricted by the I^2C Bus standard.
Please see the official I^2C Bus standard for further details.

(7-2) Timing 2



Item	Symbol	Min	Max	Unit
Data Setup Time	tSU:DAT	100 (1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(1) In case of normal I^2C Bus mode tSU:DAT≥250nsec
(2) Using under minimum tLOW, this value must be satisfied

6. Functional Summary

(1) Clock

The AK8851 operates in one of 3 clock modes.

1. Line Locked Clock mode:
   An operating mode where the device uses a clock that is synchronized with the Horizontal Sync signal for each line.
2. Frame Locked Clock mode:
   The device operates by a clock that is synchronized with the Vertical Sync signal for each Frame.
3. Fixed Clock mode:
   An operating mode where the device operates by an asynchronous clock.

These clock modes are set by the [Control 1 register].

Since both Line Locked and Frame Locked modes use an input-signal synchronized clock, ITU-R BT.656* compatible output is available (however ,depending upon the input signal quality, ITU-R BT.656 may not be satisfied).

(2) Analog Interface

The AK8851 accepts Composite and discrete Y/C signals (S-video) as input. 6 channels are assigned for these input pins. Channel selection is set via register.

The following input signal combinations are possible.

(a) select a single channel from composite video signal x 4
(b) select a single channel from composite signal x 2 + S-video signal input x2

(3) Input Signals

The device accepts NTSC-M,NTSC-4.43,PAL-B,D,G,H,I,N,NcM,60,SECAM composite video signals and S Video signals.

It is also possible to accept an input signal with set-up features by setting the set-up register bit. In this case, the set-up is set at the 7.5% point. The automatic input signal detect function is also enabled via register settings.

Required input signal quality is as follows.

(3-1) input signal quality

Item	Input Range	Unit	Conditions
Video Input Level	+/- *6*	dB	Video signal should be input with -6dB level (divided be the resistor), and through 0.1uF capacitor.)
Color Burst Level	+/-10	dB	

(3-2) Non-Standard input signal treatment

Item	Process
Lack of HSYNC	Running with self timing
Lack of VSYNC	Running with self timing
B/W Video Signal input	Set register to B/W mode . Auto transition to B/W mode in auto signal detection mode.
Macrovision	Information with Macrovision control register. Certified Macrovision device .

(4) Analog Input Signal Processing

Input Selector (inter-channel isolation): better than –60 dB

PGA : 0 ~ 12 dB (approx. 0.1 dB/step)

AD converter : operates at 27 MHz

For normal operation, the Frame-locked PLL generates by the Line-locked PLL or a required internal clock.

(5) Clamp processing

Analog Sync-Tip clamping is done and the Digital signal-processing block processes the Digital Pedestal clamping.

(6) AGC function

The AGC adjusts the input signal level based on the amplitude difference between the Sync-Tip level and the Pedestal level of the input signal.

(7) ACC function

The ACC adjusts the input color signal level based on the color burst level of the input signal. ACC does not function for SECAM signals.

(8) Y/C Separation Function

For NTSC,NTSC-4.43 signal inputs :

Adaptive Y/C separation is used. It is also possible to lock this function to either 3-line 2 dimensional Y/C separation, or primary dimensional (BPF) Y/C separation.

For PAL-B,D,G,H,I,M,N,Nc,NTSC-4.43,PAL 60 signal inputs :

Adaptive Y/C separation is used. It is also possible to lock this function to either 5-line 2 dimensional Y/C separation, or primary dimensional (BPF) Y/C separation.

For SECAM signal input :

Only the primary dimensional (BPF) Y/C separation is effective (even if the adaptive type is set, primary Y/C separation is performed).

(9) input signal synchronization

The AK8851 automatically synchronize the incoming input signal when the input signal is switched or when the number of lines in a Frame changes (VLOCK function).

(10) Output Signal Bandwidth

Luminance Signal Bandwidth : DC ~ 5.5 MHz - 0.5 dB (DC ~ 5MHz +/- 0.1 dB ripple)
The luminance bandwidth is selectable among 3 ranges via a register setting.
Chroma Signal Bandwidth : 750 KHz ~ 1.5 MHz (-3 dB) (2 ranges selectable)

(11) Video Image Quality Control Function

Contrast, Brightness, HUE, Saturation levels and Sharpness level are adjustable.
* HUE and Color Saturation levels are not adjustable when using SECAM signals.

(12) Output Interface

- ITU-R BT.601 compatible signal output levels (with Limit On/Off function)
- Decoded data output is ITU-R BT.656 format (depending on the input signal quality).
- Enables to detect only those signals which are valid during Active Video period (720 pixels), by HSYNC/VSYNC (FIELD)/ DVALID signals.
- 8-Bit output form at 27 MHz rate or 16-Bit output form at 13.5 MHz rate (selectable by register).

(13) Other Functions

- Black level signal is output in self-operating mode when no signal is applied (Y = 16Cb,Cr = 128). It is also possible to output Blue level (register selectable).
- Dedicated output pin for no-signal-input detection
- I2C Bus Host Interface (400 KHz)
- Power Down mode
- Decoding Function for Closed Caption, VBID (CGMS-A) and WSS signals.
  CRCC that is added to CGMS-A is decoded by the AK8851.

(note) In this data sheet, Sync level and Burst level of the NTSC signals are also converted and expressed in [mV], not in [IRE].

7. Input Signal Selector

The AK8851 has 4 analog signal input pins. Signal selection is done by [AFE Control Register](R/W)[Sub Address 0x00] and the type of Video signals to be decoded is set by [Input Video Standard Register](R/W)[Sub Address 0x01]. Video signals to be decoded by the AK8851 are NTSC, NTSC-4.43, PAL B, D, G, H, I, M, N, 60 and SECAM.
It is also possible to automatically distinguish input signal types by setting the AUTODET-bit of [Input Video Standard Register].
However Automatic detections of Black and White signals and those with / without the SETUP features are not possible.

Input signals are converted into Digital codes as follows:

Composite Video signal: After it conversion to digital data through the functional blocks shown in Fig.2 Analog Block description,

CLAMP1 BLOCK --- PGA1 BLOCK --- ADC1 BLOCK,

It is then processed in the Digital Block.

Discrete Y/C Video signal input (S-Video signal input):

The input Luminance Signal (Y) is converted into digital data through the functional blocks shown in Fig.2 Analog Block description,

CLAMP1 BLOCK --- PGA1 BLOCK --- ADC1 BLOCK

and the Input Chroma Signal (C) is converted in digital data through

CLAMP2 BLOCK --- PGA2 BLOCK --- ADC2 BLOCK,

then each digital data is processed in the Digital block.

The following describes the Register Setting of [AFE Control Register](R/W)[Sub Address 0x00] and [Input Video Standard Register](R/W)[Sub Address 0x01].

[AFE Control Register](R/W)[Sub Address 0x00]:

this register sets the input signal.
Its Bit Allocation is shown below:

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPWIDTH1	CLPWIDTH0	CLPSTAT1	CLPSTAT0	EXTCLP	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	0	0	0	0	0

[INSEL2 : INSEL0]-bit:
to set the input port of input signal.
The setting is done as follows. This input port setting also controls the Analog Block's Power Saving mode.

[INSEL2:INSEL0]	Select Input port	Input Video	Power Save
[000]	AIN1	CVBS	ADC2 set to Power save mode.
[001]	AIN2	CVBS	
[010]	AIN3	CVBS	
[011]	AIN4	CVBS	
[101]	AIN2/AIN5	AIN2: Y AIN5: C	
[110]	AIN3/AIN6	AIN3: Y AIN6: C	
[100] [111]	No signal in		ADC1 and ADC2 are set to Power save mode.

Note: when [INSEL2:INSEL0]-bit is set to [1,0,0] or [1,1,1], ADC1 and ADC2 in Power Saving mode, including the CLAMP and PGA blocks (timing signal outputs are driven by the self-running clock as the digital blocks are in normal operating mode).

[Input Video Standard Register](R/W)[Sub Address 0x01]:

This register sets the input signal attributes.
its Bit Allocation is as follows.

Sub Address 0x01 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	B/W	VLF	VCEN1	VCEN0	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

* [VSCF1:VSCF0]-bit:

Input signal Sub-carrier frequency is set using the [VSCF1:VSCF0]-bit.

[VSCF1:VSCF0]	Sub-Carrier Freq.[MHz]	Note
[00]	3.57954545	NTSC
[01]	3.57561188	PAL-M
[10]	3.582054	PAL-N(Arg.)
[11]	4.43361875	PAL-B,D,G,H,I

* [VCEN1:VCEN0]-bit:

Input signal Color encoding is set using the [VCEN1:VCEN0]-bit.

[VCEN1:VCEN0]-bit	Color Encode Type	Note
00	NTSC	
01	PAL	
10	SECAM	
11	Reserved	

*[VLF]-bit:

Number of input signal Lines per Frame is set using the [VLF]-bit.

[VLF]-bit	Number of Lines	Note
0	525 lines	
1	625 lines	

*[B/W]-bit:

When the input signal is Black and White, set the [B/W]-bit.

[B/W]-bit	Type of Signal	Note
0	Color Signal	
1	Black and White Signal	

(footnote)

When this bit is set, the input signal is processed as a Black and White signal and the digitized sampling data through the ADC is processed as Luminance through Luminance process. Namely, when this bit is ON, all input signals fed to the Y/C separation block are treated as Luminance, and the data is output to the Luminance signal-processing block from Y/C Separation block.

*[SETUP]-bit:

Lack or presence of input signal SETUP features is set by [SETUP]-bit.

[SETUP]-bit	SETUP	Note
0	w/o Setup Signal	
1	with Setup Signal	7.5% SETUP

(footnote)

when [SETUP]-bit is set to “1”,Luminance and Chroma signals are processed as follows.

Luminance signal: Y=Y(1-0.075)/0.925

Chroma signal : U=U/0.925

V=V/0.925

[AUTODET]-bit:

SET the [AUTODET]-bit in order to automatically distinguish input signals.

[AUTODET]-bit	On/Off	Note
0	OFF	
1	ON	Cannot detect with or w/o Setup

(footnote)

following input signal characteristics are automatically detected.

Number of Lines per each Frame:525/625
Sub-Carrier frequency : 3.58/4.43 MHZ
Color Encoding systems: NTSC/PAL/SECAM

With the automatic distinguishing capability described above, the input signal is verified to be one of the following:

NTSC/NTSC-4.43/PAL-B, D, G, H, I/PAL-M/PAL-N (ARG)/PAL-60/SECAM.

The verification result is stored in [Input Video Status Register][sub Address 0x00].

Automatic verification of the SETUP feature is not performed. The following set-up process is performed while the automatic verification function is enabled.

Recognized Signal	Setup Recognition (Default) [Control 2 Register] [STUPATOFF-bit] = 0	Validation of SETUP-bit
NTSC	No setup process	Setup Procedure is done with SETUP-bit is 1
PAL-B,D,G,H,I,N,Nc,60		
SECAM		
PAL-M	Setup process	Setup-bit is disable. The setup procedure is always done.
NTSC-4.43		

Please set the [Input Video Standard Register][Sub Address 0x01] [SETUP]-bit when an input signal with values other than those shown above is input (SETUP process is performed regardless of SETUP-bit status for PAL-M and NTSC-4.43 signal).

The automatic set-up process can be turned off by [STUPATOFF-bit] of the Control2 Register. In this case, use the SETUP-bit to enable/disable the set-up process. .

Please refer to [SETUP]-bit description for details.

Automatic input signal detect registers are listed below:

***[Input Video Status Register]:**

Sub Address 0x19

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_B/W	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VSCF0

***[ST-VSCF1:ST-VSCF0]-bit:**

Input signal Sub-carrier verification result is indicated by [ST-VSCF1: ST-VSCF0]-bit.

[ST_VSCF1:ST_VSCF0]	Sub-Carrier Freq.[MHz]	Note
[00]	3.57954545	
[01]	3.57561188	
[10]	3.582054	
[11]	4.43361875	

***[ST-VCEN1:ST-VCEN0]-bit:**

Color Encoding System Verification is indicated by [VCEN1:VCEN0]-bit.

[ST_VCEN1:ST_VCEN0]-bit	Type of Color Encode	Note
00	NTSC	
01	PAL	
10	SECAM	
11	Reserved	

***[ST-VLF]-bit:**

Number of Lines per each Frame is indicated by [VLF]-bit.

[ST_VLF]-bit	Number of Lines	Note
0	525lines	
1	625lines	

***[ST-B/W]-bit:**

when the input signal is Black and White,[ST-B/W]-bit indicates the status.

[ST_B/W]-bit	Type of Signal	Note
0	Color Signal	
1	Black and White Signal	

Since Black and White signal decisions are made by the color killer level, the color killer bit must be turned “ON”.
When a user intentionally enables the B/W-bit, the automatic input signal detect function only checks if the Line number is 525 or 625. In this case, please refer to [ST-VLF]-bit information only.

***[UNDEF]-bit:**

if the input signal type is not identified, this bit becomes “1”.

[UNDEF]-bit	Status	Note
0	During recognition	
1	Cannot be recognized	

***[FIXED]-bit:**

when the input signal type is identified, this bit becomes “1”.

[FIXED]-bit	Status	Note
0	During recognition	
1	Recognized	

8.PGA (Programmable Gain Amp.)

The Ak8851 has 2 PGAs (Programmable Gain Amps), PGA1 and PGA2 on the input stage. The gain range of each PGA is from 0dB to 12dB with a gain step of approx. 0.1 dB/step. Input signals to the AK8851 are attenuated to 50 % level by an external resistor-divider.

PGA1 adjusts the gains of Composite and Y signals for discrete Y/C signals, and PGA2 handles the C signal gain of the discrete Y/C signal (refer to Fig.2).

PGA1 set is done by [PGA1 Control Register](R/W)[Sub Address 0x0A].
PGA2 set is done by [PGA2 Control Register](R/W)[Sub Address 0x0B].

When the AGC function is enabled by [AGC and ACC Control Register], the PGA registers are disabled. When the AGC function is disabled, the gains of PGA1 and PGA2 can be adjusted independently.
Bit Allocation of [PGA1/PGA2 Control Register] is shown below.

***[PGA1 Control Register]**

Sub Address 0x0A **Default Value : 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA1_6	PGA1_5	PGA1_4	PGA1_3	PGA1_2	PGA1_1	PGA1_0
Default Value							
0	1	0	0	0	0	0	0

***[PGA2 Control Register]**

Sub Address 0x0B **Default Value : 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA2_6	PGA2_5	PGA2_4	PGA2_3	PGA2_2	PGA2_1	PGA2_0
Default Value							
0	1	0	0	0	0	0	0

9.AGC

The AK8851 measures the input signal's SYNC signal level (the difference between SYNC-Tip level and Pedestal level) and then judges the input signal level. The AGC function controls PGA gain so that the SYNC signal level equals 286 [mV]/300 [mV].

This function ensures a proper level to the ADC by amplifying the incoming input signal.
For Y/C inputs, the C signal is either amplified or attenuated by the same gain value as the SYNC level of the Y signal adjustment to be 286 [mV]/300 [mV] (a fine tuning of the C signal is done by the Auto Color Control (ACC) function in the digital block).
AGC Adjustable levels expressed in 10-bit code are shown in the following table.

Input Signal	Target ADC value(decimal)	Note
NTSC-M	224	286[mV]
NTSC-4.43		
PAL-M		
PAL-B, D, G, H, I, N, Nc	236	300[mV]
SECAM		
PAL-60		

AGC value can be frozen via a register setting. When it is frozen, the pre-set gain constant is held in the AGC.
When AGC function is disabled, PGA1 and PGA2 gains can be independently set.

Set the AGC parameter by programming [AGC and ACC Control Register](R/W)[Sub Address 0x06].

Sub Address 0x06 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACCFRZ	ACC1	ACC0	AGCFRZ	Reserved	AGCC	AGCT1	AGCT0
Default Value							
0	0	0	0	0	0	0	0

[AGCT1:AGCT0]-bit:

* AGC time constant is set by [AGCT1:AGCT0]-bit.

[AGCT1:AGCT0]-bit	Time constant of AGC	Note
[00]	Disable	PGA control Register is valid
[01]	Fast	
[10]	Middle	
[11]	Slow	

[AGCC]-bit:

*[AGCC]-bit sets the non-sensing range (coring level) of AGC.

[AGCC]-bit	non-sensing range of AGC	Note
0	+/-2-bit	
1	+/-3-bit	

[AGCFRZ]-bit:

* This bit controls the AGC freeze function.

When [AGCFRZ]-bit is stopgap gain values are maintained.

[AGCFRZ]-bit	Status of AGC	Note
0	AGC function is working	Invalid when AGC function is disable.
1	AGC function is frozen	Current AGC Value is kept

(footnote)

AGC gain set function is set based on the SYNC signal level only.

When the input signal's SYNC signal level is small but still at a valid level, PGA gain set by the AGC function becomes larger than normal.

If the decoded output code exceeds 254, [PKWHITE]-bit in [Status 1 Register](R)[Sub Address 0x16] or [OVCOL]-bit becomes "1", which indicates an overflow of the decoded data. As for the input level overflow, it is described in a later section.

10.CLAMP

[Analog Clamp circuit]:

The AK8851 uses an analog circuit to clamp the input signal to the Sync-Tip level (Analog Sync-Tip clamp). Clamp timing is set by [AFE Control Register](R/W)[Sub Address 0x00].

The clamp timing pulse is generated for a fixed time specified by [AFE Control Register] at the falling edge of SYNC signal as a starting point that is SYNC-separated within the AK8851. The Pedestal clamp of A to D converted input data is then processed in the digital signal-processing block (Digital Pedestal Clamp). The Digital Pedestal Clamp is described in a later section.

Analog SYNC-Tip clamping is set by [AFE Control Register](R/W)[Sub Address 0x00].

[AFE Control Register] sets the timing of the SYNC-Tip clamp in the AK8851.

This adjusts the start timing of the clamp and its pulse width.

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPWIDTH1	CLPWIDTH0	CLPSTAT1	CLPSTAT0	EXTCLP	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	0	0	0	0	0

[CLPSTAT1:CLPSTAT0]-bit:

This sets the clamp position of input signal. The clamp timing pulse position is internally generated by the AK8851. Clamp timing pulse is generated at the center position of SYNC signal. Its pulse position is adjustable(refer to Fig.5).

[CLPSTAT1:CLPSTAT0]-bit	Start position of Clamp timing pulse [clock counts]	Note
[00]	Center of Sync signal	
[01]	1/128H(496nsec) Delay from center of Sync signal.	
[10]	1/128H(496nsec) before from center of Sync signal	
[11]	2/128H (1usec) before from center of Sync signal	

[CLPWIDTH1:CLPWIDTH0]-bit:

This sets the clamp timing pulse width for the input signal.
*Pulse Width is set by [CLPWIDTH1:CLPWIDTH0]-bit (refer to Fig.5)

[CLPWIDTH1:CLPWIDTH0]-bit	Width of clamp timing pulse [clock counts]	Note
[00]	275nsec	
[01]	555nsec	
[10]	1.1usec	
[11]	2.2usec	

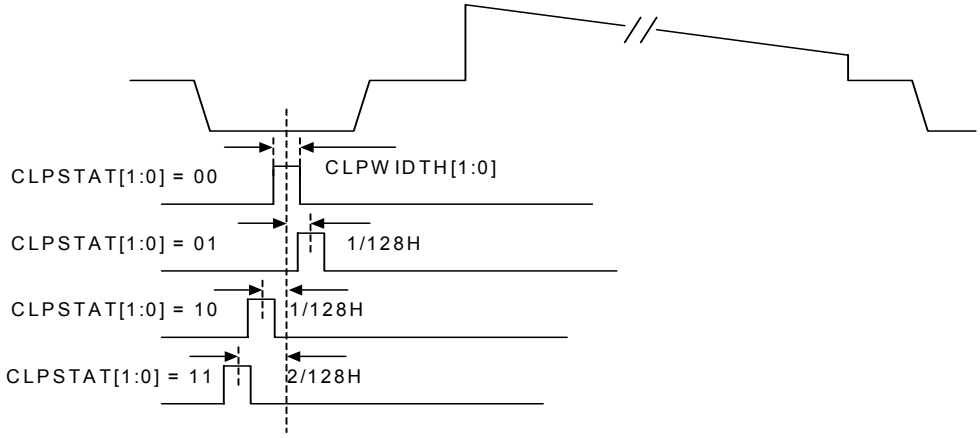


Fig.5 Clamp timing pulse

[EXTCLP]-bit:

This sets the attributes of the EXTCLP pin. Input/Output selection of EXTCLP pin is done by [EXTCLP]-bit register settings. By switching the pin function, it is possible to output an internally- generated Clamp timing pulse or to clamp the input signal by an externally generated Clamp timing pulse.

[EXTCLP]-bit	Attribution of EXTCLP	Note
0	Output the clamp timing pulse of internal pulse generator	Default
1	Input external clamp timing pulse.	

11. CLOCK

The AK8851 operates under the following ,3 clock modes.

(1) Line-Locked Clock Mode

A clock can be derived from the Horizontal SYNC signal (HSYNC) of an input signal. This input signal can be a high quality source like a Standard Signal Generator or DVD. A clock generated in this way is called Line-Locked Clock. If no input signal is present while in Line-locked mode, the AK8851 will automatically switch to Fixed-Clock mode.

(2) Frame-Locked Clock Mode

The input signal's Vertical SYNC can be used to generate a clock when unstable input signals are present, such as those from typical consumer-grade VCR.

A clock generated in this way is called Frame-Locked Clock. If no input signal is present while in Frame-locked mode, the AK8851 will automatically switch to Fixed-Clock mode.

(3) Fixed-Clock Mode

This mode is not controlled by the PLL. This mode is enabled only when no signal is fed into the AK8851 or when this mode is selected via a register setting.

Clock modes are set by [Control 1 Register](R/W)[Sub Address 0x08].
When the clock auto select mode is enabled, the AK8851 automatically shifts its clock mode from/to the Line-locked mode to/from the Frame-locked mode until it selects an optimum mode It shifts to fixed-clock mode only when no input signal condition is detected.

Since the AK8851 uses a clock that is synchronized with an input signal in both the Line-locked and Frame-locked clock modes, ITU-R.656* compatible output is available with input signals of appropriate quality.

PLLs in the AK8851 do not operate when the Fixed-clock mode is selected. The device uses this mode when no input signal is detected in auto select mode (register setting) . For ITU-R.BT656-compatible output, the input clock must be synchronized with the input signal.

A detailed description of the clock mode registers [Control 1 Register] is shown below.

Sub Address 0x08 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	16BITOUT	UVFILSEL	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

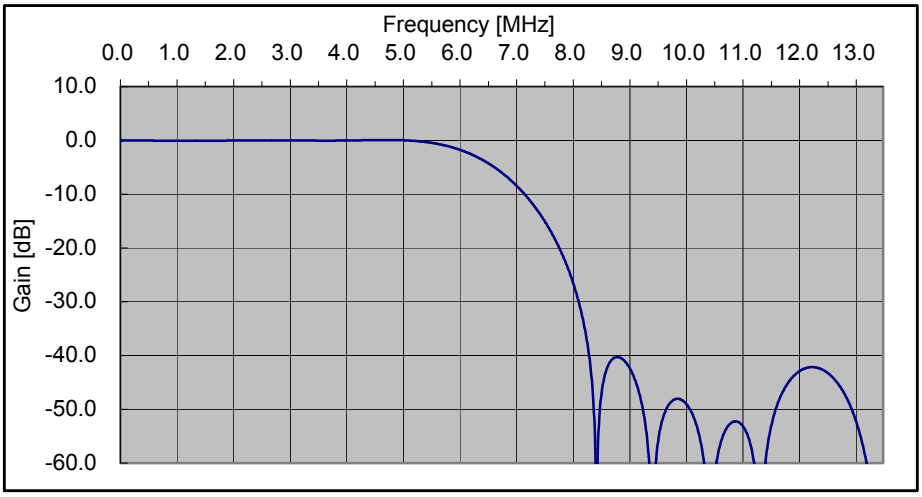
[CLKMODE1:CLKMODE0] -bit

[CLKMODE1: CLKMODE0] (bit-7: bit-6)	Clock mode	Explanation of Clock mode
00	Auto Clock mode	Optimized clock is selected based on the input video signal. (default)
01	Line lock clock	Line Lock clock mode When no signal is input, clock mode changes to Fixed clock mode.
10	Frame lock clock	Frame Lock clock mode. When no signal is input, clock mode changes to Fixed clock mode.
11	Fixed clock mode	Fixed clock mode

12. Decimation Filter

In the AK8851, the input signal is 2x over-sampled at 27 MHz, which is synchronized with the input signal, then it is down-sampled to 13.5 MHz using a decimation filter.

The decimation filter's frequency response plot is shown below.



13.SYNC Separation/SYNC Detection/Phase-Error Detection/Black Level Fine Tuning

SYNC detection and SYNC separation are done on the digitized input signal. The recognized sync-signal is used as a reference the timing for decoding process. The phase error signal is calculated based on the separated SYNC signal which then controls the sampling clock.

In the SYNC separation block, the Luminance signal's Black level can be fine-tuned.

The Fine-tuning band of the Black level is 10-bit wide (before REC 601 conversion) and up to +7 LSB addition or –8 LSB subtraction is possible, in one LSB steps. Output code changes approx. 0.4 LSB per each [1] set.

Black level adjustments are done by [Pedestal Level Control Register](R/W)[Sub Address 0x0C]. Bit allocation of [Pedestal Level Control Register] is shown below.

Sub Address 0x0C **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DPCC1	DPCC0	DPCT1	DCPT0	BKLVL3	BKLVL2	BKLVL1	BKLVL0
Default Value							
0	0	0	0	0	0	0	0

***[BKLVL3:BKLVL0]-bit:**

This register controls fine-tuning of the Black level. Preset register values are added to or subtracted from the Black level. The preset value must be set in 2's complement form. Black level fine-tuning is also valid during the Vertical Blanking period.

[BKLVL3:BKLVL0]-bit	Proc.	Change value in 601 level
0111	Add 7 code to black Level	about 2.8LSB is added.
0110	Add 6 code to black Level	about 2.4LSB is added.
0101	Add 5 code to black Level	about 2.0LSB is added.
0100	Add 4 code to black Level	about 1.6LSB is added.
0011	Add 3 code to black Level	about 1.2LSB is added.
0010	Add 2 code to black Level	about 0.8LSB is added.
0001	Add 1 code to black Level	about 0.4LSB is added.
0000	Default	
1111	Subtract 1 code from black level	about 0.4LSB is subtracted.
1110	Subtract 2 code from black level	about 0.8LSB is subtracted.
1101	Subtract 3 code from black level	about 1.2LSB is subtracted.
1100	Subtract 4 code from black level	about 1.6LSB is subtracted.
1011	Subtract 5 code from black level	about 2.0LSB is subtracted.
1010	Subtract 6 code from black level	about 2.4LSB is subtracted.
1001	Subtract 7 code from black level	about 2.8LSB is subtracted.
1000	Subtract 8 code from black level	about 3.2LSB is subtracted.

14. Digital Pedestal Clamp

The input signal's digitally-converted Pedestal position is clamped in the digital signal-processing block. It handles 2 types of input signals (286 mV-type SYNC signal and 300 mV-type SYNC signal) and it outputs the pedestal position as code 16 (8-bit Rec.601 level) for both input cases.

The digital pedestal clamp function sets the time constant (including ON/OFF) and it also sets the coring level.

Digital Pedestal Clamp characteristics are set by [DPCT1:DPCT0]-bit and [DPCC1:DPCC0]-bit of [Pedestal Level Control Register](R/W)[Sub Address 0x0C].

Bit allocation of [Pedestal Level Control Register] is as follows.

Sub Address 0x0C **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
DPCC1	DPCC0	DPCT1	DCPT0	BKLVL3	BKLVL2	BKLVL1	BKLVL0
Default Value							
0	0	0	0	0	0	0	0

***[DPCT1:DPCT0]-bit:**

This sets the time constant of the digital pedestal clamp.

[DPCT1:DPCT0]-bit	Time constant of Digital Pedestal Clamp	Note
[00]	Fast	
[01]	Middle	
[10]	Slow	
[11]	Disable	

***[DPCC1:DPCC0]-bit:**

This sets the non-sensing bandwidth (coring level) of the digital pedestal clamp.

[DPCC1:DPCC0]-bit	Non-sensing bandwidth of digital pedestal clamp	Note
[00]	1-bit	
[01]	2-bit	
[10]	3-bit	
[11]	No non-sensing range	

15.YC Separation

The AK8851 employs adaptive, two-dimensional Y/C separation.

In the adaptive YC separation function, a correlator detector selects a best-correlated direction among vertical, horizontal and diagonal samples and an optimized YC separation method is selected.

For NTSC-4.43,PAL 60 and SECAM signal input, a primary dimensional Y/C separation mode is selected, regardless of the bit setting.

YC separation control register is set by [Control 1 Register](R/W)[Sub Address 0x08].

Bit allocation of [Control 1 Register] is as follows.

Sub Address 0x08 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	16BITOUT	UVFILSEL	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

*[YCSEP1:YCSEP0]-bit:

this selects YC separation method.

[YCSEP1:YCSEP0]-bit	YC Separation mode	Note
[00]	Adaptive YC Separation mode	1-D YC separation mode is selected when SECAM signal is input
[01]	1-Dim YC Separation mode	
[10]	2-Dim YC Separation mode	1-D YC separation mode is selected when SECAM signal is input
[11]	Reserved	

16. Auto Color Control (ACC)

This function adjusts the input signal's Color Burst level to its appropriate level (NTSC:286 [mV]/ PAL:300 [mV]). The ACC control value can be frozen by register settings. The input color signal level is detected from the Color Burst signal. ACC characteristics are set by [ACC1: ACC0]-bit of [AGC and ACC Control Register](R/W)[Sub Address 0x06]. Bit allocation of [AGC and ACC Control Register] is shown below.

Sub Address 0x06 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACCFRZ	ACC1	ACC0	AGCFRZ	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
0	0	0	0	0	0	0	0

[ACC1:ACC0]-bit:

This selects enabling/disabling ACC function and its time constant.

[ACC1:ACC0]-bit	ACC Time Constant	Note
[00]	Disable	
[01]	Fast	
[10]	Middle	
[11]	Slow	

The ACC and Color Saturation functions operate independently (when the ACC is enabled, Color Saturation adjustment is done on the properly adjusted signal by the ACC).

***[ACCFRZ]-bit:**

This is a control bit to freeze the ACC control value.

[ACCFRZ]-bit	ACC Status	Note
0	ACC function is working	
1	ACC control Value is frozen	

17.Color Killer

The Chroma signal quality is evaluated from the input signal's Color Burst level.

The incoming signal quality's threshold level is setusing the [Color Killer Control Register].

When the input chroma signal level is lower than the preset level, the input chroma signal is treated as insufficient and it is processed as a Black and White signal.

When the Color Burst signal level is lower than the Standard signal levels (NTSC:286 [mV] / PAL:300 [mV]), the Color Killer function is activated.

In this case, Cb/Cr data from the AK8851 is fixed at 0x80 in 601 levels.

Note)

When the Color Killer function is activated, all input signals fed to the YC separation module are processed as Y signal in the same way as in the Black and White mode which is set by [B/W]-bit of [Input Video Standard Register].

Bit allocation of [Color Killer Control Register](R/W)[Sub Address 0x0D] is shown below.

Sub Address 0x0D **Default Value : 0x08**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COLKILL	Reserved	CKSCM1	CKSCM0	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
0	0	0	0	1	0	0	0

***[COLKILL]-bit:**

This selects to enable or disable the Color Killer function.

COLKILL-bit	Color Killer	Note
0	Enable	
1	Disable	

***[CKLVL3:CKLVL0]-bit:**

This sets the level to activate the Color Killer function.

[CKSCM1:CKSCM0]-bit:

This sets the level to activate the Color Killer function in SECAM mode.

18. Black and White Mode

Black and White mode is to process all input signals as Y signal. In this mode, C signal output becomes 0x80 (REC.601 level). When the Black and White mode is selected, YC separation function is disabled.

When the discrete Y/C input signal is fed, only the Y signal is processed and C signal outputs the fixed 0x80 (REC.601 level).

Black and White mode set is done by [B/W]-bits of [Input Video Standard Register](R/W)[Sub Address0x01].

Bit allocation of [Input Video Standard Register] is shown below.

Sub Address 0x01 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	B/W	VLF	VCEN1	VCEN0	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

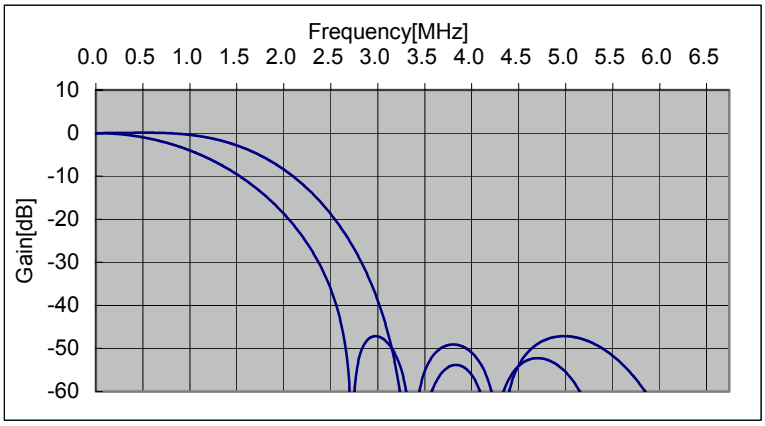
[B/W]-bit:

* This sets the ON/OFF of Black and White mode.

B/W-bit	Status of B/W mode	Note
0	OFF	Normal Decode
1	ON	Y-Signal: Sampling data is output after converting to Rec.601 Level C-Signal: All the C-data is output as the value of 0x80. (All data is output through Luminance data process)

19.UV Filter

The U/V signal bandwidth can be altered by switching the characteristics of the low pass filter positioned after de-modulation of the C signal. Two filter types can be selected.



Switching the U/V low pass filters is done by [UVFILSEL1:UVFILSEL0]-bit of [Control 1 Register](R/W)[Sub Address 0x08].

Bit allocation of [Control 1 Register] is shown below.

Sub Address 0x08 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	16BITOUT	UVFILSEL	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

***[UVFILSEL]-bit:**

This selects the bandwidth of the UV filters. Please refer to the frequency response characteristics.

[UVFILSEL]-bit		Note
0	Wide	
1	Narrow	

20.Image Quality Adjusting Function

The AK8851 has Image Quality Adjusting functions that include Contrast, Brightness, Sharpness , Color Saturation and Hue adjustments.

By default, the Image Quality adjustment function is invalid during the Vertical Blanking period. However Contrast and Brightness adjustments can be enabled by setting [VBIIMGCTR]-bit of [Image Control Register].

(1) Contrast Adjustment

Contrast Adjustments are made by multiplying the Luminance signal (Y) by the gain factor set by [Contrast Control Register](R/W)[Sub Address 0x0E].

Contrast factor is processed on the 8-bit data after 601 level conversion as shown in the following equation.

Yout = CONT* (YIN-128)+128; where Yout : Contrast arithmetic result
Yin : Contrast level before arithmetic operation
CONT: Contrast factor (register set value)

Adjustable range of the Contrast Gain factor is from 0 ~ 1.99 (1/128 step).When the result exceeds the specified range, it is clipped to upper limit (254) or lower limit (1) (output result ranges from 16 to 235 with 601 limit-bit at “1”).

Bit allocation of [Contrast Control Register] is as follows.

Sub Address 0x0E **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

(2) Brightness Control

Brightness adjustment is accomplished by adding to the Luminance signal (Y) a value set by [Brightness Control Register](R/W)[Sub Address 0x0F].

Brightness factor is processed on the 8-bit data after 601 level conversion as follows.

Yout = Yin + BR where Yout : Brightness arithmetic result
Yin : Brightness before arithmetic operation
BR: Brightness Factor (register set value)

The Adjustable range of Brightness is from –127 to +127.The value setting is done in 2’s complement number.
When the result exceeds the specified range, it is clipped to the upper limit (254) or the lower limit (1).(output result ranges from 16 to 235 with 601 limit-bit at “1”).

Bit allocation of [Brightness Control Register] is shown as follows.

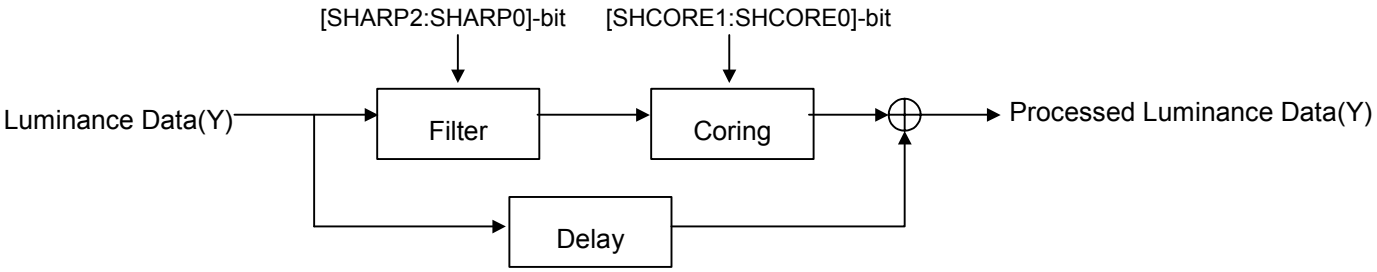
Sub Address 0x0F **Default Value : 0x00**

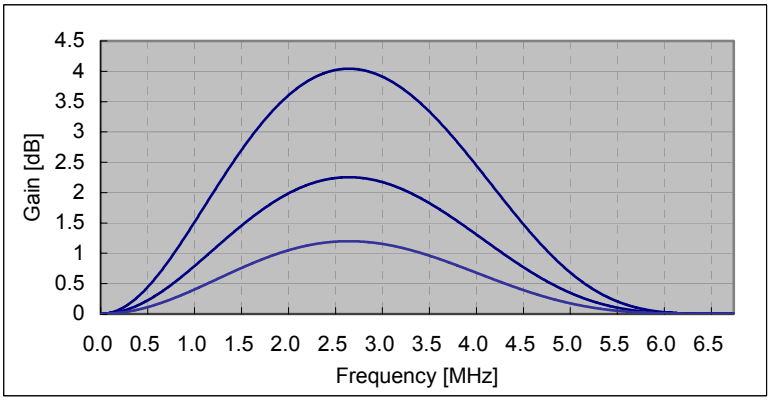
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

(3) Sharpness Control

For sharpness control, the following signal processing is performed on the Luminance (Y) signal as shown in the block diagram below. One of the 3 different type filter characteristics in the block is selected by [SHARP1: SHARP0]-bit of [Image Control Register](R/W)[Sub Address 0x10]. The Coring level is adjustable within the range of 0 LSB ~ +/- 3 LSBs which is set by [SHCORE1: SHCORE0]-bit.

Image Sharpness is controlled by properly selecting the filter characteristics.





Bit Allocation of [Image Control Register] is shown.

Sub Address 0x10 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIIMGCTL	SEPIA	LUMFIL1	LUMFIL0	SHCORE1	SHCORE0	SHARP1	SHARP0
Default Value							
0	0	0	0	0	0	0	0

[SHARP1:SHARP0]-bit:

* This selects sharpness filter types.

[SHARP2:SHARP0]-bit	Selected filter	Note
[00]	Through	
[01]	Sharpness effect Min.	
[10]	Sharpness effect Mid.	
[11]	Sharpness effect Max.	

[SHCORE1:SHCORE0]-bit:

* This sets the Coring Level after sharpness filtering is done.

[SHCORE1:SHCORE0]-bit	Coring Level	Note
[00]	No Coring	
[01]	+/- 1LSB	
[10]	+/- 2LSB	
[11]	+/- 3LSB	

(4) Color Saturation Control

Color Saturation adjustment is made by multiplying the Chroma signal (C) with a fixed value set by [Saturation Control Register](R/W)[Sub Address 0x11]. The Saturation factor is performed on C signal. A result of multiplied Saturation factor is U/V- modulated.

Adjustable range of Saturation multiplying factor is from 0 to 255/128 in 1/128 per step.

Default value of this register is an un-adjusted value of (0x80).

Bit allocation of [Saturation Control Register] is shown below.

Sub Address 0x11 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

(5) HUE Control

The AK8851 can rotate HUE characteristics. Rotation of Hue is controlled by [Hue Control Register](R/W)[Sub Address 0x12].

Hue adjustment ranges from + 45 degrees to – 45 degrees in 0.35 per step.

Default value of this register is the un-adjusted value (0x80),set the value in 2's complement number.

Bit allocation of [HUE Control Register] is as shown below.

Sub Address 0x12 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

(6) SEPIA Color Output

This is a function to output the decoded result in sepia color, which is set by [SEPIA]-bit of [Image Control Register].

* [SEPIA]-bit:

This is to output the decoded result in sepia color.

[SEPIA]-bit	function	Note
0	Normal	
1	Sepia color	

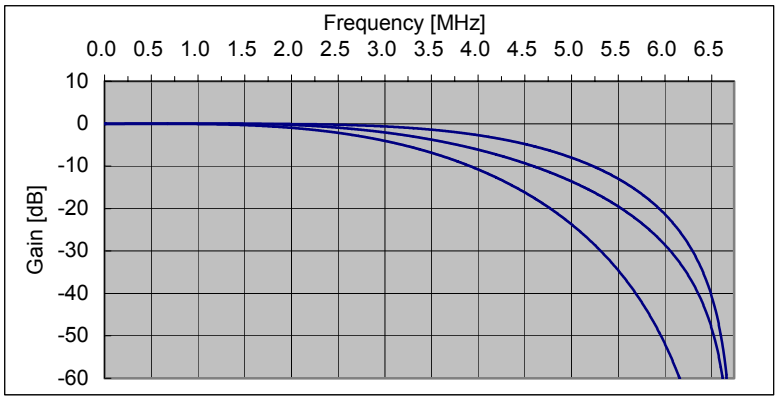
(7) Luminance Bandwidth Adjustment

To maximize the compression ratios in MPEG and other digital video formats, it is often desirable to limit the Luminance bandwidth through pre-processing before compression. T.

For this purpose, Luminance signal band-limiting-filters can be selected. When these filters are not used, the frequency response of the Luminance signal tracks the decimation filter characteristics.

Selection of Luminance band-limiting-filters is done by [LUMFIL1:LUMFIL0]-bit of [Image Control Register](R/W)[Sub Address 0x10].

Selectable filter characteristics are shown below.



Bit allocation of [Image Control Register]-bit is shown below.

Sub Address 0x10 Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIIMGCTL	SEPIA	LUMFIL1	LUMFIL0	SHCORE1	SHCORE0	SHARP1	SHARP0
Default Value							
0	0	0	0	0	0	0	0

[LUMFIL1:LUMFIL0]-bit:

* This selects Luminance signal band limiting filters.

[LUMFIL1:LUMFIL0]-bit	Filter	Note
[00]	No band limiting filter	Frequency characteristic is same as the decimation filter -3dB@6.29MHz
[01]	Narrow	-3dB@2.94MHz
[10]	MID.	-3dB@3.3MHz
[11]	WIDE	-3dB@4MHz

21. Vertical Blanking Interval

Setting of Vertical Blanking Interval and selecting tasks to be performed during this interval are set by [Output Format Register](R/W)[Sub Address 0x02].
Default values of Vertical Blanking Interval are as follows:

525 Line system : Line 1 ~ Line19 and Line 263.5 ~ Line 282.5
625 Line system : Line 623.5 ~ Line 625-Line 1 ~ Line 22 and Line 311 ~ Line 335.5

Vertical Blanking Interval is set by [VBIL2:VBIL0]-bit.

Transition point of V-bit in Video Timing Reference code can be changed by [TRSVSEL]-bit of [Output Format Register]. By properly setting [TRSVSEL]-bit, the transition point of V-bit can be ITU-R BT.656-3, ITU-R BT.656-4 or SMPTE125M compatible.

During the Vertical Blanking Interval, the default value of the output is set to Black level (Y=0x10,Cb/Cr= 0x80).
By setting [VBIDEC]-bit of [Output Format Register] to "1", the YC separation function is turned off on those Lines that to be processed during the Vertical Blanking Interval, and input signal is directly output as a Y signal as in the case of Black and White mode.
During the Vertical Blanking Interval, the set-up processing is not performed even when [SETUP]-bit of [Input Video Standard Register] is set.

Bit allocation of [Output Format Register] is shown below.

Sub Address 0x02 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVEL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

[VBIL2:VBIL0]-bit:
Length of the default Vertical Blanking Interval is adjusted via the[VBIL2:VBIL0]-bit.
* Set Value vs. Vertical Blanking Interval relationship is shown in the following table.

[VBIL2:VBIL0]-bit	Vertical Blanking Interval		Note
	525-line system	625-Line system	
000	Line 1 ~ Line 19	Line 623.5 ~ Line 625 - Line 1 ~ Line 22	Default
	Line 263.5 ~ Line 282.5	Line 311 ~ Line 335.5	
001	Line1 ~ Line20	Line 623.5 ~ Line 625 - Line 1 ~ Line 23	+ 1 Line
	Line263.5 ~ Line 283.5	Line 311 ~ Line 336.5	
010	Lie 1 ~ Line 21	Line 623.5 ~ Line 625 - Line 1 ~ Line 24	+2 Line
	Line 263.5 ~ Line 284.5	Line 311 ~ Line 337.5	
011	Line 1 ~ Line 22	Line 623.5 ~ Line 625 - Line 1 ~ Line 25	+ 3 Line
	Line 263.5~Line 285.5	Line 311 ~ Line 338.5	
111	Line 1 ~ Line 18	Line 623.5 ~ Line 625 - Line 1 ~ Line 21	- 1 Line
	Line 263.5 ~ Line 281.5	Line 311 ~ Line 334.5	
110	Line 1 ~ Line 17	Line 623.5 ~ Line 625 - Line 1 ~ Line 20	- 2 Line
	Line 263.5 ~ Line 280.5	Line 311 ~ Line 333.5	
101	Line 1 ~ Line 16	Line 623.5 ~ Line 625 – Line 1 ~ Line 19	- 3 Line
	Line 263.5 ~ Line 279.5	Line 311 ~ Line 332.5	
100	LIne-1 ~ Line15	Line 623.5 ~ Line 625 – Line 1 ~ Line 18	- 4 Line
	Line 263.5 ~ Line278.5	Line 311 ~ Line 331.5	

[TRSVSEL]-bit:
TRSVSEL-bit is a control bit specify the handling of the V-bit in Rec.656 EAV/SAV code.
This bit performs as in the following table, and is independent of the Vertical Blanking Interval specified by the [VBIL2:VBIL0]-bit.

< V-bit value vs. Line relation >

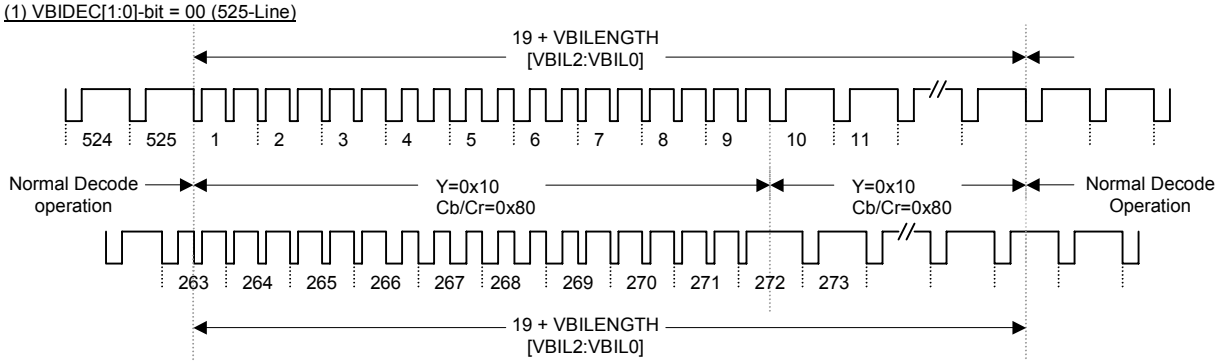
V-bit	NTSC(525 System)		PAL/SECAM(625 System)	
	TRSVSEL=0 ITU-R Bt.656-3	TRSVSEL=1 ITU-R Bt.656-4 SMPTE125M	TRSVSEL=0	TRSVSEL=1
V-bit = 0	Line10~Line263 Line273~Line525	Line20~Line263 Line283~Line525	Line23~Line310 Line336~Line623	
V-bit = 1	Line1~Line9 Line264~Line272	Line1~Line19 Line264~Line282	Line1~Line22 Line311~Line335 Line624~Line625	

note)
TRSVSEL-bit setting applies to all 525 and 625 Line systems as shown in the above table.

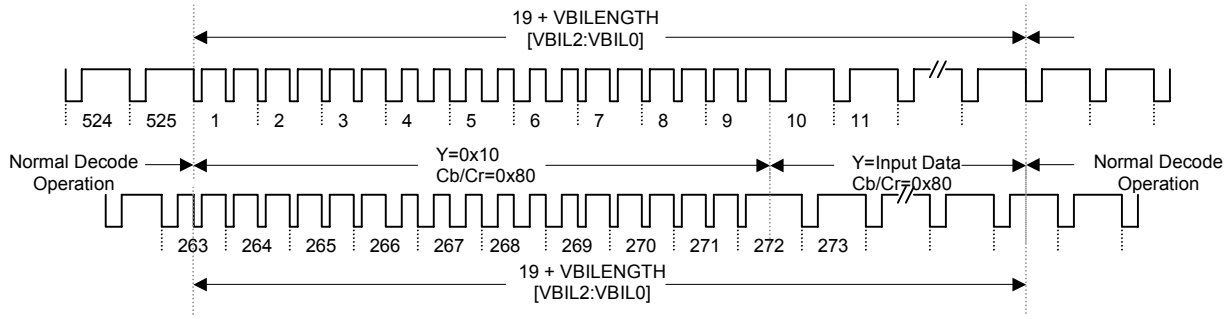
[VBIDEC1:VBIDEC0]-bit:
This is a control bit to set tasks during Vertical Blanking Interval specified by [VBIL2:VBIL0]-bit.

[VBIDEC1:VBIDEC0]-bit	VBI data output	Note
00	Black Level Output	Y = 0x10 Cb/Cr = 0x80
01	Black and White mode	Y = sampling data is converted to Rec.601 Level Cb/Cr = 0x80
10	Sliced data is output during VBI Interval	Y/Cb/Cr = Sliced level which set at the Slicer Register
11	Reserved	Reserved

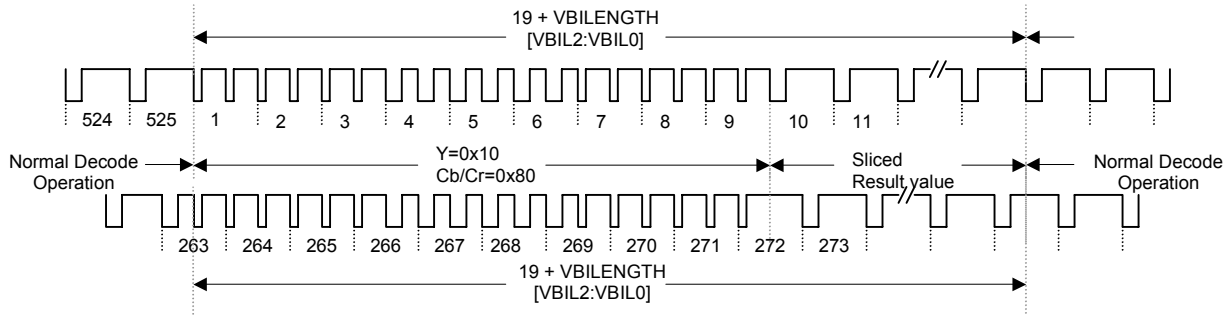
(1) VBIDEC[1:0]-bit = 00 (525-Line)



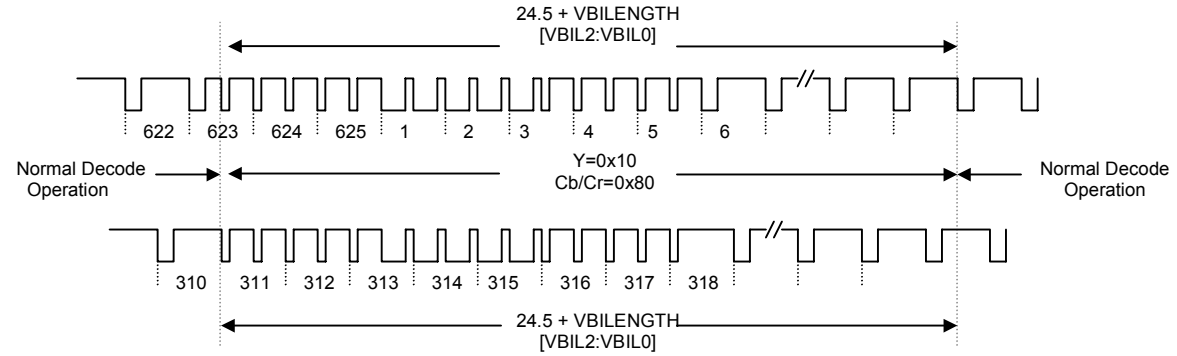
(2) VBIDEC[1:0]-bit = 01 (525-Line)



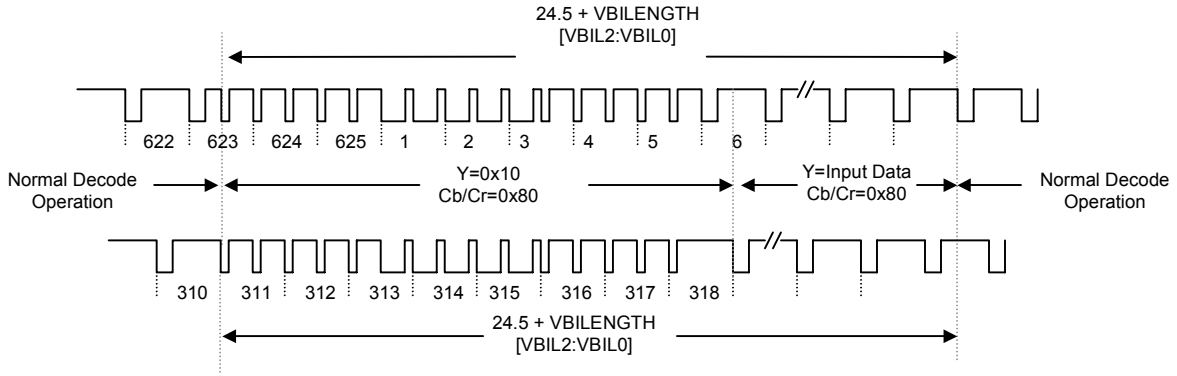
(2) VBIDEC[1:0]-bit = 10 (525-Line)



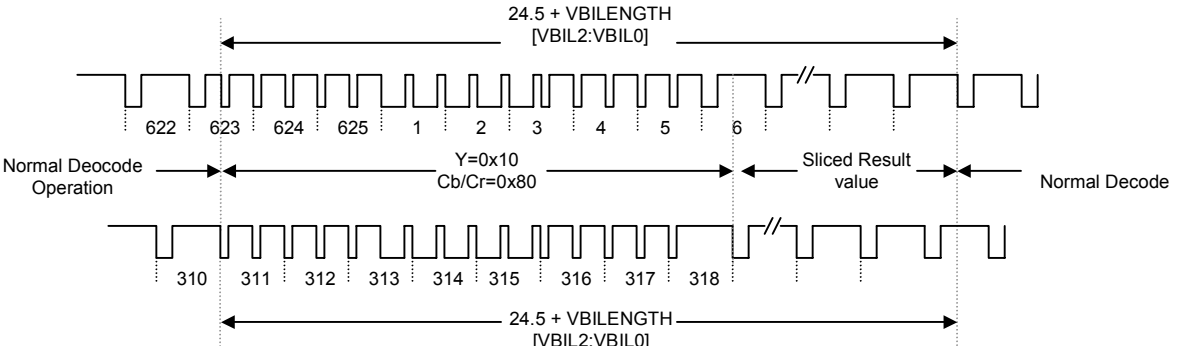
(1) VBIDEC[1:0]-bit = 00 (625-Line)



(2) VBIDEC[1:0]-bit = 01 (625-Line)



(2) VBIDEC[1:0]-bit = 10 (625-Line)



22. Closed Caption/Closed Caption Extended Data/ VBID (CGMS)/WSS

The AK8851 decodes Closed Caption, Closed Caption extended, , VBID (CGMS) and WSS signals that are super-imposed on the Vertical Blanking signal. Decoded data is written into a register.

When the request bit [bit3:bit0] of [Request VBI INFO Register](R/W)[Sub Address 0x15] is set, the AK8851 is put into a data wait state as each data decode request is made.

After data detect and decoding, [bit3:bit0] of [Status 2 Register](R)[Sub Address0x17] tells a host that decoding is complete. Decoded results are written into [Closed Caption 1/2 Register],[Extended Data 1/2 Register],[WSS 1/2 Register] and [VBID 1/2 Register] respectively.

Each data is super-imposed on the lines listed below. As for the VBID data (CGMS-A), CRCC code is decoded and its result only is stored in register.

Signal	Decoded Line	Note
Closed Caption	NTSC: Line-21	525-Line System
Closed Caption Extended	NTSC: Line-284	525-Line System
VBID	NTSC: Line-20/283 PAL: Line-20/333	525-Line System 625-Line System
WSS	PAL: Line-23	625-Line System

Bit allocation of [Request VBI INFO Register] is shown below.

Sub Address 0x15

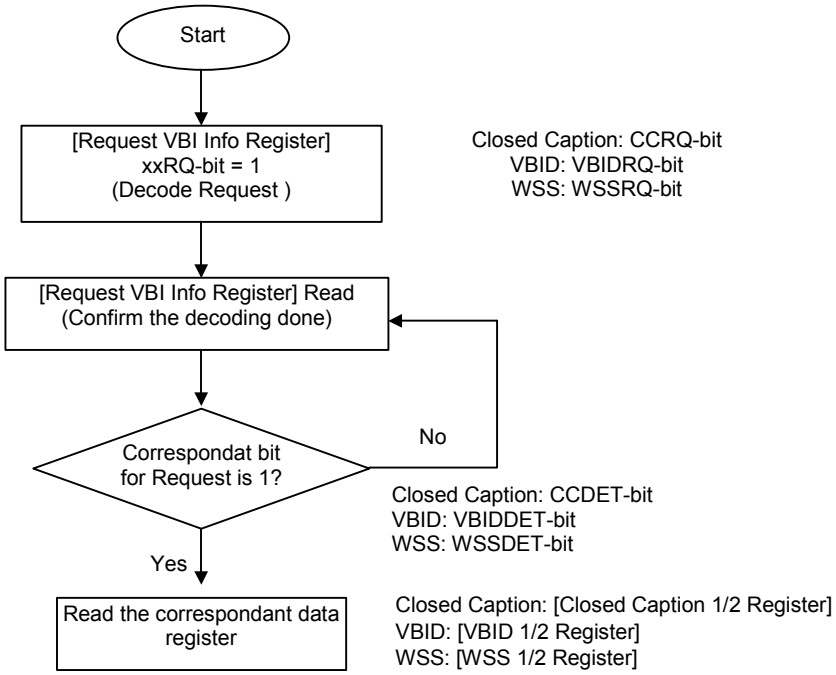
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Bit allocation of [Status 2 Register] is shown below.

Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	REALFLD	WSSDET	VBIDDET	EXTDET	CCDET

VBI interval Read operation of is shown in the following flow chart.



Read Operation of Closed Caption Data:

When the CCRQ-bit is “1”, the AK8851 is placed into a wait state for the Closed Caption data decoding. Data is decoded as data is received, and after the decoding is completed, ”1” is sent back to CCDET-bit of [Request VBI INFO Register]. CCDET-bit is at “1” right after a reset (it becomes “0” by writing “1” at CCRQ-bit).
The decoded data is then written into [Closed Caption 1 Register](R)[Sub Address 0x1A] and [Closed Caption 2 Register](R)[Sub Address 0x1B] as shown.
Data in [Closed Caption 1 Register] and [Closed Caption 2 Register] are maintained until they are over-written.

Bit allocation of [Closed Caption 1 Register] and [Closed Caption 2 Register] are shown below.

[Closed Caption 1 Register] (R) [Sub Address 0x1A]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

[Closed Caption 2 Register] (R) [Sub Address 0x1B]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

Closed Caption Extended Data Read Operations:

When the EXTRQ-bit=”1”, the AK8851 is put into a wait state for the Extended Data decoding. Data is decoded as data is received, and after the decoding is completed, ”1” is sent back to EXTDET-bit of [Request VBI INFO Register]. EXTDET-bit is “1” right after a reset (it becomes “0” by writing “1” at EXTRQ-bit). The decoded data is written into [Extended Data 1 Register](R)[Sub Address 0x1E] and [Extended Data 2 Register](R)[Sub Address 0x1F] as shown.
Data in [Extended Data 1 Register] and [Extended Data 2 Register] are maintained until they are over-written.

Bit allocation for [Extended Data 1 Register] and [Extended Data 2 Register] are shown below.

[Extended Data 1 Register] (R) [Sub Address 0x1E]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

[Extended Data 2 Register] (R) [Sub Address 0x1F]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

Read Operation of VBID Data :

When the VBIDRQ-bit = “1”, the AK8851 is put into a wait state for the VBID data decoding. Data is decoded as data is received, and after the decoding is completed ”1” is sent back to VBIDDET-bit of [Request VBI INFO Register](R/W)[Sub Address 0x15].
VBIDDET-bit is at “1” right after a reset (it becomes “0” by writing “1” at VBIDRQ-bit). The decoded 13-bit data is written into [VBID 1 Register](R)[Sub Address 0x20] and [VBID 2 Register](R)[Sub Address0x21] as shown.
CRCC code is decoded and only the result is stored in register. Data in [VBID1 Register] and [VBID 2 Register] are maintained until they are over-written.

Bit Allocation of [VBID 1 Register] and [VBID 2 Register] are shown below.

[VBID 1 Register] (R) [Sub Address 0x20]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

[VBID 2 Register] (R) [Sub Address 0x21]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

Read Operation of WSS Data :

When the WSSRQ-bit = “1”, the AK8851 is put into a wait state for the WSS data decoding. Data is decoded as data is received, and after the decoding is completed, ”1” is sent back to WSS-bit of [Status 2 Register]. WSS-bit is at “1” right after the reset (it becomes “0” by writing “1” at WSSRQ-bit).

The decoded data is written into [WSS 1 Register](R)[Sub Address0x1C] and [WSS 2 Register](R)[Sub Address 0x1D]. Data in [WSS 1 Register] and [WSS 2 Register] are maintained until they are over-written.

[WSS1 Register] (R) [Sub Address 0x1C]

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

[WSS 2 Register] (R) [Sub Address 0x1D]

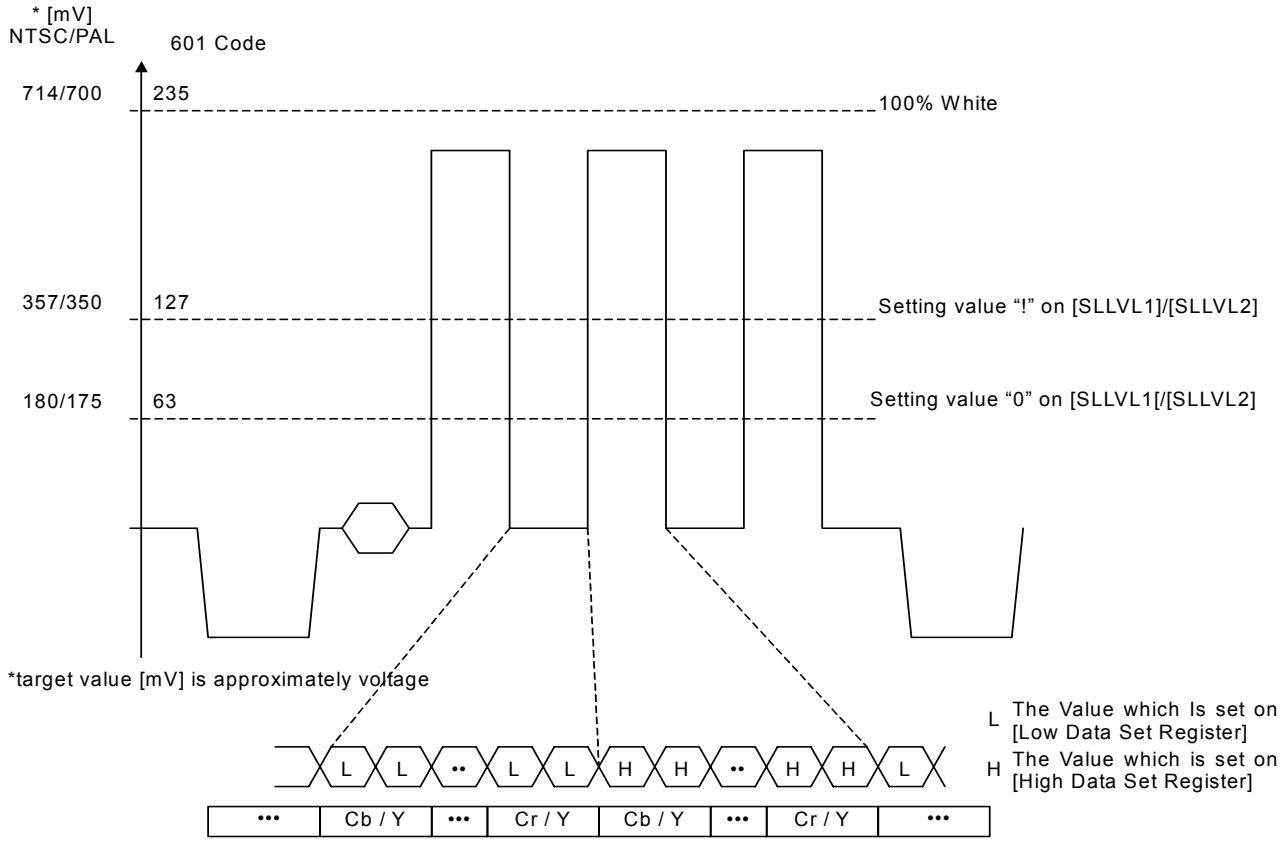
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

23. VBI Slice Function

The AK8851 has a function to slice VBI data. The sliced data is output in 601 digital format.

The VBI slice function is handled in the Luminance signal-processing path. In the VBI function, the 601-output codes for Cb/Cr values for the selected Lines are equal to corresponding Luminance signals.

Slice level and the output code are set via register. Lines to be sliced include all Lines within the VBLANK interval that are specified by the [Output Format Register].



Bit allocation of [Output Format Register] is shown below.

Sub Address 0x02 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

[VBIDEC1:VBIDEC0]-bit:

* This is a control bit to set tasks during the Vertical Blanking interval which is specified by [VBIL2 :VBIL0]-bit.

[VBIDEC1:VBIDEC0]-bit	VBI data output	Note
00	Black Level Output	Y = 0x10 Cb/Cr = 0x80
01	Black and White mode	Y = sampling data is converted to Rec.601 Level Cb/Cr = 0x80
10	Sliced data is output during VBI Interval	Y/Cb/Cr = Sliced level which set at the Slicer Register
11	Reserved	Reserved

[SLLVL1 : SLLVL0]-bit :

* Those are to set the slice level.

[SLLVL]-bit	Setting	Note
0	Slice level is set to about 25IRE.	63@ Rec.601 Level
1	Slice level is set to about 50IRE	127@ Rec.601 Level

High and low values of the sliced and binary-converted data are set by [High Data Set Register] and [Low Data Set Register].The values set here are output as 656 data. Default values are 235 for High and 16 for Low.

[High Data Set Register]

Sub Address 0x13 **Default Value : 0xEB**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0
Default Value							
1	1	1	0	1	0	1	1

[Low Data Set Register]

Sub Address 0x14 **Default Value : 0x10**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L_7	L_6	L_5	L_4	L_3	L_2	L_1	L_0
Default Value							
0	0	0	1	0	0	0	0

24. MACROVISION Decoder

When a MACROVISION copy-protected signal is fed to the input, the AK8851 decodes the added MACROVISION information and stores its result in [Macrovision Status Register](R)[Sub Address 0x18]. Configuration of [Macrovision Status Register] is shown below.

Sub Address 0x18

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	CSTYPE	CSDET	AGCDET

[AGCDET]-bit :

when the Macrovision AGC process is detected, this bit becomes “1”.

[AGCDET]-bit	Status of Macrovision detection	Note
0	AGC Process is not detected	
1	AGC Process is detected	

[CSDET]-bit :

when the Macrovision Color Stripe Process is detected, this bit becomes “1”.

[CSDET]-bit	Status of Macrovision detection	Note
0	Color Stripe Process is not detected	
1	Color Stripe Process is detected	

[CSTYPE]-bit :

When CSDET-bit is “1”, this bit shows types of Color Stripe Process.

[CSTYPE]-bit	Status of Macrovision detection	Note
0	Detected Color Stripe is Type 2	
1	Detected Color Stripe is Type 3	

When CSDET-bit is not “1” , this bit has no meaning.

25. Decode Data Output (Rec.601 limit / YC Delay / Timing)

The AK8851 outputs decoded data in ITU-R BT.601 compatible format (Y /Cb /Cr 4:2:2). The minimum and maximum output code values are selectable by the [601 LIMIT]-bit of [Output Format Register](R/W)[Sub Address 0x02].
The AK8851 also allows ine-tuning of the decoded data's output timing ..
Adjustable parameters are the Active Video Interval Start Position and Delay Time for Luminance and Chroma signals. YC Delay time and Active Video Interval Start Position are programmable via the [Start and Delay Control Register].

Bit allocation of [Output Format Register] is shown below.

Sub Address 0x02 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

[601 LIMIT]-bit :
This bit specifies Min. and Max. values of output data. Internal arithmetic operation is performed, based on Min.=1 and Max.=254 always.
The output code Clipping value also differs by [601 LIMIT]-bit setting. Default value is "0".

[601LIMIT]-bit	Output code Min/Max	Note
0	Y: 1~254 Cb/Cr: 1~254	Default
1	Y: 16~235 Cb/Cr: 16~240	

Bit allocation of [Start and Delay Control Register] is listed below.

Sub Address 0x05 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	ACTSTAT2	ACTSTAT1	ACTSTAT0	Reserved	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

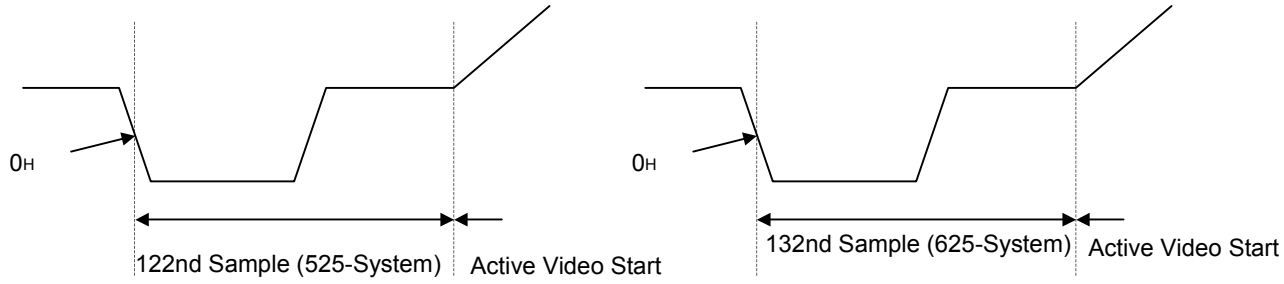
[YCDELAY2 : YCDELAY0]-bit :
This control bit to fine-tunes the YC output timing (YC Output Delay) for the decoded data.
* Fine-tuning of YC Output Delay Time is set in 2's complement number.

[YCDELAY2:YCDELAY0]-bit	YC Delay	Note
101	Y data is delayed 3 samples (222nsec) to C data	
110	Y data is delayed 2 samples (148nsec) to C data	
111	Y data is delayed 1 sample (74nsec) to C data	
000	No delay between Y data and C data	Default
001	Y data is advanced 1 sample (72nsec) to C data.	
010	Y data is advanced 2 samples (148nsec) to C data.	
011	Y data is advanced 3 samples (222nsec) to C data.	

[ACTSTAT2 : ACTSTAT0]-bit :

This bit allows fine-tuning of the Active Video Start Position.

The Default Start Position is shown in the following diagram (information from Rec.601 specification)



[ACTSTAT2:ACTSTAT0]-bit	Function	Note
101	525-System: Active Video starts from 120th sample 625-System: Active Video starts from 130th sample	
110	525-System: Active Video starts from 121st sample 625-System: Active Video starts from 131st sample	
111	525-System: Active Video starts from 122nd sample 625-System: Active Video starts from 132nd sample	
000	525-System: Active Video starts from 123rd sample 625-System: Active Video starts from 133rd sample	Default
001	525-System: Active Video starts from 124th sample 625-System: Active Video starts from 134th sample	
010	525-System: Active Video starts from 125th sample 625-System: Active Video starts from 135th sample	
011	525-System: Active Video starts from 126th sample 625-System: Active Video starts from 136th sample	

26. Output Interface

(1) ITU-R BT.656 Interface

The AK8851 outputs decoded data in ITU-R BT.656 compatible interface format.

ITU-R BT.656 compatible output data means:

* Samples per Line: 858 samples (525 system)/864 samples (625 system)
* Line numbers per Frame : 525 Lines / 625 Lines

The above output cannot be obtained when the input signal quality is poor (if using the fixed clock mode, and a good input signal, the above specification may not be met).

In the AK8851, the PLL is locked to the input signal and buffers on the output stage absorb input signal jitter, which assures ITU-R BT.656 compatible output.

However when the input signal jitter is very large and exceeds the allowable range of the output buffer, ITU-R BT.656 output cannot be met. In this case, one of the following output modes is set via registers.

(1-1) Guarantee of 858 samples:

Number of samples per Line is guaranteed to be 858 or 864.

When ITU-R BT.656 is not met, Line-drop or Line-repeat processing is performed. This means that the number of Lines per Frame is not necessarily 525 or 625 (524 or 624 Lines for Line-drop cases. 526 or 626 Lines at Line-repeat cases).

The above Line-drop or Line-repeat processing can take place at any arbitrary Lines of each Frame.

(1-2) Guarantee of 525 / 625 Lines :

Number of Lines per Frame is guaranteed to be 525 or 625. In this mode, Pixel-drop or Pixel-repeat processing is performed at the last Line of each Field/Frame. This means that the number of samples per Line is not always 858 or 864 (the output buffer is cleared at the last Line of either each Frame or each Field so that the remaining size of the output buffer is set to its maximum value).

Field or Frame selection of this processing is set by register.

ITU-R BT.656 interface process-related register is [ERRHND1 ERRHND0]-bit of [Control 2 Register][Sub Address 0x09].

Sub Address 0x09 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	ERRHND1	ERRHND0	NOSIGDET	BLUEBACK	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

[ERRHND1:ERRHND0]-bit

[ERRHND1:ERRHND0]-bit	Function	Note
00	Line drop/repeat is done The number of sample is 858/864. Depending of the input video signal quality, the number of Lines for output data is not 525/625 lines.	Default
01	Pixel drop/repeat is done. Pixel drop/repeat is done at line in the end of frame. The number of lines in the frame is 525/625. Depending of the input video signal quality, the number of samples in the last of line in field is not 858/864 samples.	
10	Pixel drop/repeat is done. Pixel drop/repeat is done at line in the end of frame. The number of lines in the frame is 525/625. Depending of the input video signal quality, the number of samples in the last of line in frame is not 858/864 samples.	
11	Reserved	

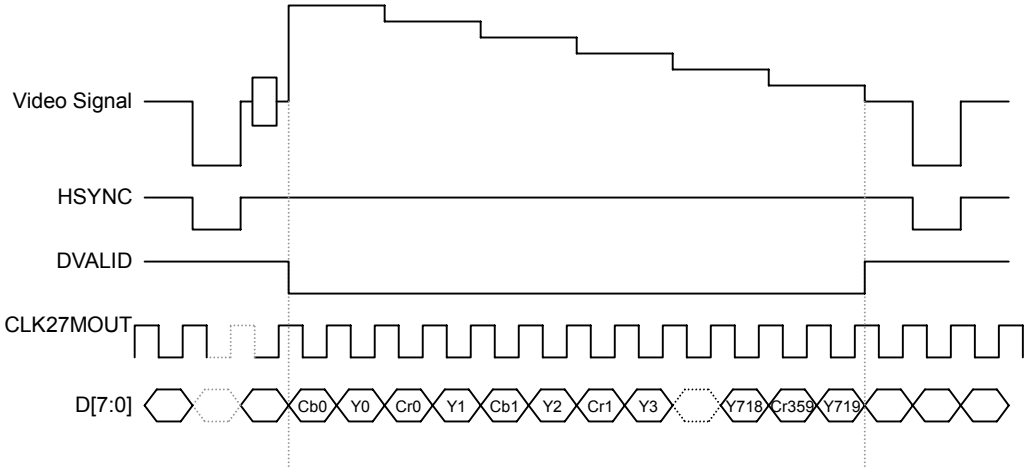
(2) Interface by DVALID Signal

When the ITU-R BT.656 interface is not available, the AK8851 can output data by the DVALID signal that becomes valid during the Active Video interval.

DVALID signal and data output relation is shown in the following timing diagram.

* DVALID Signal Timing

DVALID signal timing to indicate Active Video interval is shown.

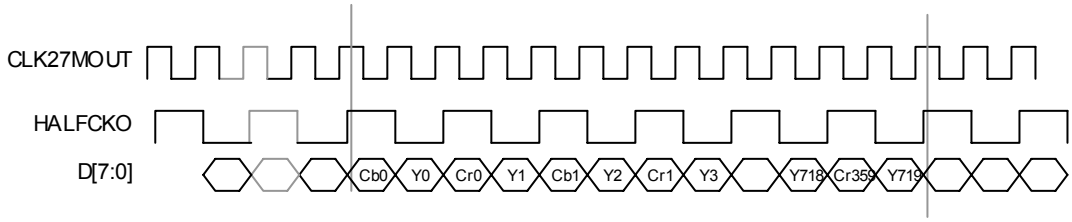


Start position of Active Video
(Normally, 123rd/133rd(NTSC/PAL) sample from 0H sample)

(3) Output Mode

(3-1) 8-Bit Output Mode (default)

Output timing of D[7:0] and HALFCKO is as follows. HALFCKO functions as reference signal of Luminance and Color data.

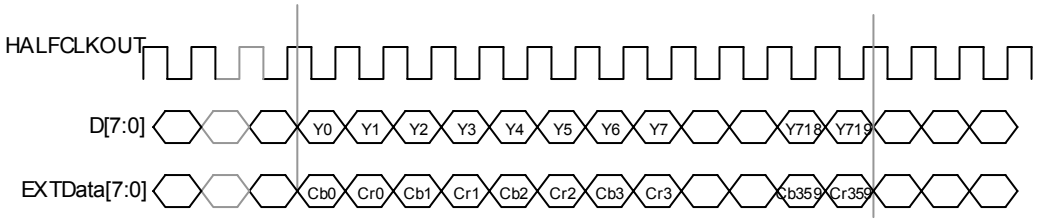


(3-2) 16-Bit Output Mode

The AK8851 can output data in 16-Bit format by setting a register.

The register is [16BITOUT]-bit of [Control 1 Register](R/W)[Sub Address 0x08].

Output timing is as follows.

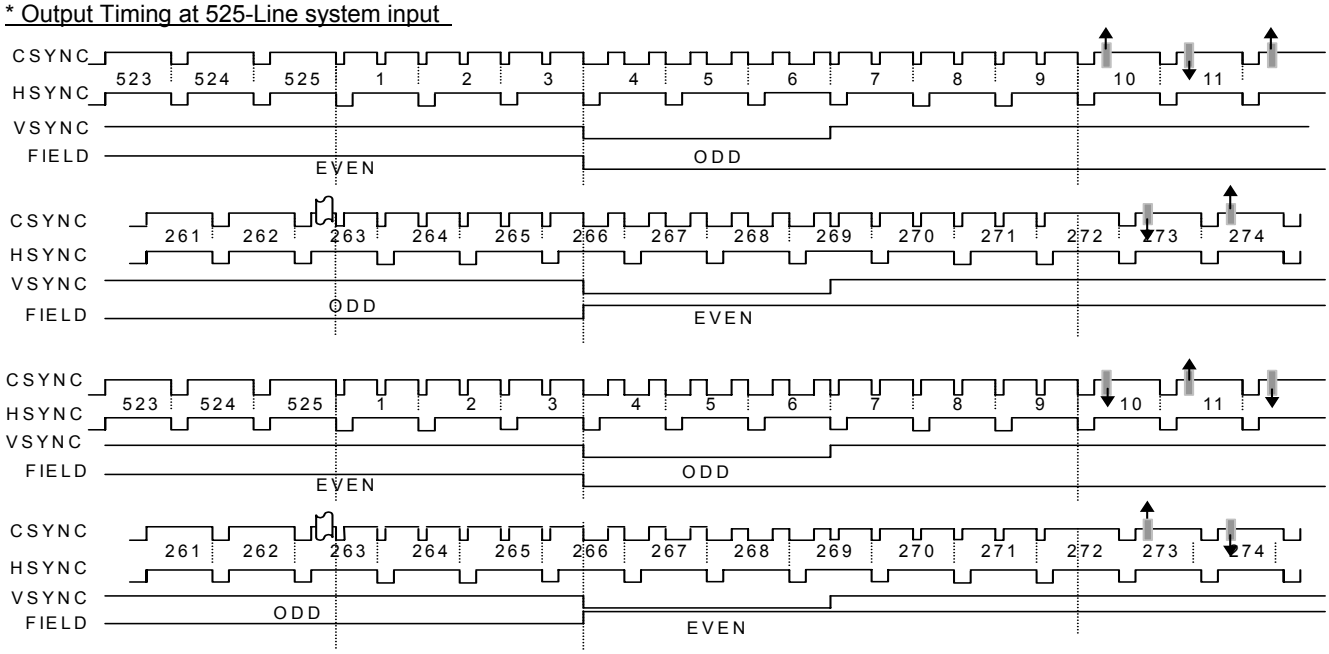


(4) Output of Various Timing Signals

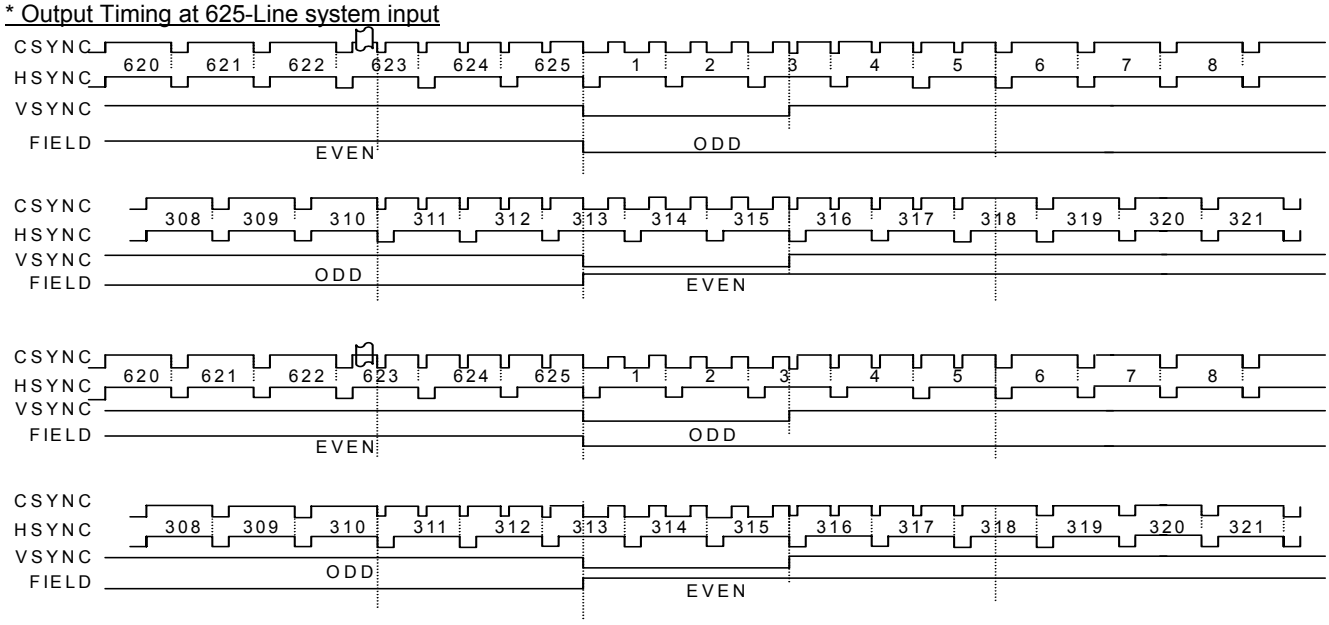
The AK8851 generates following timing signal outputs.

Pin Name	525-Line System	625-Line System
HSYNC	15.734kHz Interval. Low interval is about 4.7[usec]	15.625kHz Interval Low Interval is about 4.7[usec]
VSYNC	Low output between Line4 ~ Line6 / Line266.5~Line269.5	Low output between Line1~ Line3.5/Line313.5~ Line315
CSYNC	Composite Sync output	
FIELD	ODD-Field: Low EVEN-Field: High	
DVALID	Low while Active video. (Index timing signal)	

* Output Timing at 525-Line system input



* Output Timing at 625-Line system input



27.Blue-Back Function

The Output can be set to Blue-Back mode by setting a register via the host CPU.
The output code at Blue-Back mode is
Y=41,Cb=240,Cr=110

The Blue-Back mode set is done by [BLUEBACK]-bit of [Control 2 Register]((R/W)[Sub Address 0x09].
* Bit allocation of [Control 2 Register] is as follows.

Sub Address 0x09 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	STUPATOFF	ERRHND1	ERRHND0	Reserved	BLUEBACK	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

*** [BLUEBACK]-bit :**

Output code becomes blue by setting this bit.

[BLUEBACK]-bit	Output Code	Note
0	Normal Decode Process	
1	Blueback code output	Y = 41 Cb = 240 Cr = 110

28.Phase Compensation Function of PAL Decoder

This is a phase compensation function for each Line when decoding PAL signals.
Correlation detection is used for phase error compensation and it is applicable only for correlated samples. For NTSC signals, a color averaging process between Lines is performed.
This function is set by [Control 2 Register](R/W)[Sub Address 0x09].

Sub Address 0x09 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	STUPATOFF	ERRHND1	ERRHND0	Reserved	BLUEBACK	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

[DPAL1:DPAL0]-bit :

* PAL Phase Error compensation is set by [DPAL]-bit.

[DPAL1:DPAL0]-bit	function	Note
00	Adaptive PAL Phase compensation is on	
01	PAL Phase compensation is on ON	
10	PAL Phase compensation is on OFF	
11	Reserved	

29. Digital Pixel Interpolator

In order to align Vertical Pixel positions, a Digital Pixel Interpolator is used in the AK8851. When the auto mode (default state) of the Pixel Interpolator is selected by [INTPOL1:INTPOL0]-bit of [Control 1 Register], ON/OFF control of the interpolator is automatically switched as follows which is linked with [CLKMODE1:CLKMODE0]-bit set.

Line-locked clock mode : OFF
Frame-locked clock mode : ON
Fixed clock mode : ON

[INTPOL1:INTPOL0]-bit	Pixel Interpolator
00	Auto
01	ON
10	OFF
11	Reserved

30. Status Information Function of Internal Operation

The AK8851 has [Status 1 Register] to show the internal status.
Bit Allocation of [Status 1 Register] is as follows.

Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVCOL	PKWHITE	CLKMODE1	CLKMODE0	COLKIL	FRMSTD	VLOCK	NOSIG

(1) No-Signal Input Detection

The AK8851 detects no-signal input conditions. When it is detected, the output data becomes Black level (Y = 0x10,Cb / Cr = 0x80).
The result is output via the NSIG output pin and [NOSIG]-bit of [Status 1 Register] is also set.
* Output state is shown below.

Status of Signal	[Status 1 Register][NOSIG]-bit	NSIG Pin
Detect Signal	0	0
NO Signal	1	1

(2) VLOCK Function

This bit indicates the synchronous state of input signal. The AK8851 synchronizes its internal operation with the input signal's Frame configuration.

For example, if the input signal Frame configuration consists of 524 lines, the chip internals operate in the 524-line configuration. This is called the VLOCK configuration.

When the input signal configured with 525-Lines per Frame is switched to 524 line signal system, the operation tracks to the switched signal system. In this case, VLOCK function is unlocked during the tracking time. This un-locked state is checked by [Status 1 Register].

When the input signal is switched, as when switching channels, it takes approximately 4 Frames until the VLOCK function is locked.

[VLOCK]-bit	Status of Synchronization	Note
0	Synchronized to Input video signal	
1	Unsynchronized to Input video signal	

(3) FRMSTD-bit :

This detects the input signal's Frame configuration. . When a non-standard Frame configuration is detected, this bit is set to "1".

[FRMSTD]-bit	Status of Frame Standard	Note
0	Frame Configuration is standard	
1	Frame Configuration is non standard	

(4) COLKIL-bit :

Indicates that the color killer function is active, since the color signal level is very low.

[COLKIL]-bit	Color killer	Note
0	Color killer is not work (Decoding normally)	
1	Color killer is working	

(5) Overflow Indication of Input Signal Level

The AK8851 has 2 types of overflow indicators," Luminance signal overflow indication " and " Chroma signal overflow indication " to indicate that the ADC input signal has exceeded its acceptable range on its way through the AGC (Automatic Gain Control) and ACC (Automatic Color Control) blocks.

[PKWHITE]-bit :

When Luminance signal overflow is detected, this bit is set to "1" which indicates that an overflow has occurred in the Luminance signal processing path.

[PKWHITE]-bit	Status of Signal	Note
0	Input signal is normal level	
1	Input signal is overflowed	

(6) REALFLD-bit :

This resides at [Status 2 Register]. It indicates if an EVEN or/ ODD Field is being decoded.

[REALFLD]-bit	real field status	Note
0	Field is EVEN field	
1	Field is ODD field	

[OVCOL]-bit :

This bit is set to "1" when a Chroma signal overflow is detected in the Chroma signal data path.

[OVCOL]-bit	Over color status	Note
0	Color signal is not overflowed	
1	Color signal is overflowed	

(footnote)

When an input overflow occurs, the following causes of overflow are likely.

It is assumed that input signal with following characteristics is applied when [PKWHITE]-bit or [OVCOL]-bit is set to "1" :

(a) Effective Video signal level is appropriate but SYNC-signal level is not large enough. In this case, the AGC adjusts the amplitude of the SYNC-signal level to be equal to 40-IRE / 300 mV. This pushes the effective Video signal level higher and causes an overflow to occur in the data processing block.

(b) Effective C-signal level is optimum but Color-Burst signal is not large enough. In this case, the AGC amplifies the Color-Burst signal to be equal to 40-IRE / 300 mV. This pushes the effective C-signal level higher and causes an overflow to occur in the data processing block.

31. Power Down Mode

The AK8851 has a Power-Saving mode. To put only the Analog functional blocks into this mode, set the input set bits [INSEL1:INSEL0]-bit to [1,1,1] of [AFE Control Register](R/W)[Sub Address 0x00]. In this case, Analog blocks such as Clamp, ADC1 and ADC2, including the PGAs, are switched to power saving mode. Since the digital blocks are in normal operation, correct timing outputs are available and are externally accessible.

When a Composite signal is input, CLAMP2 / PGA2 / ADC2 blocks are automatically switched to power saving mode.

The AK8851 /PD pin is used to place the entire chip into power saving mode, including all digital blocks.

By setting /PD pin to “low”, all analog and digital blocks are put into power saving mode, and output pins become “low”. To recover from the power saving mode using the /PD pin, a reset sequence must be executed.

32. Device Control Interface

The AK8851 operation is controlled via I2C bus control interface.

[I2C Bus SLAVE Address]

Either of 0x88 or 0x8A I2C Slave Address is selected by SELA pin.

SELA	SLAVE Address
PULL DOWN [LOW]	0x88
PULL UP [High]	0x8A

[I^2C Control Sequence]

(1) Write Sequence

After receiving a “write mode slave address” first byte, the AK8851 receives sub-address in the second byte and data in the third and successive bytes.

In write sequences, there is a single-byte write sequence and a continuous write sequence (sequential write operation).

(a) Single-byte Write Sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	

(b) Multiple-byte write sequence (sequential write operation)

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data(n+1)	A	.. .	Data(n+m)	A	stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit		8-bits	1-bit	

(2) Read Sequence

After receiving the “Slave address for read” first byte, the AK8851 sends data in the second and successive bytes.

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	. . .	Data n	Ā	stp
	8-bits		1	8-bits	1		8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	

S, rS : Start Condition
A : Acknowledge (SDA Low)
Ā: Not Acknowledged (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write

: Master device. Normally micro-processor

: Slave device: Slave device: AK8851

33.Register Definition

Sub Address	Register	Default	R/W	Function
0x00	AFE Control Register	0x00	R/W	Input video signal select / Clamp timing pulse adjustment
0x01	Input Video Select Register	0x00	R/W	Set the video standard
0x02	Output Format Register	0x00	R/W	Set the VBI parameter
0x03	Reserved Register	0x00	R/W	Reserved Register
0x04	Out Control Register	0x00	R/W	Fixed Output pin
0x05	Start and Delay Control Register	0x00	R/W	Set the output I/F configuration
0x06	AGC and ACC Control Register	0x00	R/W	Control register for AGC/ACC
0x07	Reserved Register	0x00	R/W	Reserved Register
0x08	Control 1 Register	0x00	R/W	Control 1 Register
0x09	Control 2 Register	0x00	R/W	Control 2 Register
0x0A	PGA1 Control Register	0x46	R/W	PGA1 Control Register
0x0B	PGA2 Control Register	0x46	R/W	PGA2 Control Register
0x0C	Pedestal Level Control Register	0x00	R/W	Pedestal Level Control Register
0x0D	Color Killer Control Register	0x08	R/W	Color killer control Register
0x0E	Contrast Control Register	0x80	R/W	Contrast Control Register
0x0F	Brightness Control Register	0x00	R/W	Brightness Control Register
0x10	Image Control Register	0x00	R/W	Image Control Register
0x11	Saturation Control Register	0x80	R/W	Saturation Control Register
0x12	HUE Control Register	0x00	R/W	HUE Control Register
0x13	High Data Set Register	0xEB	R/W	High Data Set Register
0x14	Low Data Set Register	0x10	R/W	Low Data Set Register
0x15	Request VBI Info Register	0x00	R/W	Request VBI Info Register
0x16	Status 1 Register		R	Status 1 Register
0x17	Status 2 Register		R	Status 2 Register
0x18	Macrovision Status Register		R	Macrovision Status Register
0x19	Input Video Status Register		R	Input Video Status Register
0x1A	Closed Caption 1 Register		R	Closed Caption 1 Register
0x1B	Closed Caption 2 Register		R	Closed Caption 2 Register
0x1C	WSS 1 Register		R	WSS 1 Register
0x1D	WSS 2 Register		R	WSS 2 Register
0x1E	Extended Data 1 Register		R	Extended Data 1 Register
0x1F	Extended Data 2 Register		R	Extended Data 2 Register
0x20	VBID 1 Register		R	VBID 1 Register
0x21	VBID 2 Register		R	VBID 2 Register
0x22	Device and Revision ID Register	0x33	R	Device and Revision ID Register

AFE Control Register (R/W) [Sub Address 0x00]

This sets the Analog Front End functions.
Input signal selection and analog clamp control related-tasks are set.
Generation Clamp pulse timing and its pulse width can be adjusted to control the clamp timing of SYNC-Tip clamping.

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPWIDTH1	CLPWIDTH0	CLPSTAT1	CLPSTAT0	EXTCLP	INSEL2	INSEL1	INSEL0
Default Value							
0	0	0	0	0	0	0	0

AFE Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	INSEL0 ~ INSEL2	Input Select	R/W	Set the video input port [VBIL2:VBIL0] = 000 : AIN1 (CVBS) 001 : AIN2 (CVBS) 010 : AIN3 (CVBS) 011 : AIN4 (CVBS) 101 : AIN2 Y (YC) AIN5 C 110: AIN3 Y (YC) AIN6 111: No Input When these bits are set 000/001/010/011, ADC2 enters power save mode. When these bits are set 111/100 Clamp/PGA/ADC enters power save mode.
bit 3	EXTCLP	External Clamp Pin Configuration	R/W	Attribution of EXTCLP pin 0: Output the internal clamp timing pulse. 1: Input external clamp timing pulse.
bit 4 ~ bit 5	CLPSTAT0 ~ CLPSTAT1	Clamp Slice Level bit	R/W	Set the start of clamp timing pulse. See. [10.CLAMP] [CLPSTAT1:CLPSTAT0]-bit 00 : Center of Sync signal 01: 1/128H(496nsec) Delay from center of Sync signal. 10: 1/128H(496nsec) before from center of Sync signal 11 : 2/128H (1usec) before from center of Sync signal
bit 6 ~ bit 7	CLPWIDTH0 ~ CLPWIDTH1	Clamp Pulse Width	R/W	Set the width of Clamp timing pulse CLPWIDTH1: CLPWIDTH0 00 : 275nsec 01 : 555nsec 10 : 1.1usec 11 : 2.2usec

Input Video Standard Register (R/W) [Sub Address 0x01]

Register to set various input signal characteristics

Sub Address 0x01 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	B/W	VLF	VCEN1	VCEN0	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCF0 ~ VSCF1	Subcarrier Frequency	R/W	Set Sub-Carrier frequency of the input video signal VSCF1 - VSCF0 [MHz] 00 : 3.57954545 01 : 3.57561188 10 : 3.5820558 11 : 4.43361875
bit 2 ~ bit 3	VCEN0 ~ VCEN1	Video Color Encode	R/W	Set the color encode type for the input video signal 00 : NTSC 01 : PAL 10 : SECAM 11 : Reserved
bit 4	VLF	Video Line Frequency	R/W	Set the number of Line of the input video signal 0 : 525 Lines System 1 : 625 Lines System
bit 5	B/W	Black and White bit	R/W	Set the Black and White mode 0 : Color mode 1 : Black and White mode
bit 6	SETUP	Setup	R/W	Setup (7.5%) process. 0 : without SETUP signal 1 : with SETUP signal
bit 7	AUTODET	Video Standard Auto Detect	R/W	Autodetection of the input video signal 0 : OFF (AK8851 does not auto detect.) 1 : ON (AK8851 auto detects)

Output Format Register (R/W) [Sub Address 0x02]

Register to set the format of output data. The following contents are pre-settable

* Vertical Blanking Interval
* Upper / Lower limits of 601 data
* handling of output if ITU-R BT.656 output is not available
* V-bit set of EAV / SAV
* task-handling during VBI interval

Sub Address 0x02 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

Output Format Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	VBIL0 ~ VBIL2	Vertical Blanking Length	R/W	Set the Vertical Blanking Interval Default setting is 525-system : Line1~19/Line263.5~282.5 625-system : Line623.5~22/Line311~335.5 This register sets the difference to the default value. See "21. Vertical Blanking Interval" VBIL2:VBIL0] = 000 : default 001 : VBI interval becomes 1line longer 010 : VBI interval becomes 2lines longer 011 : VBI interval becomes 3lines longer 111 : VBI interval becomes 1line shorter 110 : VBI interval becomes 2lines shorter 101 : VBI interval becomes 3lines shorter 100 : VBI interval becomes 4lines shorter
bit 3	601LIMIT	601 Output Limit	R/W	This bit specifies Min. and Max. values of output data. 0 : 1-254 (Y/Cb/Cr) 1 : 16-235 (Y) / 16-240 (Cb/Cr)
bit 4	TRSVSEL	Time Reference Signal V Select bit	R/W	TRSVSEL-bit is a control bit to specify handling of V-bit in Rec.656 EAV/SAV code. NTSC (525) TRSVSEL=0 : Line1~Line9/Line264~Line272 V-bit=1 Line10~Line263/Line272~Line525V-bit=0 TRSVSEL=1: Line1~Line19/Line264~Line282 V-bit=1 Line20~Line263/Line283~Line525 V-bit=0 PAL(625System) Always Line1~Line22/Line311~Line335/Line624~Line625 V-bit =1 Line23~Line310/Line336~Line623 V-bit=0
bit 5	SLLVL	Slice Level	R/W	Set the sliced level 0 : Slice level is 25 IRE 1 : Slice level is 50 IRE
bit 6 ~ bit 7	VBIDEC0 ~ VIBDEC1	VBI Decode	R/W	Output data between VBI intervals. VBIDEC1:VBIDEC0 00 : Black level data is output 01 : Black and White data is output 10 : Sliced result is output 11 : Reserved

Reserved Register (R/W) [Sub Address 0x03]

Reserved Register

Sub Address 0x03 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Out Control Register (R/W) [Sub Address 0x04]

Register to fix the output pin status.

Sub Address 0x04 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	HLFCKL	NL	SL	FL	DL
Default Value							
0	0	0	0	0	0	0	0

Start and Delay Control Register Definition

BIT	Register Name		R/W	Definition
bit 0	DL	Doutput Low bit	R/W	0 : 1 : [D0:D7] / DVALID is always “Low”
bit 1	FL	FIELD Low bit	R/W	0 : 1 : Field is always “Low”
bit 2	SL	Sync Low bit	R/W	0 : 1 : HSYNC/VSYNC/CSYNC are always “Low”
bit 3	NL	NSIG Low bit	R/W	0 : 1 : NSIG always “Low”
bit 4	HLFCKL	HALFCK Low bit		0 : 1 : HALFCKO is always “Low”
bit 5 ~ bit 7	Reserved	Reserved bit	R/W	Reserved bit

Start and Delay Control Register (R/W) [Sub Address 0x05]

Register to set the output data

Sub Address 0x05 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	ACTSTAT2	ACTSTAT1	ACTSTAT0	HALFCKP	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

Start and Delay Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	YCDELAY0 ~ YCDELAY2	Y/C Delay Control	R/W	Y/C delay setting for output data. One delay time is 74nsec(1clock@13.5MHz) Set the value with 2's complement [YCDELAY2-YCDELAY0]= 101 : Y-data is 3clocks delay against C-data 110 : Y-data is 2clocks delay against C-data 111 : Y-data is 1clock delay against C-data 000 : No delay [Default] 001 : C-data is 1clock delay against Y-data 010 : C-data is 2clocks delay against Y-data 011 : C-data is 3clocks delay against Y-data
bit 3	HALFCKP	HALFCKO Polarity bit	R/W	Set the polarity of HALFCKO. 0 : 1 : Invert
bit 4 ~ bit 6	ACTSTA0 ~ ACTSTA2	Active Video Start Control bit	R/W	Set fine adjustment of Start position of decoded video data. Set the value with 2's complement [ACTSTA2:ACTSTA0]= 101 : Decoding the video data 3pixels earlier. 110 : Decoding the video data 2pixels earlier. 111 : Decoding the video data 1pixel earlier. 000 : Normal position [Default] 001 : Decoding the video data 1pixel delayed. 010 : Decoding the video data 2pixels delayed. 011 : Decoding the video data 3pixels delayed.
bit 7	Reserved	Reserved	R/W	Reserved

AGC and ACC Control Register (R/W) [Sub Address 0x06]

Register to set the AGC and ACC characteristics.

Sub Address 0x06 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACCFRZ	ACC1	ACC0	AGCFRZ	Reserved	AGCC0	AGCT1	AGCT0
Default Value							
0	0	0	0	0	0	0	0

AGC and ACC Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	AGCT0 ~ AGCT1	AGC Time Constance	R/W	Set the AGC time constants. When AGC is set to Disable, each PGA can be set manually. [AGCT1:AGCT0] = 00 : Disable [default] 01 : Fast [T = 1Field] 10 : Middle [T = 7Field] 11 : Slow [T = 29Field] (T : Time constants)
bit 2	AGCC	AGC Coring Control	R/W	Set the non-sensing bandwidth of AGC AGCC 0 : +/-2bits 1 : +/-3bits
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	AGCFRZ	AGC Freeze	R/W	AGC Freeze bit 0 : AGC is functioned 1 : AGC is frozen
bit 5 ~ bit 6	ACC0 ~ ACC1	Auto Color Control bit	R/W	Setting the ACCf function [ACC1:ACC0] = 00 : Disable ACC [Default] 01 : Fast [T = 2-Field] 10 : Middle [T = 8-Field] 11 : Slow [T = 30-Field] (T : Time constants)
bit 7	ACCFRZ	ACC Freeze	R/W	ACC Frozen bit 0 : ACC is functioned 1 : ACC is frozen.

Reserved Register (R/W) [Sub Address 0x07]

Reserved

Sub Address 0x07 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register (R/W) [Sub Address 0x08]

Control register to set various functions as shown in the table below.

Sub Address 0x08 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	16BITOUT	UVFILSEL	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	YCSEP0 ~ YCSEP1	YC Separation Control	R/W	YC Separation setting YCSEP1:YCSEP 00 : Adaptive YC Separation mode 01 : 1-Dim YC Separation mode 10 : 2-Dim YC Separation mode 11 : Reserved
bit 2	UVFILSEL	UV Filter Selection	R/W	UV Filter selection 0 : Wide 1 : Narrow
bit 3	16BITOUT	16-bit Output mode	R/W	16-bit output mode setting 0 : 8-bit output mode(656 standard) 1 : 16-bit output mode
bit 4 ~ bit 5	INTPOL0 ~ INTPOL1	Interpolator On/Off bit	R/W	Setting for Pixel Interpolator [INTPOL1:INTPOL0]-bit 00 : Auto [Default] 01 : ON 10 : OFF 11 : Reserved
bit 6 ~ bit 7	CLKMODE0 ~ CLKMODE1	Clock Mode Set bit	R/W	Setting of Clock mode [CLKMODE1:CLKMODE0] = 00 : Clock Mode Auto Select mode 01 : Line-Lock Clock mode 10 : Frame-Lock Clock mode 11 : Fixed Clock mode

Control 2 Register (R/W) [Sub Address 0x09]

Control register to set various functions as shown in the table below.

Sub Address 0x09 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	STUPATOFF	ERRHND1	ERRHND0	Reserved	BLUEBACK	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

Control 2 Register Definitions

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	DPAL0 ~ DPAL1	Deluxe PAL	R/W	Phase Compensation mode. This procedure is also valid at NTSC mode. [DPAL1:DPAL0]-bit 00 : Adaptive ON 01 : ON 10 : OFF 11 : Reserved
bit 2	BLUEBACK	Blue Back output	R/W	Output data at the No-signal Input 0 : Black data out 1 : Blue back data out
bit 3	Reserved	Reserved bit	R/W	Reserved
bit 4 ~ bit 5	ERRHND0 ~ ERRHND1	656 Error Handling bit	R/W	Sets the data handling procedure when AK8850 cannot output the data follow to ITU-R. Bt.656. Error handling is normally handled on the last lines of the Frame. 00 : Line Drop/Repeat 01 : Number of Samples of the Last line of the field is change. 10 : Number of Samples of the Last line of the frame is change.11 : Reserved 11 : Reserved
bit 6	STUPATOFF	Setup Auto Control Off	R/W	Setup Process at the auto signal detection See. Autodetection 0 : Automatic Setup procedure is done 1 : Automatic Setup procedure is not done
bit 7	Reserved	Reserved bit	R/W	Reserved

PGA1 Control Register (R/W) [Sub Address 0x0A]

Set PGA1

Sub Address 0x0A **Default Value : 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA1_6	PGA1_5	PGA1_4	PGA1_3	PGA1_2	PGA1_1	PGA1_0
Default Value							
0	1	0	0	0	1	1	0

PGA1 Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 6	PGA1_0 ~ PGA1_6	PGA1 Gain Set	R/W	Set the gain of PGA1 Gain step of PGA is about 0.1dB
bit 7	Reserved	Reserved	R/W	Reserved

PGA2 Control Register (R/W) [Sub Address 0x0B]

Set PGA2

Sub Address 0x0B **Default Value : 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA2_6	PGA2_5	PGA2_4	PGA2_3	PGA2_2	PGA2_1	PGA2_0
Default Value							
0	1	0	0	0	1	1	0

PGA2 Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 6	PGA2_0 ~ PGA2_6	PGA2 Gain Set	R/W	Set the gain of PGA2 Gain step of PGA is about 0.1dB
bit 7	Reserved	Reserved	R/W	Reserved

Pedestal Level Control Register (R/W) [Sub Address 0x0C]

Fine adjustment of Pedestal Level

Sub Address 0x0C **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DPCC1	DPCC0	DPCT1	DPCT0	BKLVL3	BKLVL2	BKLVL1	BKLVL0
Default Value							
0	0	0	0	0	0	0	0

Black Level Adjust Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	BKLVL0 ~ BKLVL3	Black Level	R/W	See “13.SYNC Separation/SYNC Detection/Phase-Error Detection/Black Level Fine Tuning” [BKLVL3:BKLVL0]-bit 0111 Add 7 code to black Level 0110 Add 6 code to black Level 0101 Add 5 code to black Level 0100 Add 4 code to black Level 0011 Add 3 code to black Level 0010 Add 2 code to black Level 0001 Add 1 code to black Level 0000 Default 1111 Subtract 1 code from black level 1110 Subtract 2 code from black level 1101 Subtract 3 code from black level 1100 Subtract 4 code from black level 1011 Subtract 5 code from black level 1010 Subtract 6 code from black level 1001 Subtract 7 code from black level 1000 Subtract 8 code from black level
bit 4 ~ bit 5	DPCT0 ~ DPCT1	Digital Pedestal Clamp Control	R/W	Setting of Time constants of the digital pedestal clamp. DPCT1:DPCT0 00 : Fast 01 : Middle 10 : Slow 11 : Disable
bit 6 ~ bit 7	DPCC0 ~ DPCC1	Digital Pedestal Clamp Coring Control bit	R/W	Setting the non-sensing bandwidth of digital pedestal clamp. DPCC1:DPCC0 00 : 1bit 01 : 2bits 10 : 3bits 11 : No non-sensing bandwidth [Default]

Color Killer Control Register (R/W) [Sub Address 0x0D]

Setting the color killer function

Sub Address 0x0D **Default Value : 0x08**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COLKILL	Reserved	CKSCM1	CKSCM0	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
0	0	0	0	1	0	0	0

Color Killer Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	CKLVL0 ~ CKLVL3	Color Killer Level Control	R/W	Set the color killer level
bit 4 ~ bit 5	CKSCM0 ~ CKSCM1	Color Killer Level for SECAM	R/W	Set the color killer level at SECAM decode mode.
bit 7	COLKILL	Color Killer Enable	R/W	Color killer on/off control bit 0 : Enable 1 : Disable

Contrast Control Register (R/W) [Sub Address 0x0E]

Register to set Contrast adjustment.
Default value (0x80) corresponds to un-adjusted condition.

Sub Address 0x0E **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CONT0 ~ CONT7	Contrast Control	R/W	Contrast adjustment range is 0 to 2 by 1/256 steps.

Brightness Control Register (R/W) [Sub Address 0x0F]

Register to set Brightness adjustment.
Default value (0x00) corresponds to un-adjusted condition.

Sub Address 0x0F **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	BR0 ~ BR7	Brightness Control	R/W	Brightness level is defined following formula Setting is done with 2's Complement value.

Image Control Register (R/W) [Sub Address 0x10]

Register to control sharpness of image.

For sharpness and softness filter characteristics and Luminance band-limiting filter characteristics, please refer to the corresponding sections of this data sheet.

Sub Address 0x10 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIIMGCTL	SEPIA	LUMFIL1	LUMFIL0	SHCORE1	SHCORE0	SHARP1	SHARP0
Default Value							
0	0	0	0	0	0	0	0

Image Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	SHARP0 ~ SHARP1	Sharpness Control	R/W	Sharpness control bits [SHARP1SHARP0]-bit 00 : No sharpness filter 01 : Sharpness effect is min. 10 : Sharpness effect is middle 11 : Sharpness effect is max.
bit 2 ~ bit 3	SHCORE0 ~ SHCORE1	Sharpness Coring	R/W	Coring level of Sharpness filter is set with these bit [SHCORE1:SHCORE0]-bit 00 : No Coring 01 : +/- 1LSB 10 : +/- 2LSB 11 : +/- 3LSB
bit 4 ~ bit 5	LUMFIL0 ~ LUMFIL1	Luminance Filter	R/W	Luminance limiting bandwidth [LUMFIL1:LUMFIL0]-bit 00 : No limitation for Luminance bandwidth 01 : narrow 10 : mid. 11 : wide
bit 6	SEPIA	Sepia output	R/W	Sepia Output 0 : 1 : Sepia output on
bit 7	VBIIMGCTL	VBI Image Control	R/W	On/Off control bit for Brightness and Contrast adjustment inside the VBI interval. 0 : Brightness and Contrast adjustment is invalid inside VBI interval. 1 : Brightness and Contrast adjustment is invalid inside VBI interval

Saturation Control Register (R/W) [Sub Address 0x11]

This adjusts the color saturation level. The default value of 0x80 corresponds to the un-adjusted value.

Sub Address 0x11 **Default Value : 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

Saturation Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SAT0 ~ SAT7	Saturation Control	R/W	Saturation adjustment range is 0 to 2 by 1/256 steps. It corresponds to the range between -∞ to 6dB. SAT7:SAT0 0 : -∞ 0xff : 255/128

HUE Control Register (R/W) [Sub Address 0x12]

Register to adjust the color Hue level. The default value of 0x00 corresponds to the un-adjusted value

Sub Address 0x12 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HUE0 ~ HUE7	HUE Control	R/W	The range of Hue adjustment can be set form -45deg. to 45deg. by 1/256 Step Set with 2's complement value.

High Data Set Register (R/W) [Sub Address 0x13]

Register to set “HIGH” level of binary-coded data that is sliced by the VBI Slicer.
The default value is equal to 100 % White level (235).

Sub Address 0x13 **Default Value : 0xEB**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0
Default Value							
1	1	1	0	1	0	1	1

High Data Set Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	H_0 ~ H_7	High Data 0~7 Set bit	R/W	It is necessary to be careful to set 0x00 and 0xFF. These values are the special codes for Rec.601.

Low Data Set Register (R/W) [Sub Address 0x14]

Register to set “LOW” level of binary-coded data that is sliced by the VBI Slicer. The default value is equal to Pedestal level (16).

Sub Address 0x14 **Default Value : 0x10**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L_7	L_6	L_5	L_4	L_3	L_2	L_1	L_0
Default Value							
0	0	0	1	0	0	0	0

Low Data Set Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	L_0 ~ L_7	Low Data 0~7 Set bit	R/W	It is necessary to be careful to set 0x00 and 0xFF. These values are the special codes for Rec.601.

Request VBI Info Register (R/W) [Sub Address 0x15]

This Register requests VBLANK decode information such as Closed Caption data/Extended data/ VBID (CGMS)/WSS data. When “1” is written into each decode request bit of VBLANK information register, the AK8851 is put into a Data-Decode-Ready state and waits for data. When the decoding of data is completed, ”1” is written into each bit of Status Register2 and the decoded data are stored in the following registers respectively.

* Closed Caption Data 1 and2 Registers
* Extended Data 1 and 2 Registers
* VBID Data 1 and 2 Registers
* WSS Data 1 and 2 Registers

Sub Address 0x15 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Info Register Definition

BIT	Register Name		R/W	Definition
bit 0	CCRQ	Closed Caption Decode Request	R/W	Decode request for Closed Caption Data 0 : 1 : Request to decode
bit 1	EXTRQ	Extended Data Decode Request	R/W	Decode request for Extended Data0 : 0 : 1 : Request to decode
bit 2	VBIDRQ	VBID Data Decode Request	R/W	Decode request for VBID Data 0 : 1 : Request to decode
bit 3	WSSRQ	WSS Data Decode Request	R/W	Decode request for WSS Data 0 : 1 : Request to decode
bit 4 ~ bit 5	Reserved	Reserved	R/W	Reserved

Status 1 Register (R/W) [Sub Address 0x16]

Status 1 Register (R/W)[Sub Address 0x16]

This is to show the internal state of the AK8851.

Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVCOL	PKWHITE	SCLKMODE1	SCLKMODE0	COLKIL	FRMSTD	VLOCK	NOSIG

Status 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0	NOSIG	No Signal	R	No signal indicator This data also output from NSIG pin. 0 : Signal is input 1 : No signal is input
bit 1	VLOCK	Video Locked	R	Shows the synchronization state of the input signal. 0 : Unsynchronized to the input signal. 1 : Synchronized to the input signal.
bit 2	FRMSTD	Frame Standard	R	Shows the synchronization state of the input signal. 0 : Unsynchronized to the input signal. 1 : Synchronized to the input signal.
bit 3	COLKILON	Color killer	R	Shows the Color Killer Status 0 : Color Killer is not active 1 : Color Killer is active
bit 4 ~ bit 5	SCLKMODE0 ~ SCLKMODE1	Clock Mode[1:0]-bit	R	Shows the clock-mode. [CLKMODE1:CLKMODE0] = 00 : Working with Fixed clock mode. 01 : Working with Line-Locked Clock mode 10 : Working with Frame-Locked Clock mode 11 : Reserved
bit 6	PKWHITE	Peak White Detection	R	0 : 1 : Input video signal has overflowed
bit 7	OVCOL	Over Color Level	R	0 : 1 : Input Color signal has overflowed

Status 2 Register (R/W) [Sub Address 0x17]

This is to show the internal state of the AK8851

Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	REALFLD	WSSDET	VBIDDET	EXTDET	CCDET

Status2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	CCDET	Closed Caption Detect	R	Closed Caption Data detect bit 0 : Closed Caption is not detected. 1 : Closed Caption is found.
bit 1	EXTDET	Extended Data Detect	R	Extended Data detect bit 0 : Extended data is not detected. 1 : Extended data is found.
bit 2	VBIDDET	VBID Data Detect	R	VBID data detect bit 0 : VBID data is not detected. 1 : VBID data is found.
bit 3	WSSDET	WSS Data Detect	R	WSS Data detect bit. 0 : WSS data is not detected. 1 : WSS data is found. 1 : WSS Data is found
bit 4	REALFLD	Real Filed	R	Showing the Field status 0 : EVEN Field 1 : ODD Field
bit 5	Reserved	Reserved	R	Reserved
bit 6 ~ bit 7	Reserved	Reserved	R	Reserved

Macrovision Status Register (R/W) [Sub Address 0x18]

This register detects Macrovision data.

Sub Address 0x18

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	CSTYPE	CSDET	AGCDET

Macrovision Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	AGCDET	AGC Process Detect	R	The result of AGC Process of Macrovision detection 0 : No AGC Process is measured 1 : AGC Process is measured
bit 1	CSDET	Color Stripe Detect	R	The result of Color stripe Process of Macrovision detection 0 : No Color Stripe process is measured 1 : Color Stripe Process is measured
bit 2	CSTYPE	Color Stripe Type	R	Type of Color stripe is indicate on this bit 0 : Color Stripe Type2 1 : Color Stripe Type3 * this bit is valid when CSDET-bit is 1
bit 3 ~ bit 7	Reserved	Reserved	R	Reserved

Input Video Status Register (R) [Sub Address 0x19]

This shows a result of automatic input signal distinguishing function.

Sub Address 0x19 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Fixed	Undef	ST_B/W	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VSCF0

Input Video Status Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	ST_VSCF0 ~ ST_VSCF1	Status of Video Sub Carrier Freq	R	Sub-Carrier frequency of the input video signal [ST_VSCF1:STVSCF0]-bit 00 : 3.57954545 MHz 01 : 3.57561188 MHz 10 : 3.5820558 MHz 11 : 4.43361875 MHz
bit 2 ~ bit 3	ST_VCEN0 ~ ST_VCEN1	Status of Video Color Encode	R/W	Color Encode type of the input video signal [VCEN1:VCEN0]-bit 00 : NTSC 01 : PAL 10 : SECAM 11 : Reserved
bit 4	ST_VLF	Status of Video Line Frequency	R/W	Number of Lines of the input video signal 0 : 525 1 : 625
bit 5	ST_B/W	Status of B/W Signal	R	Black and White detection 0 : Color signal 1 : Black and White signal
bit 6	UNDEF	Undefined bit	R	Recognition status 0 : Under recognition (Recognition is done) 1 : Unable to recognize the input video signal
bit 7	FIXED	Input Video Standard fixed bit	R	Recognition status 0 : Under recognition 1 : Recognition is finished

Closed Caption 1 Register (R) [Sub Address 0x1A]

Register to store the Closed Caption data.

Sub Address 0x1A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register (R) [Sub Address 0x1B]

Register to store the Closed Caption data.

Sub Address 0x1B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

WSS 1 Register (R) [Sub Address 0x1C]

Register to store the WSS data.

Sub Address 0x1C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

WSS 2 Register (R) [Sub Address 0x1D]

Register to store the WSS data.

Sub Address 0x1D

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

Extended Data 1 Register (R) [Sub Address 0x1E]

Register to store the Closed Caption extended data.

Sub Address 0x1E

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register (R) [Sub Address 0x1F]

Register to store the Closed Caption extended data.

Sub Address 0x1F

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

VBID 1 Register (R) [Sub Address 0x20]

Register to store the VBID data.

Sub Address 0x20

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

VBID 2 Register (R) [Sub Address 0x21]

Register to store the VBID data.

Sub Address 0x21

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

Device and Revision ID Register (R) [Sub Address 0x22]

Register to indicate the device ID and revision number of the AK8851.
The device ID of the AK8851 is 51 in decimal format.
Revision number is renewed only when the control software is modified.

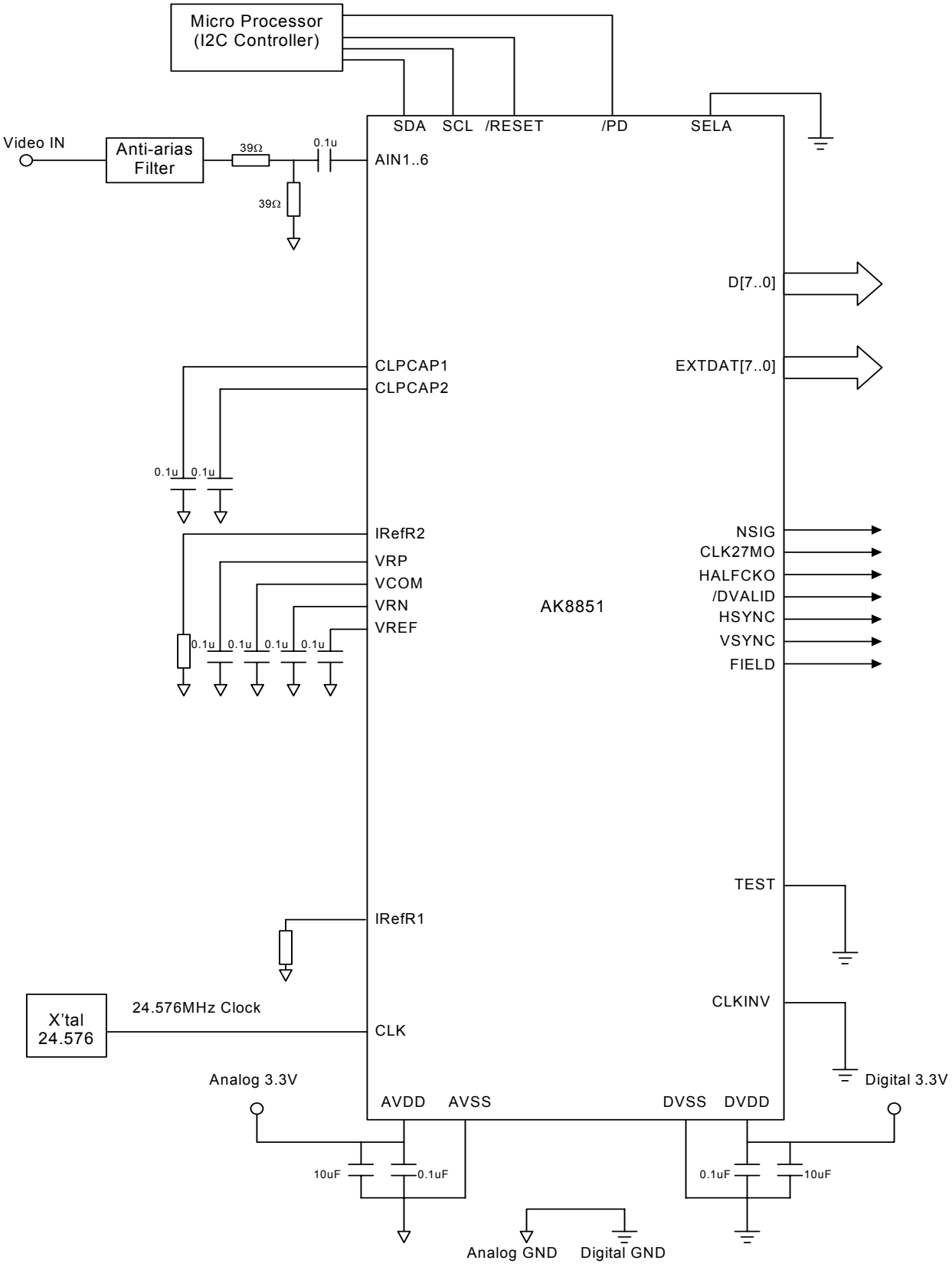
Sub Address 0x22 **Default Value 0x33**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1	REV0	DID5	DID4	DID3	DID2	DID1	DID0
0	0	1	1	0	0	1	1

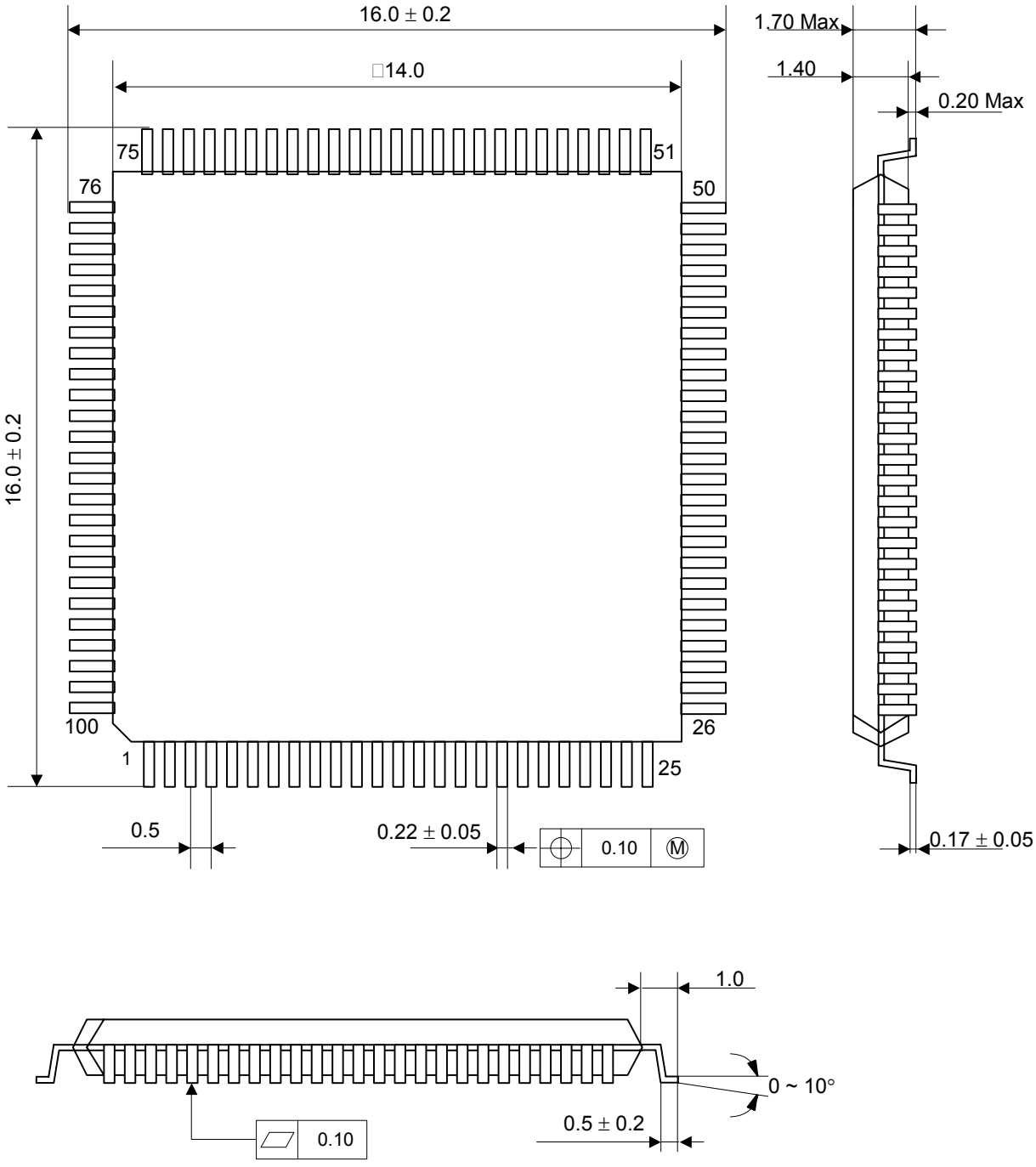
Revision Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DID0 ~ DID5	Device ID	R	Indicates Device ID Device ID is 51(Decimal)(0x33)
bit 6 ~ bit 7	REV0 ~ REV1	Revision	R	Revision information is indicated REV1 - REV0 Revision ID is 0x00

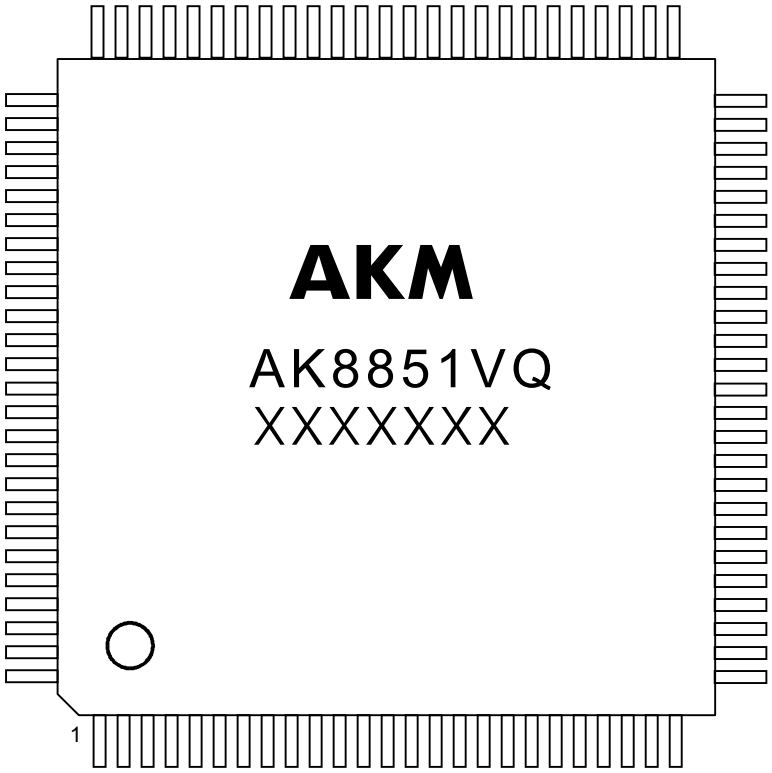
34. System connection



35 Package



36 Marking



1) AKM : AKM Logo

2) AK8851VQ : Marketing Code

3) XXXXXXX (7digits) : Date Code

4) O : Pin #1 indication

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