AKD5393
Evaluation board Rev.A for AK5393

General description

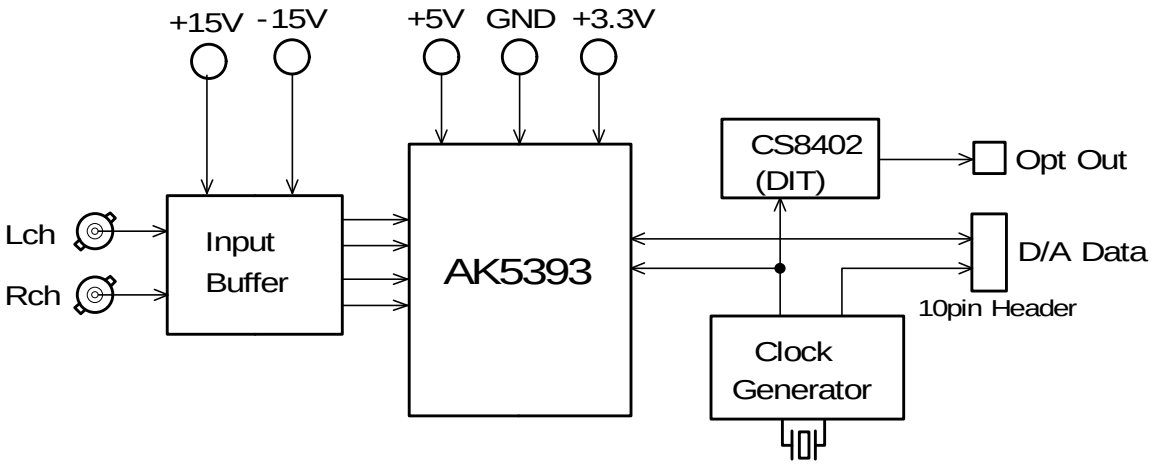
The AKD5393 is an evaluation board for the AK5393 professional audio 24bit A/D converter. The AKD5393 includes the input buffer circuit and also has a digital interface transmitter. Further, the AKD5393 can evaluate direct interface with AKM's DAC evaluation boards.

■ Ordering guide

AKD5393 Rev.A --- Evaluation board for AK5393VS

Function

- On-board Full-differential input buffer circuit
- On-board clock generator
- Compatible with 2 types of interface
  1) Direct interface with AKM's DAC evaluation boards.
  2) On-board CS8402 as DIT which transmits optical output.
- A BNC connector for an external clock input.



* Circuit diagram and PCB layout are attached at the end of this manual.

■ Input buffer circuit

The AKD5393 includes full-differential input buffer circuit with an inverted-amp (gain: -10dB). The capacitor of 10nF between AIN+ /- decreases the clock feed through noise of modulator, and composes a 1st order LPF (fc=360kHz) with 22ohm resistor before the capacitor. This circuit also has a 1st order LPF (fc=370kHz) composed of op-amp. External analog signal can be fed through the BNC connector or the Cannon connector.

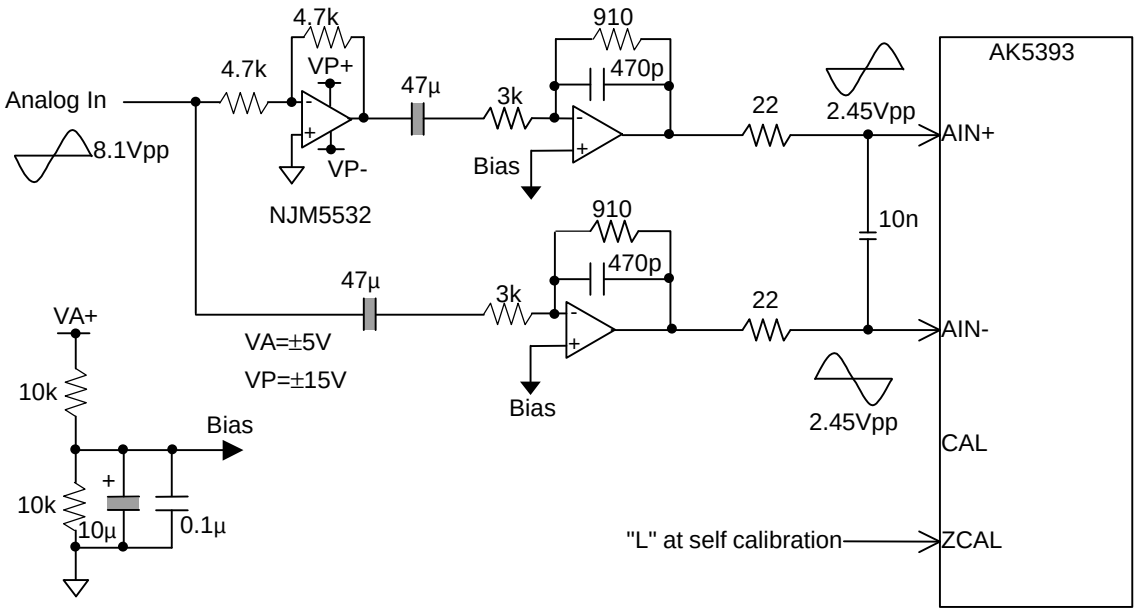


Figure 1. Full-differential input buffer circuit example

1: In case of using the BNC connector

[JP2, JP3, JP4, JP5]: Short
[R11, R18]: Open
The resistor value of R10 and R19 should be properly selected in order to much the output impedance of the signal source.

2: In case of using the Cannon connector

[JP2, JP3, JP4, JP5]: Open
The resistor value of R10, R11, R18 and R19 should be properly selected in order to much the output impedance of the signal source.

* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Power supply and Decoupling

VA and VD supplies to the AK5393 are decoupled separately in order to minimize the effect of the digital noise. A system analog supply is fed to VA. VA and VD lines should be distributed separately from the power unit.
Decoupling capacitors are connected to AK5393 as near as possible, particularly the ceramic capacitor to the VREFL/R pin.

■ Operation sequence

(1) Set up the power supply lines
VP+=+15V, VP- = -15V, VA+=+5V, VD+=+3.3V~5.25V, AGND=DGND=0V
Each supply line should be distributed from the power unit.

(2) Set up the evaluation modes and jumper pins. (See next item)
There are many jumper pins to cover many evaluation modes.
Please take care of setting.

(3) Set up the DIP SW position for the DIT. (See next item)
This does not affect AK5393 operation.

(4) Power On.
The AK5393 should be reset once by bringing PD "L"(SW4) upon power-up.

(5) AK5393 can be reset by SW4 during operation.
Lower position resets the device, and the upper position is for normal operation.

Note: In any case of changing clocks during operation, the device should be reset by bringing PD "L". If not followed, the AK5393 may be destroyed since its internal logic uses dynamic circuit.

■ The evaluation modes and corresponding jumper pin settings.

1. Evaluation Mode

Applicable Evaluation Mode

1-1 Using D/A converter board for the analog performance analysis.
1-2 DIT (Optical Link) [Default]
1-3 All interface signals (MCLK, BICK and LRCK) are fed from external circuit.
1-4 Feed all interface signals to the external circuit through PORT2.

1-1. Using D/A converter board for the analog performance analysis.

The AK5393 can be evaluated by distortion analyzer using various AKM's D/A converter evaluation boards through PORT2.

[Slave mode]

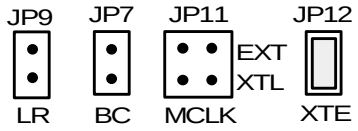
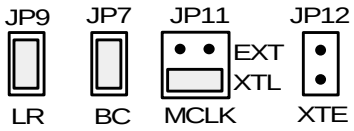


Figure 2. Jumper set up (D/A)

1-2DIT (Optical Link)

PORT1 is used. DIT generates audio Bi-phase signal from received data and which is output through optical connector (TOTX174). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. There are two kinds of jumper setting depend on the SMODE1 and SMODE2 pin. The interface signals are output from PORT2. (See the (4)). In case of using external clock through a BNC connector, select EXT on JP11 (MCLK) and short JP12 (XTE).

[Slave mode] (Default)



[Master mode]

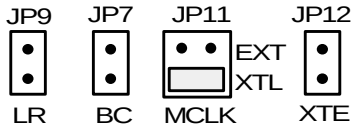


Figure 3. Jumper set up (DIT)

1-3 All interface signals (MCLK, BICK and LRCK) are fed from external circuit. [Slave mode]

Under the following setup, MCLK, LRCK and SCLK signals needed for the A/D to operate could be Fed through PORT2.

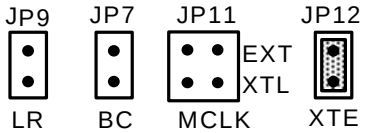
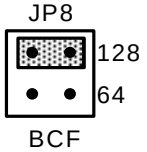


Figure 4. Jumper set up (EXT)

1-4 Feed all interface signals to the external circuit through PORT2. [Master, Slave mode]
Please set up as same as 1-2. All interfacing signal which drive AK5393 are output through PORT2. However, the FSYNC signal is input when the position of the SDATA is needed to be controlled.

* Setting for double speed sampling (fs=96kHz)
For the double speed sampling, DFS="L", MCLK=128fs, BICK=64fs(max) are required.
So, when BICK and LRCK are created from 74HC4040 on the board, the crystal oscillator should be changed to 24.576MHz and set JP14 (MCLK2) to 128fs side (see the schematics).

2. BIT CLK (BCF) set up



[JP8] Either 64fs or 128fs for the BCF can be selected. Figure shows 128fs example.
When DFS="H", set JP8 to 64 side.
128: 128fs is fed to AK5393 as BICK.
64: 64fs is fed to AK5393 as BICK.

3. Jumper-set up and explanation

Set up the CS8402's data format corresponding the serial data interface of the AK5393.

AKD5393 Data Format	SMODE2 (SW2-5)	SMODE1 (SW2-4)	8402 (SW2-1)	BCF (JP6)	LRP (JP10)
Slave mode	ON	ON	ON	F	H
Mater mode	ON	OFF	OFF	R	L
I^2S Slave mode	OFF	ON	OFF	R	H
I^2S master mode	OFF	OFF	OFF	R	H

*DIP-SW is ON="L" OFF="H"

Table 1. Serial data interface of AK5393 and CS8402

[SW2-1]: CS8402's data format
ON: MSB justified, 24bit
OFF: IIS Compatible

[JP6]: Define the polarity of SCLK.
F: SCLK is inverted.
R: SCLK coincides with AK5393

[JP10]: Define the polarity of LRCK.
L: LRCK is inverted.
H: LRCK coincides with AK5393.

4. The other function set up

No.	PIN	ON	OFF
1	8402	See the Table1.	
2	DFS	48k	96k
3	HPFE	disable	enable
4	SM1	Seethe Table 1.	
5	SM2		
6	CALMODE	VCOM	AIN

*DIP-SW is ON="L" OFF="H"

→Selects the sampling rate.
→Selects HPF of AK5393.
→Selects the reference signal for Offset-Cal of K5383

Table 2. DIP-SW2 set-up

VCOM:VCOML,VCOMR pin
AIN: Analog input pin (AINL±, AINR±)

[JP13]: Selects the analog power supply source to VA pin of the AK5393.
Open: Supply from the power supply terminal (VA+).
Short: Supply from 3-terminal-voltage regulator (+5V) on the board.

■ The function of the toggle SW.

[SW3] Resets the CS8402. Upper position resets the internal counter of CS8402, then Bi-phase signal is not output. Keep the "L" position during normal operation.

[SW4] Resets the AK5393. Keep the "H" position during conversion.

■ DIP switch set up. (Default is the consumer mode.).

The DIP-SW1 sets the C-bit of CS8402. This set up does not affect the evaluation of the AK5383. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 datasheet.

Switch	OFF=0,ON=1	Contents
8	$\overline{\text{PRO}}$ = 0	Professional mode, C0=1
7,6	$\overline{\text{C6}}$, $\overline{\text{C7}}$	C6,C7 - Sampling frequency
	11	00 - Not indicated. Receiver default to 48kHz.
	10	01 - 48kHz
	01	10 - 44.1kHz
	00	11 - 32kHz
5	$\overline{\text{C9}}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to 2-channel mode.
	0	0100 - Stereophonic.
4	$\overline{\text{C1}}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Not audio
3	TRNPT	Transparent mode *CS8402 is CRE
	0	Normal mode
	1	Transparent mode
1,2	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no emphasis with manual override enable.
	1 0	100 - None
	0 1	110 - 50/15usec
	0 0	111 - CCITT J.17

Table 3. DIP switch set up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
8	$\overline{\text{PRO}}$ = 0	Consumer mode, C0=0 (Default)
7	$\overline{\text{C2}}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
6	$\overline{\text{C3}}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
5	$\overline{\text{C15}}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
3,4	FC1, FC0	C24,C25,C26,C27- Sampling frequency
	00	0000 - 44.1kHz
Default	01	0100 - 48kHz
	10	1100 - 32kHz
	11	0000 - 44.1kHz, CD mode
1,2	$\overline{\text{C8}}$, $\overline{\text{C9}}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 4. DIP switch set up of CS8402 (Consumer mode)

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AK5393 Measurement Result

[Measurement condition]

- Measurement unit : ROHDE & SCHWARZ, UPD04
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz (fs=48kHz), 40Hz~40kHz (fs=96kHz)
- Power Supply : AVDD=3.3V, DVDD=5V
- Interface : DIT (fs=48kHz), Serial Multiplex (fs=96kHz)
- Temperature : Room

fs	48kHz	96kHz	BW, filter
THD+N(-1dB)	-106.1	-106.0	20Hz~20kHz
	-	-103.3	40Hz~40kHz
DR(-60dB)	114.0	113.5	20Hz~20kHz
	117.2	115.5	20Hz~20kHz , A-weighted
	-	105.1	40Hz~40kHz
S/N	114.0	113.5	20Hz~20kHz
	117.2	115.5	20Hz~20kHz, A-weighted
		105.1	40Hz~40kHz
unit	[dB]	[dB]	

■ Plot

fs=48kHz

Figure 1. FFT (Input Level = -1dB)

Figure 2. FFT (Input Level = -60dB)

Figure 3. FFT (Input Level =-120dB)

Figure 4. FFT (Input =”0”data)

Figure 5. THD+N vs Input Frequency (Input level=-1dB)

Figure 6. THD+N vs Input Level (fin=1kHz)

Figure 7. Linearity

Figure 8. Frequency Response

Figure 9. Crosstalk

fs=96kHz

Figure 10. FFT (Input Level = -1dB)

Figure 11. FFT (Input Level = -60dB)

Figure 12. FFT (Input Level =-120dB)

Figure 13. FFT (Input =”0”data)

Figure 14. THD+N vs Input Frequency (Input level=-1dB)

Figure 15. THD+N vs Input Level (fin=1kHz)

Figure 16. Linearity

Figure 17. Frequency Response

Figure 18. Crosstalk

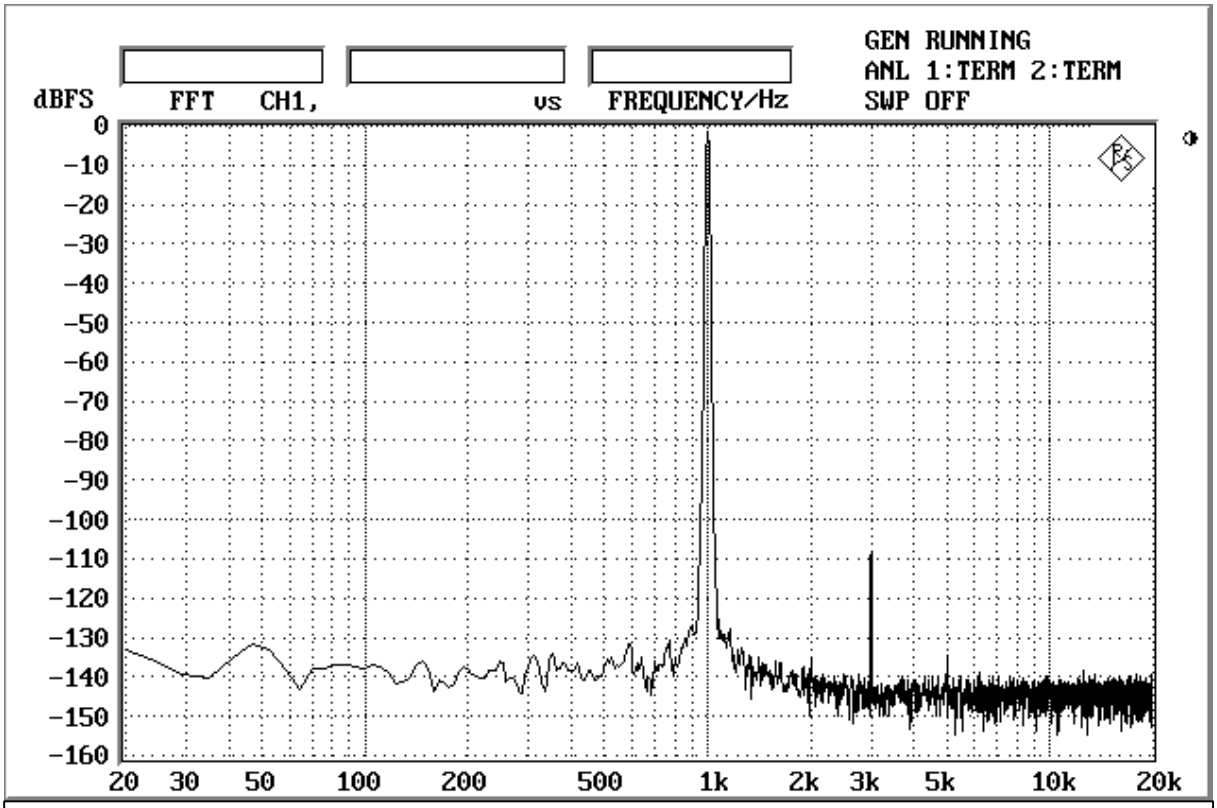


Fig. 1 FFT plot (Input Level = -1dB)

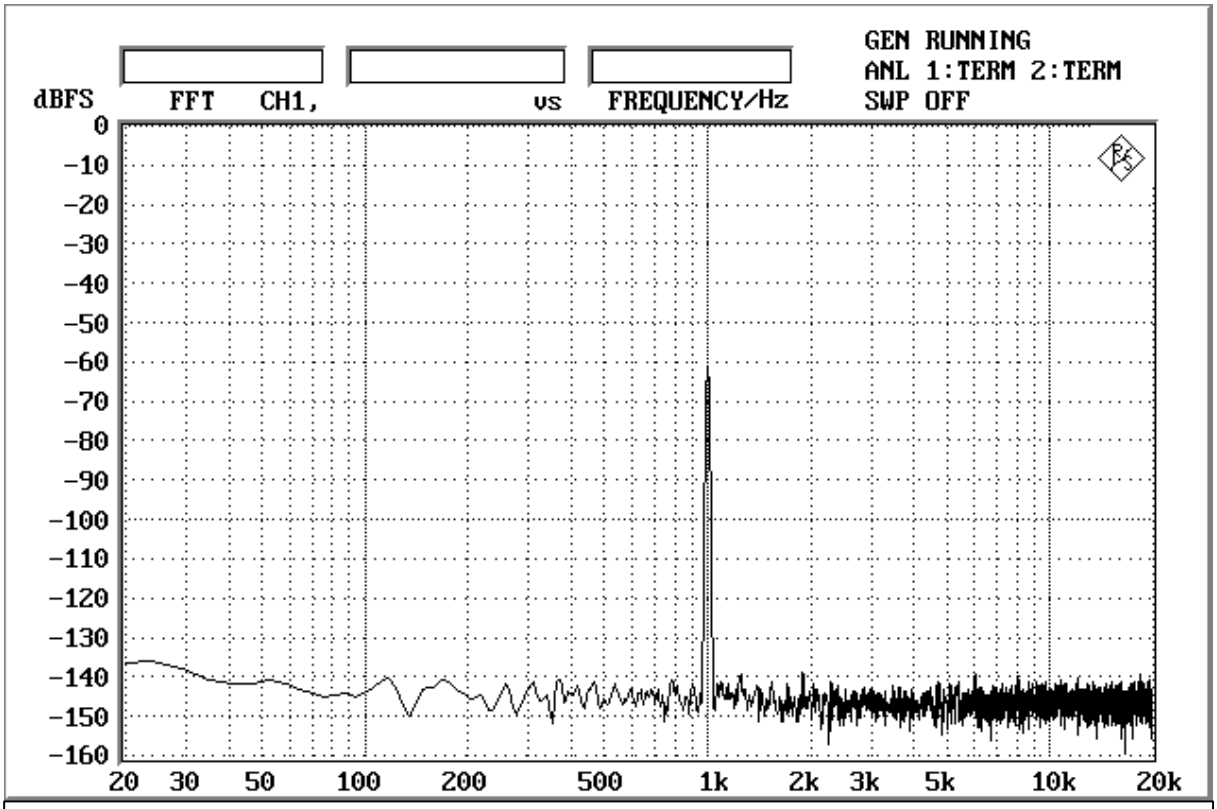


Fig. 2 FFT plot (Input Level = -60dB)

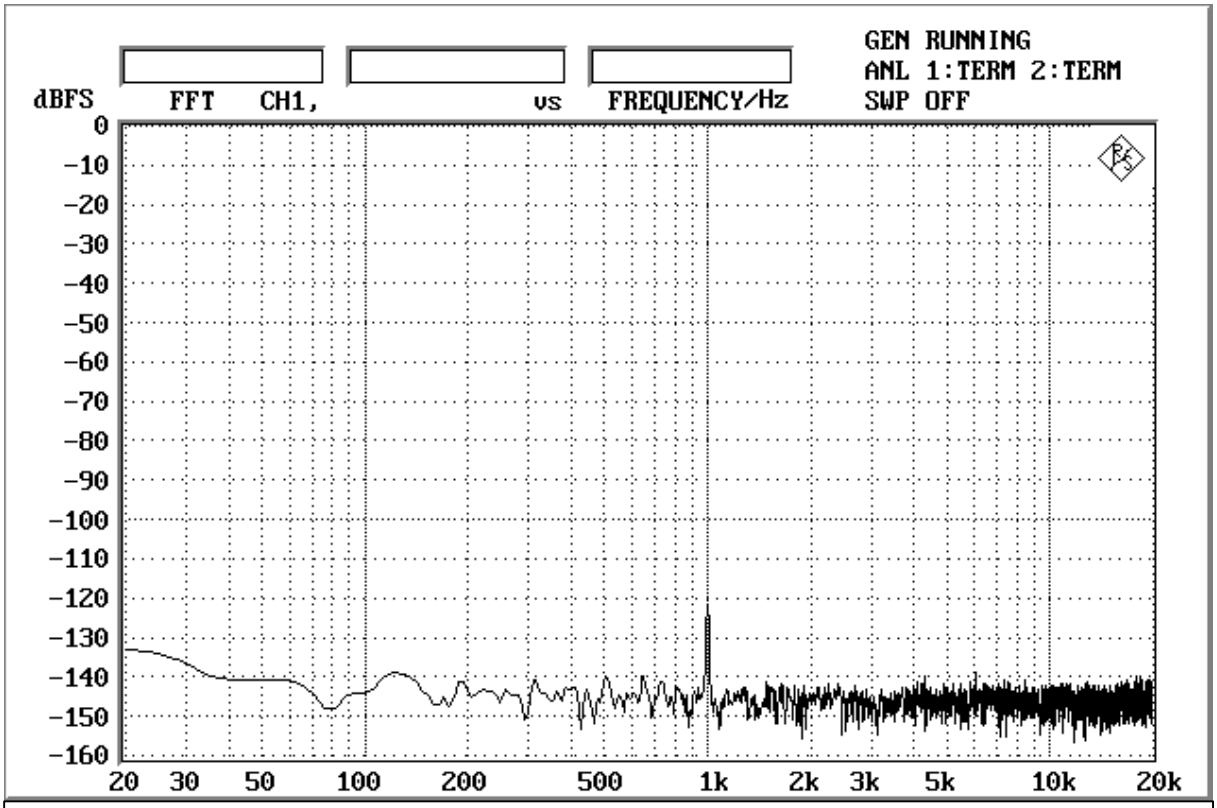


Fig. 3 FFT plot (Input Level = -120dB)

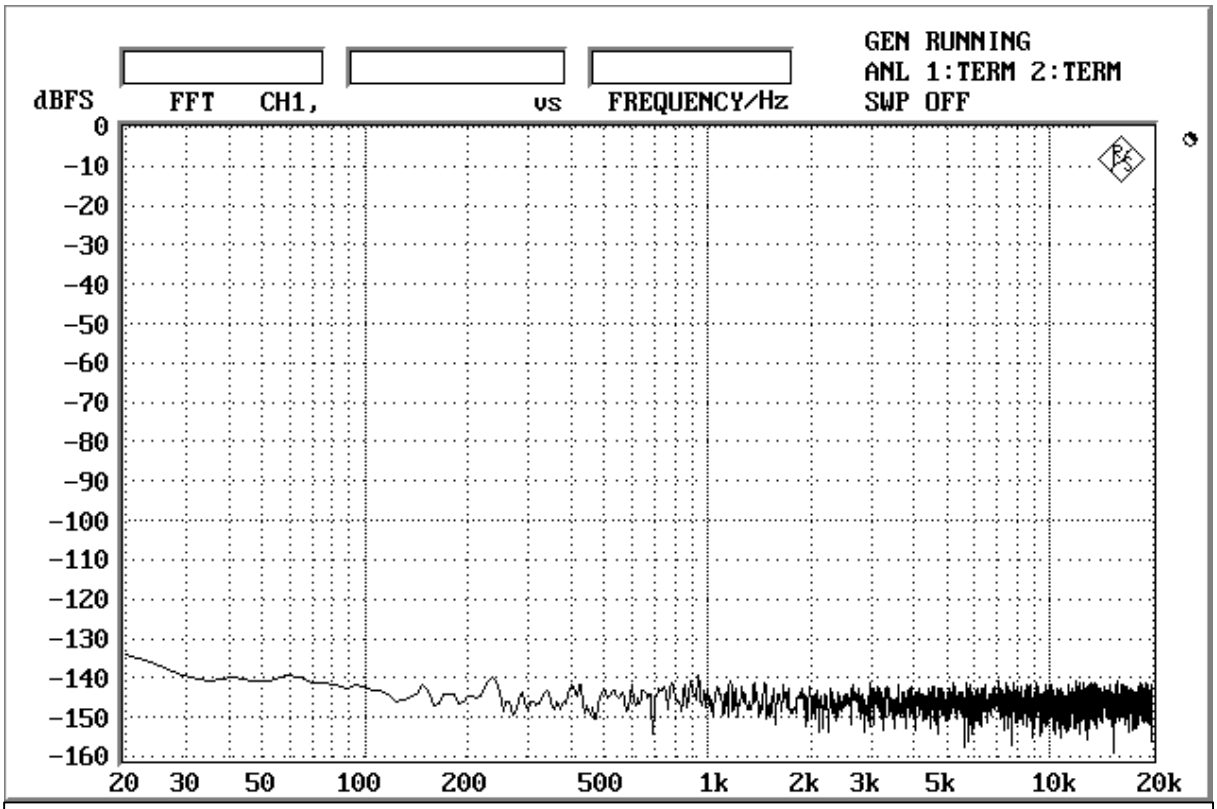


Fig. 4 FFT plot (Input = “0”data)

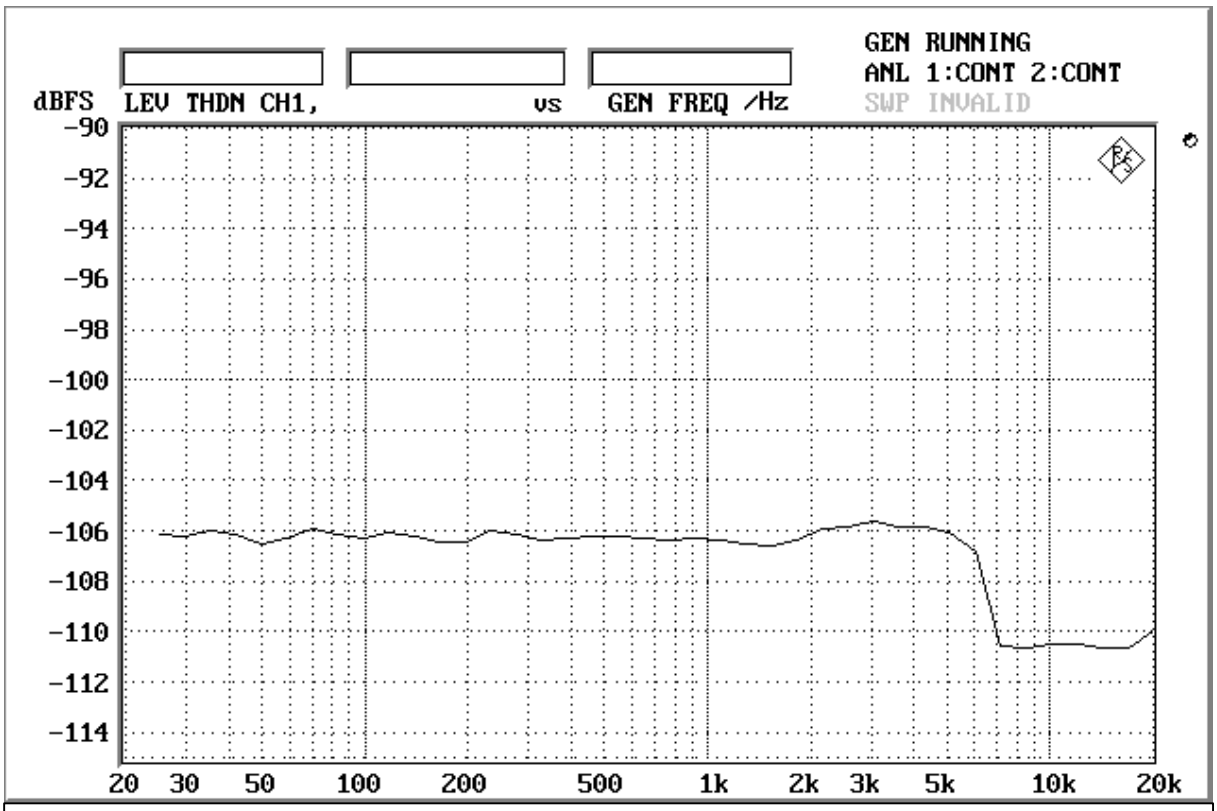


Fig. 5 THD+N vs. Input frequency (Input level = -1dB)

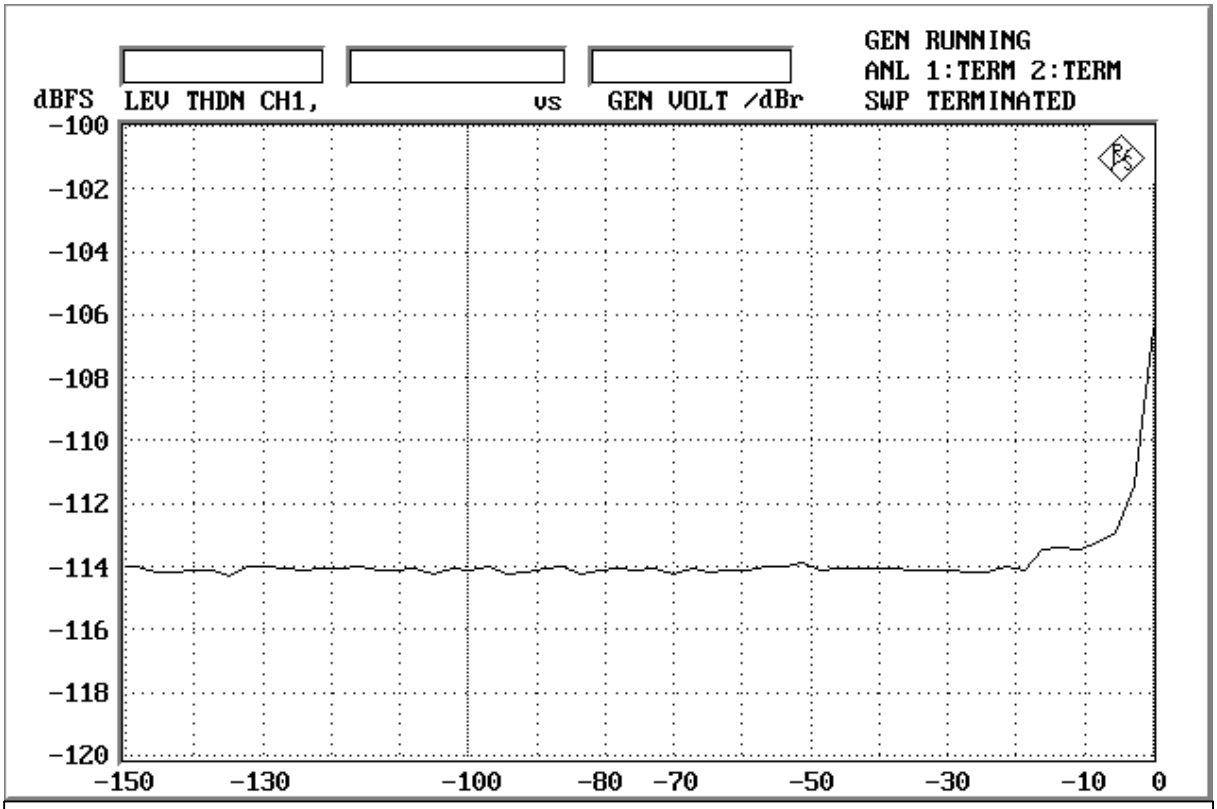


Fig. 6 THD+N vs. Input level (fin=1kHz)

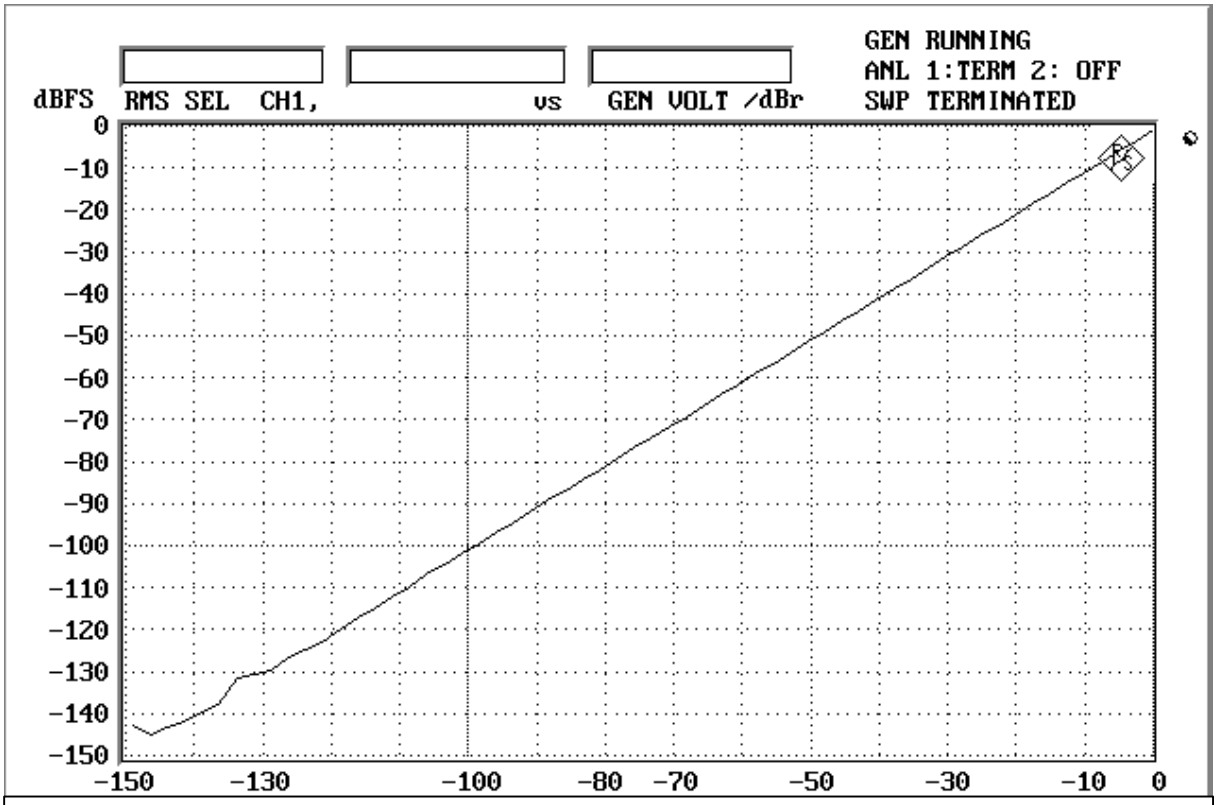


Fig.7 Linearity

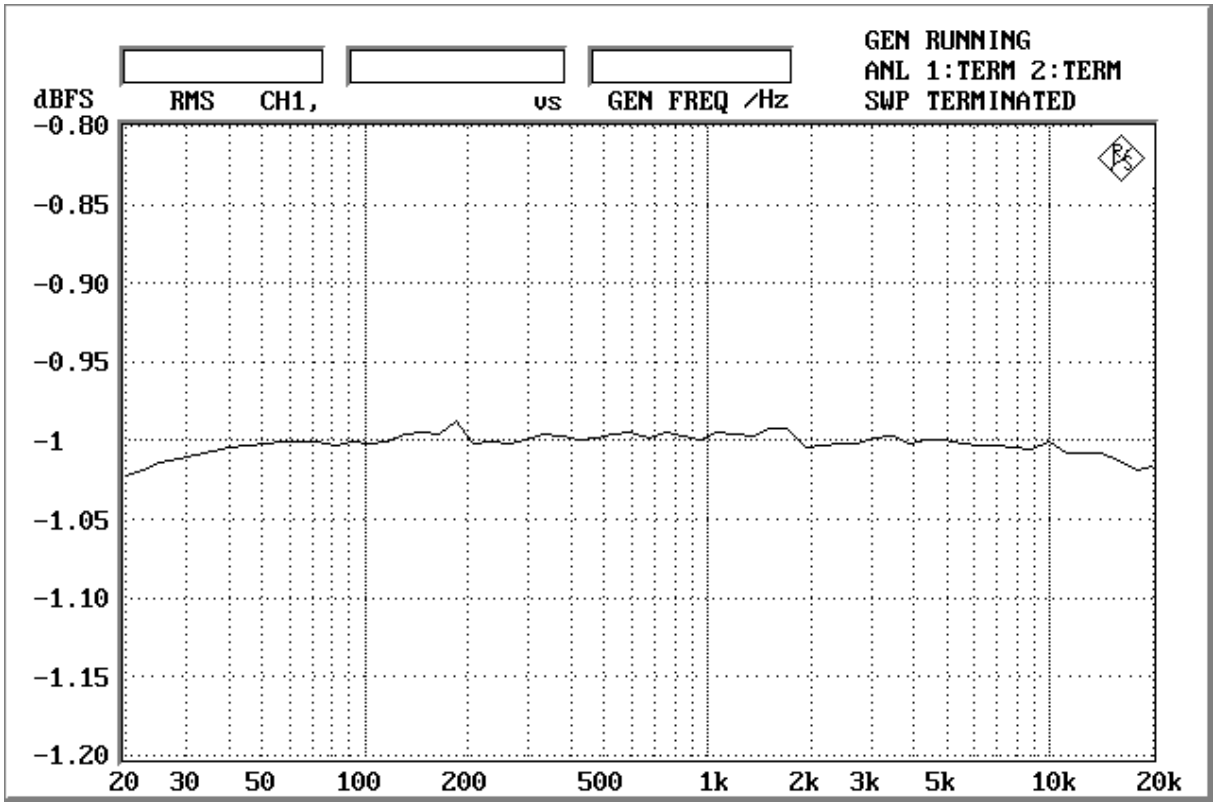


Fig. 8 Frequency response

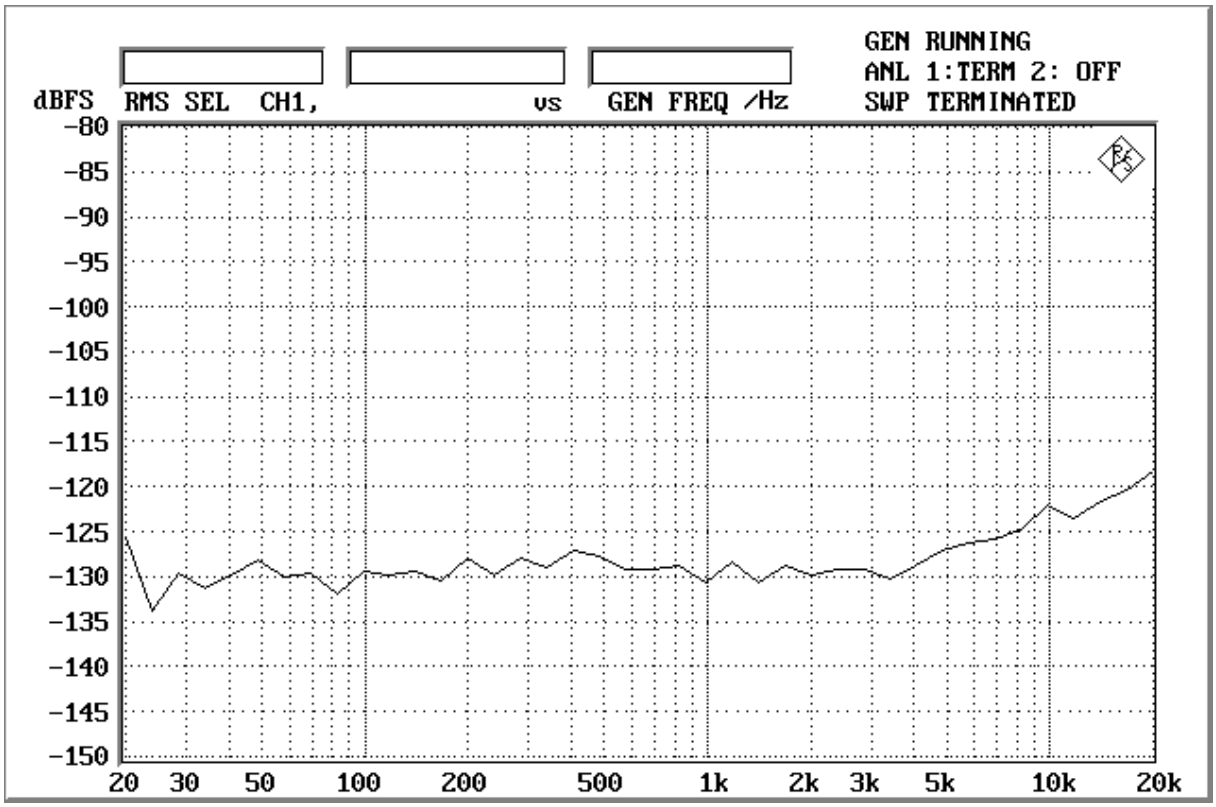


Fig. 9 Crosstalk

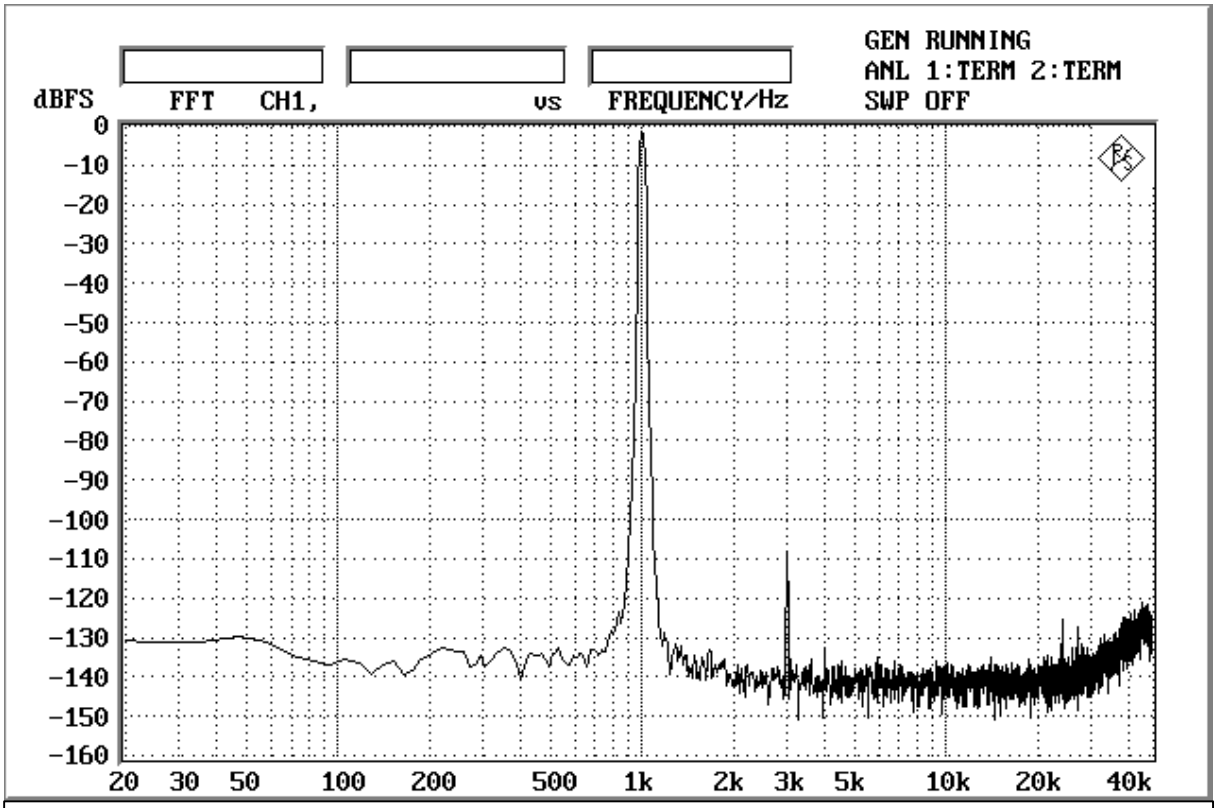


Fig.10 FFT plot (Input Level = -1dB)

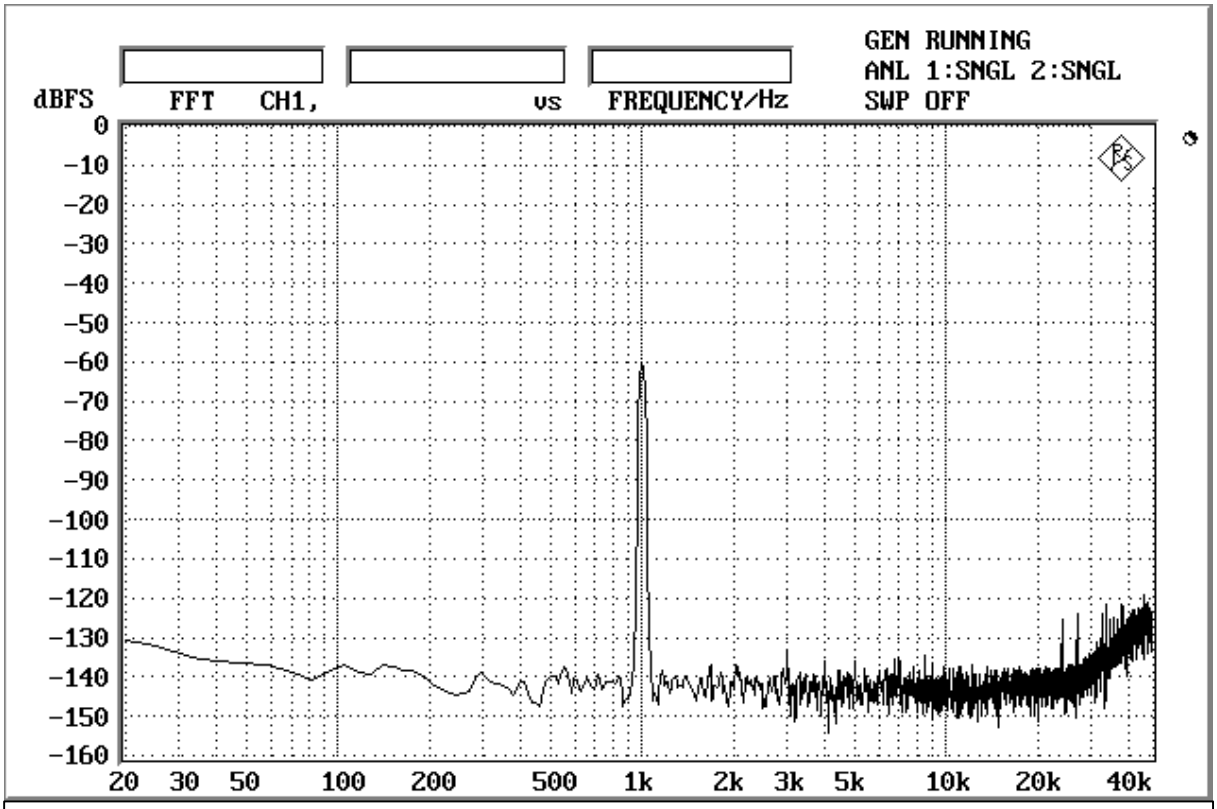


Fig.11 FFT plot (Input Level = -60dB)

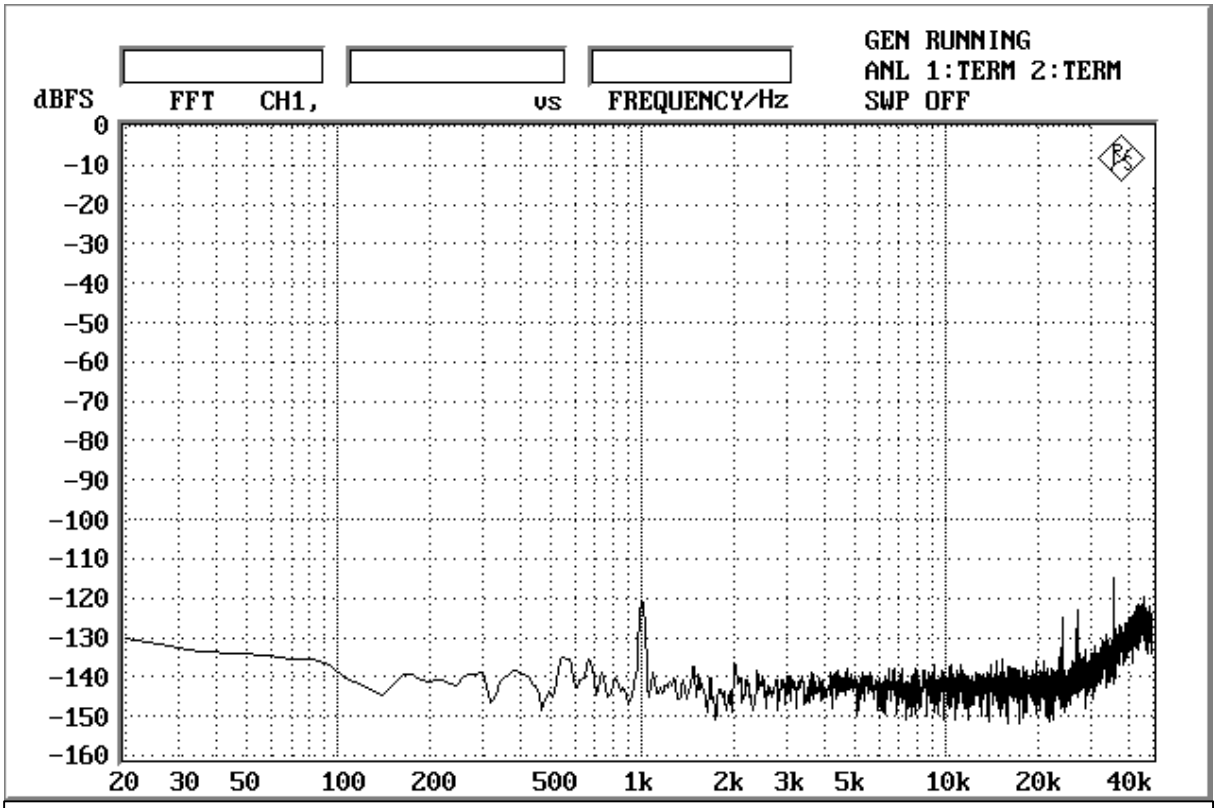


Fig.12 FFT plot (Input Level = -120dB)

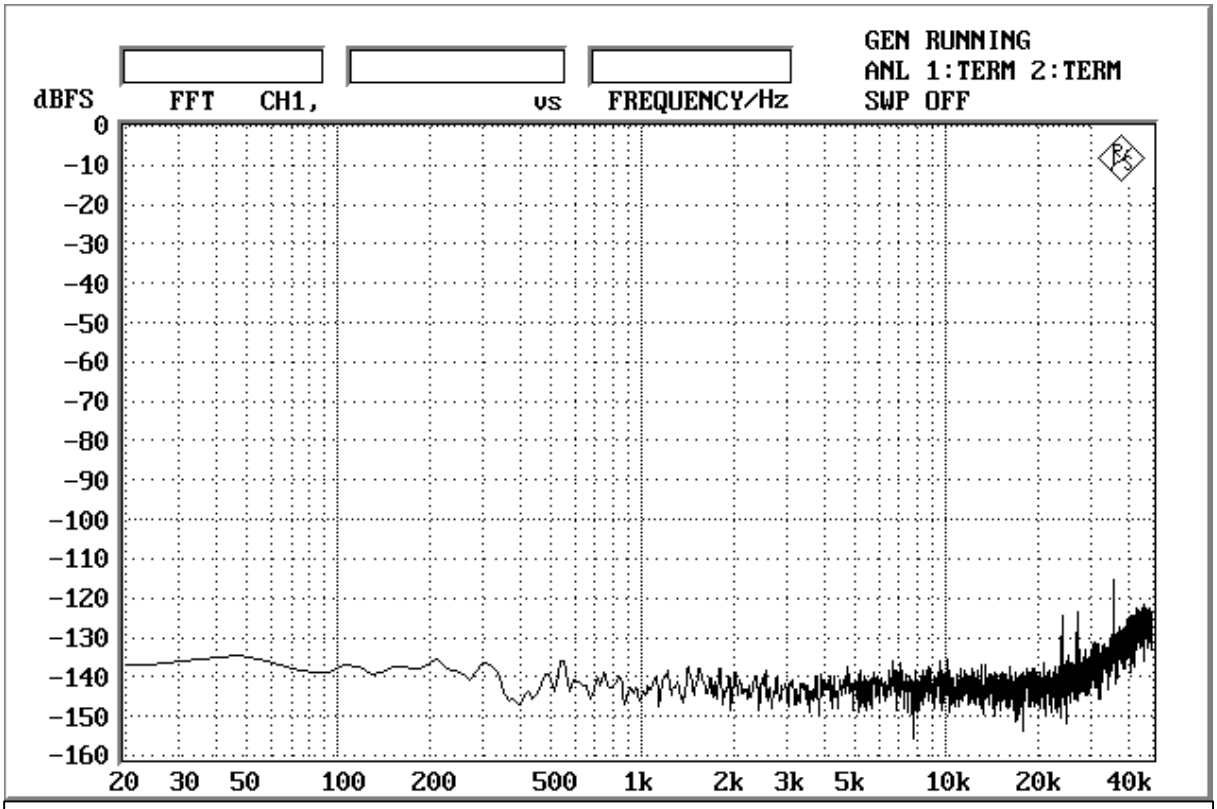


Fig.13 FFT plot (Input = “0”data)

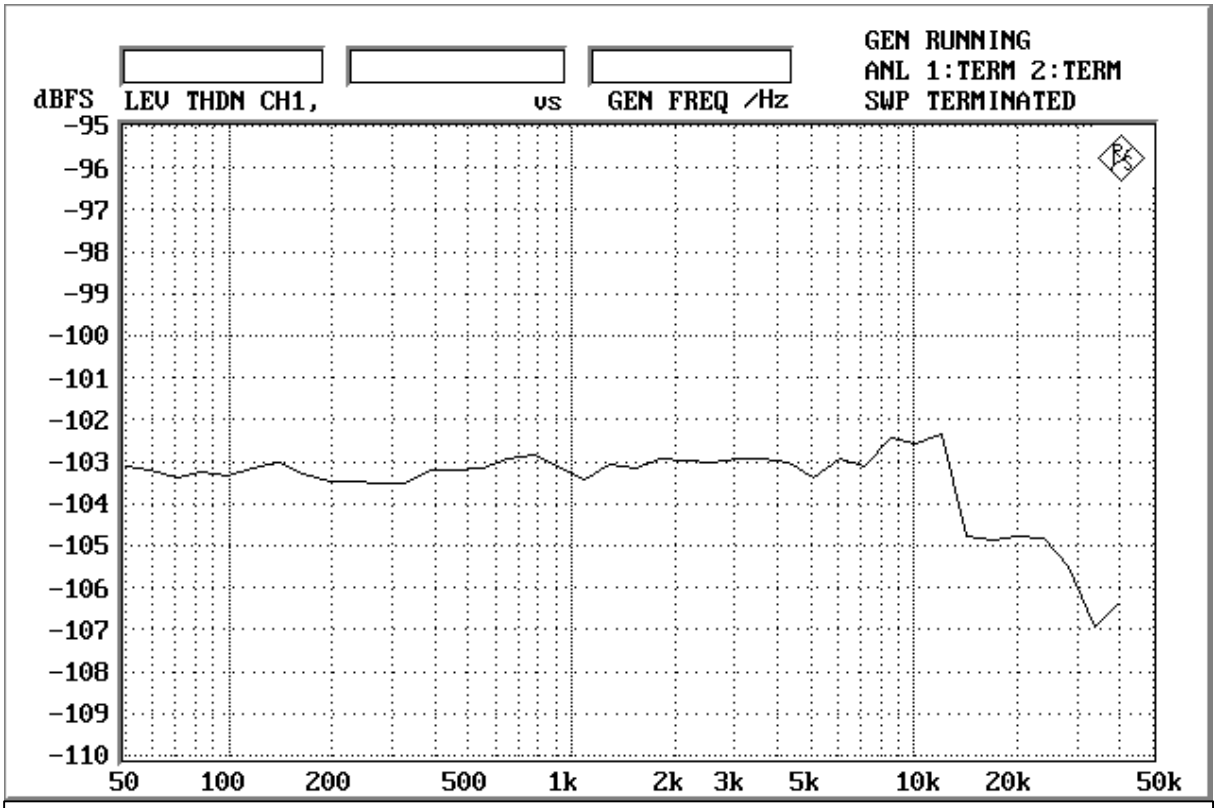


Fig.14 THD+N vs. Input frequency (Level = -1dB)

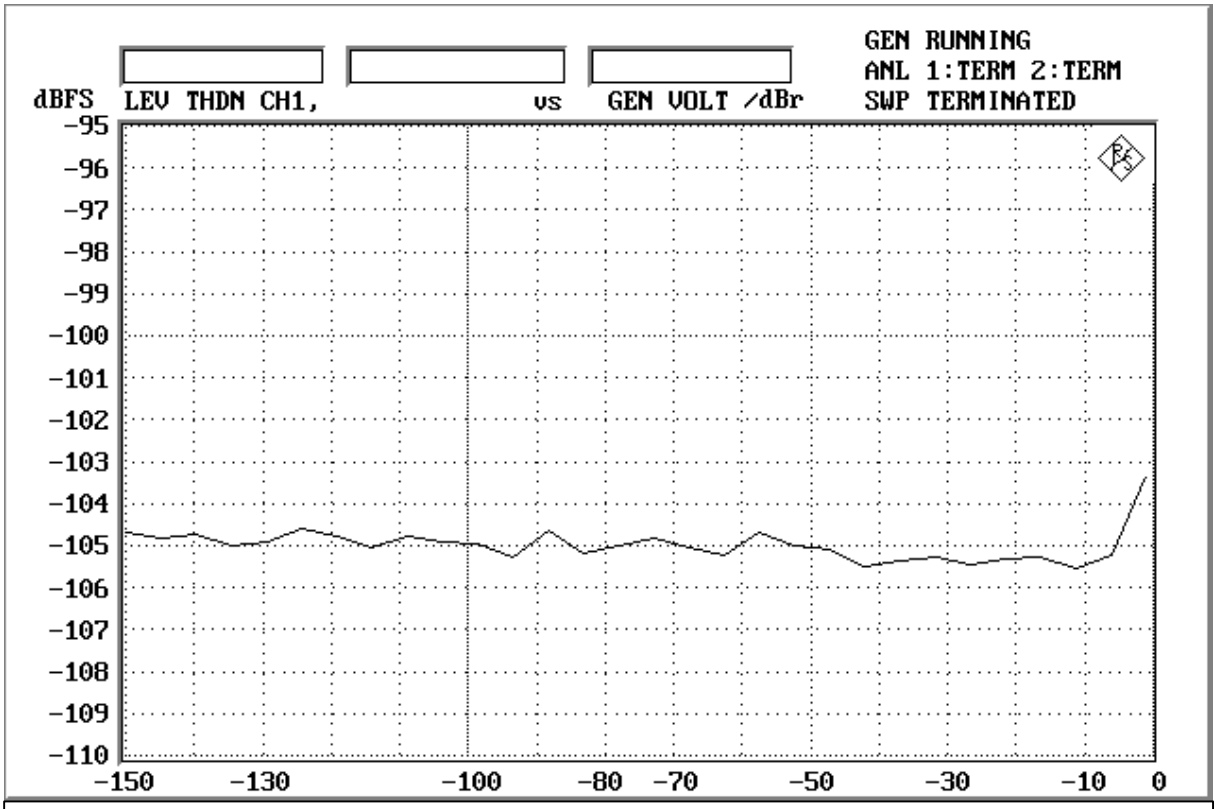


Fig.15 THD+V vs. Input level (fin = 1kHz)

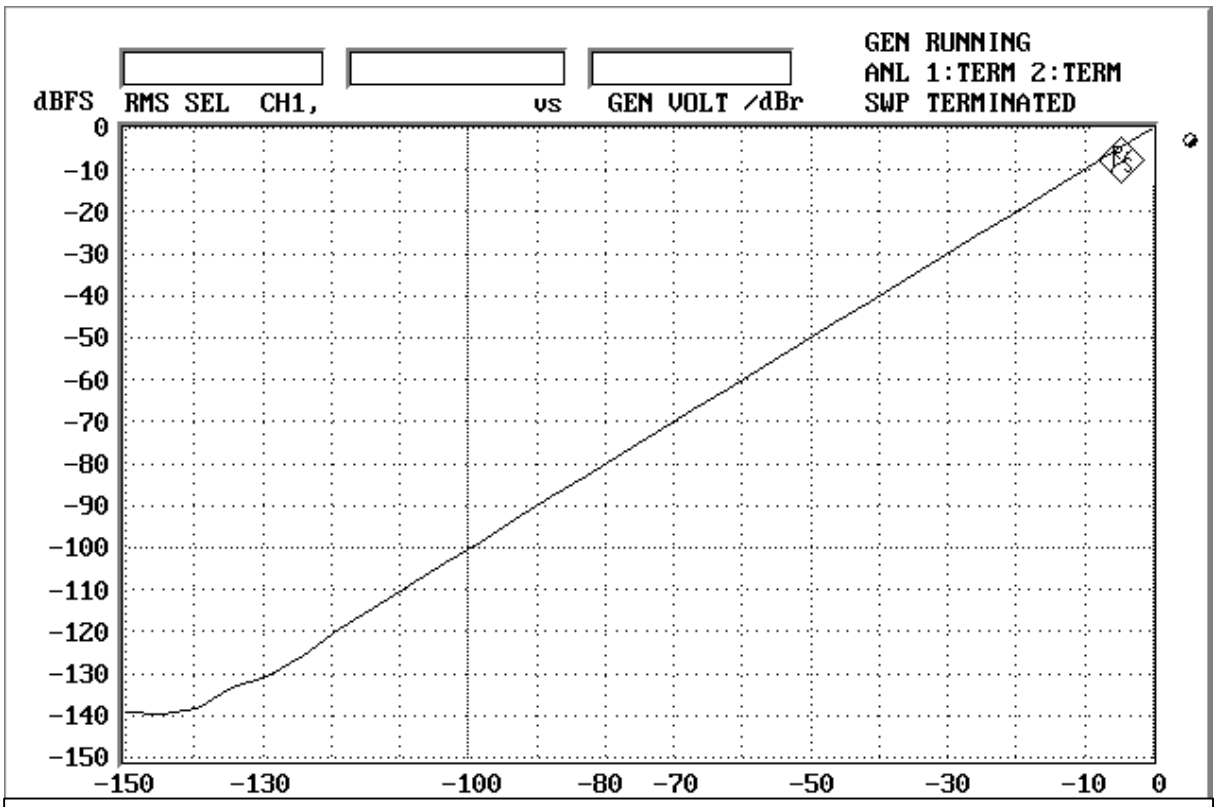


Fig.16 Linearity

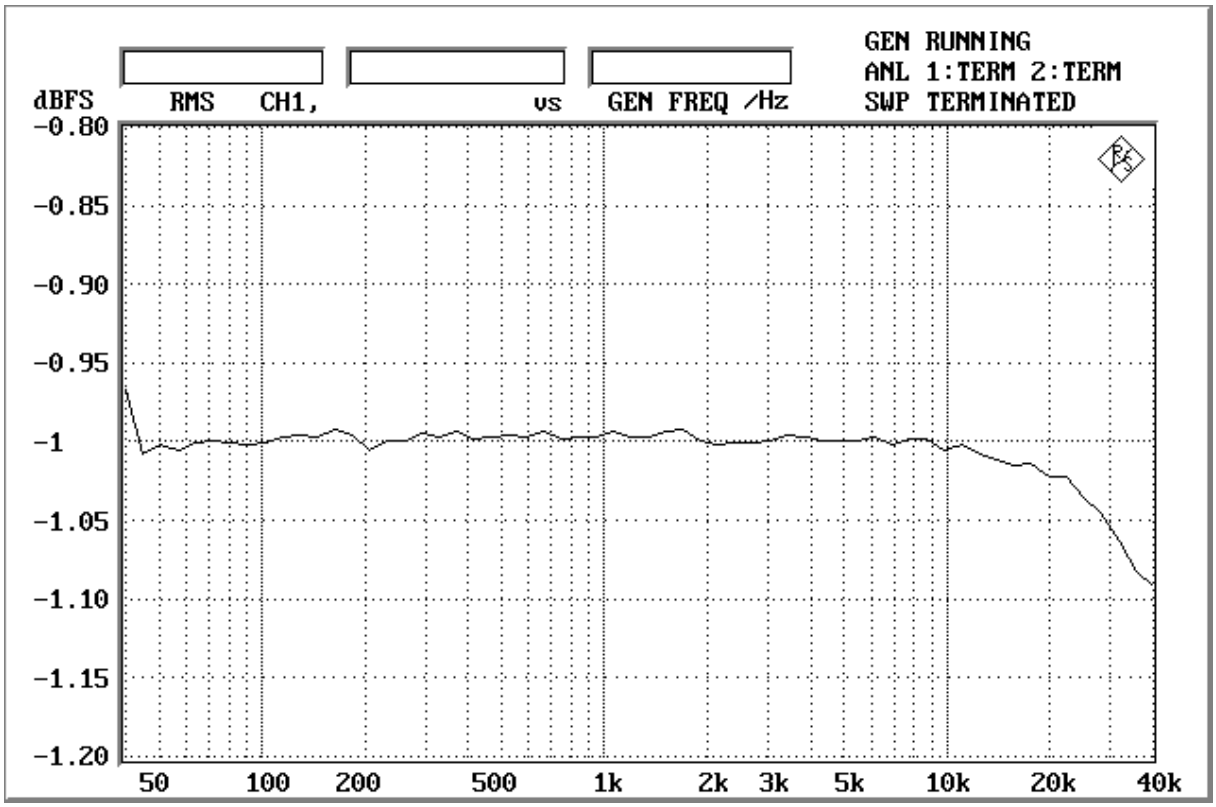


Fig.17 Frequency Response

AK5393(fs=96kHz)

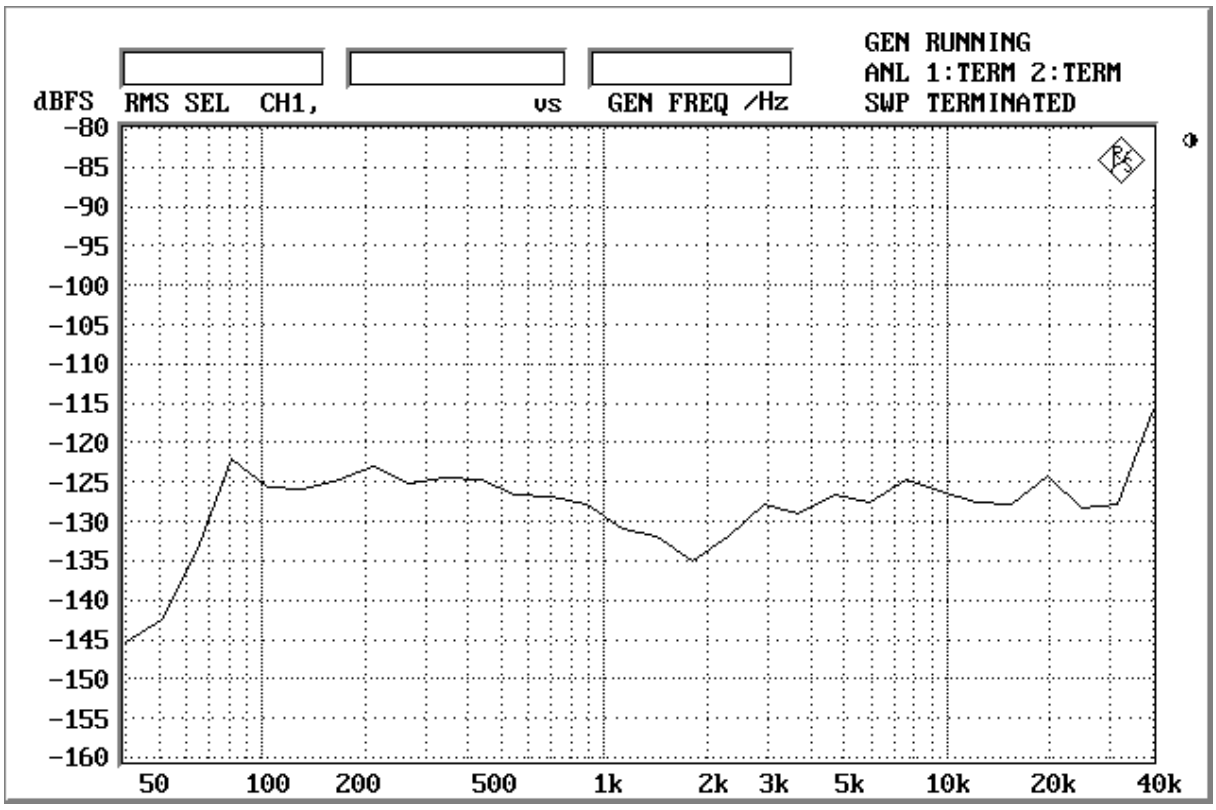
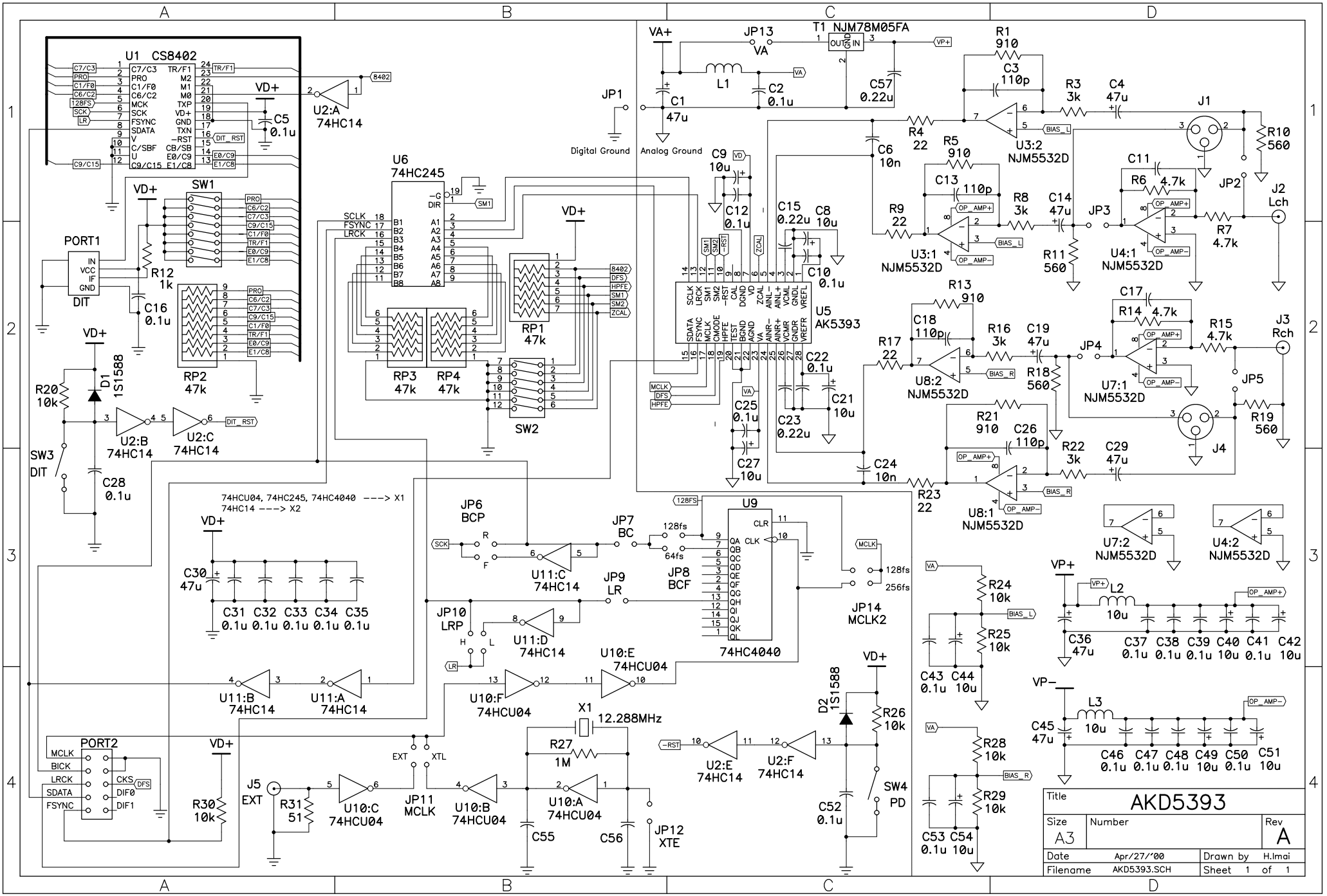
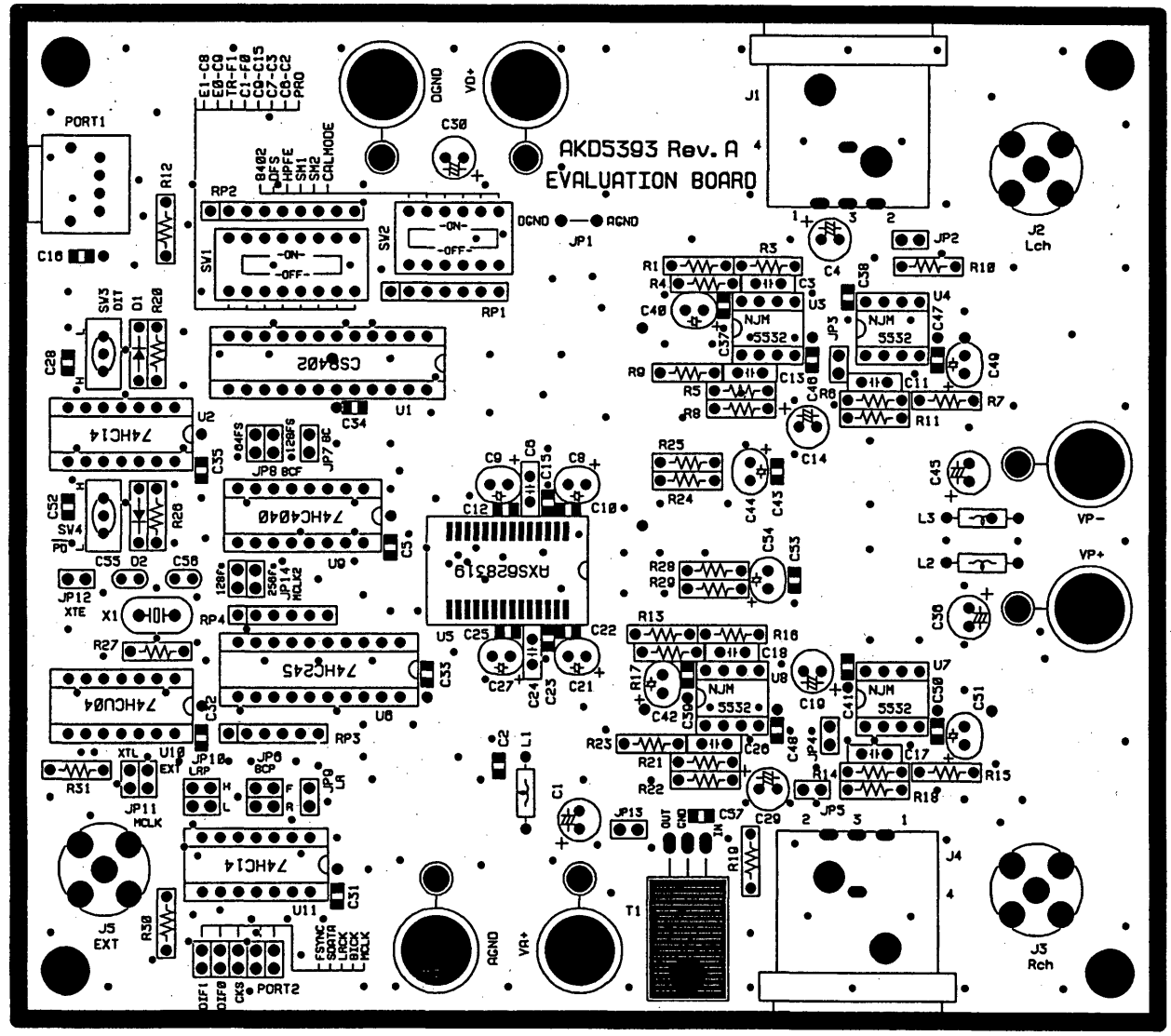
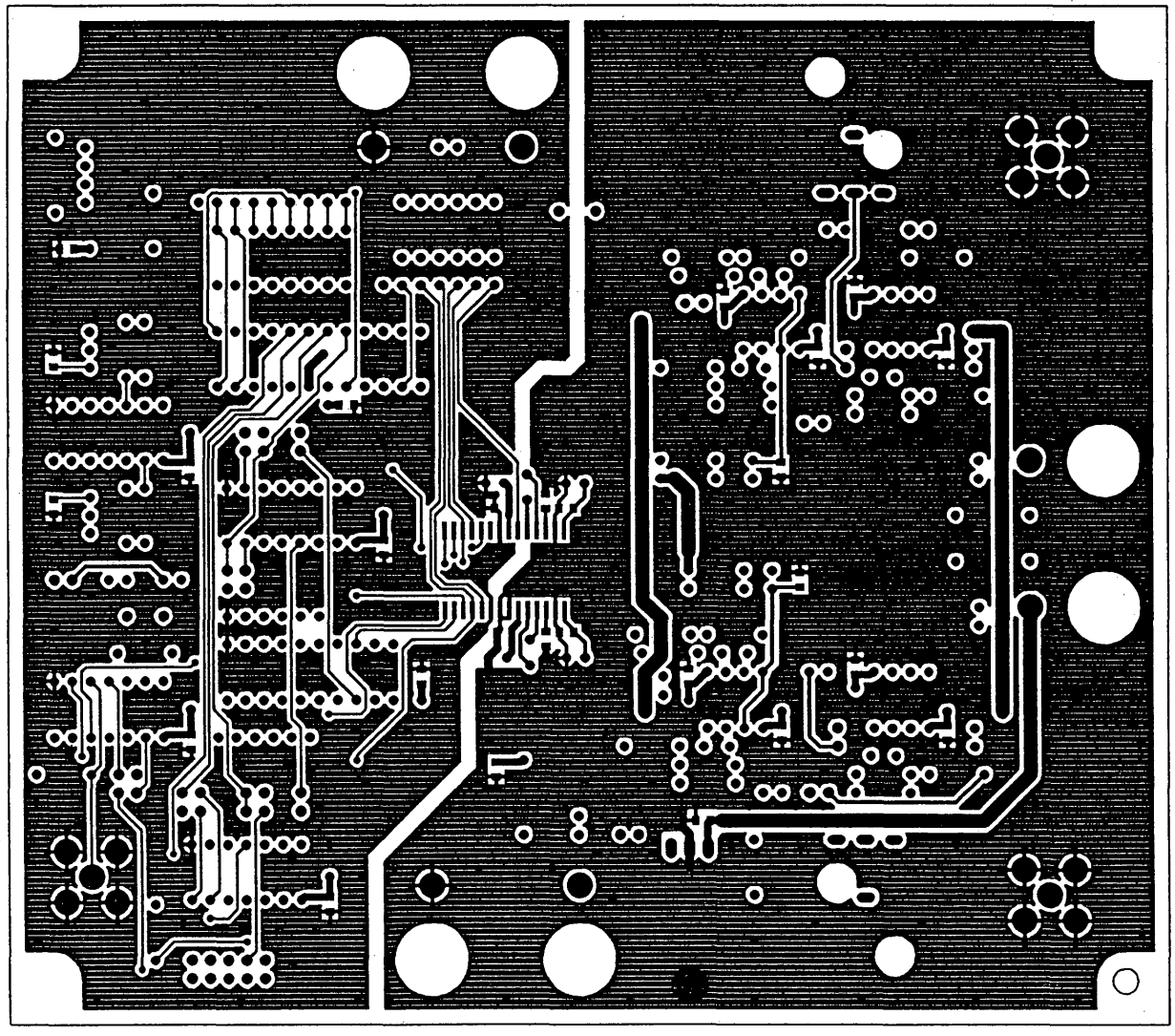


Fig.18 Crosstalk


U1 CS8402
U2:A 74HC14
U6 74HC245
U5 AK5393
U9 74HC4040
T1 NJM78M05FA
U3:2 NJM5532D
U3:1 NJM5532D
U4:1 NJM5532D
U8:2 NJM5532D
U7:1 NJM5532D
U8:1 NJM5532D
U7:2 NJM5532D
U4:2 NJM5532D
U2:B 74HC14
U2:C 74HC14
U11:C 74HC14
U11:D 74HC14
U11:B 74HC14
U11:A 74HC14
U10:E 74HCU04
U10:F 74HCU04
U10:C 74HCU04
U10:B 74HCU04
U10:A 74HCU04
U2:E 74HC14
U2:F 74HC14
PORT1 DIT
PORT2
SW1
SW2
SW3 DIT
SW4 PD
RP1 47k
RP2 47k
RP3 47k
RP4 47k
D1 1S1588
D2 1S1588
X1 12.288MHz
J1
J2 Lch
J3 Rch
J4
J5 EXT
JP1 Digital Ground
Analog Ground
JP6 BCP
JP7 BC
JP8 BCF
JP9 LR
JP10 LRP
JP11 MCLK
JP12 XTE
JP13 VA
JP14 MCLK2
74HCU04, 74HC245, 74HC4040 ---> X1
74HC14 ---> X2
Title AKD5393
Size A3
Number
Rev A
Date Apr/27/'00
Drawn by H.Imai
Filename AKD5393.SCH
Sheet 1 of 1



akd5393 rev.a L1 SR
akd5393 rev.a L1 SILK



akd5393 rev. a L1

ok92393 rev. a LS