AK4363
96kHz 24Bit ΔΣ DAC with PLL

GENERAL DESCRIPTION

The AK4363 is a stereo CMOS D/A Converter and Phase Locked Loop for use in digital video broadcast set-top box applications or DVD. The DAC signal outputs are single-ended and are analog filtered to remove out of band noise. Therefore no external filters are required. The PLL provides selectable sampling clock frequencies locked to the 27MHz recovered MPEG clock.

FEATURES

- **Stereo ΔΣ DAC**
- **S/(N+D): 90dB@5V**
- **DR: 102dB@5V**
- **S/N: 102dB@5V**
- **Multiple Sampling Frequencies:**
  - **16kHz, 22.05kHz, 24kHz (Half speed)**
  - **32kHz, 44.1kHz, 48kHz (Normal speed)**
  - **64kHz, 88.2kHz, 96kHz (Double speed)**
- **On-Chip Low Jitter Analog PLL:**
  - **Multiple Master Clock Frequencies generated from 27MHz**
    - **256fs/384fs/512fs/768fs/1024fs/1536fs for Half speed**
    - **256fs/384fs/512fs/768fs for Normal speed**
    - **128fs/192fs/256fs/384fs for Double speed**
- **Master Clock: PLL / External**
- **Data Input Formats:**
  - **LSB justified / MSB justified / I^2S selectable**
- **Selectable Function:**
  - **Soft Mute**
  - **Digital Attenuator (256 Steps)**
  - **Digital De-emphasis (44.1kHz/48kHz/32kHz)**
- **Output Mode: Stereo, Mono, Reverse, Mute**
- **Input Level: TTL/CMOS Selectable**
- **Output Level: 3.0Vpp@5V**
- **Control mode: 3-wire Serial / I^2C Bus**
- **Low Power Dissipation: 80mW@5V**
- **Small 24pin VSOP Package**
- **Power Supply: 2.7~5.5V**
- **Ta: -40~85°C**

■ Block Diagram

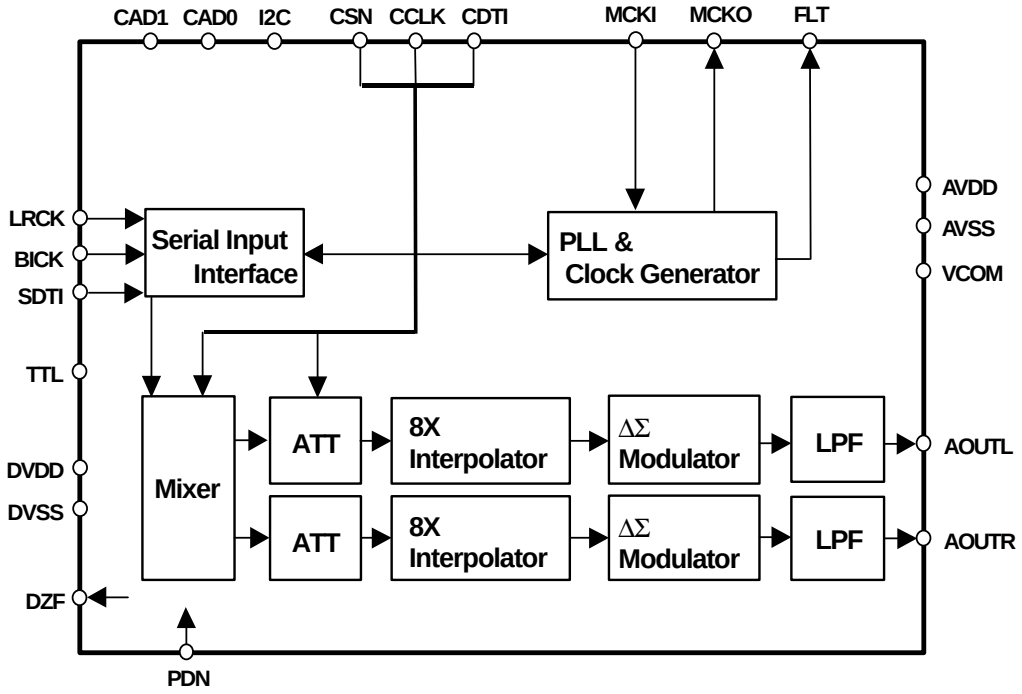


Figure 1. 3-wire Serial Control Mode (I2C = "L")

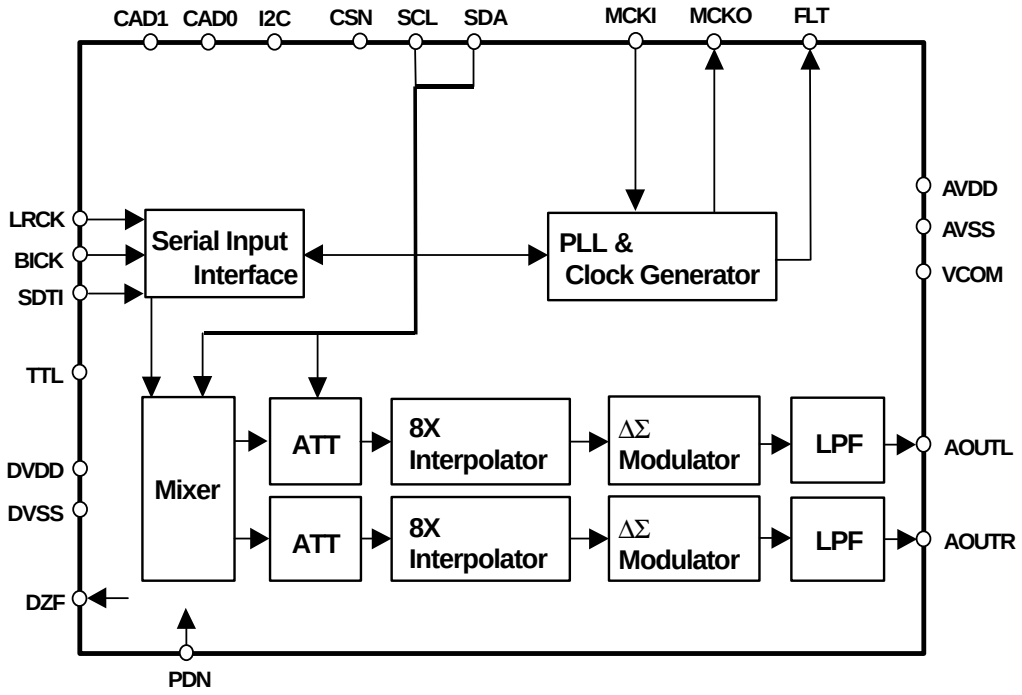
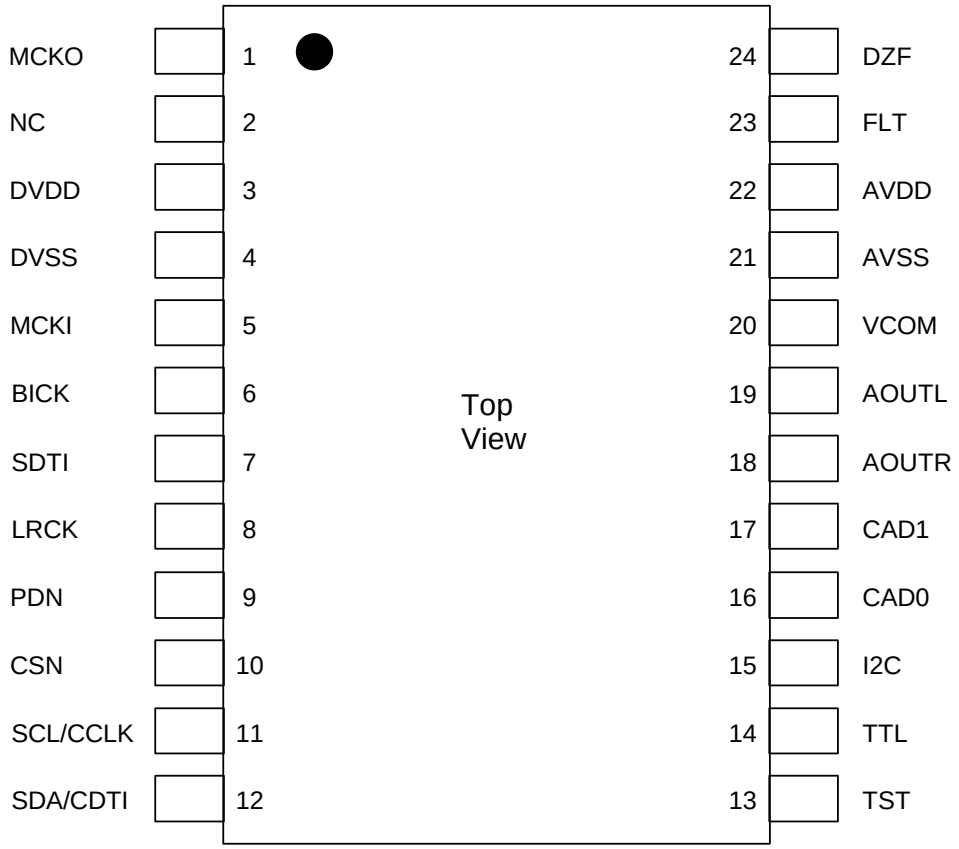


Figure 2. I^2C Bus Control Mode (I2C = "H")

■ Ordering Guide

AK4363VF	-40~+85°C	24pin VSOP
AKD4363	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Description
1	MCKO	O	Master Clock Output Pin EXT = "0": System clock is output from PLL circuit (PLL mode), EXT = "1": Same frequency as MCKI is output (External mode)
2	NC	-	No Connect Nothing should be connected externally to this pin.
3	DVDD	-	Digital Power Supply Pin, +2.7~+5.5V
4	DVSS	-	Digital Ground Pin, 0V
5	MCKI	I	System Clock Input Pin EXT = "0": 27MHz (PLL mode), EXT = "1": Other frequency (External mode)
6	BICK	I	Serial Data Clock Pin
7	SDTI	I	Serial Data Input Pin
8	LRCK	I	Serial Input Channel Clock Pin
9	PDN	I	Power-Down Pin When "L", the circuit is in power-down mode. The AK4363 should always be reset upon power-up.
10	CSN	I	Chip Select Pin at 3-wire Serial control mode This pin should be connected to DVDD at I^2C Bus control mode.
11	SCL	I	Control Clock Pin at I^2C bus control mode
	CCLK	I	Control Clock Pin at 3-wire serial control mode
12	SDA	I/O	Control Data Input/Output Pin at I^2C Bus control mode
	CDTI	I	Control Data Input Pin at 3-wire serial control mode
13	TST	I	Test pin This pin should be connected to DVSS.
14	TTL	I	Digital Input Level Select Pin "L": CMOS, "H": TTL
15	I2C	I	Control Mode Select Pin "L": 3-wire Serial, "H": I^2C Bus
16	CAD0	I	Chip Address Select 0 Pin
17	CAD1	I	Chip Address Select 1 Pin
18	AOUTR	O	Rch Analog Output Pin
19	AOUTL	O	Lch Analog Output Pin
20	VCOM	O	Common Voltage Output Pin, AVDD/2 Used for analog common voltage. Large external capacitor is used to reduce power supply noise.
21	AVSS	-	Analog Ground Pin
22	AVDD	-	Analog Power Supply Pin
23	FLT	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resister and one capacitor in series. (See "SYSTEM DESIGN".)
24	DZF	O	Zero Input Detect Pin When SDTI follows a total 8192 LRCK cycles with "0" input data or RSTN = "0", this pin goes to "H".

Note: No input pins should be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.
2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	3V operation (TTL = "L")					
	Analog	AVDD	2.7	3.0	5.5	V
	Digital	DVDD	2.7	3.0	3.6 or AVDD	V
	5V operation (TTL = "H")					
	Analog	AVDD	4.5	5.0	5.5	V
	Digital	DVDD	4.5	5.0	AVDD	V

Note:1. All voltages with respect to ground.
3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; AVDD, DVDD=5V; fs=44.1kHz; EXT = "1"; FS1-0 = "00"; DFS1-0 = "00"; CKS2-0 = "000"; DIF2-0 = "101"; Signal Frequency =1kHz; Measurement frequency=20Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics					
Resolution				24	Bits
S/(N+D)	AVDD=5V	84	90		dB
	AVDD=3V	80	86		dB
DR (-60dB input, A-weighted)	AVDD=5V	94	102		dB
	AVDD=3V	90	97		dB
S/N (A-weighted)	AVDD=5V	94	102		dB
	AVDD=3V	90	97		dB
Interchannel Isolation		90	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage AOUT=0.6x(AVDD-AVSS)	AVDD=5V	2.8	3.0	3.2	Vpp
	AVDD=3V	1.66	1.8	1.94	Vpp
Load Resistance	(Note 4)	10			kΩ
Load Capacitance				25	pF
Power Supplies					
Power Supply Current					
Normal Operation (PDN = "H")	(Note 5)				
AVDD			8	12	mA
DVDD			8	16	mA
Power-Down-Mode (PDN = "L")					
AVDD+DVDD			10	100	μA

Note:4. AC load.

5. AVDD is 9mA(typ) at EXT = "0". DVDD drops to 4mA at DVDD=3V.

ANALOG CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD, DVDD=5V; fs=96kHz; EXT = "1"; FS1-0 = "01"; DFS1-0 = "01"; CKS2-0 = "001"; DIF2-0 = "101"; Signal Frequency =1kHz; Measurement frequency=20Hz~40kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics					
Resolution				24	Bits
S/(N+D)	AVDD=5V	80	86		dB
	AVDD=3V	78	84		dB
DR (-60dB input)	AVDD=5V	88	96		dB
	AVDD=3V	84	92		dB
S/N	AVDD=5V	88	96		dB
	AVDD=3V	84	92		dB
Interchannel Isolation		90	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage AOUT=0.6x(AVDD-AVSS)	AVDD=5V	2.8	3.0	3.2	Vpp
	AVDD=3V	1.66	1.8	1.94	Vpp
Load Resistance	(Note 4)	10			kΩ
Load Capacitance				25	pF
Power Supplies					
Power Supply Current					
Normal Operation (PDN = "H")	(Note 6)				
AVDD			8	12	mA
DVDD			13	26	mA
Power-Down-Mode (PDN = "L")					
AVDD+DVDD			10	100	μA

Note:4. AC load.

6. AVDD is 9mA(typ) at EXT = "0". DVDD drops to 7mA at DVDD=3V.

FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; AVDD, DVDD=2.7~5.5V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 7)	-0.02dB	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband (Note 7)		SB	24.1			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 8)		GD	-	20.1	-	1/fs
Digital Filter + Analog Filter						
Frequency Response: 0~20.0kHz		FR	-	±0.2	-	dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.02dB), SB=0.546*fs.

8. The calculating delay time which occurred by digital filtering. This time is from setting the 24bit data of both channels on the input register to the output of analog signal.

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD, DVDD=2.7~5.5V; fs=96kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 7)	-0.02dB	PB	0		43.5	kHz
	-6.0dB		-	48.0	-	kHz
Stopband (Note 7)		SB	52.5			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 8)		GD	-	20.1	-	1/fs
Digital Filter + Analog Filter						
Frequency Response: 0~20.0kHz		FR	-	±0.2	-	dB
40.0kHz			-	±0.2	-	dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.02dB), SB=0.546*fs.

8. The calculating delay time which occurred by digital filtering. This time is from setting the 24bit data of both channels on the input register to the output of analog signal.

DIGITAL CHARACTERISTICS (CMOS level input)

(Ta=25°C; AVDD=2.7~5.5V; DVDD=2.7~3.6V; TTL = "L")

Parameter		Symbol	min	typ	max	Units
High-Level input voltage		VIH	0.7xDVDD	-	-	V
Low-Level input voltage		VIL	-	-	0.3xDVDD	V
High-Level Output Voltage						
(MCKO pins:	Iout=-100μA)	VOH	DVDD-0.5	-	-	V
(DZF pin:	Iout=-100μA)	VOH	AVDD-0.5	-	-	V
Low-Level Output Voltage						
(MCKO, DZF pins:	Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin:	Iout= 3mA)	VOL	-	-	0.4	V
Input leakage current		Iin	-	-	±10	μA

DIGITAL CHARACTERISTICS (TTL level input; except for TTL pin)

(Ta=25°C; AVDD, DVDD=4.5~5.5V; TTL = "H")

Parameter		Symbol	min	typ	max	Units
High-Level input voltage	(TTL pin)	VIH	0.7xDVDD	-	-	V
	(All pins except for TTL pin)	VIH	2.2	-	-	V
Low-Level input voltage	(TTL pin)	VIL	-	-	0.3xDVDD	V
	(All pins except for TTL pin)	VIL	-	-	0.8	V
High-Level Output Voltage						
(MCKO pins:	Iout=-100μA)	VOH	DVDD-0.5	-	-	V
(DZF pin:	Iout=-100μA)	VOH	AVDD-0.5	-	-	V
Low-Level Output Voltage						
(MCKO, DZF pins:	Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin:	Iout= 3mA)	VOL	-	-	0.4	V
Input leakage current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~5.5V; C_L=20pF)

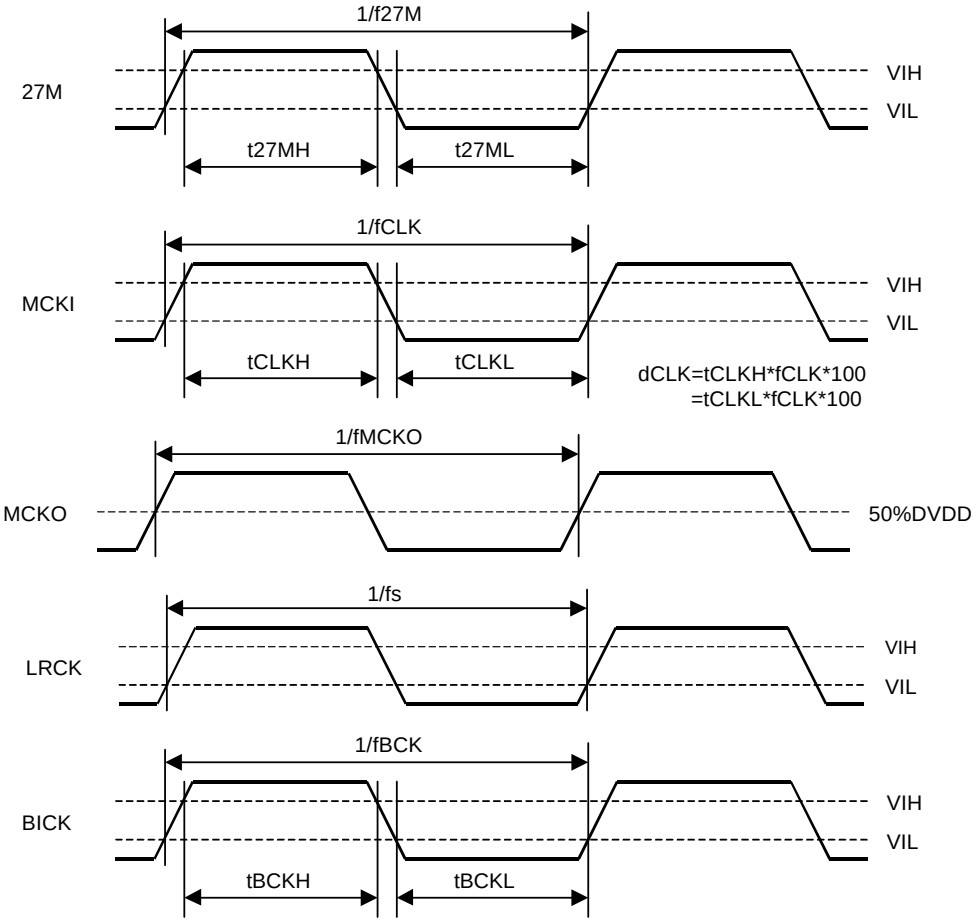
Parameter	Symbol	min	typ	max	Units
27MHz Input (PLL mode):					
Frequency	f27M		27		MHz
Pulse Width Low	t27ML	14			ns
Pulse Width High	t27MH	14			ns
Master Clock Input (External mode):					
Frequency					
128fs/256fs/512fs/1024fs	fCLK	4.096		24.576	MHz
192fs/384fs/768fs/1536fs	fCLK	6.144		36.864	MHz
Duty Cycle	dCLK	40		60	%
MCKO Output (PLL mode):					
Frequency	fMCKO	4.096		36.864	MHz
Duty Cycle	dMCKO	40		60	%
Rise time (20% to 80% DVDD)	trMCKO		2		ns
Fall time (80% to 20% DVDD)	tfMCKO		2		ns
LRCK: (Note 9)					
Frequency					
Half Speed Mode (DFS1-0 = "11")	fsh	16		24	kHz
Normal Speed Mode (DFS1-0 = "00")	fsn	32		48	kHz
Double Speed Mode (DFS1-0 = "01")	fsd	64		96	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing:					
BICK Period					
Half Speed Mode	tBCK	1/128fs			ns
Normal Speed Mode	tBCK	1/128fs			ns
Double Speed Mode	tBCK	1/64fs			ns
BICK Pulse Width Low	tBCKL	70			ns
BICK Pulse Width High	tBCKH	70			ns
BICK "↑" to LRCK Edge (Note 10)	tBLR	40			ns
LRCK Edge to BICK "↑" (Note 10)	tLRB	40			ns
SDTI Hold Time	tSDH	40			ns
SDTI Setup Time	tSDS	40			ns
Power-down & Reset Timing					
PDN Pulse Width (Note 11)	tPDW	150			ns

Note: 9. If sampling speed mode (DFS0-1) changes, please reset by PDN pin or RSTN bit.
10. BICK rising edge must not occur at the same time as LRCK edge.
11. The AK4363 can be reset by PDN pin "L" upon power up.
If CKS0-2 or DFS0-1 changes, the AK4363 should be reset by PDN pin or RSTN bit.

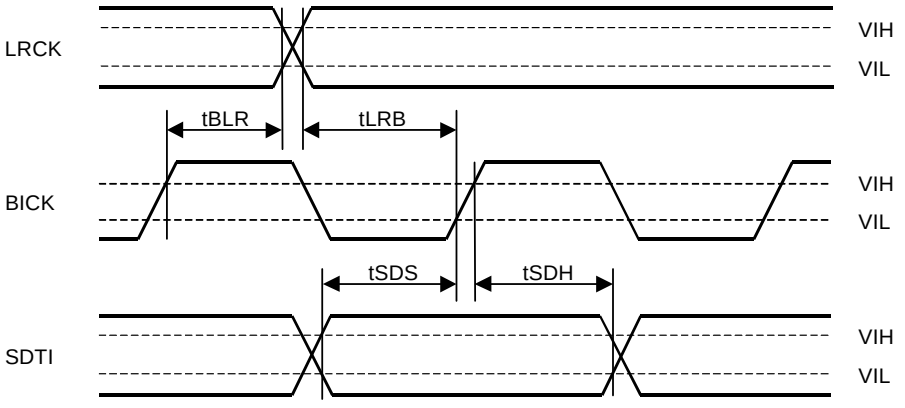
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	µs
Clock Low Time	tLOW	4.7		-	µs
Clock High Time	tHIGH	4.0		-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	µs
SDA Hold Time from SCL Falling (Note 12)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0		-	µs
Pulse Width of Spike Noise suppressed by Input Filter	tSP	0		50	ns

Note:12. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

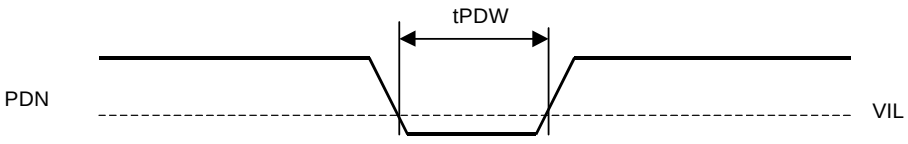
■ Timing Diagram



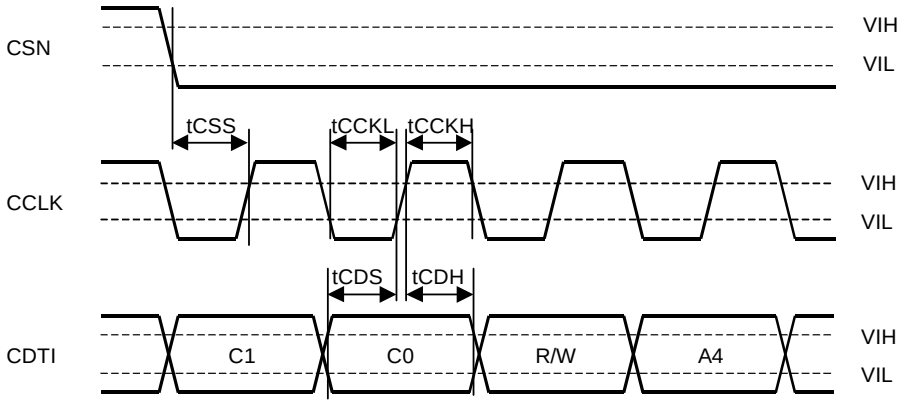
Clock Timing



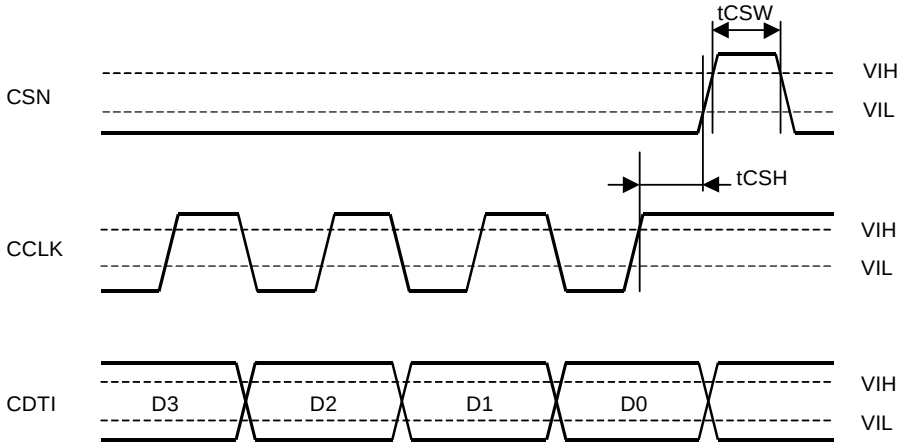
Serial Interface Timing



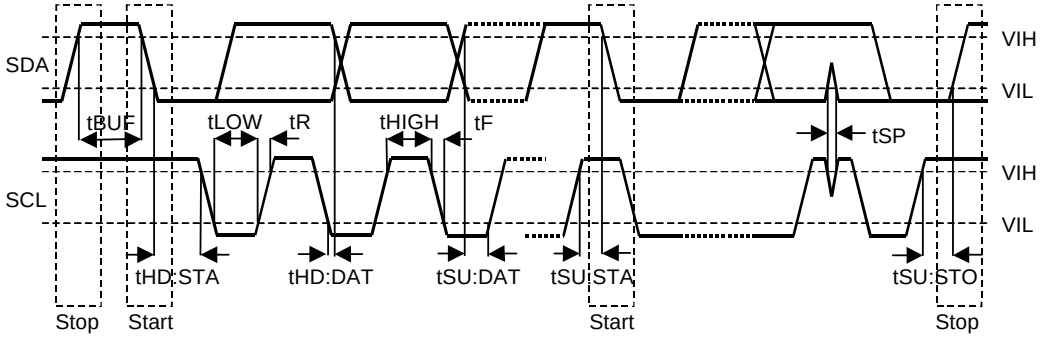
Power-down & Reset Timing



WRITE Command Input Timing (3-wire Serial mode)



WRITE Data Input Timing (3-wire Serial mode)



I^2C Bus mode Timing

OPERATION OVERVIEW

■ System Clock Input

1) PLL mode (EXT = "0")

A fully integrated analog phase locked loop generates MCKO which is locked to the 27MHz reference input. The frequency of the MCKO output is selectable via register data of CKS2-0, DFS1-0 and FS1-0 as defined in Table 1-3.

The PLL requires 20ms lock time whenever MCKO frequency selection changes or MCKO source changes from EXT mode to PLL mode, but 100ms upon power-up after 27MHz system clock stabilizes. Serial input data is zeroed internally while PLL is unlocked to prevent spurious output. When 27MHz clock is not present, the internal VCO frequency is pulled to its minimum value.

The LRCK input must be synchronous with MCKO, however the phase is not critical. Internal timing is synchronized to LRCK input upon power-up.

When MCKO frequency changes by register data of CKS2-0, DFS1-0 or FS1-0 during normal operation, the AK4363 should be reset by PDN pin "L" or RSTN bit "0". Serial input data is zeroed internally until PLL is locked after exiting resetting.

2) External mode (EXT = "1")

When EXT bit is set to "1", master clock can be input via MCKI pin. In this case, MCKO frequency is same as MCKI and it is not necessary to change the register data of FS1-0. The external clocks which are required to operate the AK4363 are MCKI, LRCK and BICK. The master clock (MCKI) should be synchronized with sampling clock (LRCK) but the phase is not critical. MCKI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCKI can be set by CKS2-0, and can be selected to half, normal or double speed mode by DFS1-0 (See Table 2).

In this case, internal VCO is powered down. Therefore, all external clocks should always be present whenever the AK4363 is in the normal operation mode (PDN = "H"). If these clock are not provided, the AK4363 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4363 should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4363 is in the power-down mode until MCKI and LRCK are input.

When the register data of CKS2-0 or DFS1-0 is changed during normal operation, the AK4363 should be reset by PDN pin "L" or RSTN bit "0".

FS1	FS0	DFS1-0			
		"11" (Half speed)	"00" (Normal speed)	"01" (Double speed)	
1	0	16	32	64	
0	0	22.05	**44.1**	88.2	default (DFS1-0 = "00")
0	1	24	48	96	

Table 1. Sampling Frequency [kHz] (FS1-0 = "11", DFS1-0 = "10": reserved)

CKS2	CKS1	CKS0	DFS1-0			
			"11" (Half speed)	"00" (Normal speed)	"01" (Double speed)	
0	0	0	512fs	**256fs**	128fs	default (DFS1-0 = "00")
0	0	1	256fs	256fs	256fs	
0	1	0	768fs	384fs	192fs	
0	1	1	384fs	384fs	384fs	
1	0	0	1024fs	512fs	256fs	
1	0	1	512fs	512fs	N/A	
1	1	0	1536fs	768fs	384fs	
1	1	1	768fs	768fs	N/A	

Table 2. System Clock (DFS1-0 = "10": reserved)

fs [kHz]	Mode	128fs	192fs	256fs	384fs	512fs	768fs	1024fs	1536fs
16	Half	-	-	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760
32	Normal	-	-	8.1920	12.2880	16.3840	24.5760	-	-
64	Double	8.1920	12.2880	16.3840	24.5760	-	-	-	-
22.05	Half	-	-	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688
44.1	Normal	-	-	11.2896	16.9344	22.5792	33.8688	-	-
88.2	Double	11.2896	16.9344	22.5792	33.8688	-	-	-	-
24	Half	-	-	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640
48	Normal	-	-	12.2880	18.4320	24.5760	36.8640	-	-
96	Double	12.2880	18.4320	24.5760	36.8640	-	-	-	-

Table 3. Example of System Clock [MHz]

■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. 6 serial data modes are supported and selected by register data of DIF2-0 as shown in Table 4. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 4 can be used for 20, 18 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI	L/R	BICK	
0	0	0	0	16bit, LSB justified	H/L	≥32fs	
1	0	0	1	18bit, LSB justified	H/L	≥36fs	
2	0	1	0	20bit, LSB justified	H/L	≥40fs	
3	0	1	1	24bit, LSB justified	H/L	≥48fs	
4	1	0	0	24bit, MSB justified	H/L	≥48fs	
5	1	0	1	I^2S	L/H	≥48fs	default
6	1	1	0	Reserved			
7	1	1	1	Reserved			

Table 4. Audio Data Format

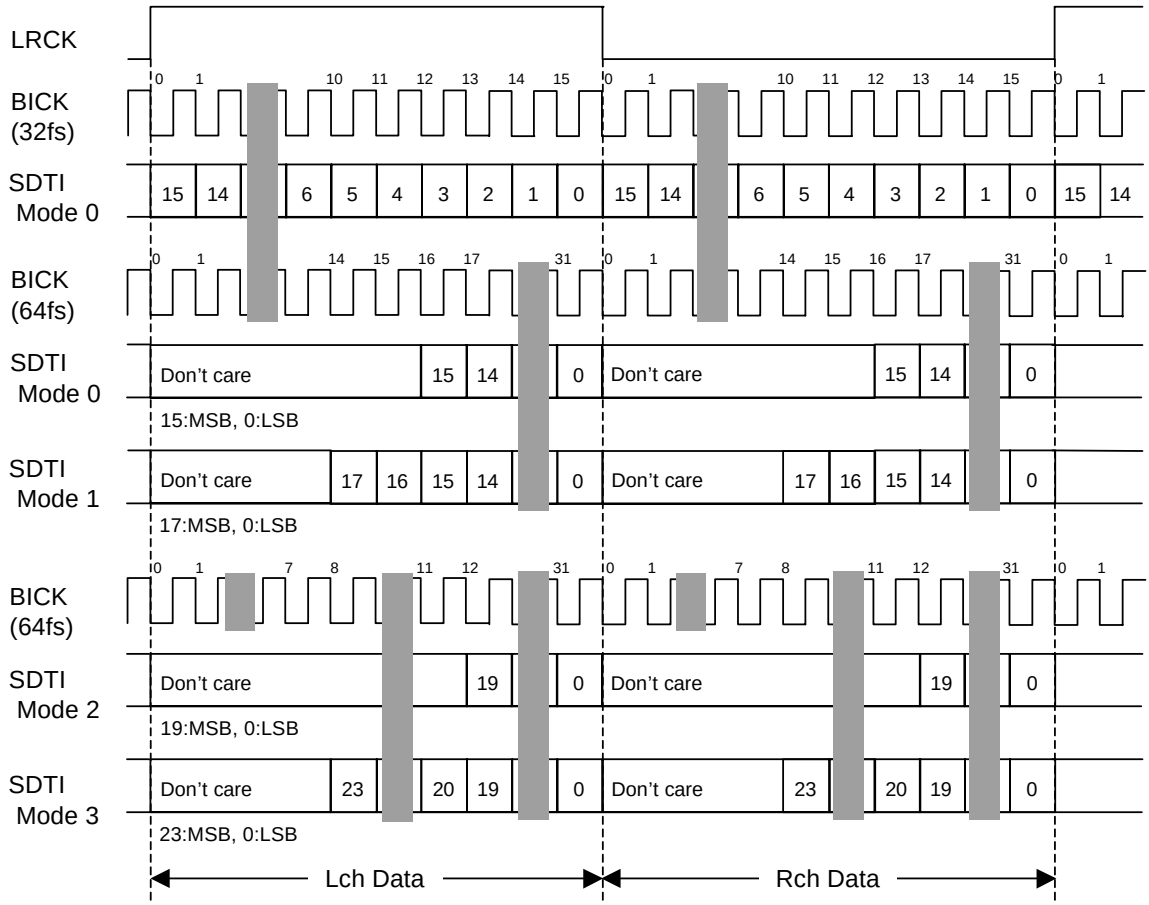


Figure 3. Mode 0-3 Timing

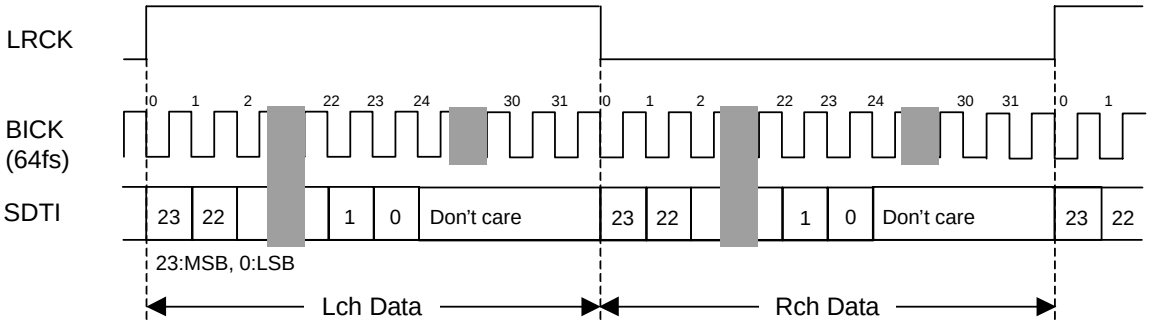


Figure 4. Mode 4 Timing

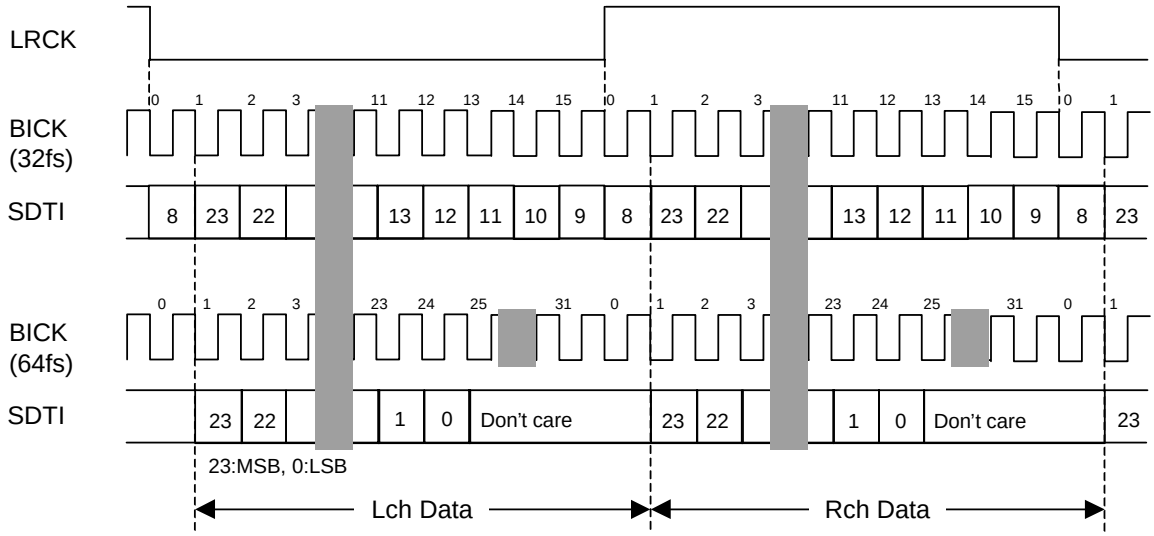


Figure 5. Mode 5 Timing

■ De-emphasis filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling speed (tc=50/15μs). It is enabled or disabled with the control register data of DEM1-0 and DFS1-0. The de-emphasis filter is disabled at half/double sampling mode.

DEM1	DEM0	De-emphasis	
0	0	44.1kHz	
0	1	OFF	default
1	0	48kHz	
1	1	32kHz	

Table 5. De-emphasis filter control with DEM1-0 (DFS1-0 = "00")

DFS1	DFS0	De-emphasis	
0	0	See Table 5.	default
0	1	OFF	
1	0	OFF	
1	1	OFF	

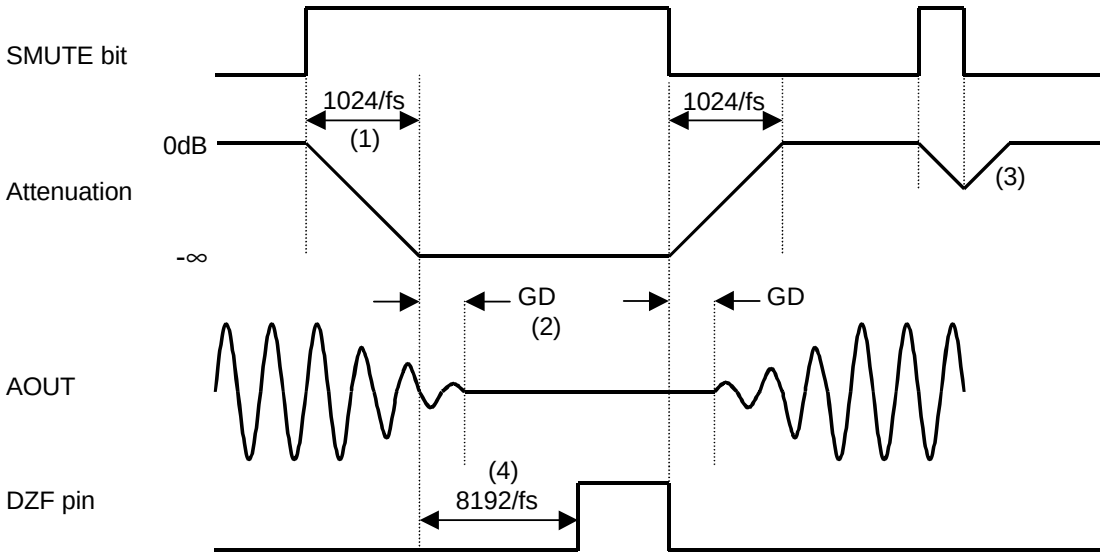
Table 6. De-emphasis filter control with DFS1-0

■ Zero detection

When the input data at both channels is continuously zeros for 8192 LRCK cycles, DZF pin goes to "H". DZF pin immediately goes to "L" if input data is not zero after going DZF "H". If RSTN bit becomes "0", DZF pin goes to "H". DZF pin goes to "L" at 4~5/fs after RSTN bit returns to "1".

■ Soft mute operation

Soft mute operation is performed at digital domain. When the serial control register data of SMUTE goes "1", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

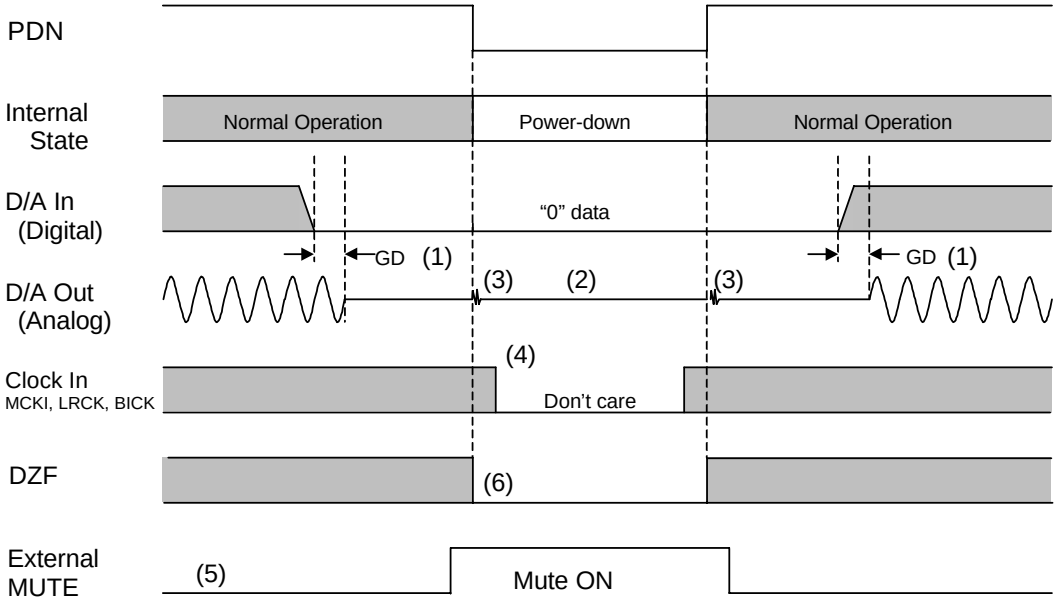


Notes:
(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input have the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
(4) When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF pin goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

Figure 6. Soft mute and zero detection

■ Power-down

The DAC is placed in the power-down mode by bringing PDN pin "L" and the digital filter is also reset at the same time. The internal register values are initialized by PDN "L". This reset should always be done after power-up. Because some click noise occurs at the edge of PDN, the analog output should be muted externally if the click noise influences system application.



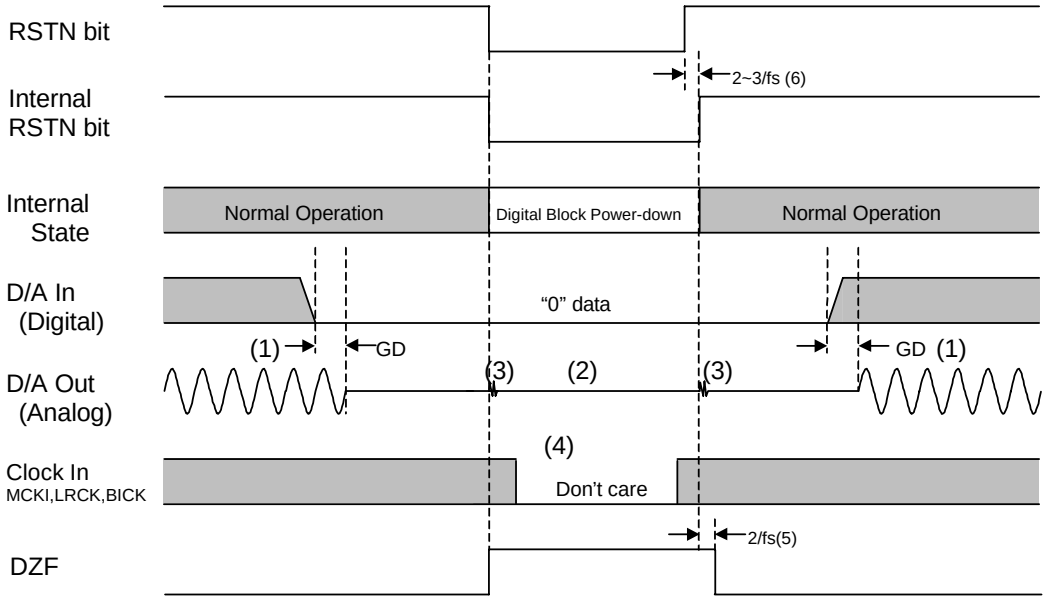
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCKI, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.
(6) DZF pin is "L" in the power-down mode (PDN = "L").

Figure 7. Power-down/up sequence example

■ Reset function

When RSTN = "0", the DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZF pin goes to "H". Figure 8 shows the sequence of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCKI, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pin goes to "H" when the RSTN bit becomes "0", and goes to "L" at 4~5/fs after RSTN bit becomes "1".
(6) There is a delay, 2~3/fs from RSTN bit "1" to the internal RSTN "1".

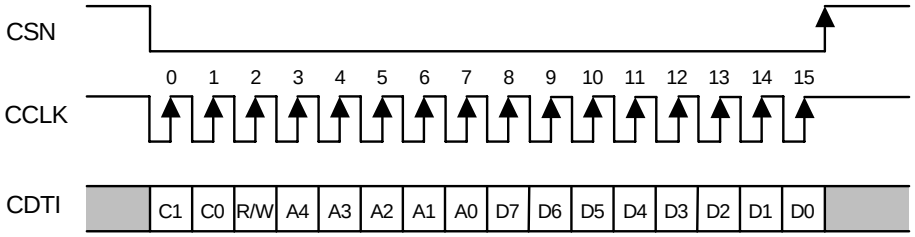
Figure 8. Reset sequence example

■ Serial Control Interface

The AK4363 can control its functions via registers. Internal registers may be written by 2 types of control mode. The chip address is determined by the state of the CAD0 and CAD1 inputs. PDN = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit. But in this case, the register data is not be initialized.

(1) 3-wire Serial Control Mode (I2C = "L")

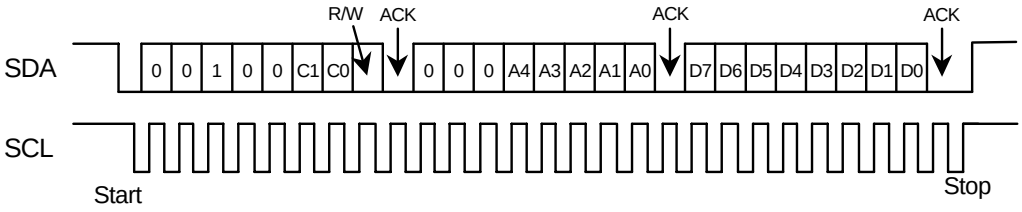
Internal registers may be written to the 3 wire µP interface pins (CSN,CCLK and CDTI). The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit, Fixed to "1"; Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max). The CSN and CCLK pins should be held to "H" except for access.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "1" : Write only)
A4-A0: Register Address
D7-D0: Control Data

(2) I^2C Bus Control Mode (I2C = "H")

Internal registers may be written to I^2C Bus interface pins: SCL & SDA. The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit, Fixed to "0"; Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of SCL and data is clocked out on the falling edge. Data can be written after a high-to-low transition of SDA when SCL is "H"(start condition), and is latched after a low-to-high transition of SDA when SCL is "H"(stop condition). The clock speed of SCL is 100kHz(max). The CSN pin should be connected to DVDD at I^2C Bus control mode. The AK4363 does not have a register address auto increment capability.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "0" : Write only)
A4-A0: Register Address
D7-D0: Control Data
ACK: Acknowledge

* When the AK4363 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Mapping of Program Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	EXT	DIF2	DIF1	DIF0	RSTN
01H	Control 2	FS1	FS0	DFS1	DFS0	CKS2	CKS1	CKS0	RSTN
02H	Control 3	PL3	PL2	PL1	PL0	DEM1	DEM0	ATC	SMUTE
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Note: For addresses from 05H to 1FH, data should not be written.
When PDN goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset, DZF pin goes to “H” and registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	EXT	DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	1	0	1	1

RSTN: Internal timing reset
0: Reset. DZF pin goes to “H” and registers are not initialized.
1: Normal operation
When the states of DIF2-0,EXT,CKS2-0,DFS1-0 or FS1-0 changes, the AK4363 should be reset by PDN pin or RSTN bit. Some click noise may occur at that timing.

DIF2-0: Audio data interface modes (See Table 4.)
Initial: “000”, Mode 0

EXT: Master clock select
0: PLL mode (27MHz clock input)
1: External clock mode. Internal VCO is powered down.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	FS1	FS0	DFS1	DFS0	CKS2	CKS1	CKS0	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. DZF pin goes to “H” and registers are not initialized.
1: Normal operation
When the states of DIF2-0,EXT,CKS2-0,DFS1-0 or FS1-0 changes, the AK4363 should be reset by PDN pin or RSTN bit. Some click noise may occur at that timing.

CKS2-0: Clock select (See Table 2.)
Initial: “000”

DFS1-0: Half/Normal/Double sampling modes (See Table 1,2), De-emphasis response (See Table 6.)
Initial: “00”

FS1-0: Sampling frequency modes (See Table 1.)
Initial: “00”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	PL3	PL2	PL1	PL0	DEM1	DEM0	ATC	SMUTE
Default		1	0	0	1	0	1	0	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

ATC: Attenuation Control
0: The attenuation data for each register is applied separately to left and right channels.
1: The attenuation data loaded in addr=03H is used for both left and right channels.

DEM1-0: De-emphases response (See Table 5,6.)
Initial: “01”, OFF

PL3-0: Mixing mode

PL3	PL2	PL1	PL0	Lch Output	Rch Output	Note	
0	0	0	0	MUTE	MUTE	MUTE	
0	0	0	1	MUTE	R		
0	0	1	0	MUTE	L		
0	0	1	1	MUTE	(L+R)/2		
0	1	0	0	R	MUTE		
0	1	0	1	R	R		
0	1	1	0	R	L	REVERSE	
0	1	1	1	R	(L+R)/2		
1	0	0	0	L	MUTE		
1	0	0	1	L	R	STEREO	default
1	0	1	0	L	L		
1	0	1	1	L	(L+R)/2		
1	1	0	0	(L+R)/2	MUTE		
1	1	0	1	(L+R)/2	R		
1	1	1	0	(L+R)/2	L		
1	1	1	1	(L+R)/2	(L+R)/2	MONO	

Table 7. Programmable Output Format

STEREO: Normal stereo output
REVERSE: L/R Reverse output
MONO: Monaural output
MUTE: Soft mute operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

Equation of attenuation level: ATT = 20 x Log_{10} (Binary level / 255) [dB]

FFH: 0dB

:

01H: -48.1dB

00H: Mute

The transition between ATT values is same as soft mute operation. When current value is ATT1 and new value is set as ATT2, ATT1 gradually becomes ATT2 with same operation as soft mute. If new value is set as ATT3 before reaching ATT2, ATT value gradually becomes ATT3 from the way of transition.

Cycle time of soft mute: Ts=1024/fs

When PDN pin goes to “L”, the ATT values are set to 00H. The ATT values fade to FFH(0dB) during Ts after PDN pin returns to “H”.

When RSTN bit goes to “0”, the ATT values are set to 00H. The ATT values fade to their current values after RSTN bit returns to “1”.

Digital attenuator is independent of soft mute function.

SYSTEM DESIGN

Figure 9 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Condition: AVDD=DVDD=5V(TTL mode), PLL mode, I2C mode, Chip Address = "00"

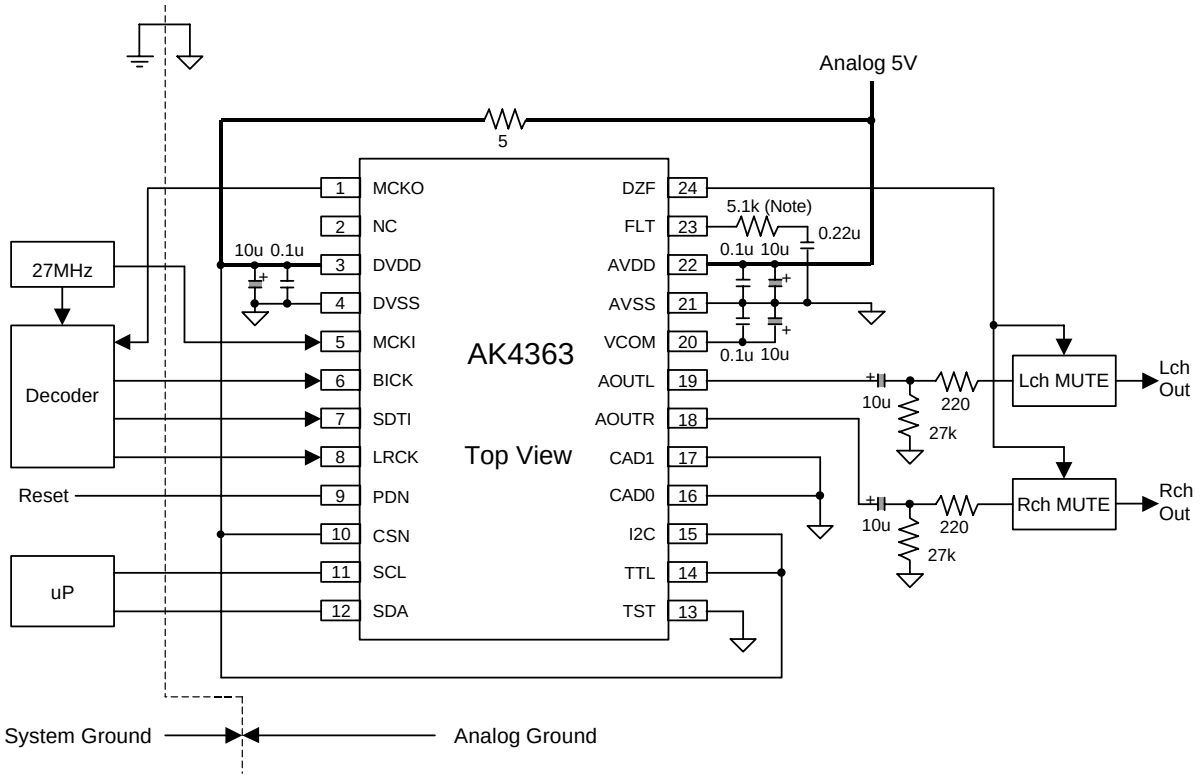


Figure 9. Typical Connection Diagram

Note: This resister can be changed to 10kΩ if the distortion at low frequency (around 1kHz) is critical. However the distortion at high frequency degrades in this case.

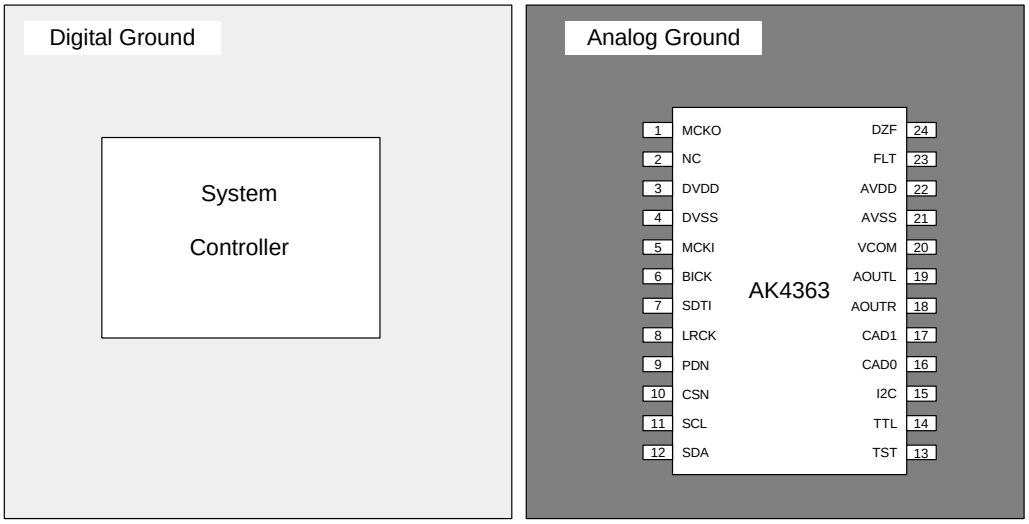


Figure 10. Ground Layout

Note: AVSS and DVSS must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4363 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from analog supply in system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4363 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be near to the AK4363 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference Inputs

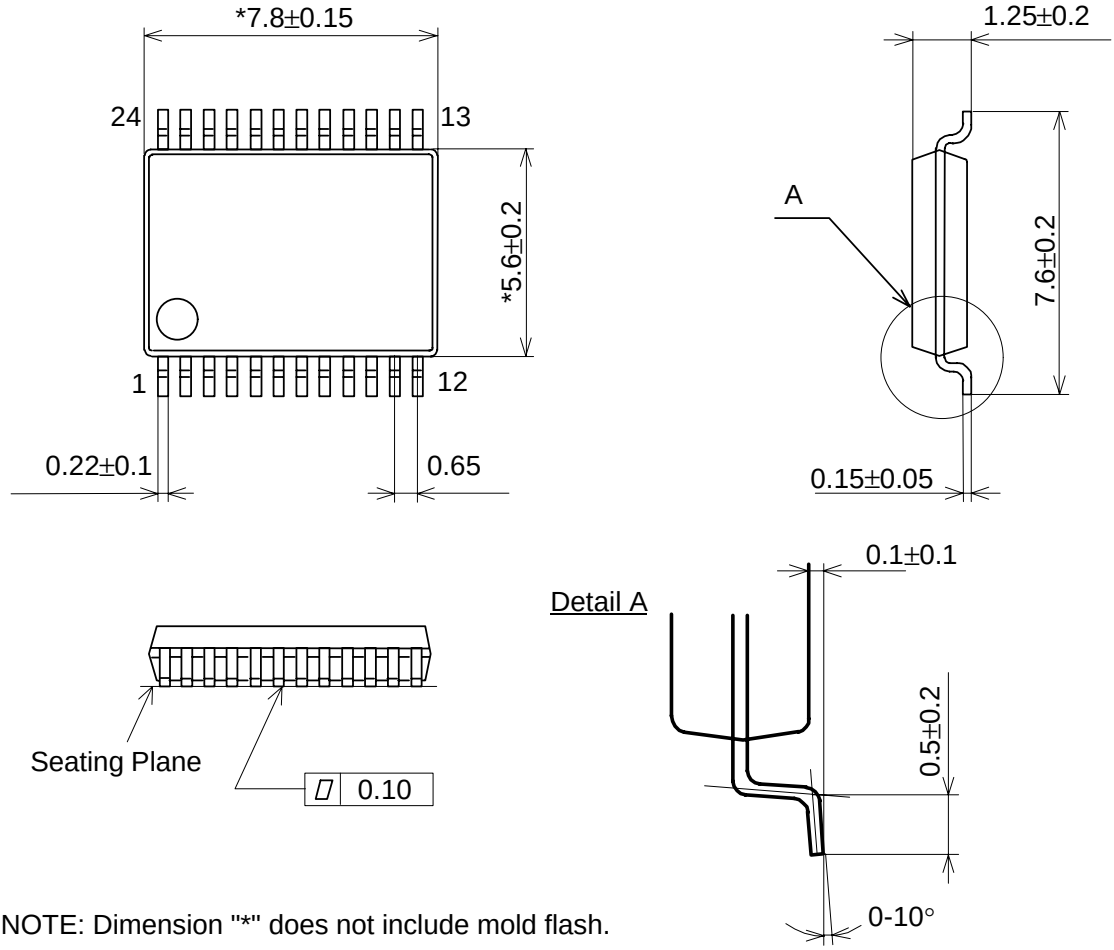
The differential voltage between AVDD and AVSS sets the analog output range. VCOM is AVDD/2 and normally connected to AVDD with a 0.1µF ceramic capacitor. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4363.

3. Analog Outputs

The analog outputs are single-ended outputs and 0.6x(AVDD-AVSS) Vpp (typ) centered around the VCOM voltage. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFF(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is 0V for 000000H(@24bit).

PACKAGE

24pin VSOP (Unit: mm)

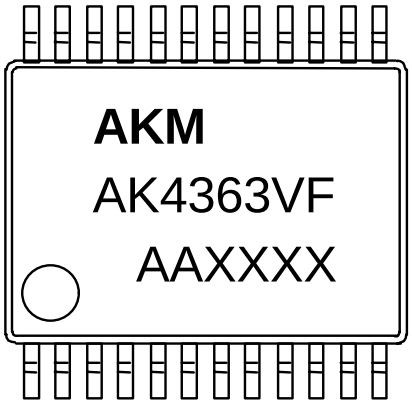


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXX
AA: Lot#
XXXX: Date Code

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.