# Technical Reference Note
# AIF - PFC Power Factor Correction Series

## *AIF - PFC 1600W AC-DC Converter Module*

The PFC Power Factor Correction module is part of Astec's family of advanced High Density modular power supply components. Featuring high reliability and convenient control and monitoring functions, these modules are designed to reduce product development time and enhance system performance. The PFC is designed to work over all typical line voltages used worldwide, and provide unity power factor with very low levels of harmonic distortion in line current. The PFC includes active start-up current control. Power Line Disturbance (PLD) circuitry copes with a wide range of input voltage fluctuations..



## Special Features

- **Unity Power Factor**
- **DC input (Configurable)**
- **High Efficiency - up to 95%**
- **Universal input voltage and frequency range**
- **Up to 1600W output power**
- **Parallelable with current sharing within 10%**
- **< 10% harmonic distortion conforming to IEC 1000-3-2 Compliance**
- **100°C baseplate operating temperature.**
- **High Reliability - over 1 million hours MTBF @ baseplate temperature 50°C**
- **Programmable Power Fail Warning Signal**
- **EEPROM data storage via $I^2C$ interface**
- **Power Density up to 290W/$in^3$**
- **Switching Frequency 125KHz**

## Environmental Specifications

- **Operating temperature: -20°C to +100°C (baseplate)**
- **Storage temperature: -40°C to +110°C**
- **Meet power line disturbance immunity specification per IEC 61000-4-11 " Generic Immunity Standards against voltage dips, interruptions"**
- **Pb-free reflow compatible and ROHS Compliant**

## Electrical Parameters

### Input

| | |
|---|---|
| **Input range** | **85 – 264 VAC** |
| | **120 - 370VDC (Configurable)** |
| **Input Surge** | **290Vac / 1s** |
| **Efficiency** | **95%@ 230Vac, 1600W (Typical)** |
| **Total Harmonic Distortion** | **10%** |

### Control

**Enable TTL compatible**
**(Positive & negative enable options)**

### Output

| | |
|---|---|
| **Output Voltage** | |
| **Io =4.2A / Vi > 180Vac** | **380V typ** |
| **Io = 0** | **393V typ** |
| **Maximum output Power** | |
| **85Vac ≤ Vin ≤ 120Vac** | **1000W** |
| **120Vac < Vin < 220Vac** | **See P. 16** |
| **Vin ≥ 220Vac** | **1600W** |
| **Output voltage Adjust range** | **76% - 100% of nominal output** |
| **Overvoltage Protection** | **430V** |

## Safety

| | |
|---|---|
| **UL, cUL** | **60950 Recognized** |
| **TUV** | **EN60950 Licensed** |

AIF - PFC SERIES
THIS SPECIFICATION COVERS THE REQUIREMENTS
FOR A New Full Brick 1600W AC/DC Converter

| MODEL NAME | Vout,Iout |
|---|---|
| AIF04ZPFC-01L | 380V, 4.2A |
| AIF04ZPFC-01NL | 380V, 4.2A |
| AIF04ZPFC-02L | 380V, 4.2A |
| AIF04ZPFC-02NL | 380V, 4.2A |
| AIF04ZPFC-01NTL | 380V, 4.2A |
| AIF04ZPFC-01NNTL | 380V, 4.2A |
| AIF04ZPFC-02NTL | 380V, 4.2A |
| AIF04ZPFC-02NNTL | 380V, 4.2A |

* 1600W max

| Suffix | Option |
|---|---|
| **NL** | **Negative Logic Enable** |
| **L** | **Positive Logic Enable** |
| **NTL** | **Non-thread hole** |

## Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage and temperature conditions. Standard test condition on a single unit.

| | |
|---|---|
| Tambient: | 25°C |
| L1: | 115Vac, 220Vac |
| L2: | return pin for L1 |
| Enable: | Open |
| +Vout1: | connect to load |
| –Vout1: | connect to load (return) |
| Trim(Vadj): | connect to S GND |
| Output Cap: | 470uF x 2 |

### ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the specs. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

| Parameter | Device | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage: | | | | | | |
| Continuous: | All | $V_I$ | 85 | - | 264 | Vac |
| Surge Voltage (1 sec) | All | $V_I$ | | | 290 | Vac |
| Input Frequency | | | 47 | 50/60 | 63 | Hz |
| Operating Case Temperature | All | Tc | -20 | - | 100 | ºC |
| Start up Case Temperature | All | | -40 | | 100 | ºC |
| Storage Temperature | All | $T_{STG}$ | -40 | - | 110 | ºC |
| Operating Humidity | All | - | - | - | 95 | % |
| Isolation | | | | | | |
| Input to Baseplate | All | - | - | - | 2700 | Vdc |
| Output to Baseplate | | - | - | - | 2700 | Vdc |
| Baseplate Capacitance | | - | | - | 1300 | PF |

***CONTROL SIGNALS***

| Control Function | Conditions | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| TEMP MON - temperature monitor signal | | $V_{TEMP\ MON}$ Sensitivity | 9.8 | 10 | 10.2 | mV/°C |
| | | Source impedence | | 16 | | KΩ |
| V ADJ - voltage adjust* | Adjust using external resistor | Vo | 60 | | 100 | % $VO_{nom}$ |
| C MON - current monitor signal | IO = 4.2A | $I_{C\ MON}$ | 0.9 | 1 | 1.1 | mA |
| | IO = 20 to 100% IOrated | $I_O/I_{C\ MON}$ | | 4.2 | | A/mA |
| C SHARE - current share function** | C SHARE pins of modules in parallel connected | C SHARE accuracy | | ? % | ? 0 | $\%IO_{rated}$ |
| | | Max no. of units | | | 10 | |
| CLK OUT - clock output | | $V_{CLK\ OUT}$ | | 5 | | Vp-p |
| | CLK IN open | Clock freq. | 0.97 | 1 | 1.03 | MHz |
| | | Max fan out | | | 2 | |
| CLK IN - clock input | | VCLK IN | 4.5 | | 6 | Vp-p |
| | | Clock freq | 0.95 | 1 | 1.05 | MHz |
| PFW ADJ - power fail warning adjust | PFW ADJ=0 to 2.05 VDC | PFW set point | 195 | 205 | 215 | VDC |
| | PFW ADJ=3.2 VDC | PFW set point | 305 | 320 | 335 | VDC |
| | PFW ADJ = 3.40VDC | PFW set point | 325 | 340 | 355 | VDC |
| | | PFW ADJ current source | | 1 | | mA |
| PFW - power fail warning*** | Input Power OK, $I_{PFW} = 0$ | $V_{PFW}$ | 12 | 13.7 | 15 | V |
| | Input Power Fail, $I_{PFW} = 15mA$ | $V_{PFW}$ | 0 | 0.2 | 0.4 | V |
| | (PFW short to S_GND) | PFW current source | – | 2.9 | - | mA |
| LD ENABLE - load enable | Load enabled, ($I_{LD\ ENABLE} = 0$) | $V_{LD\ ENABLE}$ | 12 | 13.7 | 15 | V |
| | Load disabled, ($I_{LD\ ENABLE} = 15mA$) | $V_{LD\ ENABLE}$ | 0 | 0.2 | 0.4 | V |
| | LD ENABLE short to S_GND | LD ENABLE current source | – | 2.9 | - | mA |
| PF ENABLE - module enable*** | Negative Enable: | | | | | |
| | Module enabled | $V_{PF\ ENABLE}$ | 0 | | 0.8 | V |
| | Module disabled | $V_{PF\ ENABLE}$ | 2.2 | | 5 | V |
| | Positive Enable: | | | | | |
| | Module enabled | $V_{PF\ ENABLE}$ | 2.2 | | 5 | V |
| | Module disabled | $V_{PF\ ENABLE}$ | 0 | | 0.8 | V |
| | $V_{ENABLE} = 0.8V$ | PF ENABLE current source | | 400 | | µA |
| PV_AUX*** | $I_{PV\ AUX} = 0A$ | PV_AUX Voltage | | | 11 | V |
| | $I_{PV\ AUX} = 20mA$ | PV_AUX Voltage | 8 | | 9 | V |

* PFW is not valid when using voltage adjust feature
** For AIF04ZPFC-01L, total input current of all the modules must not exceed 16A rms
*** Only apply on primary side

## INPUT SPECIFICATIONS

| Parameter | Device | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | All | $V_I$ | 85 | | 264 | $V_{AC}$ |
| Input Current ($V_I$ = 115Vac, Load = 1000W) | | $I_{I,max}$ | - | - | 10 | A |
| Inrush Transient (Need external inrush limiting circuit) | | | - | | 20 | Apk |
| Power Factor | Po ≥ 500W<br>Po ≥ 1000W | | 0.96<br>0.98 | 0.97<br>0.99 | | |
| No Load Input Power ($V_I = V_{I,nom}$ ) | All | - | - | - | 3.8 | W |
| Total Harmonic Distortion (IEC1000-3-2) | All | - | - | - | 10 | % |

**Note:**

1) **Half cycle surge current due to input transient surge must be limited to 20A peak or less**
2) **Need external inrush limiting circuit**
3) **For AIF04ZPFC-01L, total input current for modules connected in parallel must not exceed 16A**
4) **For AIF04ZPFC-02L, negative rail input rectifiers must be provided by external circuitry. See P.24**
5) **Total harmonic distortion – input harmonics meet the requirements of IEC 1000-3-2**
6) **The PFC's LD ENABLE signal is recommended to be used to enable the load in case of initial surge load condition**

## OUTPUT SPECIFICATIONS

| Parameter | Device | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | | | | | | |
| Io = 4.2A / $V_I$ > 180V | | | 370 | 380 | | V |
| Io = 0 | | | | 393 | 400 | V |
| Maximum output power | | | | | | |
| For 85Vac ≤ VI ≤ 120Vac | | | | | 1000 | W |
| For VI > 220 Vac | | | | | 1600 | W |
| For 120Vac < VI < 220Vac | | | | | See P.17 | |
| Efficiency | | | | | | |
| VI = 115Vac, (1000W) | | | 90 | 92 | | % |
| VI = 230Vac, (1000W) | | | 92 | 94 | | % |
| VI = 230Vac, (1600W) | | | 92 | 95 | | % |
| Turn-On Time | | | | | | |
| VI = 115Vac | | | 0.5 | 2.5 | 4.0 | Sec |
| VI = 230Vac | | | 0.5 | 2.5 | 3.5 | Sec |
| External Output Capacitor | | | 470 | | 3000 | μ F |

## GENERAL SPECIFICATIONS

| Parameter | Device | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Calculated MTBF (Io = 2.6A ; $T_B$ = 40°C, MIL-217FN2) | All | - | - | 450K | - | Hours |
| Weight | All | - | - | 300 (9.6) | | g(oz.) |

## FEATURE SPECIFICATIONS

| Parameter | Device | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PF ENABLE Interface : | | | | | | |
| Positive Logic – No suffix | | | | | | |
| Low Logic – Module Off | All | $V_{enable}$ | 0 | | 0.8 | V |
| High Logic – Module On | All | $V_{enable}$ | 2 | | 5 | V |
| Negative Logic – Suffix "N" | | | | | | |
| Low Logic – Module On | All | $V_{enable}$ | 0 | | 0.8 | V |
| High Logic – Module Off | All | $V_{enable}$ | 2 | | 5 | V |
| Enable current source (Venable = 0.8V) | All | | | | 400 | µA |
| Output Voltage Adjustment Range | | - | 76 | - | 100 | %Vo |
| Output Overvoltage Shutdown (latch off) | All | | 420 | | 430 | V |
| Output ripple Vin = 115Vac, Vo = 380V, Io = 2.6A | | | 11 | | | Vp-p |
| Undervoltage Lockout | | | | | | |
| Turn-on Point | All | - | 79 | | 84.5 | V |
| Turn-off Point | All | - | 57 | | 62 | V |
| Overtemperature shutdown (Baseplate temperature) | All | | 105 | | 120 | °C |

## Function Description

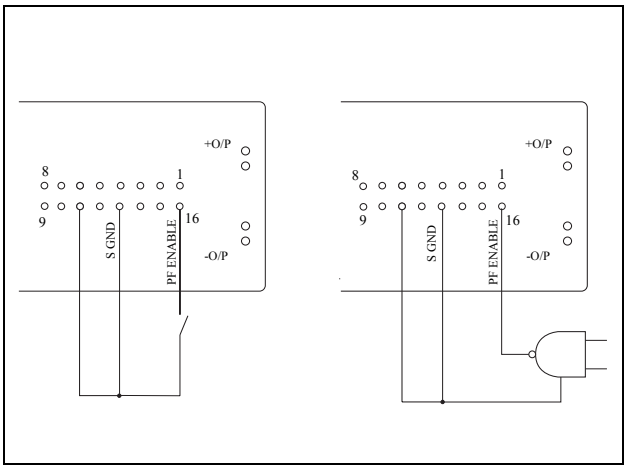
This section explains how to implement the functions found on the AIF - PFC Series. All signals are on primary side.

### PFC Enable Input (PF ENABLE)

The enable pin is a TTL compatible input used to turn the output of the module on or off.

For module with no suffix, the output is enabled when the PF ENABLE (pin 16) is open or driven to a logic high > 2.2V. The output is disabled when the PF ENABLE is connected to S GND (pin 13) or driven to a logic low of < 0.8V (but not negative).

For module with suffix "N", the output is enabled when the PF ENABLE is connected to S GND or driven to a logic low < 0.8V (but not negative). The output is disabled when the PF ENABLE is open or driven to a logic high > 2.2V.




### S GND (Signal Ground)

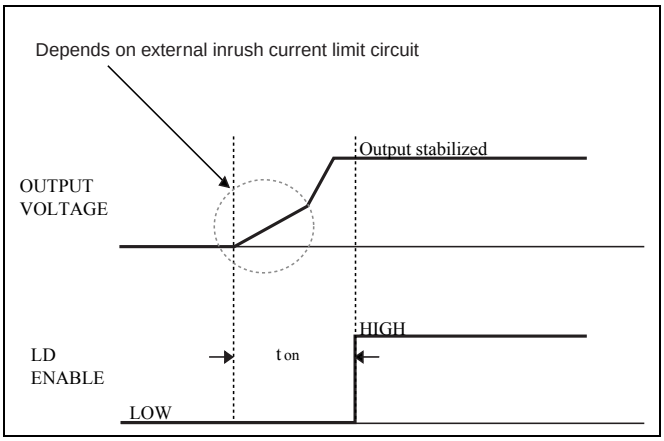
The S GND pin is connected to the internal common ground of the module. It is also internally connected to the –O/P terminals.

NOTE:

When connecting S GND to external circuitry care must be taken to ensure that the current flowing through this pin is kept below 25mA.

## DC-DC Converter Module Enable Output (LD ENABLE)

After the PFC power up sequence, the power to the load can be enabled. This can be performed manually or the PFC can automatically enable the load using the LD ENABLE signal.

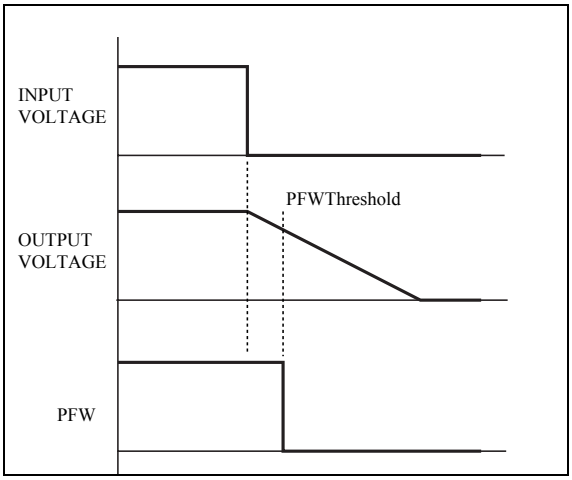



Initially the load is disabled and the LD ENABLE (pin 15) is at 0.4V (LOW). When the PFC power up sequence has completed, the LD ENABLE voltage goes HIGH. And the LD ENABLE will stay high as long as Vin is above 175Vac or Vout is above 250V, even if PF_ENABLE is in disable mode**. (Please see the application example section at P.25 for the external circuit to interlock the LD-ENABLE from PF_ENABLE)**

The LD ENABLE pin is capable of delivering 2.7mA at 1.5V when HIGH. See electrical specifications for exact figures.

## Power Fail Warning

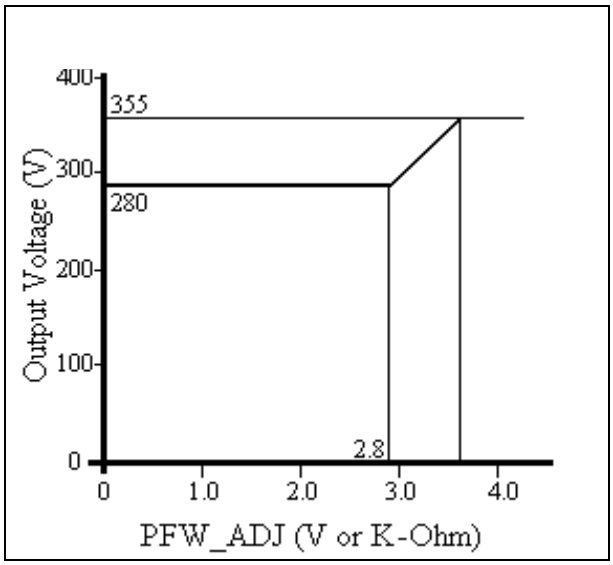
If output voltage can not be maintained at the pre-programmed PFW threshold voltage, the PFW (pin 14) will go from HIGH to LOW.




The output of the PFW signal can drive an opto-coupler to provide an isolated signal from primary side to the secondary side. The nominal factory set PFW threshold is set at 340V.

## Power Fail Warning Adjust

The level at which a Power Fail Warning occurs can be programmed using the PFW Adjust input (pin 12). If the pin is left unconnected then the PFW operates at the default factory set value.

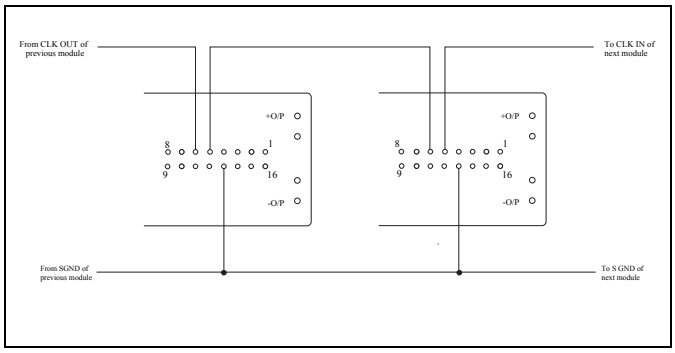



The output from the PFW ADJ pin is a 1mA current source. To adjust the PFW threshold, a voltage source (0 – 4Volts) or a programming resistance (0 – 4Kohm) referenced to s S GND (pin 13) should be connected. This allows adjustment of the PFW threshold from 280V up to 340V. The value of resistance or voltage required can be read from the graph above.

## Clock Signals (CLK IN, CLK OUT)

The PFC's internal clock is accurate and stable over its full operating range and synchronization is not normally required, but it can reduce noise in paralleled systems.

Clock signals can be wired in series (the CLK OUT pin of one module to the CLK IN pin of the next etc) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of TTL level at 1MHz ± 10% can be connected to the CLK IN pins of all the modules.



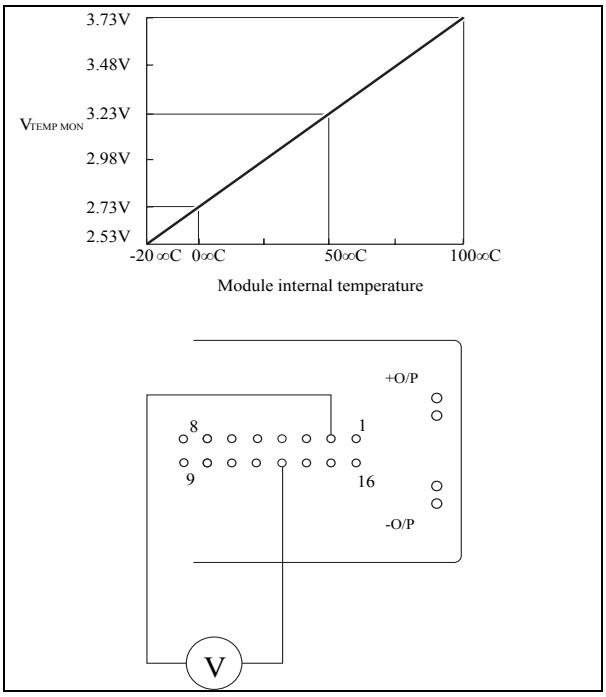

If the clock input to any module fails, the module will automatically switch back to its internal clock and will continue to operate at full power even in current sharing systems.. The CLK IN and CLK OUT signals are AC coupled.

## Temperature Monitoring (TEMP MON)

The TEMP MON pin provides an indication of the module's internal temperature. The voltage at the TEMP MON pin is proportional to the temperature of the module baseplate at 10mV per °C, where:

Module temperature (°C) = (Vtemp mon X 100) - 273

The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for overtemperature warning circuits and for thermal design verification of prototype power supplies and heatsink.



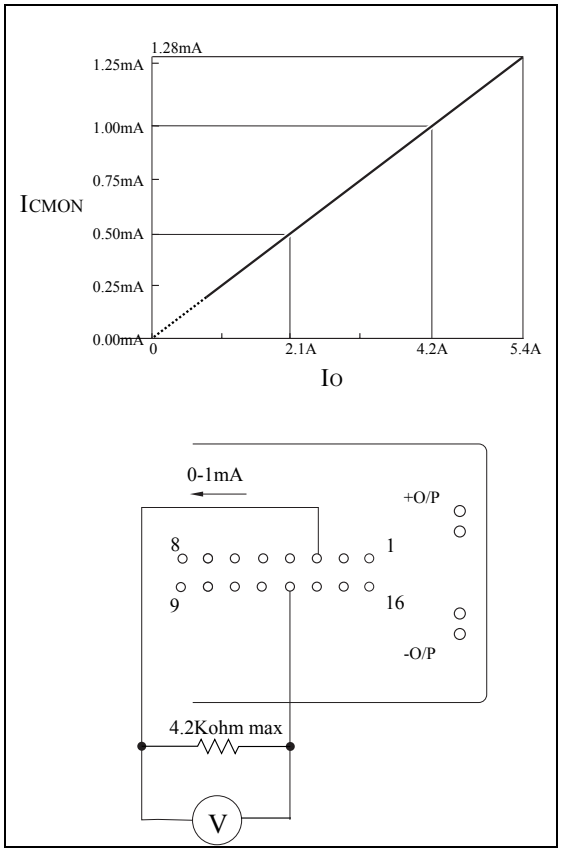
## Current Monitoring (C MON)

The C MON pin provides an indication of the amount of current supplied by the module. The output of the C MON pin is a current source proportional to the output current of the module,

where $I_O / I_{CMON} = 4.2A/1mA$

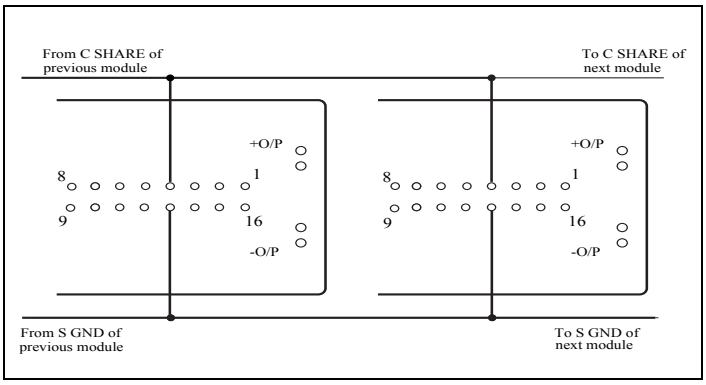
If a 4.2K Ohm resistor is connected then the voltage in Volts on the C MON pin is directly equivalent to the current supplied by the module in Amps.

Maximum voltage on C MON is 6V



## Current Sharing (C SHARE)

To ensure that all modules in a parallel system accurately share current, the C SHARE pins on each module should be connected together.

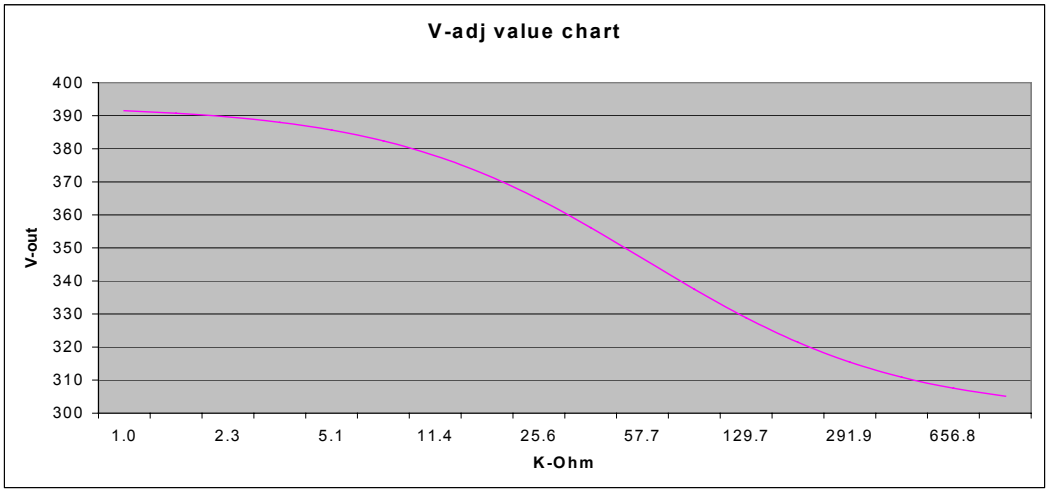


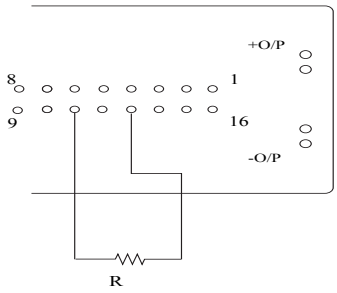

The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing even under variable or light load conditions.

**Note:** 1) The S GND pins of each module must also be connected together to ensure accurate current sharing.
2) Current flow to S GND must less than 25mA

## Output Voltage Adjust (V ADJ)

The output voltage of the module may be accurately adjusted from 76% to 100% of the nominal output voltage. Adjustment can be made using a resistor connected as below.

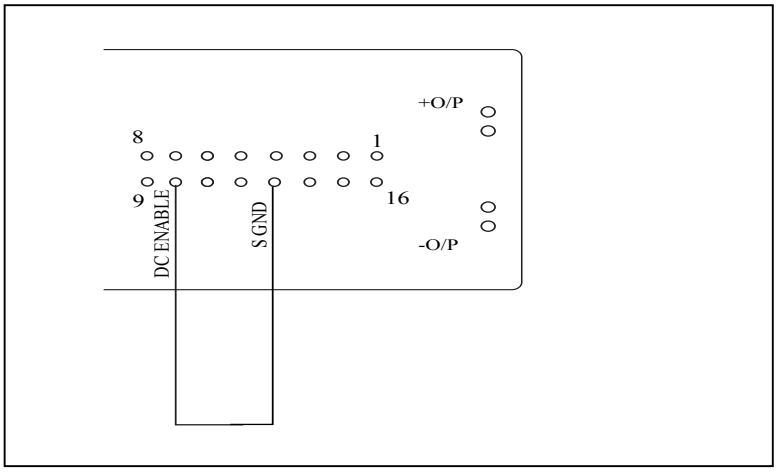



**Vout = Vr * (1 + Rh * ( 1 / (Rj + R) + 1 / Rw)) + 10.94**

**Where**
**R is the resistor connected between the Vadj pin to S_GND (units in kOhm)**
**Vr = 5.029**
**Rh = 1084**
**Rw = 19.2**
**Rj = 58.5**

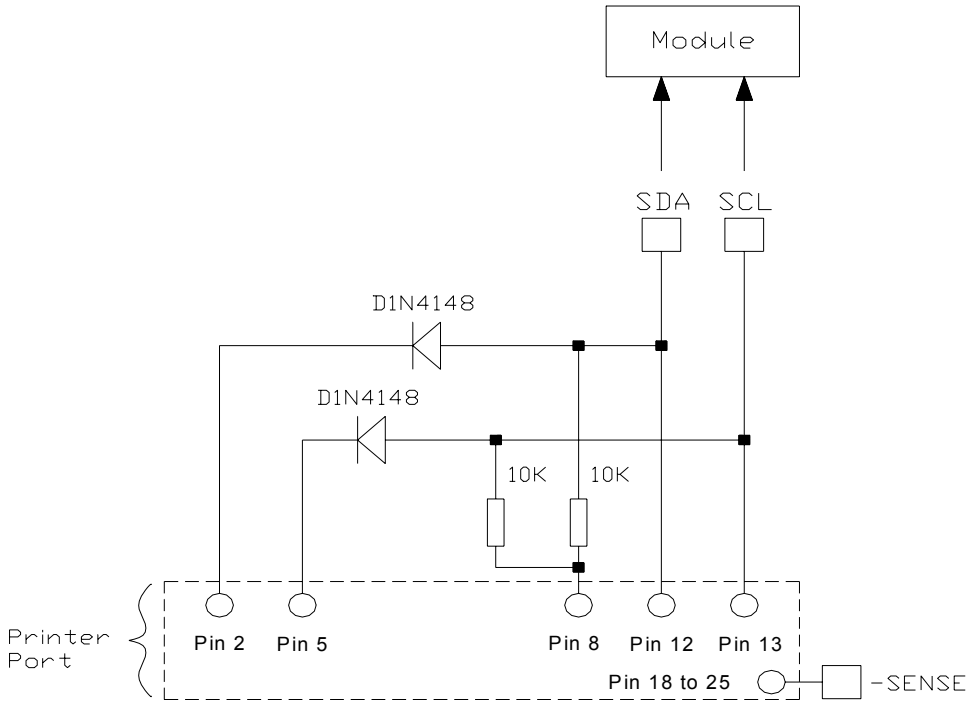
## DC ENABLE




For using DC input, connect the DC ENABLE pin to S GND

## I²C EEPROM Content Programming (SDA, SCL)

This function is provided for product information storage, template as per customer define.
Connect RS232 (Printer Port) from PC to Test unit at 300Vdc in and test with Read/Write capability of the I²C EEPROM.




**EEPROM CONTENT**

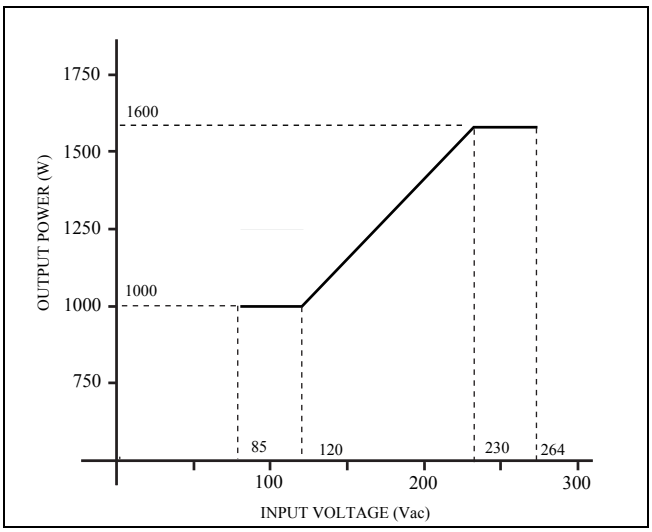
The module is equipped with a 256 byte EEPROM, 24LC2BT-E/ST or equivalent. This device will be programmed during the manufacturing process. The EEPROM content will include the following information:

- Manufacturer name string " ASTEC"
- Product name and product number
- Serial number assigned by manufacturer
- Max output power

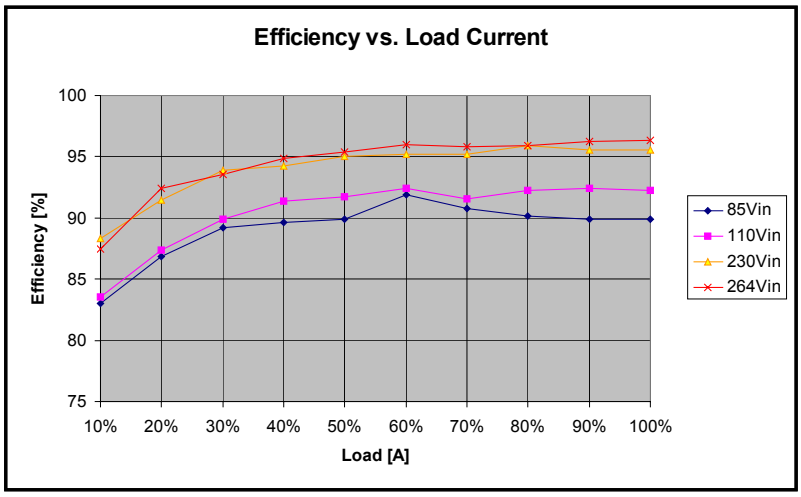
## DESIGN CONSIDERATIONS

### Maximum Output Power Vs Input Voltage

The maximum output power available varies with the input voltage as shown below.




### Efficiency Vs Input Voltage and Output Power



## Input Undervoltage Protection

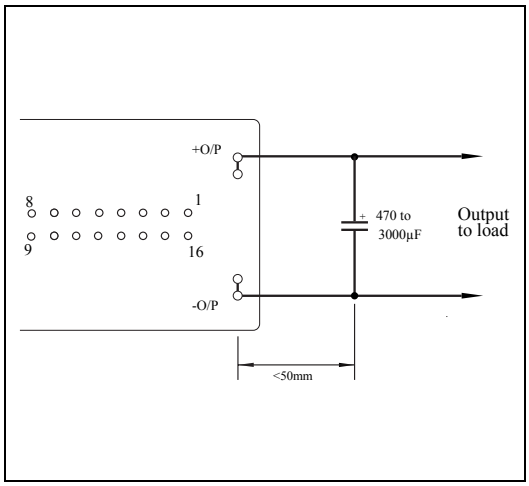
An input undervoltage protection circuit protects the module under low input voltage conditions. Hysteresis is built into the PFC Series module to allow for high levels of variation on the input supply voltage without causing the module to cycle on and off. PFC modules will operate when the input exceeds 85Vac and turn off below 63Vac.

## Input Fusing

ASTEC modules do not have an in-line fuse fitted internally. In order to comply with CSA, VDE and UL safety regulations it is recommended that a fuse of 250Vac, 15A be fitted at the module's input.

## Output Capacitor

The PFC requires an output hold-up capacitor of between 470uF and 3000uF to prevent the module from disabling due to fluctuations in output voltage. Ideally the capacitor should be connected directly to the PFC output pins. If this is not possible the connection must be less than 50mm from the pins.




**Selecting an External Output Capacitor**

The output capacitor value is determined by the following factors :
1. RMS ripple current.
2. Peak-to-peak output ripple voltage.
3. Hold-up time.
4. Expected lifetime of the capacitor.

**RMS ripple current**

The maximum permissible rms ripple current for the output capacitor should be greater than the rms ripple current for the application. The ripple current for the PFC module can be approximated as

$$I_{rms} = (P_O/Eff) \times 1/\sqrt{(V_O \times V_{rms})}$$

where :
$P_O$ = output power (W)
Eff = efficiency
$V_O$ = output voltage (V)
$V_{rms}$ = input rms voltage (V)

This gives the ripple current at 125KHz. The maximum ripple current for capacitors is usually specified at 120Hz. To convert from 125KHz to 120Hz the Irms figure should be divided by 1.3 .

**Peak to Peak Output Ripple Voltage**

The ac input causes a ripple on the output voltage. The size of the ripple is inversely proportional to the size of the capacitor. Therefore the maximum allowable ripple voltage should be decided in order to calculate the size of capacitor required. This may be calculated using the following equation:

$$C_O = P_O / (2\pi f \times Eff \times V_O \times V_{ripple})$$

where :
$C_O$ = output capacitance (µF)
Eff = efficiency
f = input voltage frequency (Hz)
$V_O$ = output voltage (V)
$V_{ripple}$ = output ripple voltage (V)

**Hold-Up Time Requirement**

The output capacitor value is different for different hold-up time requirements. The minimum capacitance corresponding to the required hold-up time of a system comprised of ASTEC DC/DC power modules and an PFC module can be calculated as follows:

$$C_{O\,min} = (2 \times P_O \times T_{hold})/[(V_O - V_{ripple})^2 - (V_{min})^2]$$

where :
$C_{O\,min}$ = output capacitance (µF)
$P_O$ = output power (W)
$T_{hold}$ = hold up time (sec)
$V_O$ = output voltage (V)

$V_{ripple}$ = output ripple voltage (V)
$V_{min}$ = minimum input voltage for DC/DC module

For example:

A PFC module driving 3 AIF80A300 400W modules @ 5V. Efficiency of the AIF80A300 module is 88%, the minimum input voltage is 250V, the output voltage of the PFC is 380V, the required hold-up time is 20mS and the peak-to-peak voltage $V_{ripple}$ is chosen to be 16V.

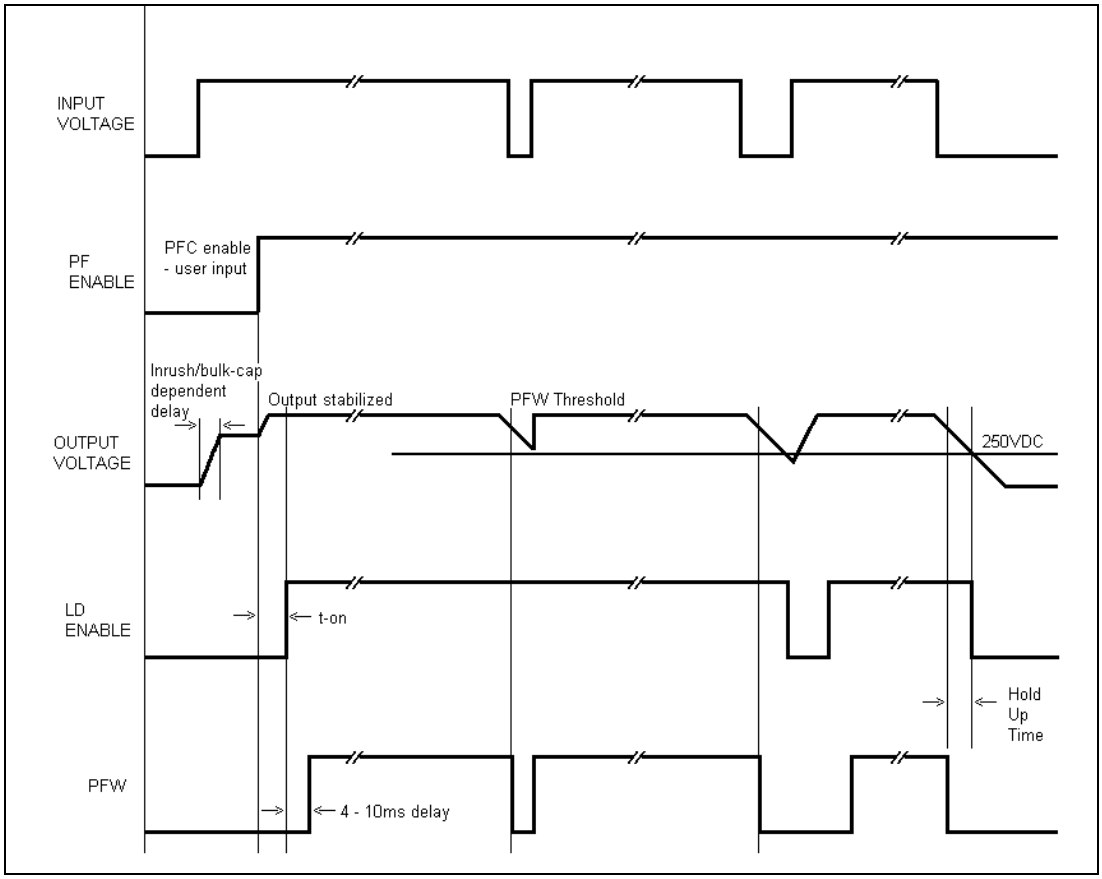
$$C_{O\ min} = \frac{2 \times (3 \times 400/0.88) \times 0.02}{[(380-16)^2-250^2]} = 390\mu F \quad (470\ \mu F \pm 20\%)$$

This figure is the minimum capacitance. To allow for capacitor tolerances and aging effects the actual value should generally be around 1.5 times greater.

## PF & Load Enable Connections and Timing

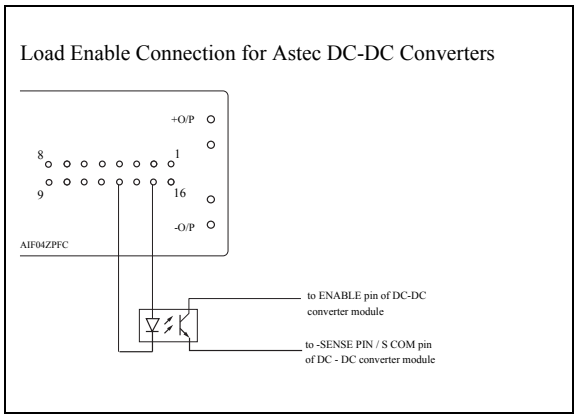
The PFC module must be supplied with a PF ENABLE signal to initiate the start-up sequence. The output of the LD ENABLE pin goes HIGH (ON) once the PFC has completed the start-up sequence.

It is recommended that the LD ENABLE signals is always used to enable the load, however, if the load is to be enabled manually it is essential that the ton time has expired before enabling occurs.



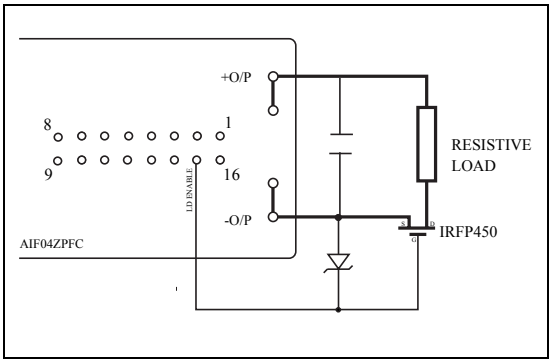
## Connections to enable Astec DC-DC converters.

The output from the PFC's LD ENABLE (pin 13) can directly drive an opto-coupler to provide an isolated signal to enable the power output of one or more Astec DC-DC converter modules.



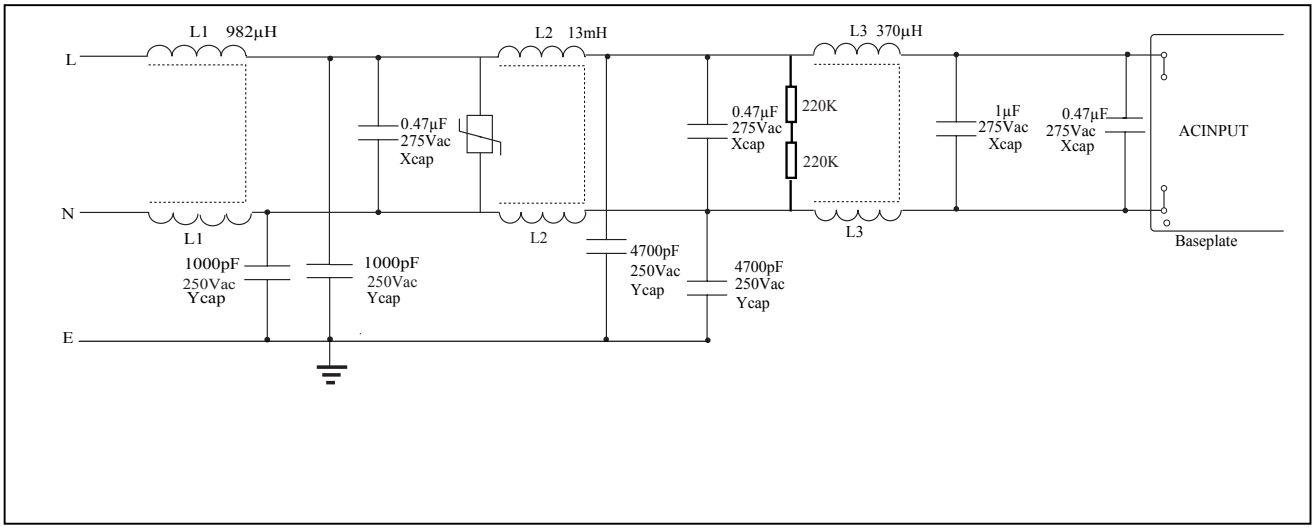

## General Connections to enable a load

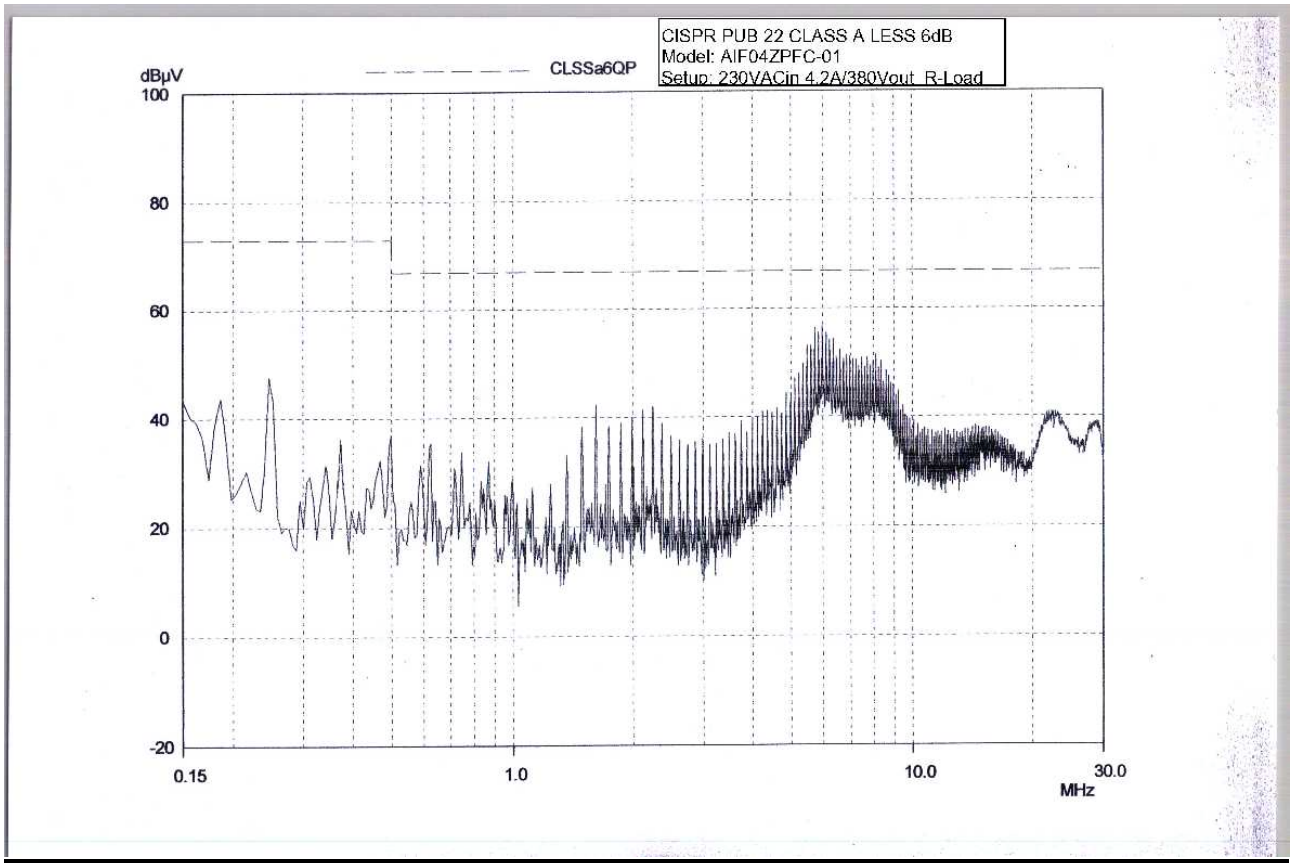
For enabling loads other than Astec DC-DC converters the following circuit can be used. The LD ENABLE pin can directly drive a MOSFET with a 15V zener clamping the gate voltage.

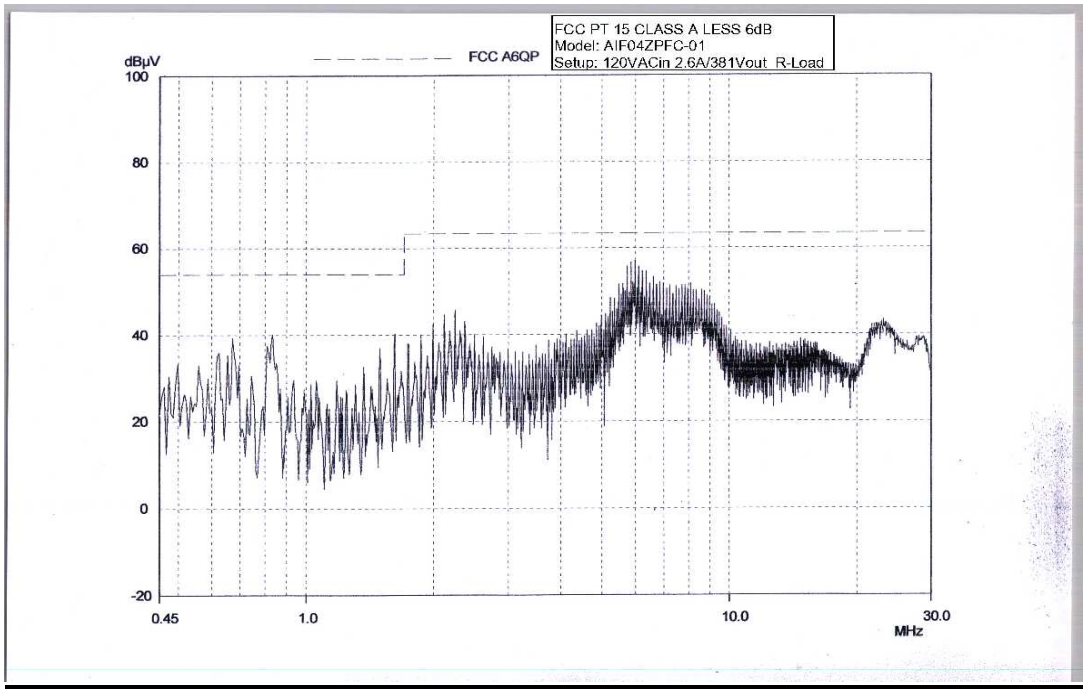


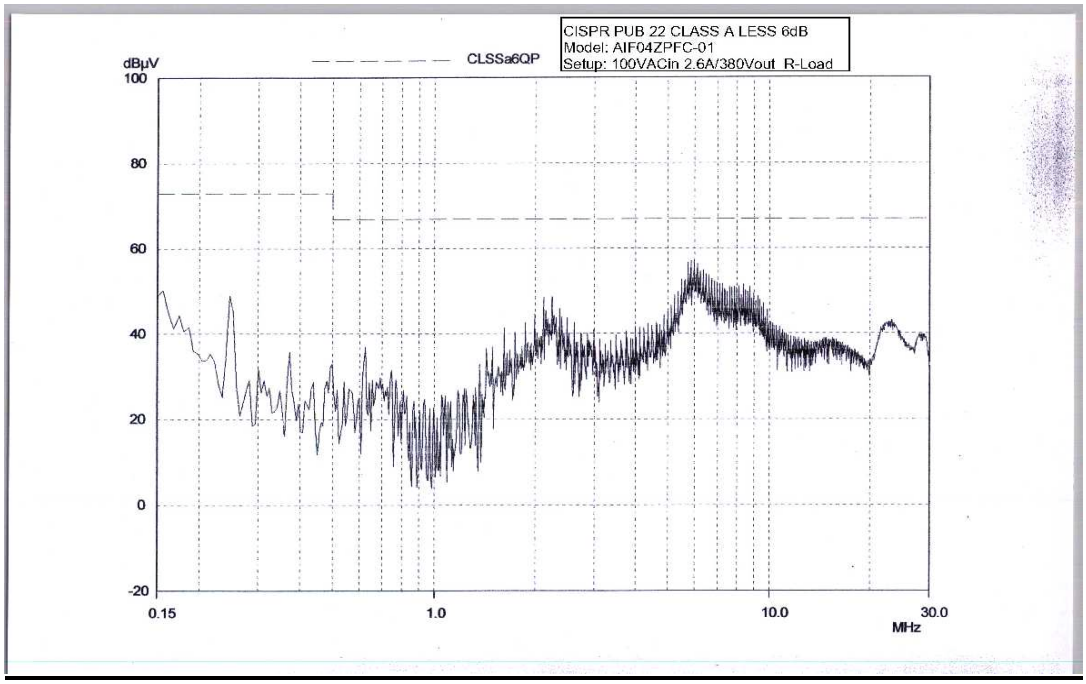

## Conducted EMI

The PFC modules will require additional EMI filtering to enable the system to meet relevant EMI standards.
PFC modules have an effective input to ground (baseplate) capacitance of 1600pF. This should be accounted for when calculating the maximum EMI 'Y' capacitance to meet ground leakage current specifications. An example filter circuit is shown below.


L1 982µH
L2 13mH
L3 370µH
L
N
E
0.47µF
275Vac
Xcap
220K
220K
1µF
275Vac
Xcap
0.47µF
275Vac
Xcap
ACINPUT
Baseplate
L1
L2
L3
1000pF
250Vac
Ycap
1000pF
250Vac
Ycap
4700pF
250Vac
Ycap
4700pF
250Vac
Ycap

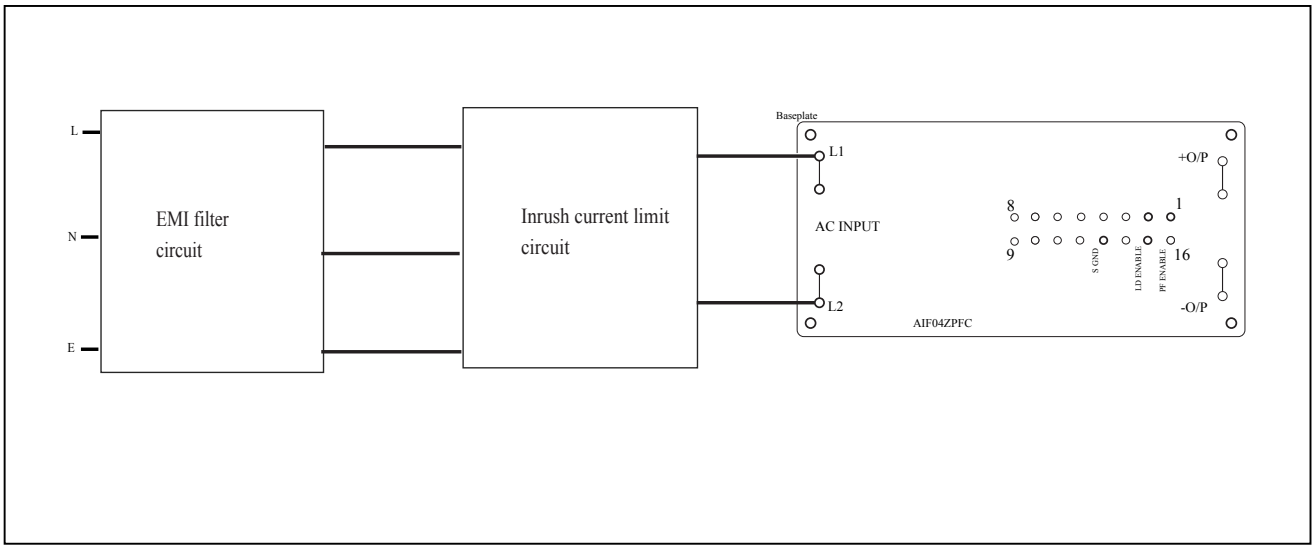

CISPR PUB 22 CLASS A LESS 6dB
Model: AIF04ZPFC-01
Setup: 230VACin 4.2A/380Vout R-Load
CLSSa6QP
dBµV
100
80
60
40
20
0
-20
0.15
1.0
10.0
30.0
MHz


FCC PT 15 CLASS A LESS 6dB
Model: AIF04ZPFC-01
Setup: 120VACin 2.6A/381Vout R-Load
FCC A6QP
dBµV
100
80
60
40
20
0
-20
0.45
1.0
10.0
30.0
MHz


CISPR PUB 22 CLASS A LESS 6dB
Model: AIF04ZPFC-01
Setup: 100VACin 2.6A/380Vout R-Load
CLSSa6QP
dBµV
100
80
60
40
20
0
-20
0.15
1.0
10.0
30.0
MHz

## APPLICATION EXAMPLE

### PFC module input connection example:




## Model AIF04ZPFC-02L Parallel Operation

The AIF04ZPFC-02L has been specifically designed for paralleling applications where the total input current exceeds 16Arms. For stand-alone applications or those where the total input current does not exceed 16Arms the AIF04ZPFC-01L is recommended.

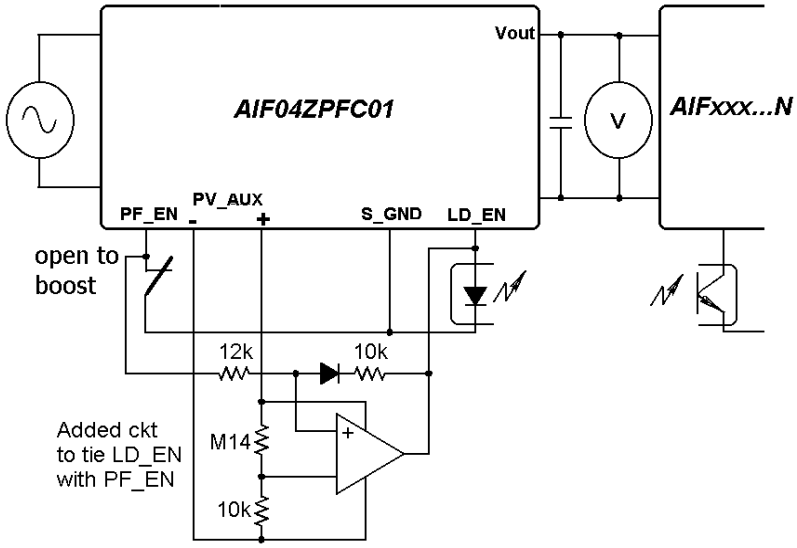
The AIF04ZPFC-02L requires external negative rail rectifiers to be implemented at the input to the system. It is possible to operate the AIF04ZPFC-02L as a stand-alone configuration although the external negative rail rectifiers must still be provided.

**Current Sharing**

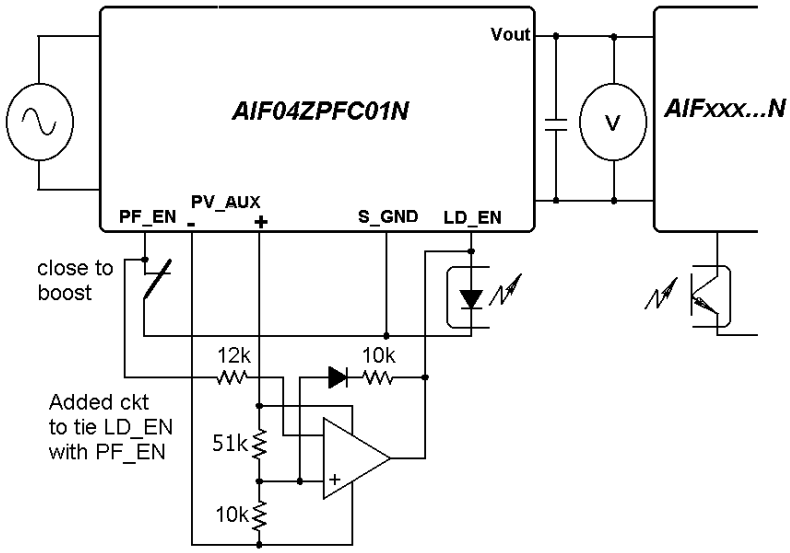
In multi-module paralleled systems, all modules will share current to within ± 10% of the average load current per module when the C-SHARE pins of each module are connected together.

## Interlock circuit between LD ENABLE and PF ENABLE (Continues from P.9, LD ENABLE)

Initially the load is disabled and the LD ENABLE (pin 15) is at 0.4V (LOW). When the PFC power up sequence has completed, the LD ENABLE voltage goes HIGH. And the LD ENABLE will stay high as long as Vin is above 175Vac or Vout is above 250V, even if PF_ENABLE is in disable mode. If the application needs the LD_EN goes low when the PF_EN is disable, please use the following interlock circuitry.



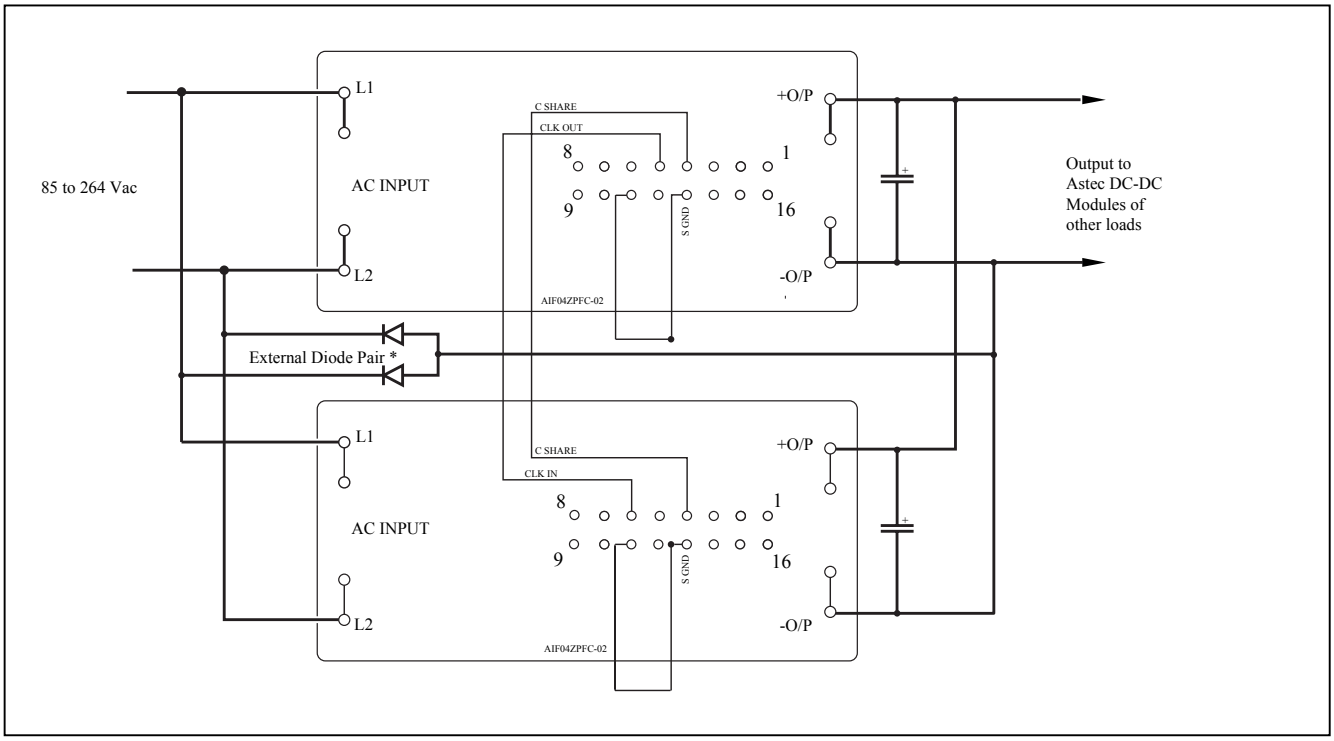

**LD_EN goes low when PF_EN is set low (AIF04ZPFC-01L)**




**LD_EN goes low when PF_EN is set high (AIF04ZPFC-01NL)**

## Synchronization

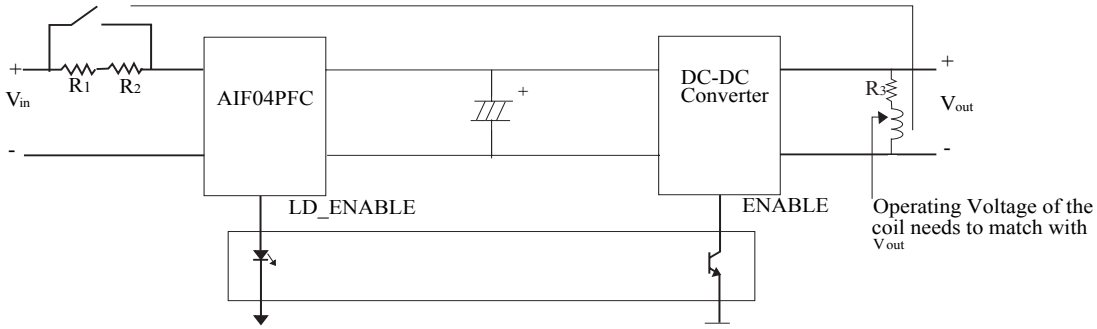
Modules are synchronized by connecting the CLK OUT pin of one module to the CLK IN of the next module in an open daisy chain configuration. If the clock input to a module fails it will automatically revert to its internal clock and continue to operate at full power.



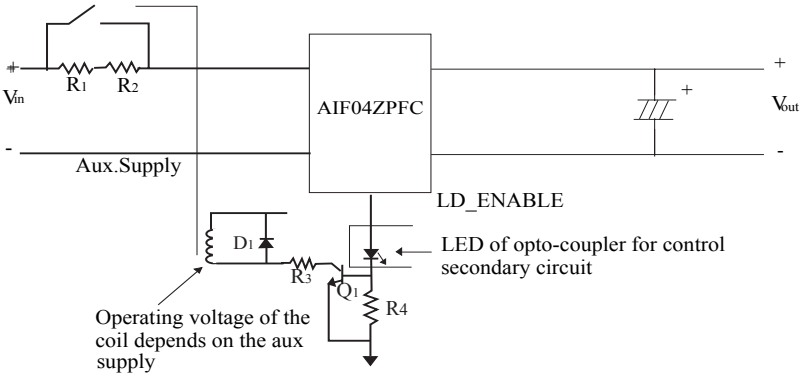

***** The current rate requirement of external rectifier for each line is 20A x number of units in parallel. For example, if there are 3 pieces of AIF04ZPFC-02L in parallel, customer will need to put 60A (20A x 3) external rectifier for each line.

## Recommend external Inrush Current Limit circuit

CIRCUIT(1): Using relay controlled from secondary side:



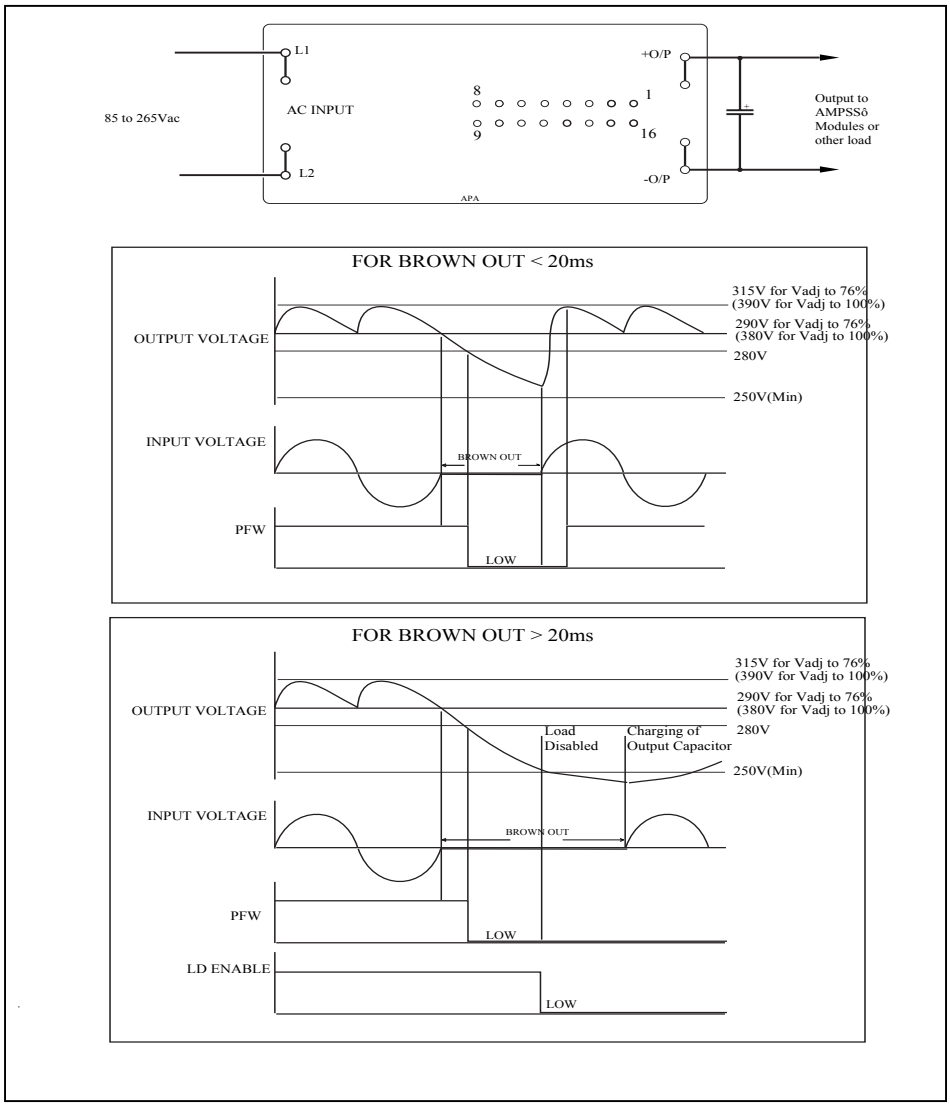

CIRCUIT(2):Using relay controlled by Auxiliary supply on primary side:




In rush Limit for PFC Series

## Brown Out Ride Through

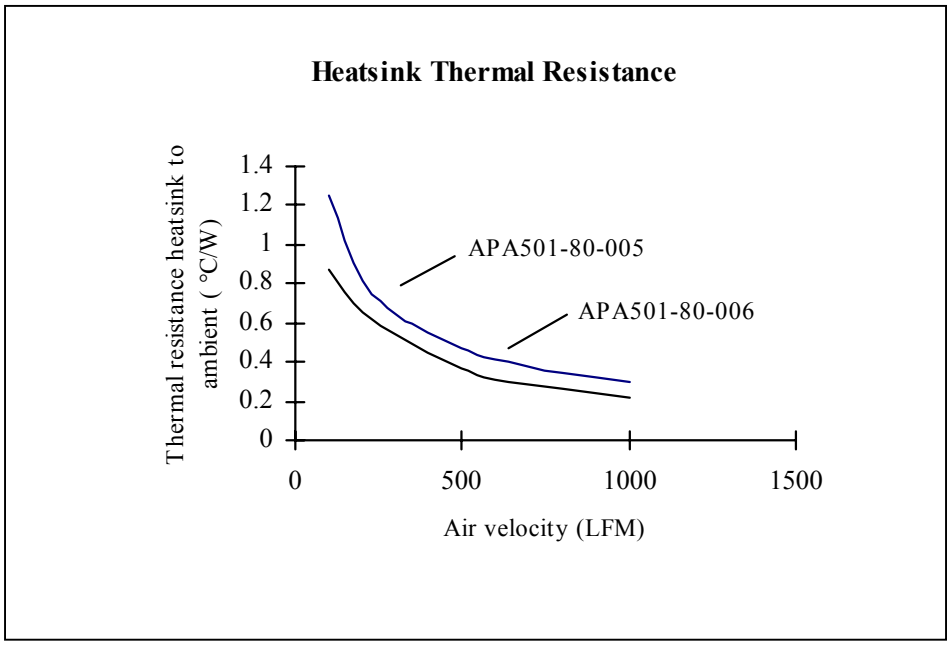
Brown Out conditions occurs when there is a transient break in input current. During this period the external output bulk capacitor holds up the voltage to the load until input current is restored. When the input voltage is restored the PFC module will continue delivering power to the load




After a Brown Out condition where the output voltage has not dropped below 250Vdc, the module will recover when input power is restored. The PFW signal can be used to monitor input power loss.

## Thermal Data

Natural convection thermal impedance of the PFC package without a heatsink is approximately 4°C/W.
A standard horizontal fin heatsink available from Astec (part number APA501-80-006) with 37mm fins and 8.8mm pitch, will reduce module thermal impedance to 0.4°C /W with a forced air flow of 2.5 m/s (500 LFM) when mounted with a thermal pad (ASTEC P/N APA502-80-001) between heatsink and module.



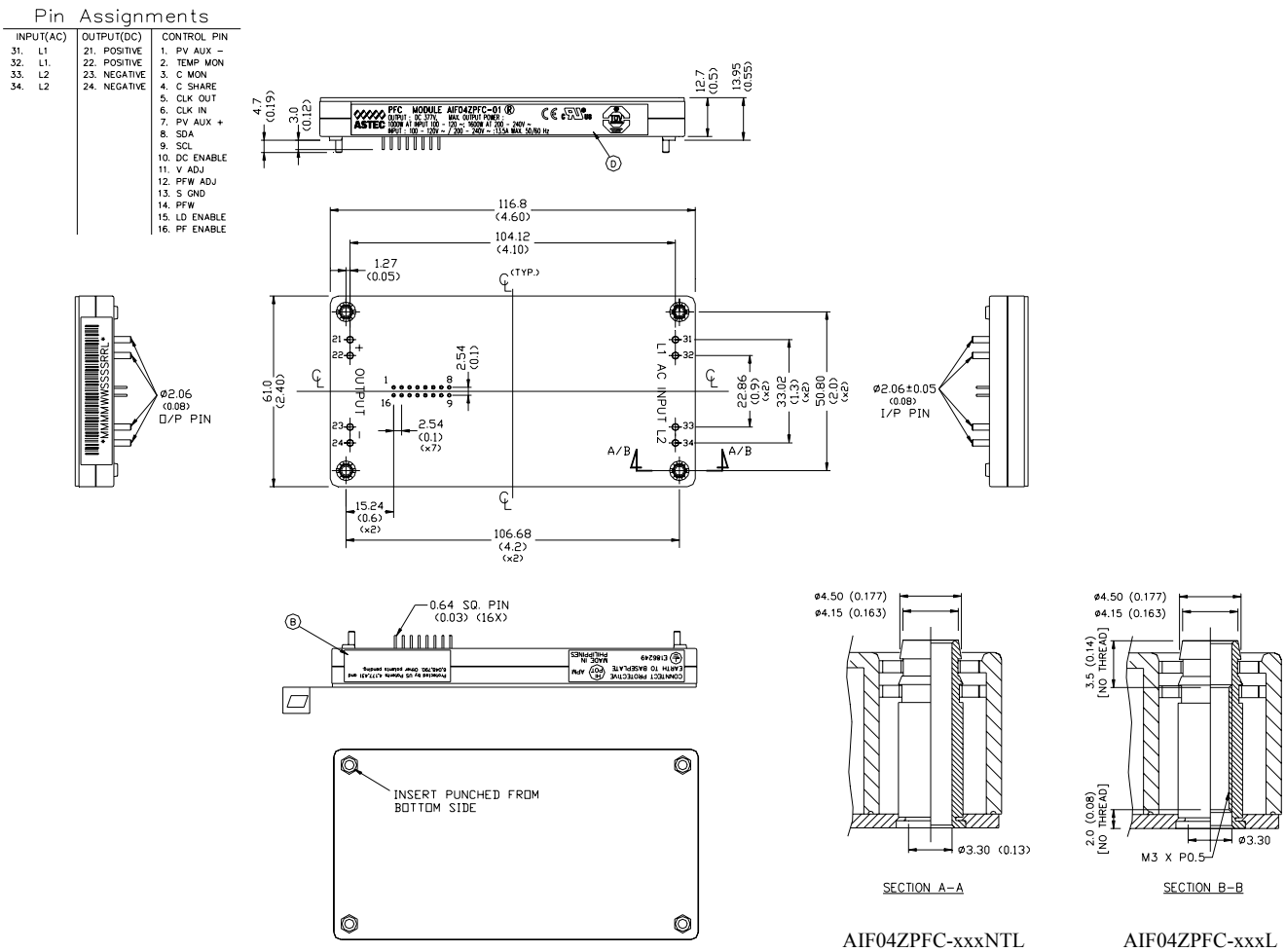

## Overtemperature Protection

If the module's internal temperature exceeds 105°C (typical), the module will protect itself by latching off

## OUTLINE DRAWING

Pin Assignments

| INPUT(AC) | OUTPUT(DC) | CONTROL PIN |
|---|---|---|
| 31. L1 | 21. POSITIVE | 1. PV AUX – |
| 32. L1 | 22. POSITIVE | 2. TEMP MON |
| 33. L2 | 23. NEGATIVE | 3. C MON |
| 34. L2 | 24. NEGATIVE | 4. C SHARE |
| | | 5. CLK OUT |
| | | 6. CLK IN |
| | | 7. PV AUX + |
| | | 8. SDA |
| | | 9. SCL |
| | | 10. DC ENABLE |
| | | 11. V ADJ |
| | | 12. PFW ADJ |
| | | 13. S GND |
| | | 14. PFW |
| | | 15. LD ENABLE |
| | | 16. PF ENABLE |




AIF04ZPFC-xxxNTL

AIF04ZPFC-xxxL

Case thickness can meet UL-V0 flammability standard.

## Comparison between AIF - PFC and APA100 series

| | AIF04ZPFC-01L | AIF04ZPFC-02L | APA100-101 | APA100-101M | APA100-102 | APA100-103 | APA100-104 |
|---|---|---|---|---|---|---|---|
| Input Voltage | 85 - 264Vac | | 85 - 265Vac | | | | |
| Max Output Power<br>85Vac ≤ Vin ≤ 120Vac<br>Vin ≥ 220Vac | 1000W<br>1600W | | 750W<br>1200W | | | 550W<br>950W | 750W<br>1200W |
| Vac under-voltage / Power interrupt | Fast-Recovery | | Full Recycle | | | | |
| Power line interrupt protection | Meet power line disturbance immunity specification per IEC61000-4-11 | | Not rated | | | | |
| Floating PV_AUX supply | Yes | | No | | | | |
| V-AUX Frequency | Fixed at 250KHz | | Non-fixed Frequency | | | | |
| Operating temperature | -20℃ - 100℃ | | -20℃ - 85℃ | | | | |
| Remote on/off | Various | | Negative logic only | | | | |
| EEPROM data storage | Yes | | No | | | | |
| Inrush current limit circuit | external | | internal | external | internal | external | external |
| Parallel Application<br>Input current<br>External Diode Pair | Total $I_{in}$ < 16Arms<br>No Need | No Limit<br>Yes | Total $I_{in}$ < 16Arms<br>No Need | | No limit<br>Yes | Total $I_{in}$ < 16Arms<br>No Need | |
| Full load Vo | 380Vdc | | 377Vdc | | | | |
| LD_ENABLE trigger point | 250Vdc output | | 180Vdc output | | | | |
| Minimum setting for PFW_ADJ | 280Vdc | | 205Vdc | | | | |
| Encapsulated | Yes | | Partial | | | | |
| Internal Fuse | No | | No | | | Yes (10A) | No |
| Fully SMT design | Yes | | No | | | | |
| QAV | Yes | | No | | | | |
| Control pins | 16 pins | | 14 pins | | | | |
| Power pins | ∅2.06mm | | ∅1.52mm | | | | |
| Mounting Kits | No Need | | Need | | | | |
| Module colour | Emerson Blue | | Black | | | | |