AH103A

High Gain, High Linearity ½-Watt Amplifier

Product Features

- 60 – 2700 MHz
- +27 dBm P1dB
- +46 dBm Output IP3
- 29 dB Gain @ 900 MHz
- Excellent ACPR
- MTTF > 100 Years
- Lead-free/green/RoHS-compliant SOIC-8 Package w/ heat slug

Applications

- Mobile Infrastructure
- W-LAN / ISM / RFID
- MDS / MMDS Infrastructure

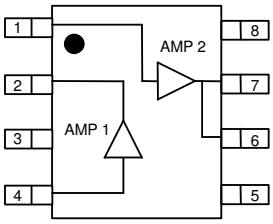
Product Description

The AH103A is a high gain, high linearity ½-Watt amplifier. This device is comprised of two individual MMIC amplifiers internally and can be used with an external interstage match for any of the mobile infrastructure frequency bands. The dual-stage amplifier achieves up to +46 dBm IP3 performance with 29 dB gain.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The AH103A has an associated MTTF of a minimum of 100 years at a mounting temperature of 85 °C and is housed in a lead-free /green/RoHS-compliant SOIC-8 package. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high linearity are required.

Functional Diagram



Function	Pin No.
Amp2 in	1
Amp1 out / Bias 1	2
Ground	3, 5, 8, Backside copper
RF in (Amp1 in)	4
RF out (Amp2 out)	6
Bias 2	7

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	60		2700
Test Frequency	MHz		900	
Gain	dB		29.1	
Output IP3	dB		+46	
Output P1dB	dBm		+27	
Test Frequency	MHz		1900	
Gain	dB	23.5	25.4	
Input Return Loss	dB		19	
Output Return Loss	dB		11	
Output IP3 (2)	dBm	+42	+45	
Output P1dB	dBm	+25	+26.7	
Noise Figure	dB		3	
Supply Voltage (Amp1)	V		+4.5	
Supply Voltage (Amp2)	V		+9	
Operating Current (3)	mA	225	275	330

1. Test conditions unless otherwise noted: 25 °C, Vdd1 = +4.5 V, Vdd2 = +9 V, in a tuned application circuit.
2. 3OIP measured with two tones at an output power of +8 dBm/tone separated by 10 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. Amp1 and Amp2 have a typical current draw of 75 and 200 mA, respectively.

Typical Performance (1)

Parameter	Units	Typical		
Frequency	MHz	900	1900	2140
Gain	dB	29.1	25.4	25
Input Return Loss	dB	20	19	24
Output Return Loss	dB	19	11	11
Output IP3	dBm	+46	+45	+45
Output P1dB	dBm	+27	+26.7	+26.3
IS-95 Ch. Power (4) @ -45 dBc ACPR	dBm	+20.7	+20.5	
W-CDMA Ch. Power (5) @ -45 dBc ACPR / ACLR	dBm			+18.5
Noise Figure	dB	2.5	3	2.9
Supply Bias Amp1		+4.5 V @ 75 mA		
Supply Bias Amp2		+9 V @ 200 mA		

4. ACPR is measured at 900 and 1900 MHz with a IS-95, 9 Channels Forward, ±885 kHz offset, 30 kHz BW, 1.23 MHz Channel BW.
5. ACLR is measured at 2140 MHz with a 3GPP W-CDMA, Test Model 1+64 DPCH, ±5 MHz offset, 3.84 MHz Channel BW.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-55 to +125 °C
DC Voltage (pin 2)	+6 V
DC Voltage (pin 6, 7)	+11 V
RF Input Power (continuous)	4 dB above Input P1dB
Junction Temperature	+160 °C
Thermal Resistance	21° C / W

Operation of this device above any of these parameters may cause permanent damage.

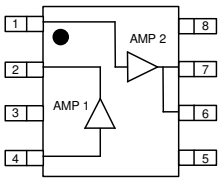
Ordering Information

Part No.	Description
AH103A-G	High Gain ½-Watt Amplifier (lead-free/green/RoHS-compliant SOIC-8 Pkg)
AH103A-PCB900	0.7 – 1.0 GHz Evaluation Circuit
AH103A-PCB1900	1.8 – 2.0 GHz Evaluation Circuit
AH103A-PCB2140	2.1 – 2.2 GHz Evaluation Circuit

Standard T/R size = 500 pieces on a 7" reel.

Specifications and information are subject to change without notice

Typical Device Data



Typical AH103A Performance Chain Analysis at 900 MHz

Stage	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)	Voltage (V)	Current (mA)	Cumulative Performance			
							Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)
Amplifier 1	14.5	18	39	2.5	+4.5	75	14.5	18	39	2.5
Amplifier 2	14.5	27.5	46.5	3.1	+9	200	28.5	26.3	45.7	2.6
AH103A	**Cumulative Performance**					**275**	**29**	**+26.3**	**+45.7**	**2.6**

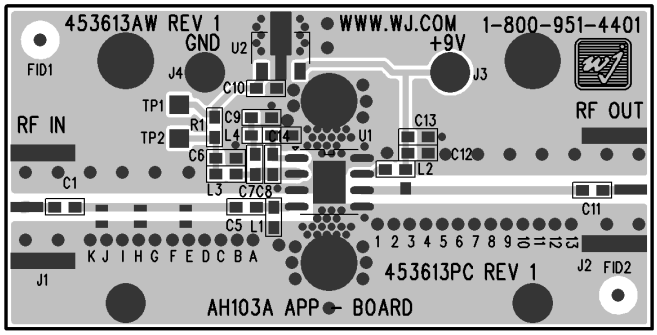
S-Parameters (Amplifier #1, V_D = +4.5 V, I_D = 75 mA, T = 25°C, calibrated to device leads, pin 4 = port 1, pin 2 = port 2)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-5.37	-33.79	15.86	160.65	-22.13	22.13	-10.55	-47.75
200	-8.33	-28.53	14.72	161.63	-21.04	1.23	-16.88	-35.01
400	-8.71	-36.36	14.53	155.57	-21.01	-2.61	-18.18	-26.80
600	-8.77	-47.76	14.39	147.36	-20.88	-5.20	-18.38	-27.81
800	-9.15	-61.06	14.12	139.46	-20.63	-6.95	-19.40	-27.61
1000	-9.05	-73.89	14.00	131.54	-20.79	-8.56	-20.14	-30.37
1200	-9.37	-85.84	13.79	123.95	-20.68	-9.16	-21.80	-36.89
1400	-9.59	-97.65	13.52	115.85	-20.70	-12.14	-21.91	-45.14
1600	-9.64	-111.10	13.20	108.12	-20.64	-13.59	-22.45	-48.69
1800	-9.21	-124.09	12.86	100.77	-20.53	-14.44	-22.22	-46.08
2000	-8.86	-136.42	12.52	93.26	-20.32	-15.72	-22.52	-35.22
2200	-8.31	-148.36	12.43	87.59	-20.44	-19.85	-25.39	-32.83
2400	-8.60	-159.16	12.06	80.18	-20.62	-21.31	-28.55	10.91
2600	-8.80	-170.83	11.72	73.78	-20.23	-23.96	-31.34	53.94

S-Parameters (Amplifier #2, V_D = +9 V, I_D = 200 mA, T = 25°C, calibrated to device leads, pin 1 = port 1, pin 6 = port 2)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-10.73	-73.81	16.87	155.39	-19.73	9.77	-13.03	-77.36
200	-17.49	-86.22	15.78	153.56	-19.37	-9.85	-27.33	-71.86
400	-16.10	-103.75	15.50	140.93	-19.51	-21.51	-28.05	-15.36
600	-14.58	-121.40	15.19	125.52	-19.71	-31.31	-22.04	-19.22
800	-12.52	-136.69	14.76	111.04	-20.10	-41.88	-17.78	-26.04
1000	-10.87	-146.69	14.45	96.62	-20.45	-52.24	-14.38	-37.86
1200	-9.59	-156.43	14.01	83.29	-20.94	-60.36	-12.17	-49.84
1400	-8.67	-165.93	13.61	69.48	-21.53	-70.30	-10.50	-64.25
1600	-7.90	-175.53	13.27	56.52	-22.11	-78.33	-9.28	-77.69
1800	-7.15	173.98	12.83	42.38	-22.90	-88.46	-8.06	-89.74
2000	-6.58	162.87	12.44	28.36	-23.56	-96.99	-6.74	-101.88
2200	-5.55	152.83	11.97	14.25	-24.57	-106.84	-5.79	-111.67
2400	-4.74	143.80	11.24	0.41	-25.97	-113.76	-5.03	-121.03
2600	-3.92	136.87	10.64	-11.41	-27.43	-122.11	-4.60	-131.14

Evaluation Board PCB Layout

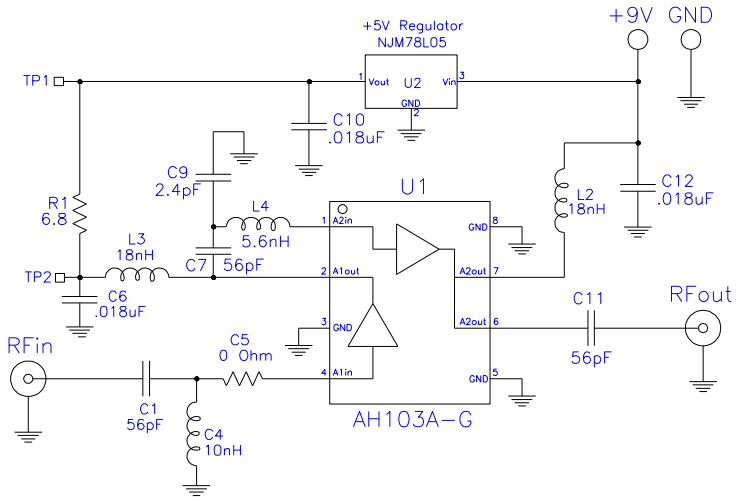


Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

Application Circuit: 700 – 1000 MHz (AH103AG-PCB900)

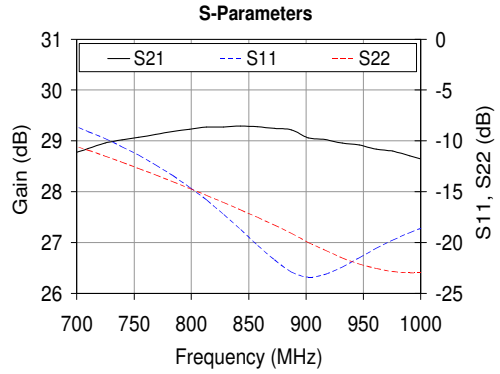
Typical RF Performance at 25°C

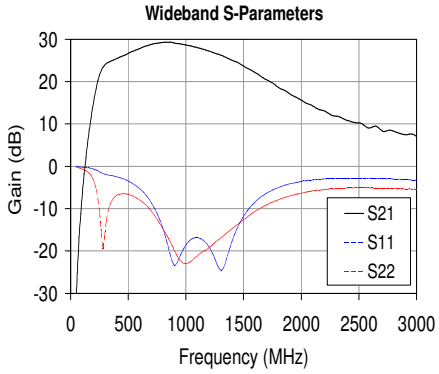
Frequency	900 MHz
Gain	29.1 dB
Input Return Loss	20 dB
Output Return Loss	19 dB
Output IP3	+46 dBm
Output P1dB	+27 dBm
IS-95A Ch. Power @ -45 dBc ACPR	+20.7 dBm
Noise Figure	2.5 dB
Supply Voltage	+9
Supply Current	275 mA

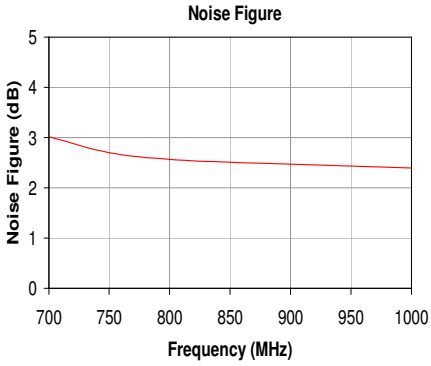


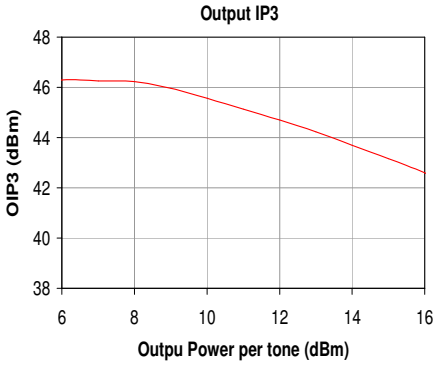
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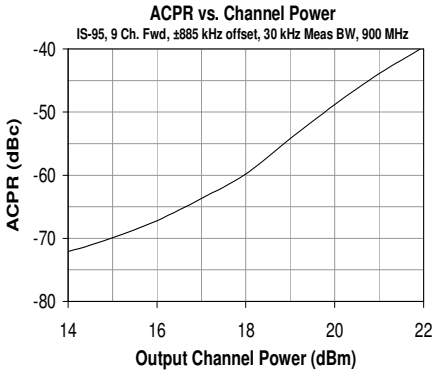
1. A voltage regulator is used in this circuit (U2) to drop the +9 V to a +5 V usable supply for the first internal amplifier. It is permissible to remove the regulator and operate the 1st amplifier stage directly off of +5 V supply onto Test Point 1 (TP1). The use of a +5 V supply on the 1st amplifier stage requires a dropping resistor of 6.8 Ω. A +4.5 V supply can also be used to bypass the 6.8 Ω and can be applied to Test Point 2 (TP2).







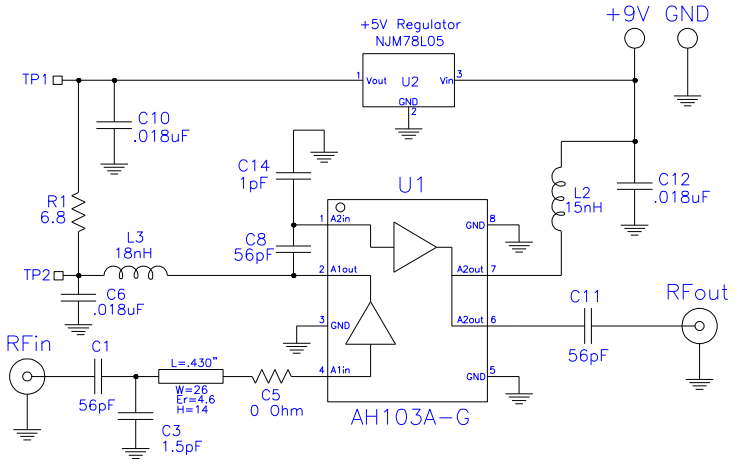




Application Circuit: 1900 – 2000 MHz (AH103AG-PCB1900)

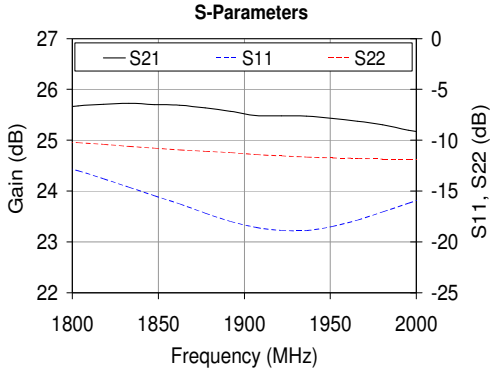
Typical RF Performance at 25°C

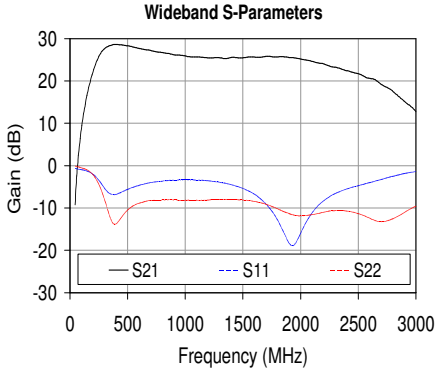
Frequency	1900 MHz
Gain	25.4 dB
Input Return Loss	19 dB
Output Return Loss	11 dB
Output IP3	+45 dBm
Output P1dB	+26.7 dBm
IS-95A Ch. Power @ -45 dBc ACPR	+20.5 dBm
Noise Figure	3 dB
Supply Voltage	+9 V
Supply Current	275 mA

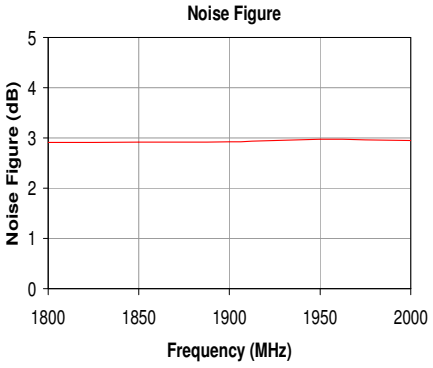


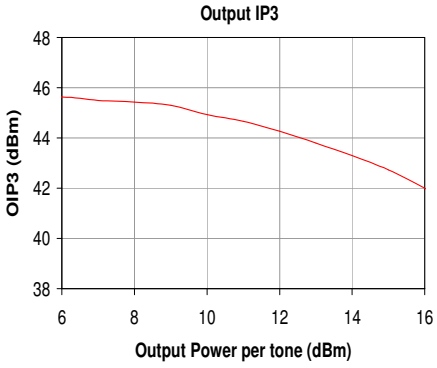
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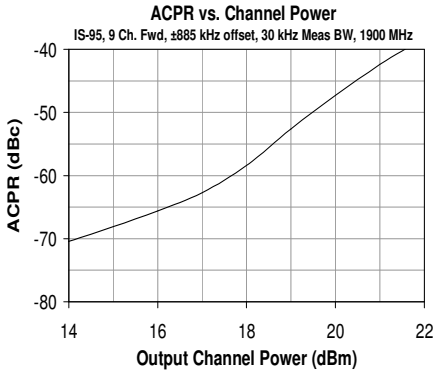
1. A voltage regulator is used in this circuit (U2) to drop the +9 V to a +5 V usable supply for the first internal amplifier. It is permissible to remove the regulator and operate the 1st amplifier stage directly off of +5 V supply onto Test Point 1 (TP1). The use of a +5 V supply on the 1st amplifier stage requires a dropping resistor of 6.8 Ω. A +4.5 V supply can also be used to bypass the 6.8 Ω and can be applied to Test Point 2 (TP2).







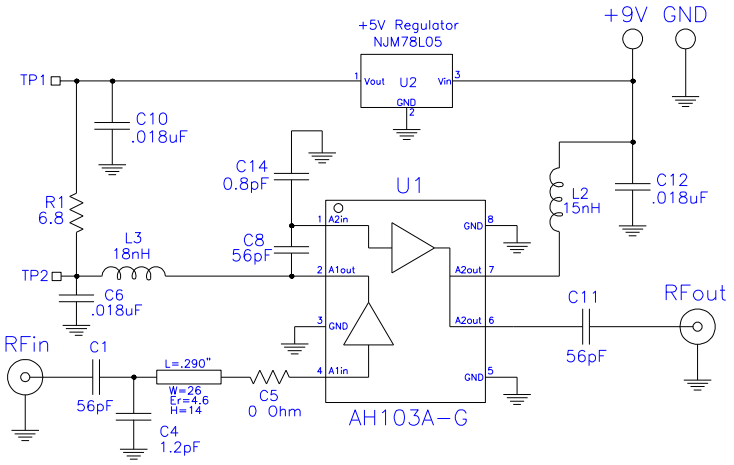




Application Circuit: 2110 – 2170 MHz (AH103AG-PCB2140)

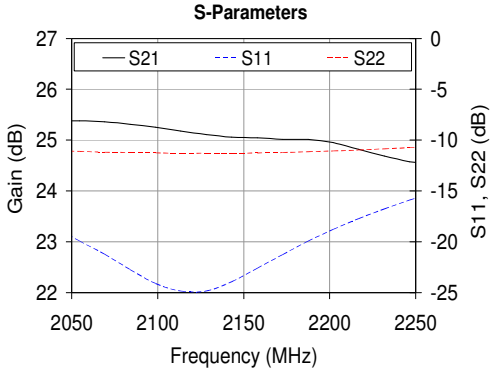
Typical RF Performance at 25°C

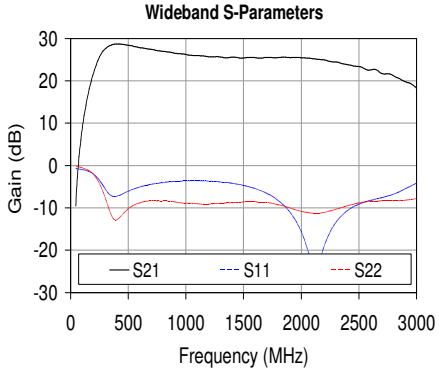
Frequency	2140 MHz
Gain	25 dB
Input Return Loss	24 dB
Output Return Loss	11 dB
Output IP3	+45 dBm
Output P1dB	+26.3 dBm
W-CDMA Ch. Power @ -45 dBc ACPR	+18.5 dBm
Noise Figure	2.9 dB
Supply Voltage	+9 V
Supply Current	275 mA

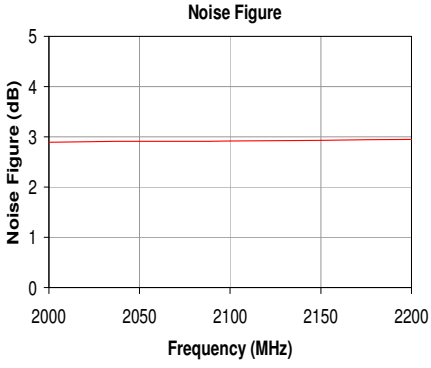


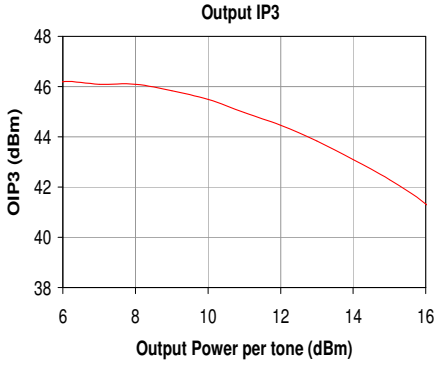
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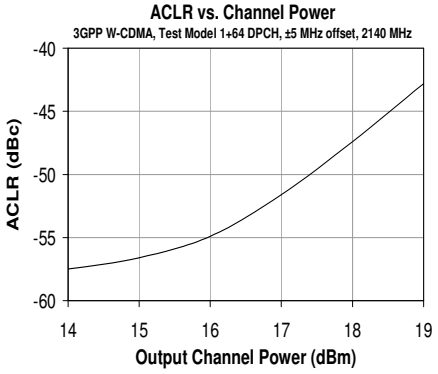
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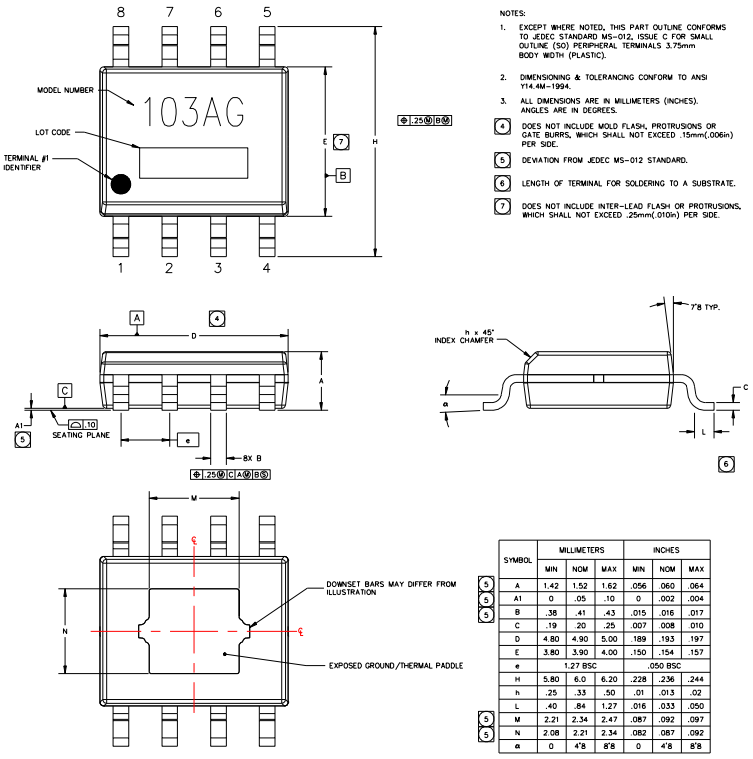




AH103A-G (Lead-Free Package) Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260°C reflow temperature) and lead (maximum 245°C reflow temperature) soldering processes.

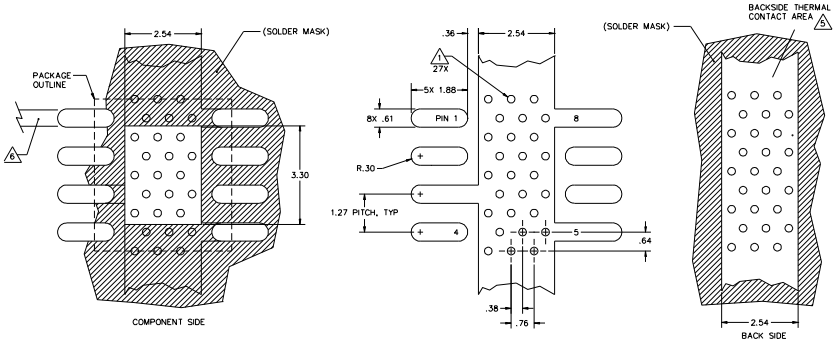
Outline Drawing



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°8	8°8	0	4°8	8°8

Mounting Configuration / Land Pattern



Product Marking

The component will be marked with an "103AG" designator followed by a alpha-numeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ≥ 500 V to <1000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Rating:	Class III
Value:	Passes ≥ 500 V to <1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Functional Pin Layout

Pin	Function
1	Amp2 input
2	Amp1 output / Bias Amp1
3, 5, 8	Ground
4	RF input (Amp1 input)
6	RF output (Amp2 output)
7	Bias Amp2

The backside paddle is the Source and should be grounded for thermal and electrical purposes. All other pins should be grounded on the PCB.

Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. To ensure reliable operation, device ground paddle-to-ground pad solder joint is critical.
4. Add mounting screws near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. For optimal thermal performance, expose soldermask on backside where it contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters. Angles are in degrees.
9. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.

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