AFE5812 Fully Integrated, 8-Channel Ultrasound Analog Front End with Passive CW Mixer, and Digital I/Q Demodulator, 0.75 nV/rtHz, 14/12-Bit, 65 MSPS, 180 mW/CH

1 Features

- 8-Channel Complete Analog Front-End
  - LNA, VCAT, PGA, LPF, ADC, and CW Mixer
- Programmable Gain Low-Noise Amplifier (LNA)
  - 24, 18, 15 dB Gain
  - 0.25, 0.5, 0.7 V_{PP} Linear Input Range
  - 0.63, 0.7, 0.9 nV/rtHz Input Referred Noise
  - Programmable Active Termination
- 40 dB Low Noise Voltage Controlled Attenuator (VCAT)
- 24/30 dB Programmable Gain Amplifier (PGA)
- 3rd Order Linear Phase Low-Pass Filter (LPF)
  - 10, 15, 20, 30, 35, 50 MHz
- 14-bit Analog to Digital Converter w/ LVDS output
  - 77 dBFS SNR at 65 MSPS
- Noise/Power Optimizations (Without Digital Demodulator)
  - 180 mW/CH at 0.75 nV/rtHz, 65 MSPS
  - 109 mW/CH at 1.1 nV/rtHz, 40 MSPS
  - 107 mW/CH at CW Mode
- Excellent Device-to-Device Gain Matching
  - ±0.5 dB(typical) and ±1.1 dB(max)
- Programmable Digital I/Q Demodulator after ADC
  - Wide Range Demodulation Frequency
  - <1KHz Frequency Resolution
  - Decimation Filter Factor M = 1 to 32
  - 16xM tap FIR Decimation Filter
  - LVDS Rate Reduction after Demodulation
  - On-chip RAM with 32 preset Profiles
- Low Harmonic Distortion
- Low Frequency Sonar Signal Processing
- Fast and Consistent Overload Recovery
- Passive Mixer for Continuous Wave Doppler(CWD)
  - Low Close-in Phase Noise –156 dBc/Hz at 1 KHz off 2.5 MHz Carrier
  - Phase Resolution of 1/16λ
  - Support 16X, 8X, 4X and 1X CW Clocks
  - 12dB Suppression on 3rd and 5th Harmonics
- Small Package: 15 mm x 9 mm, 135-BGA
- Operation Temperature: -40°C to 85°C

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipments
- Sonar applications
- Multichannel, High-Speed Data Acquisition

3 Description

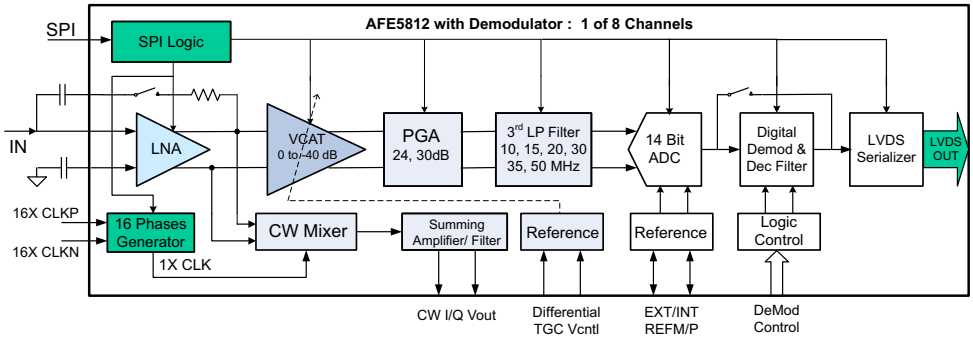
The AFE5812 is a highly-integrated analog front-end (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5812 integrates a complete time-gain-control (TGC) imaging path and a CWD path. It also enables users to select one of various power/noise combinations to optimize system performance. Therefore, the AFE5812 is a suitable ultrasound AFE solution not only for high-end systems, but also for portable ones.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE5812	NFBGA (135)	15.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

Changes from Original (March 2015) to Revision A **Page**

- Changed the device From: Product Preview To: Production Data ... 1

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6 Device Comparison Table

Part Number	Part Description	Package	Body Size (NOM)
AFE5818, SBAS687	16-Channel, Ultrasound, Analog Front-End with 124-mW/Channel, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5816, SBAS688	16-Channel, Ultrasound, Analog Front-End with 54-mW/Channel, 1.3-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5809, SLOS738	8-Channel Ultrasound Analog Front End With Passive CW Mixer, and Digital I/Q Demodulator, 0.75 nV/rtHz, 14, 12-Bit, 65 MSPS, 158 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5808A,SLOS729	8-Channel Ultrasound Analog Front End With Passive CW Mixer, 0.75 nV/rtHz, 14/12-Bit, 65 MSPS, 158 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5807, SLOS703	8-Channel Ultrasound Analog Front End with Passive CW Mixer, 1.05 nV/rtHz, 12-Bit, 80 MSPS, 117 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5803, SLOS763	8-Channel Ultrasound Analog Front End, 0.75 nV/rtHz, 14/12-Bit, 65 MSPS, 158 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5805, SBOS421	8-Channel Ultrasound Analog Front End, 0.85 nV/rtHz, 12-Bit, 50 MSPS, 122 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5804, SBOS442	8-Channel Ultrasound Analog Front End, 1.23 nV/rtHz, 12-Bit, 50 MSPS, 101 mW/CH	NFBGA (135)	15.00 mm × 9.00 mm
AFE5801, SLOS591	8-Channel Variable-Gain Amplifier (VGA) With Octal High-Speed ADC, 5.5 nV/rtHz, 12-Bit, 65MSPS, 65 mW/CH	QFN (64)	9.00 mm × 9.00 mm
AFE5851, SLOS574	16-Channel Variable-Gain Amplifier (VGA) With High-Speed ADC, 5.5 nV/rtHz, 12-Bit, 32.5 MSPS, 39 mW/CH	QFN (64)	9.00 mm × 9.00 mm
VCA5807, SLOS727	8-Channel Voltage Controlled Amplifier for Ultrasound with Passive CW Mixer, 0.75 nV/rtHz, 99 mW/CH	TQFP (80)	14.00 mm × 14.00 mm
VCA8500, SBOS390	8-Channel, Ultralow-Power, Variable Gain Amplifier with Low-Noise Pre-Amp, 0.8 nV/rtHz, 65 mW/CH	QFN (64)	9.00 mm × 9.00 mm
ADS5294, SLAS776	Octal-Channel 14-Bit 80-MSPS ADC, 75 dBFS SNR, 77 mW/CH	TQFP (80)	14.00 mm × 14.00 mm
ADS5292, SLAS788	Octal-Channel 12-Bit 80-MSPS ADC, 70 dBFS SNR, 66 mW/CH	TQFP (80)	14.00 mm × 14.00 mm
ADS5295, SBAS595	Octal-Channel 12-Bit 100-MSPS ADC, 70.6 dBFS SNR, 80 mW/CH	TQFP (80)	14.00 mm × 14.00 mm
ADS5296A, SBAS631	10-Bit, 200-MSPS, 4-Channel, 61dBFS SNR, 150 mW/CH and 12-Bit, 80-MSPS, 8-Channel, 70dBFS SNR, 65 mW/CH ADC	QFN (64)	9.00 mm × 9.00 mm

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7 Description (continued)

The AFE5812 contains eight channels of voltage controlled amplifier (VCA), 14, and 12-bit ADC, and CW mixer. The VCA includes LNA, VCAT, PGA, and LPF. The LNA gain is programmable to support 250 mV_{PP} to 0.75 V_{PP} input signals. Programmable active termination is also supported by the LNA. The ultra-low noise VCAT provides an attenuation control range of 40 dB and improves overall low-gain SNR, which benefits harmonic imaging and near-field imaging. The PGA provides gain options of 24 and 30 dB. Before the ADC, a LPF can be configured as 10, 15, 20, 30, 35 or 50 MHz to support ultrasound applications with different frequencies. In addition, the signal chain of the AFE5812 can handle signal frequency lower than 100 kHz, which enables the AFE5812 to be used in both sonar and medical applications. The high-performance 14-bit/65-MSPS ADC in the AFE5812 achieves 77 dBFS SNR. It ensures excellent SNR at low chain gain. The ADC's LVDS outputs enable flexible system integration desired for miniaturized systems.

The AFE5812 integrates a low-power passive mixer and a low-noise summing amplifier to accomplish on-chip CWD beamformer. 16 selectable phase-delays can be applied to each analog input signal. Meanwhile, a unique third- and fifth-order harmonic suppression filter is implemented to enhance CW sensitivity.

AFE5812 also includes a digital in-phase and quadrature (I/Q) demodulator and a low-pass decimation filter. The main purpose of the demodulation block is to reduce the LVDS data rate and improve overall system power efficiency. The I/Q demodulator can accept ADC output with up to 65 MSPS sampling rate and 14-bit resolution. For example, after digital demodulation and 4× decimation filtering, the data rate for either in-phase or quadrature output is reduced to 16.25 MSPS and the data resolution is improved to 16 bits, consequently. Hence, the overall LVDS trace reduction can be a factor of 2. This demodulator can be bypassed and powered down completely if it is not needed.

The AFE5812 is available in a 15-mm × 9-mm, 135-pin BGA package, and it is specified for operation from -40°C to 85°C.

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8 Pin Configuration and Functions

Table 1. ZCF (BGA-135) Top View

	1	2	3	4	5	6	7	8	9
A	AVDD	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	CM_BYP	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	AVSS	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
E	CW_IP_AMPINP	CW_IP_AMPINM	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
F	CW_IP_OUTM	CW_IP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_16X	CLKM_16X
G	AVSS	AVSS	AVSS/DTGC_SW	AVSS	AVSS	AVSS	AVSS	CLKP_1X	CLKM_1X
H	CW_QP_OUTM	CW_QP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	PDN_GLOBAL	RESET
J	CW_QP_AMPINP	CW_QP_AMPINM	AVSS	AVSS	AVSS	AVDD_ADC	AVDD_ADC	PDN_VCA	SCLK
K	AVDD	AVDD_5V	VCNTLP	VCNTLM	VHIGH	AVSS	DNC	AVDD_ADC	SDATA
L	CLKP_ADC	CLKM_ADC	AVDD_ADC	REFM	DNC	LDO_EN	TX_SYNC_IN	PDN_ADC	SEN
M	AVDD_ADC	AVDD_ADC	VREF_IN	REFP	DNC	LDO_SETV	SPI_DIG_EN	DNC	SDOUT
N	D8P	D8M	DVDD	DVDD_LDO1	DVSS	DVDD_LDO2	DVDD	D1M	D1P
P	D7M	D6M	D5M	FCLKM	DVSS	DCLKM	D4M	D3M	D2M
R	D7P	D6P	D5P	FCLKP	DVSS	DCLKP	D4P	D3P	D2P

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
ACT1 to ACT8	B9 to B2	Active termination input pins for CH1 to CH8. Bias voltage = 1.5 V
AVDD	A1	3.3-V analog supply for LNA, VCAT, PGA, LPF, and CWD blocks
	D8	
	D9	
	E8	
	E9	
	K1	
AVDD_5V	K2	5-V analog supply for LNA, VCAT, PGA, LPF, and CWD blocks
AVDD_ADC	J6	1.8-V analog power supply for ADC
	J7	
	K8	
	L3	
	M1	
	M2	
AVSS	C1	Analog ground
	D1 to D7	
	E3 to E7	
	F3 to F7	
	G1 to G2	
	G4 to G7	
	H3 to H7	
	J3 to J5	
	K6	
AVSS/DTGC_SW	G3	Analog ground; or external control pin to switch from ATGC to DTGC. Active high to enable the DTGC mode. Pull down to GND with 20 kΩ. This pin is equivalent to VCA Reg 0x3B[7], DIG_TGC_ATT and Figure 64. Tie to AVSS if not used. Note: this feature is ensured by design and characterization; NOT production tested.
CLKM_ADC	L2	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1-µF capacitor. Bias voltage = 1V

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
CLKP_ADC	L1	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1-µF capacitor. Bias voltage = 1V
CLKM_16X	F9	Negative input of differential CW 16× clock. Tie to GND when the CMOS clock mode is enabled. In the 4× and 8× CW clock modes, this pin becomes the 4× or 8× CLKM input. In the 1× CW clock mode, this pin becomes the in-phase 1× CLKM for the CW mixer. Can be floated if CW mode is not used. See register 0x36[11:10]. Bias voltage = 2.5 V
CLKP_16X	F8	Positive input of differential CW 16× clock. In 4× and 8× clock modes, this pin becomes the 4× and 8× CLKP input. In the 1× CW clock mode, this pin becomes the in-phase 1× CLKP for the CW mixer. Can be floated if CW mode is not used.See register 0x36[11:10]. Bias voltage = 2.5 V
CLKM_1X	G9	Negative input of differential CW 1× clock. Tie to GND when the CMOS clock mode is enabled (refer to Figure 107 for details). In the 1× clock mode, this pin is the quadrature-phase 1× CLKM for the CW mixer. Can be floated if CW mode is not used. Bias voltage = 2.5 V
CLKP_1X	G8	Positive input of differential CW 1× clock. In the 1× clock mode, this pin is the quadrature-phase 1× CLKP for the CW mixer. Can be floated if CW mode is not used. Bias voltage = 2.5 V
CM_BYP	B1	Bias voltage and bypass to ground. TI recommends 1 µF. To suppress the ultra-low frequency noise, the designer can use 10 µF. Bias voltage = 1.5 V
CW_IP_AMPINM	E2	Negative differential input of the in-phase summing amplifier. External LPF capacitor must be connected between CW_IP_AMPINM and CW_IP_OUTP. This pin provides the current output for the CW mixer. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used. Bias voltage = 1.5 V
CW_IP_AMPINP	E1	Positive differential input of the in-phase summing amplifier. External LPF capacitor must be connected between CW_IP_AMPINP and CW_IP_OUTM. This pin provides the current output for the CW mixer. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used. Bias voltage = 1.5 V
CW_IP_OUTM	F1	Negative differential output for the in-phase summing amplifier. External LPF capacitor must be connected between CW_IP_AMPINP and CW_IP_OUTPM. Can be floated if not used. Bias voltage = 1.5 V
CW_IP_OUTP	F2	Positive differential output for the in-phase summing amplifier. External LPF capacitor must be connected between CW_IP_AMPINM and CW_IP_OUTP. Can be floated if not used. Bias voltage = 1.5 V
CW_QP_AMPINM	J2	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor must be connected between CW_QP_AMPINM and CW_QP_OUTP. This pin provides the current output for the CW mixer. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used. Bias voltage = 1.5 V
CW_QP_AMPINP	J1	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor must be connected between CW_QP_AMPINP and CW_QP_OUTM. This pin provides the current output for the CW mixer. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used. Bias voltage = 1.5 V
CW_QP_OUTM	H1	Negative differential output for the quadrature-phase summing amplifier. External LPF capacitor must be connected between CW_QP_AMPINP and CW_QP_OUTM. Can be floated if not used. Bias voltage = 1.5 V
CW_QP_OUTP	H2	Positive differential output for the quadrature-phase summing amplifier. External LPF capacitor must be connected between CW_QP_AMPINM and CW_QP_OUTP. Can be floated if not used. Bias voltage = 1.5 V
D1M to D8M	N8	ADC CH1 to CH8 LVDS negative data outputs
	P9 to P7	
	P3 to P1	
	N2	
D1P to D8P	N9	ADC CH1 to 8 LVDS positive data outputs
	R9 to R7	
	R3 to R1	
	N1	
DCLKM	P6	LVDS bit clock (7x in 14bit resolution) negative output
DCLKP	R6	LVDS bit clock (7x in 14bit resolution) positive output
DVDD	N3	ADC digital and I/O power supply, 1.8 V
	N7	

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
DVSS	N5	ADC digital ground
	P5	
	R5	
DVDD_LDO1, DVDD_LDO2	N4	**In the internal LDO mode, i.e. LDO_EN=1, these two pins should be separated on PCB and decoupled respectively.** Internal LDO output will drive this PIN to 1.2V or 1.4V depending on LDO_SETV. In the external LDO mode,i.e. LDO_EN=0 or floating, lower demod power is achieved than the internal LDO mode. 1.4V~1.5V should be applied when ADC sampling rate is high, e.g. 50~65MSPS. **Demod SPI requires DVDD_LDO1/2.**
	N6	
FCLKM	P4	LVDS frame clock (1×) negative output
FCLKP	R4	LVDS frame clock (1×) positive output
INM1 to INM8	C9 to C2	CH1 to CH8 complementary analog inputs. Bypass to ground with ≥0.015-µF capacitors. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V
INP1 to INP8	A9 to A2	CH1 to CH8 analog inputs. AC couple to inputs with ≥0.1-µF capacitors. Bias voltage = 2.2 V
LDO_EN	L6	Enable/Disable AFE's internal LDO regulators. When it is tied to 1.8-V DVDD or Logic "1", AFE's internal LDO is enabled. When it is tied to DVSS or Logic "0", AFE's internal LDO is disabled and external 1.4V supply can be applied at N4 and N6 pins, i.e. DVDD_LDO1, DVDD_LDO2. Default is pulled down internally through a 150 KΩ resistor with input capacitance of 5 pF.Either 1.8V or 3.3V logic level can be used.
LDO_SETV	M6	Sets the internal LDO voltage. '0' is 1.2V; '1' is 1.4V. Default is pulled down internally through a 150 KΩ resistor with input capacitance of 5 pF. Either 1.8V or 3.3V logic level can be used. Please note: some voltage drop exists on chip; therefore the measured DVDD_LDO voltage is slightly lower than the sepcified ones.
PDN_ADC	L8	ADC partial (fast) power-down control pin with an internal pulldown resistor of 100 kΩ. Active high. Either 1.8-V or 3.3-V logic level can be used.
PDN_VCA	J8	VCA partial (fast) power-down control pin with an internal pulldown resistor of 20 kΩ. Active high. 3.3-V logic level should be used.
PDN_GLOBAL	H8	Global (complete) power-down control pin for the entire chip with an internal pulldown resistor of 20 kΩ. Active high. 3.3-V logic level should be used. **When the complete power-down mode is enabled, the digital demodulator may lose register settings. Therefore, it is required to reconfigure the demodulator registers, filter coefficient memory, and profile memory after existing the complete power-down mode.**
REFM	L4	0.5-V reference output in the internal reference mode. Must leave floated in the internal reference mode. TI recommends adding a test point on the PCB for monitoring the reference output
REFP	M4	1.5-V reference output in the internal reference mode. Must leave floated in the internal reference mode. TI recommends adding a test point on the PCB for monitoring the reference output
RESET	H9	Hardware reset pin with an internal pulldown resistor of 20 kΩ. Active high. The designer can use 3.3-V logic level.
SCLK	J9	Serial interface clock input with an internal pulldown resistor of 20 kΩ. This pin is connected to both ADC and VCA. The designer should use 3.3-V logic.
SDATA	K9	Serial interface data input with an internal pulldown resistor of 20 kΩ. This pin is connected to both ADC and VCA. The designer should use 3.3-V logic.
SDOUT	M9	Serial interface data readout. High impedance when readout is disabled. This pin is connected to ADC only. The designer can use 1.8-V logic.
SEN	L9	Serial interface enable with an internal pullup resistor of 20 kΩ. Active low. This pin is connected to both ADC and VCA. The designer should use 3.3-V logic.
SPI_DIG_EN	M7	Serial interface enable for the digital demodulator memory space. SPI_DIG_EN pin is required to be set to 0 during SPI transactions to demodulator registers. Each transaction starts by setting SEN as 0 and terminates by setting it back to 1 (similar to other register transactions). Pull up internally through a 20-kΩ resistor. This pin is connected to both ADC and VCA. The designer should use 3.3-V logic.
TX_SYNC_IN	L7	System trig signal input. It indicates the start of signal transmission. Either 3.3-V or 1.8-V logic level can be used. Note: TX_SYNC signal must be synchronized with ADC CLK. Typically, pulse repetition frequency (PRF) signal can be used for TX_SYNC_IN.
VCNTLM	K4	Negative differential attenuation control pin
VCNTLP	K3	Positive differential attenuation control pin
VHIGH	K5	Bias voltage; bypass to ground with ≥1 µF. Bias voltage = 1 V

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
VREF_IN	M3	ADC 1.4-V reference input in the external reference mode; bypass to ground with 0.1 µF.
DNC	L5	Do not connect. Must leave floated
	K7	
	M5	
	M8	

9 Specifications

9.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	3.9	V
	AVDD_ADC	–0.3	2.2	V
	AVDD_5V	–0.3	6	V
	DVDD	–0.3	2.2	V
	DVDD_LDO	–0.3	1.6	V
Voltage between AVSS and LVSS		–0.3	0.3	V
Voltage at CLKM_ADC, CLKP_ADC(2)		–0.3	min[2.2, AVDD_ADC+0.3]	V
Voltage at CLKM_16X, CLKP_16X, CLKM_1X, and CLKP_1X(2)		–0.3	min[5.5V, AVDD_5V+0.3]	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6, AVDD + 0.3]	V
Voltage at digital outputs		–0.3	min[2.2, DVDD+0.3]	V
Peak solder temperature(3)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Operating temperature		-40	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) When AVDD_ADC or AVDD_5V is turned off, TI recommends to switch off the input clock (or ensure the voltage on CLKP_ADC, CLKM_ADC is < |0.3V|). This prevents the ESD protection diodes at the clock input pins from turning on. CLKM/P_16X and CLKM/P_1X CLKs should follow the similar recommendations as well.
(3) Device complies with JSTD-020D.

9.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

9.3 Recommended Operating Conditions

	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
DVDD_LDO1/2 (External LDO mode)	1.4	1.5	V
AVDD_5V	4.75	5.5	V
T_A Ambient temperature	-40	85	°C

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9.4 Thermal Information

THERMAL METRIC(1)		AFE5812 BGA 135 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	10.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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9.5 Electrical Characteristics

AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500-Ω CW feedback resistor, CMOS CW clocks, at ambient temperature, T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TGC FULL SIGNAL CHANNEL (LNA + VCAT + LPF + ADC)						
en (RTI)	Input voltage noise over LNA gain (low-noise mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 24 dB		0.76, 0.83, 1.16		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 30 dB		0.75, 0.86, 1.12		
	Input voltage noise over LNA gain (low-power mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 24 dB		1.1, 1.2, 1.45		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 30 dB		1.1, 1.2, 1.45		
	Input voltage noise over LNA gain (medium-power mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 24 dB		1, 1.05, 1.25		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 15 dB, PGA = 30 dB		0.95, 1, 1.2		
en (RTI)	Input voltage noise at low frequency	f = 100 kHz, INM capacitor = 1 µF, PGA integrator disabled		0.9		nV/rtHz
	Input referred current noise	Low-noise mode/medium-power mode/low-power mode		2.7, 2.1, 2		pA/rtHz
NF	Noise figure	Rs = 200 Ω, 200-Ω active termination, PGA = 24 dB, LNA = 15, 18, 24 dB		3.85, 2.4, 1.8		dB
		Rs = 100 Ω, 100-Ω active termination, PGA = 24 dB, LNA = 15, 18, 24 dB		5.3, 3.1, 2.3		dB
NF	Noise figure	Rs = 500 Ω, 1 kΩ, no termination, low-NF mode is enabled (Reg53[9] = 1)		1.08, 0.94		dB
NF	Noise figure	Rs = 50 Ω / 200 Ω, no termination, low-noise mode (Reg53[9] = 0)		2.35, 1.05		dB
V_{MAX}	Maximum linear input voltage	LNA gain = 24, 18, 15 dB		250, 500, 700		mVpp
V_{CLAMP}	Clamp voltage	Reg52[10:9] = 0, LNA = 24, 18, 15 dB		350, 600, 825		mVpp
	PGA gain	Low-noise mode		24, 30		dB
		Medium-power/low-power mode		24, 28.5		dB
	Total gain	LNA = 24 dB, PGA = 30 dB, low-noise mode		54		dB
		LNA = 24 dB, PGA = 30 dB, medium-power mode		52.5		dB
		LNA = 24 dB, PGA = 30 dB, low-power mode		52.5		dB
	Ch-CH noise correlation factor without signal (1)	Summing of 8 channels		0		
	Ch-CH noise correlation factor with signal (1)	Full band (V_{CNTL} = 0, 0.8)		0.15, 0.17		
		1-MHz band over carrier (V_{CNTL}= 0, 0.8)		0.18, 0.75		
	Signal-to-noise ratio (SNR)	V_{CNTL}= 0.6 V (22-dB total channel gain)	68	70		dBFS
		V_{CNTL}= 0, LNA = 18 dB, PGA = 24 dB	58.3	63		dBFS
		V_{CNTL}= 0, LNA = 24 dB, PGA = 24 dB		58		dBFS
	Narrow-band SNR	SNR over 2-MHz band around carrier at V_{CNTL} = 0.6 V (22-dB total gain)	75	77		dBFS
	Input common-mode voltage	At INP and INM pins		2.2		V
	Input resistance			8		kΩ
		Preset active termination enabled		50,100,200,400		Ω
	Input capacitance			20		pF
	Input control voltage	$V_{CNTLP} – V_{CNTLM}$	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain range			–40		dB
	Gain slope	V_{CNTL}= 0.1 to 1.1 V		35		dB/V
	Input resistance	Between V_{CNTLP} and V_{CNTLM}		200		kΩ
	Input capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC response time	V_{CNTL}= 0- to 1.5-V step function		1.5		µs
	Third-order LPF			10, 15, 20, 30, 35, 50		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs

(1) Noise correlation factor is defined as Nc / (Nu + Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single-channel signal and the SNR of summed eight-channel signal are measured.

$$\frac{N_C}{Nu + N_C} = \frac{10^{-\frac{8CH_SNR}{10}}}{10^{-\frac{1CH_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

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Electrical Characteristics (continued)

AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500-Ω CW feedback resistor, CMOS CW clocks, at ambient temperature, T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY						
	LPF bandwidth tolerance			±5%		
	CH-CH group delay variation	2 to 15 MHz		2		ns
	CH-CH phase variation	15-MHz signal		11		°
	Gain matching	0 V < V_{CNTL}< 0.1 V (Dev-to-Dev)		±0.5		dB
		0.1 V < V_{CNTL}< 1.1 V(Dev-to-Dev)	–1.1	±0.5	1.1	
		1.1 V < V_{CNTL}< 1.5 V (Dev-to-Dev)		±0.5		
	Gain matching	Channel-to-channel		±0.25		dB
	Output offset	V_{CNTL}= 0, PGA = 24 dB, LNA = 18 dB	–100		100	LSB
AC PERFORMANCE						
HD2	Second-harmonic distortion	F_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–60		dBc
		F_{IN} = 5 MHz; V_{OUT} = –1 dBFS		–60		
		F_{IN} = 5 MHz; V_{IN}= 500 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL}= 0.88 V		–55		
		F_{IN} = 5 MHz; V_{IN} = 250 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 24 dB, V_{CNTL}= 0.88 V		–55		
HD3	Third-harmonic distortion	F_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–50		dBc
		F_{IN} = 5 MHz; V_{OUT} = –1 dBFS		–50		
		F_{IN} = 5 MHz; V_{IN} = 500 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL} = 0.88 V		–50		
		F_{IN} = 5 MHz; V_{IN} = 250 mV_{PP}, V_{OUT} = –1dBFS, LNA = 2 4dB, V_{CNTL}= 0.88 V		–50		
THD	Total harmonic distortion	F_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–50		dBc
		F_{IN} = 5 MHz; V_{OUT} = – 1dBFS		–50		
IMD3	Intermodulation distortion	f_1 = 5 MHz at –1 dBFS, f_2 = 5.01 MHz at –27 dBFS		–60		dBc
XTALK	Cross-talk	F_{IN} = 5 MHz; V_{OUT}= –1 dBFS		–65		dB
	Phase noise	kHz off 5 MHz (V_{CNTL}= 0 V)		–132		dBc/Hz
LNA						
	Input referred voltage noise	Rs = 0 Ω, f = 2 MHz, Rin = High Z, Gain = 24, 18, 15 dB		0.63, 0.70, 0.9		nV/rtHz
	High-pass filter (HPF)	–3 dB cut-off frequency		50, 100, 150, 200		kHz
	LNA linear output			4		Vpp
VCAT+ PGA						
	VCAT input noise	0-dB, –40-dB attenuation		2, 10.5		nV/rtHz
	PGA input noise	24 dB, 30 dB		1.75		nV/rtHz
	–3 dB HPF cut-off frequency			80		kHz

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Electrical Characteristics (continued)

AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500-Ω CW feedback resistor, CMOS CW clocks, at ambient temperature, T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CW DOPPLER						
en (RTI)	Input voltage noise (CW)	1-channel mixer, LNA = 24 dB, 500-Ω feedback resistor		0.8		nV/rtHz
		8-channel mixer, LNA = 24 dB, 62.5-Ω feedback resistor		0.33		
en (RTO)	Output voltage noise (CW)	1-channel mixer, LNA = 24 dB, 500-Ω feedback resistor		12		nV/rtHz
		8-channel mixer, LNA = 24 dB, 62.5-Ω feedback resistor		5		
en (RTI)	Input voltage noise (CW)	1-channel mixer, LNA = 18 dB, 500-Ω feedback resistor		1.1		nV/rtHz
		8-channel mixer, LNA = 18 dB, 62.5-Ω feedback resistor		0.5		
en (RTO)	Output voltage noise (CW)	1-channel mixer, LNA = 18 dB, 500-Ω feedback resistor		8.1		nV/rtHz
		8-channel mixer, LNA = 18 dB, 62.5-Ω feedback resistor		4.0		
NF	Noise figure	Rs = 100 Ω, R_{IN} = High Z, F_{IN} = 2 MHz (LNA, I/Q mixer and summing amplifier/filter)		1.8		dB
f_{CW}	CW operation range (2)	CW signal carrier frequency		8		MHz
	CW clock frequency	1× CLK (16× mode)			8	MHz
		16× CLK(16× mode)			128	
		4× CLK(4× mode)		32		
	AC coupled differential clock amplitude (3)	CLKM_16X-CLKP_16X; CLKM_1X-CLKP_1X; LVDS, LVPECL	0.4	0.7		Vpp
	CLK duty cycle	1× and 16× CLKs	35%		65%	
	Common-mode voltage	Internal provided		2.5		V
V_{CMOS}	CMOS input clock amplitude		4		5	V
	CW mixer conversion loss			4		dB
	CW mixer phase noise	1 kHz off 2-MHz carrier		156		dBc/Hz
DR	Input dynamic range	F_{IN} = 2 MHz, LNA = 24/18/15 dB		160, 164, 165		dBFS/Hz
IMD3	Intermodulation distortion	f_1 = 5.00 MHz, f_2 = 5.01 MHz, both tones at –8.5-dBm amplitude, 8 channels summed up in-phase, CW feedback resistor = 87 Ω		–50		dBc
		f_1 = 5 MHz, f_2= 5.01 MHz, both tones at –8.5-dBm amplitude, single-channel case, CW feedback resistor = 500 Ω		–60		dBc
	I/Q channel gain matching	16× mode		±0.04		dB
	I/Q channel phase matching	16× mode		±0.1		°
	I/Q channel gain matching	4× mode		±0.04		dB
	I/Q channel phase matching	4× mode		±0.1		°
	Image rejection ratio	F_{IN} = 2.01 MHz, 300-mV input amplitude, CW clock frequency = 2 MHz		–50		dBc
CW SUMMING AMPLIFIER						
V_{CMO}	Common-mode voltage	Summing amplifier inputs/outputs		1.5		V
	Summing amplifier output			4		Vpp
	Input referred voltage noise	100 Hz		2		nV/rtHz
		1 kHz		1.2		nV/rtHz
		2 kHz to 100 MHz		1		nV/rtHz
	Input referred current noise			2.5		pA/rtHz
	Unit gain bandwidth			200		MHz
	Max output current	Linear operation range		20		mApp
ADC SPECIFICATIONS						
	Sample rate		10		65	MSPS
SNR	Signal-to-noise ratio	Idle channel SNR of ADC 14b		77		dBFS
	Internal reference mode	REFP		1.5		V
		REFM		0.5		V

(2) In the 16× operation mode, the CW operation range is limited to 8 MHz due to the 16× CLK. The maximum clock frequency for the 16× CLK is 128 MHz. In the 8×, 4×, and 1× modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, see application information: *CW Clock Selection*.
(3) Clocks with fast slew rate achieves desired phase noise. 5V CMOS clock achieves the best performance in terms of phase noise. See CW Clock Selection

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Electrical Characteristics (continued)

AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500-Ω CW feedback resistor, CMOS CW clocks, at ambient temperature, T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External reference mode	VREF_IN voltage		1.4		V
	VREF_IN current		50		µA
ADC input full-scale range			2		Vpp
LVDS rate	65 MSPS at 14 bit		910		Mbps
POWER DISSIPATION					
AVDD voltage		3.15	3.3	3.6	V
AVDD_ADC voltage		1.7	1.8	1.9	V
AVDD_5V voltage		4.75	5	5.5	V
DVDD voltage		1.7	1.8	1.9	V
Total power dissipation per channel	TGC low-noise mode, 65 MSPS		180	214	mW/CH
	TGC low-noise mode, 40 MSPS		163		
	TGC medium-power mode, 40 MSPS		125		
	TGC low-power mode, 40 MSPS		109		
AVDD (3.3-V) current	TGC low-noise mode, no signal		108	130	mA
	TGC medium-power mode, no signal		68		
	TGC low-power mode, no signal		59		
	CW-mode, no signal, 16x clock = 80MHz		49		
	TGC low-noise mode, 500 mV_{PP} Input,1% duty cycle		116		
	TGC medium-power mode, 500 mV_{PP} Input, 1% duty cycle		75		
	TGC low power, 500 mV_{PP} Input, 1% duty cycle		65		
	CW-mode, 500 mV_{PP} Input to all 8 channels		281		
AVDD_5V current	TGC mode no signal		116	140	mA
	CW mode no signal, 16× clock = 80 MHz		139		
	TGC mode, 500 mVpp Input,1% duty cycle		116.5		
	CW-mode, 500 mVpp input		148		
VCA power dissipation	TGC low-noise mode, no signal		117	142	mW/CH
	TGC medium-power mode, no signal		79		
	TGC low-power mode, no signal		63		
	TGC low-noise mode, 500 mV_{PP} input,1% duty cycle		121		
	TGC medium-power mode, 500 mV_{PP} Input, 1% duty cycle		82		
	TGC low-power mode, 500 mVpp input,1% duty cycle		67		
CW power dissipation	No signal, ADC shutdown CW mode no signal, 16× clock = 80 MHz		107		mW/CH
	500 mV_{PP} input, ADC shutdown , 16× clock = 80 MHz		209		
AVDD_ADC (1.8-V) current	65MSPS		187	220	mA
DVDD (1.8-V) current	65 MSPS		90	110	mA
ADC power dissipation/CH	65 MSPS		59	69	mW/CH
	50 MSPS		51		
	40 MSPS		46		
	20 MSPS		35		
Power dissipation in power down mode	PDN_VCA = High, PDN_ADC = High		25		mW/CH
	Complete power-down PDN_Global = High		0.675		
Power-down response time	Time taken to enter power down		1		µs
Power-up response time	VCA power down		2 µs + 1% of PDN time		µs
	ADC power down		1		
	Complete power down		2.5		ms
Power supply modulation ratio, AVDD and AVDD_5V	F_{IN} = 5 MHz, at 50 mV_{PP} noise at 1 kHz on supply(4)		–65		dBc
	F_{IN} = 5 MHz, at 50 mVpp noise at 50 kHz on supply(4)		–65		

(4) PSMR specification is with respect to carrier signal amplitude.

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Electrical Characteristics (continued)

AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500-Ω CW feedback resistor, CMOS CW clocks, at ambient temperature, T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rejection ratio	f = 10 kHz,V_{CNTL} = 0 V (high gain), AVDD		–40		dBc
	f = 10 kHz,V_{CNTL} = 0 V (high gain), AVDD_5 V		–55		dBc
	f = 10 kHz,V_{CNTL} = 1 V (low gain), AVDD		–50		dBc

9.6 Digital Demodulator Electrical Characteristics

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, DVDD_LDO = 1.4 V (internal generated), 14 bit/65 MSPS, 4× decimation factor, at ambient temperature T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Additional power consumption on DVDD (1.8 V)	65 MSPS, 4× decimation factor		92		mW/CH
	Additional current on DVDD (1.8V)	65 MSPS, 4× decimation factor		410		mA/AFE
	Additional power consumption on DVDD (1.8 V)	40 MSPS, 4× decimation factor		61		mW/CH
	Additional power consumption on DVDD (1.8 V)	65 MSPS, 32× decimation factor, half LVDS pairs are powered down		79		mW/CH
	Additional power consumption on DVDD (1.8 V)	40 MSPS, 32× decimation factor, half LVDS pairs are powered down		55		mW/CH
	External DVDD_LDO1, DVDD_LDO2	65 MSPS, 4× decimation factor	1.4	1.45	1.5	V
	Additional current on external DVDD_LDO1+DVDD_LDO2	65 MSPS, 4× decimation factor		300		mA/AFE
V_{IH}	Logic high input voltage, TX_SYNC pin	Support 1.8-V and 3.3-V CMOS logic	1.3		3.3	V
V_{IL}	Logic low input voltage, TX_SYNC pin	Support 1.8-V and 3.3-V CMOS logic	0		0.3	V
I_{IH}	Logic high input current, TX_SYNC pin	V_{HIGH} = 1.8 V		11		µA
I_{IL}	Logic low input current, TX_SYNC pin	V_{LOW} = 0 V		< 0.1		µA

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9.7 Digital Characteristics

Typical values are at 25°C, AVDD = 3.3 V, AVDD_5 = 5 V and AVDD_ADC = 1.8 V, DVDD = 1.8 V unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = -40°C to T_{MAX} = 85°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		DVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V
LVDS OUTPUTS						
	Output differential voltage	With 100-Ω external differential termination		400		mV
	Output offset voltage	Common-mode voltage		1100		mV
	FCLKP and FCLKM	1× clock rate	10		65	MHz
	DCLKP and DCLKM	7× clock rate	70		455	MHz
		6× clock rate	60		390	MHz
t_{su}	Data setup time(2)			350		ps
t_h	Data hold time(2)			350		ps
ADC INPUT CLOCK						
	Clock frequency		10		65	MSPS
	Clock duty cycle		45%	50%	55%	
	Clock input amplitude, differential($V_{CLKP_ADC} - V_{CLKM_ADC}$)	Sine-wave, AC-coupled	0.5			Vpp
		LVPECL, LVDS, AC-coupled		>0.3		Vpp
	Common-mode voltage	Biased internally		1		V
	Clock input amplitude V_{CLKP_ADC} (single-ended)	CMOS clock		1.8		Vpp

(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1 with 100-Ω external termination.
(2) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins

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9.8 Timing Characteristics(1)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V. Typical values are at 25°C, Differential clock, C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, 14 bit, sample rate = 65 MSPS, digital demodulator is disabled, unless otherwise noted. Minimum and maximum values are across the full temperature range T_{MIN} = -40°C to T_{MAX} = 85°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		Fs rms
	ADC latency	Default, after reset, or / 0 x 2 [12] = 1, LOW_LATENCY = 1		11/8		Input clock cycles
t_{delay}	Data and frame clock delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T)	3	5.4	7	ns
Δt_{delay}	Delay variation	At fixed supply and 20°C T difference; device to device	–1		1	ns
t_{RISE}	Data rise time	Rise time measured from –100 to 100 mV		0.14		ns
t_{FALL}	Data fall time	Fall time measured from 100 to –100 mV 10 MHz < f_{CLKIN} < 65 MHz		0.15		
$t_{FCLKRISE}$	Frame clock rise time	Rise time measured from –100 to 100 mV		0.14		ns
$t_{FCLKFALL}$	Frame clock fall time	Fall time measured from 100 to –100 mV 10 MHz < f_{CLKIN} < 65 MHz		0.15		
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48%	50%	52%	
$t_{DCLKRISE}$	Bit clock rise time	Rise time measured from –100 to 100 mV		0.13		ns
$t_{DCLKFALL}$	Bit clock fall time	Fall time measured from 100 to –100 mV 10 MHz < f_{CLKIN} < 65 MHz		0.12		
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10 MHz < f_{CLKIN} < 65 MHz	46%		54%	

(1) Timing parameters are ensured by design and characterization; not production tested.

9.9 Output Interface Timing (14-bit)(1)(2)(3)

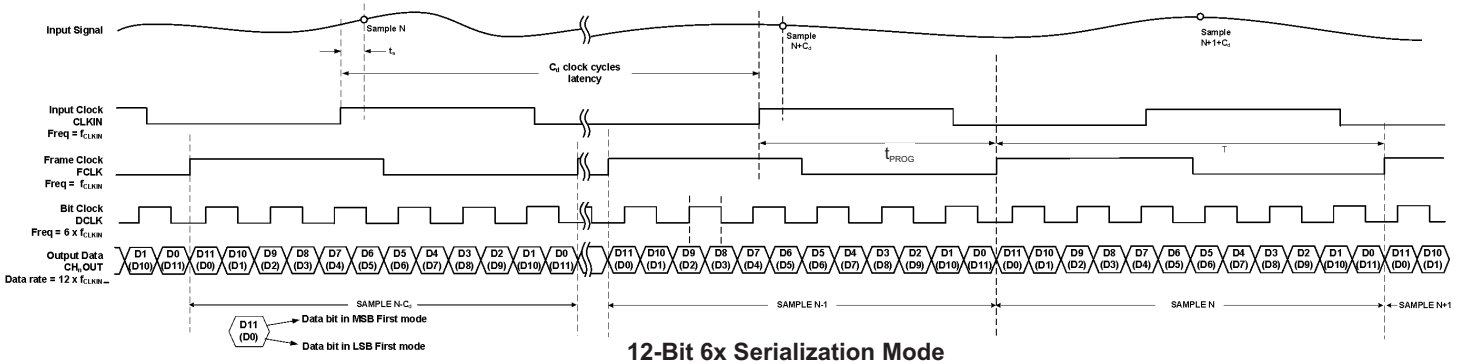
f_{CLKIN}, Input Clock Frequency	Setup Time (t_{su}), ns			Hold Time (t_h), ns			t_{PROG} = (3/7) × T + t_{delay}, ns		
	Data Valid to Bit Clock Zero-Crossing			Bit Clock Zero-Crossing to Data Invalid			Input Clock Zero-Cross (Rising Edge) to Frame Clock Zero-Cross (Rising Edge)		
MHz	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	0.24	0.37		0.24	0.38		11	12	12.5
50	0.41	0.54		0.46	0.57		13	13.9	14.4
40	0.55	0.70		0.61	0.73		15	16	16.7
30	0.87	1.10		0.94	1.1		18.5	19.5	20.1
20	1.30	1.56		1.46	1.6		25.7	26.7	27.3

(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and frame clock.
(2) Data valid is logic high = 100 mV and logic low = –100 mV
(3) Timing parameters are ensured by design and characterization; not production tested.

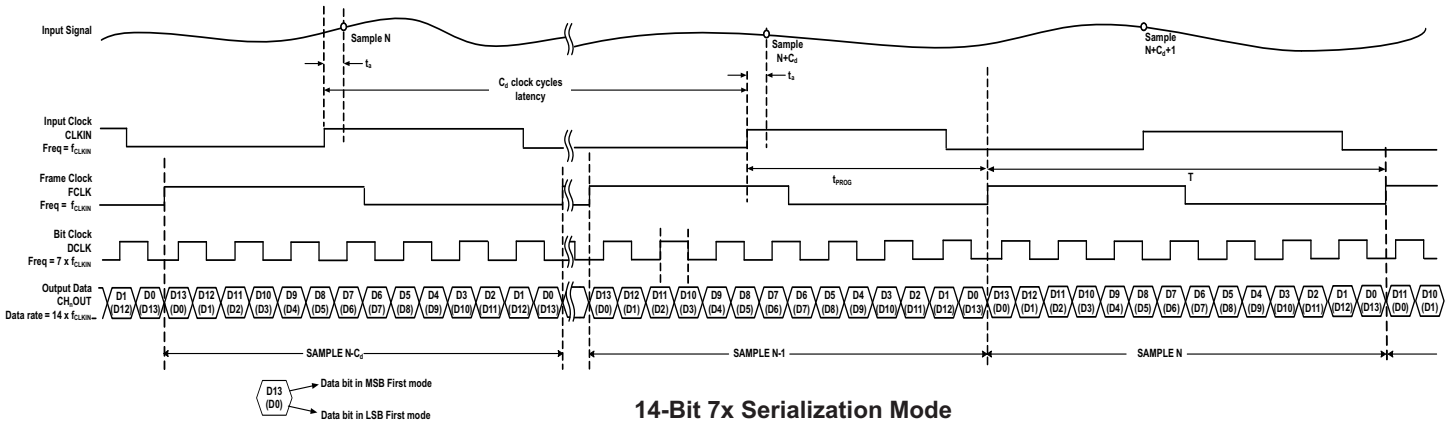
NOTE

The above timing data can be applied to 12-bit or 16-bit LVDS rates as well. For example, the maximum LVDS output rate at 65 MHz and 14-bit is equal to 910 MSPS, which is approximately equivalent to the rate at 56 MHz and 16 bits.

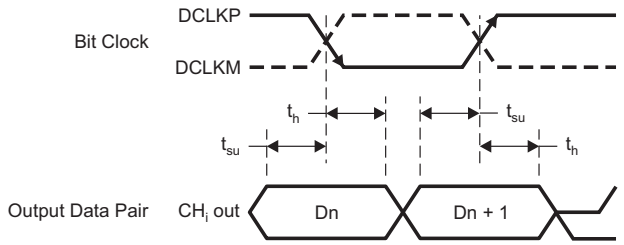
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12-Bit 6x Serialization Mode



14-Bit 7x Serialization Mode



T0434-01

LVDS Setup and Hold Timing

Figure 1. LVDS Timing Diagrams

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9.10 SPI Timing Characteristics

Minimum values across full temperature range T_{MIN} = -40°C to T_{MAX} = 85°C, AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{SEN}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{SEN}$ rising edge	8			ns
t_8	SDOUT delay	12	20	28	ns

9.11 Typical Characteristics

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

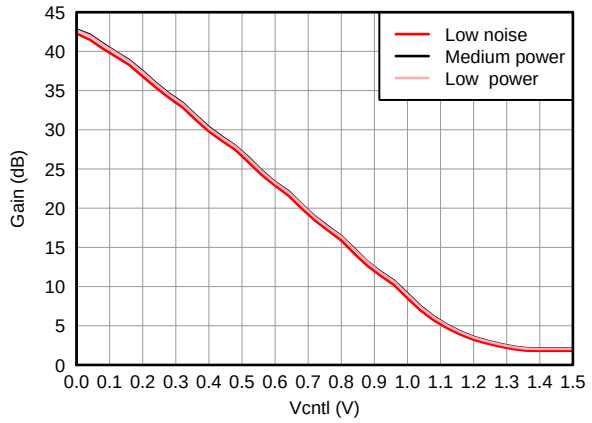


Figure 2. Gain vs V_{CNTL}, LNA = 18 dB and PGA = 24 dB

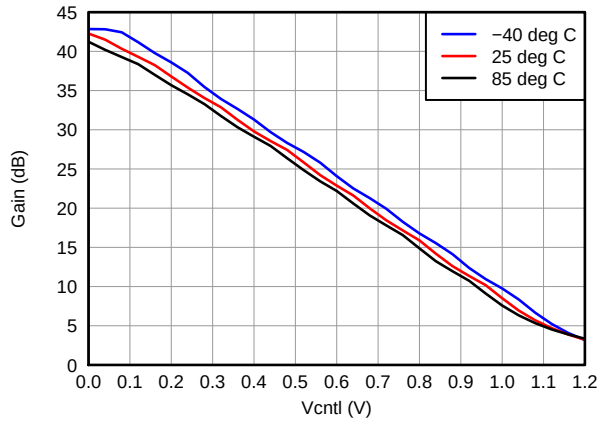


Figure 3. Gain Variation vs Temperature, LNA = 18 dB and PGA = 24 dB

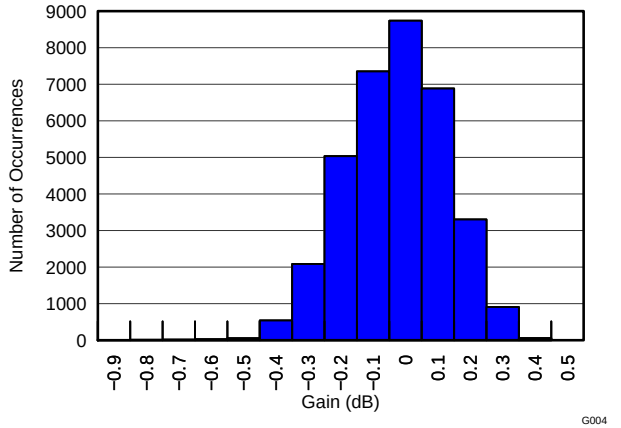


Figure 4. Gain Matching Histogram, V_{CNTL} = 0.3 V (34951 Channels)

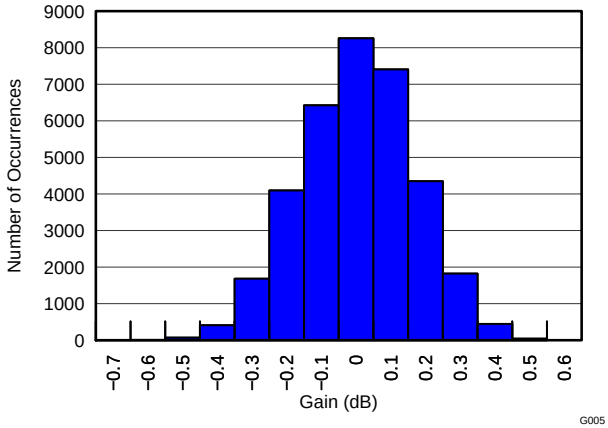


Figure 5. Gain Matching Histogram, V_{CNTL} = 0.6 V (34951 Channels)

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

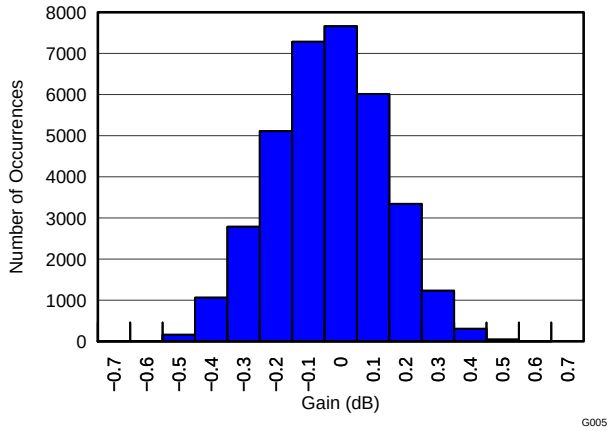


Figure 6. Gain Matching Histogram, V_{CNTL} = 0.9 V (34951 Channels)

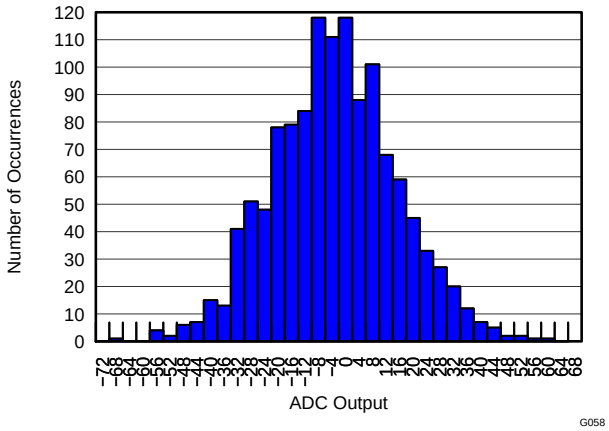


Figure 7. Output Offset Histogram, V_{CNTL} = 0 V (1247 Channels)

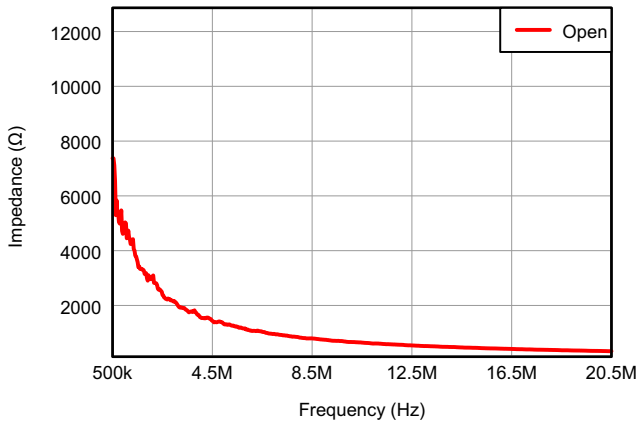


Figure 8. Input Impedance Without Active Termination (Magnitude)

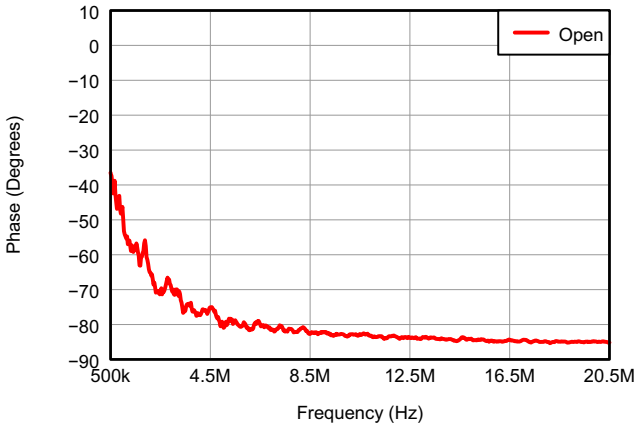


Figure 9. Input Impedance Without Active Termination (Phase)

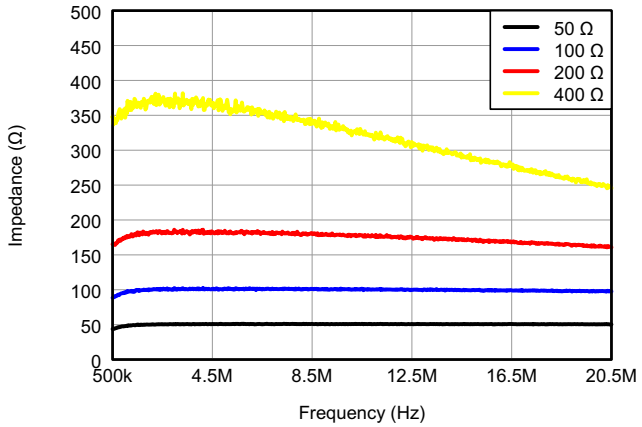


Figure 10. Input Impedance With Active Termination (Magnitude)

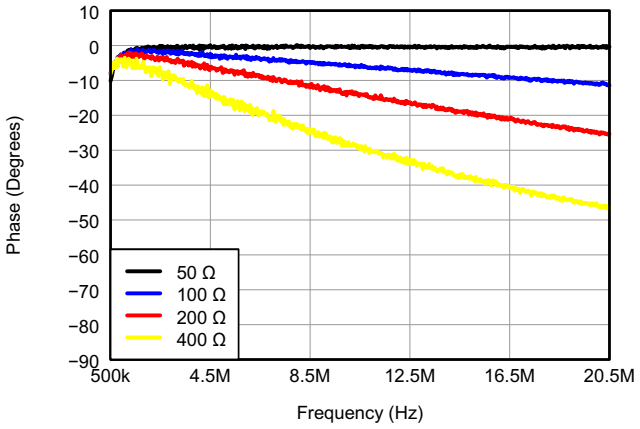


Figure 11. Input Impedance With Active Termination (Phase)

Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

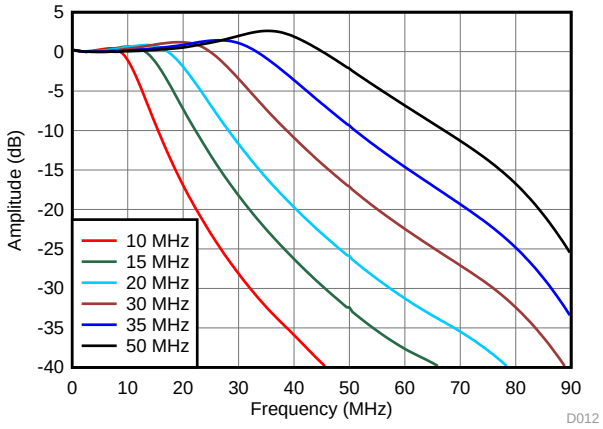


Figure 12. LPF Response

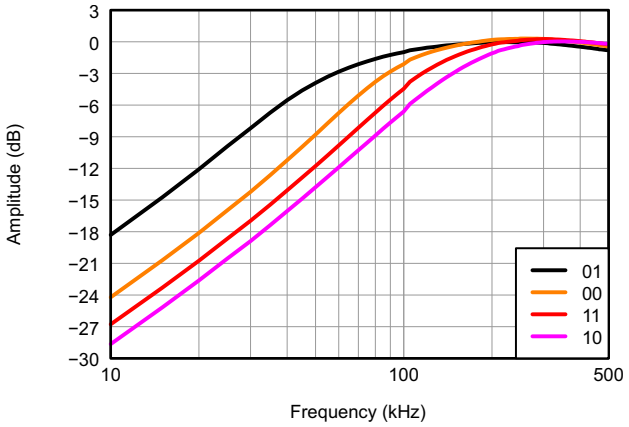


Figure 13. LNA HPF Response vs Reg59[3:2]

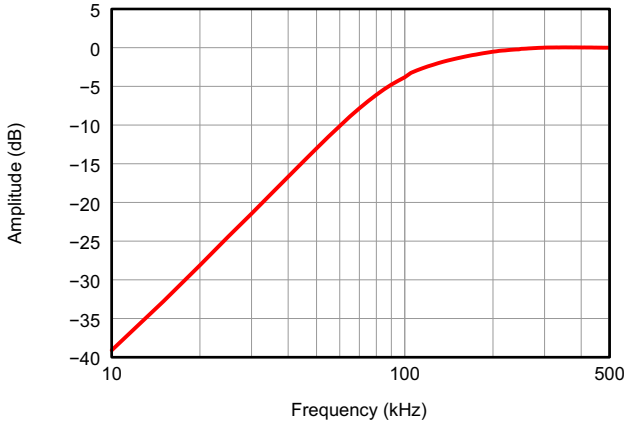


Figure 14. Full Channel HPF Response at Default Register Setting

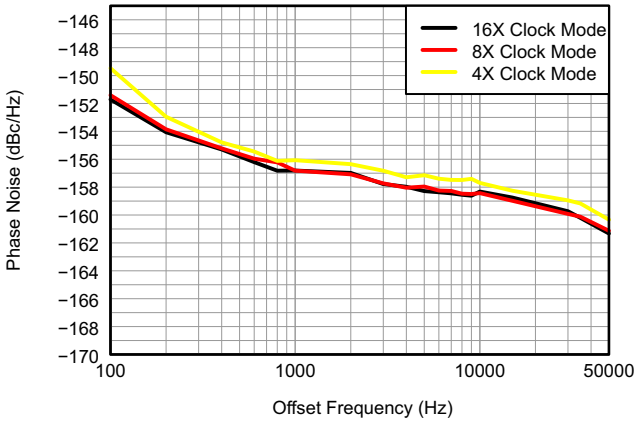


Figure 15. CW Phase Noise, F_{IN} = 2 MHz

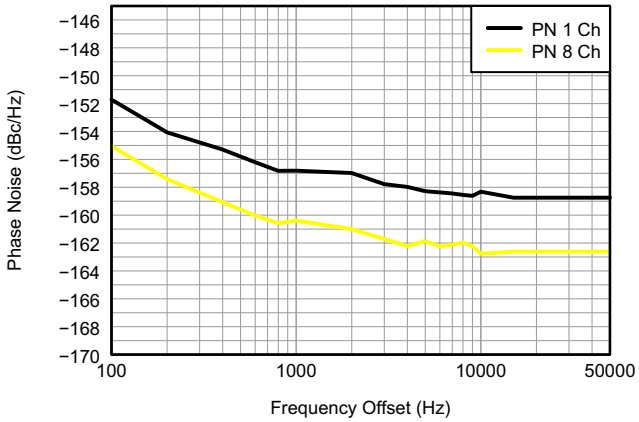


Figure 16. CW Phase Noise, F_{IN} = 2 MHz, 1 Channel vs 8 Channel

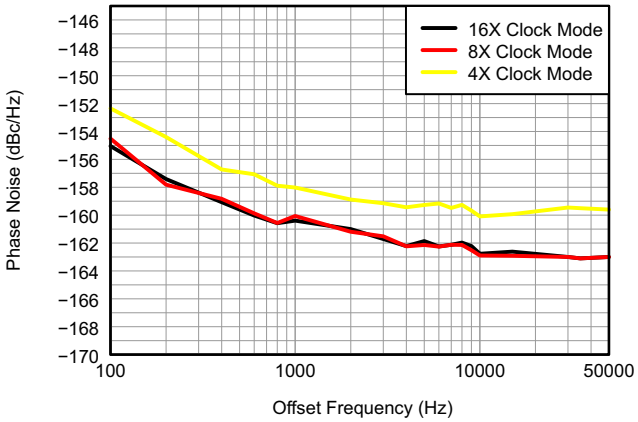


Figure 17. CW Phase Noise vs Clock Modes, F_{IN}= 2 MHz

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

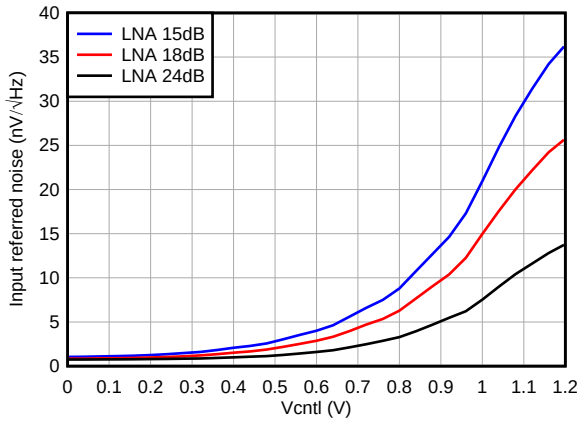


Figure 18. IRN, PGA = 24 dB and Low Noise Mode

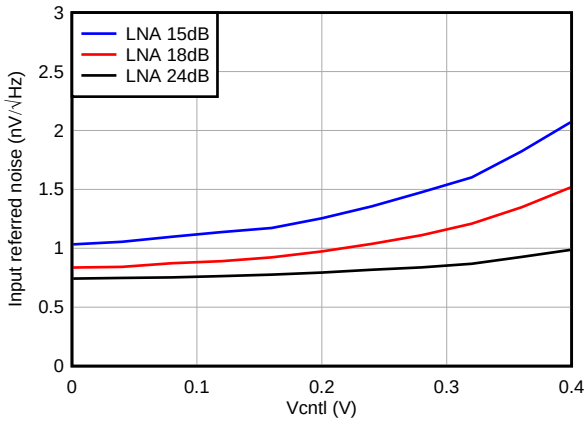


Figure 19. IRN, PGA = 24 dB and Low Noise Mode

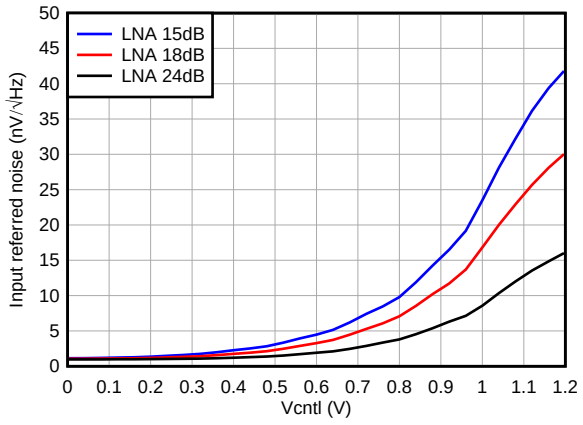


Figure 20. IRN, PGA = 24 dB and Medium-Power Mode

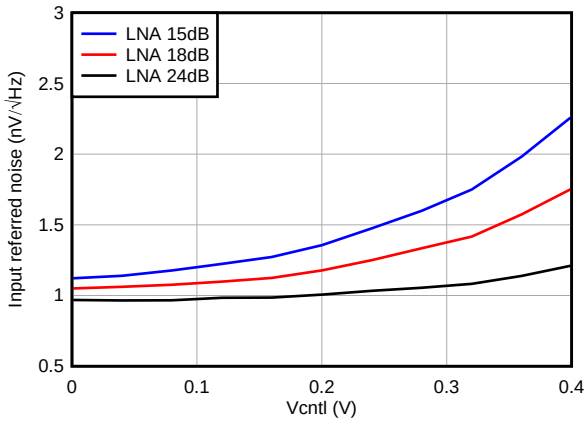


Figure 21. IRN, PGA = 24 dB and Medium-Power Mode

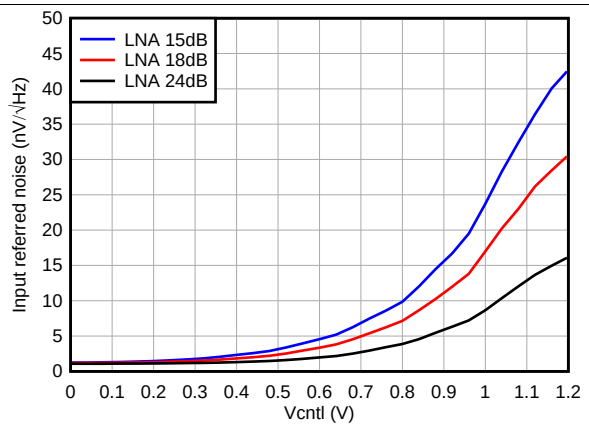


Figure 22. IRN, PGA = 24 dB and Low-Power Mode

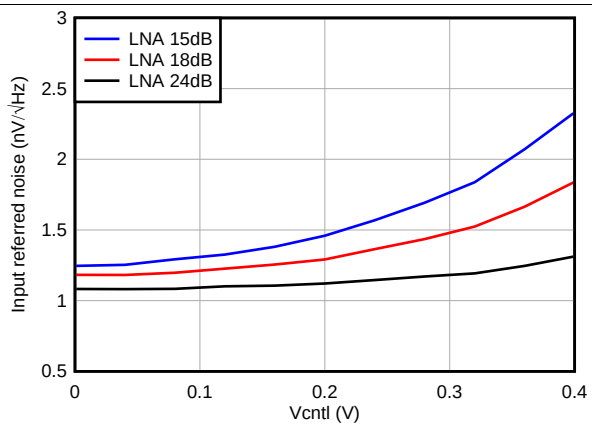


Figure 23. IRN, PGA = 24 dB and Low-Power Mode

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

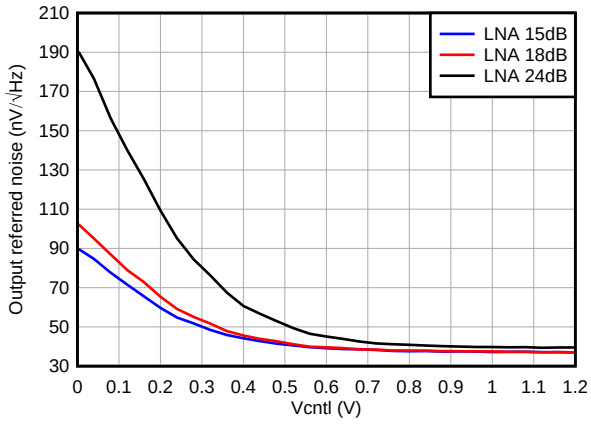


Figure 24. ORN, PGA = 24 dB and Low Noise Mode

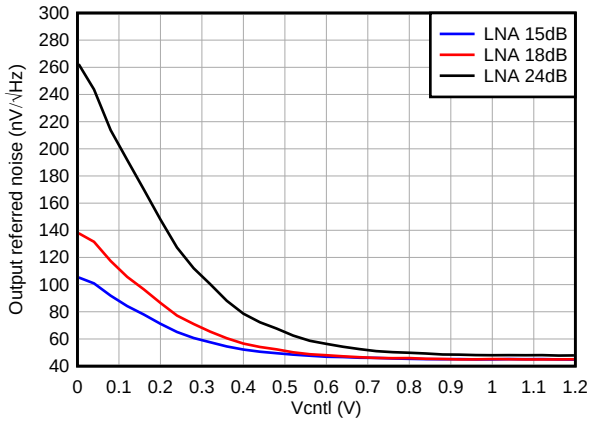


Figure 25. ORN, PGA = 24 dB and Medium-Power Mode

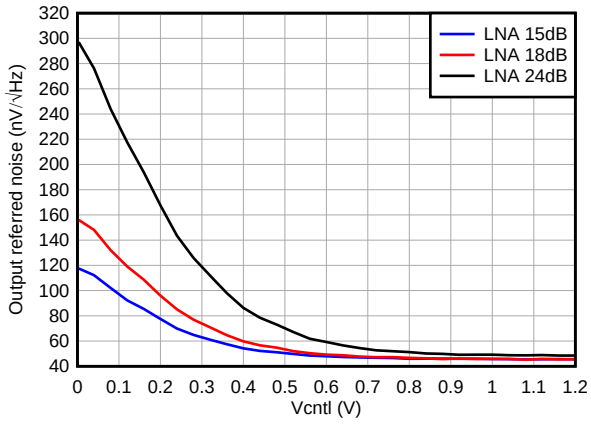


Figure 26. ORN, PGA = 24 dB and Low-Power Mode

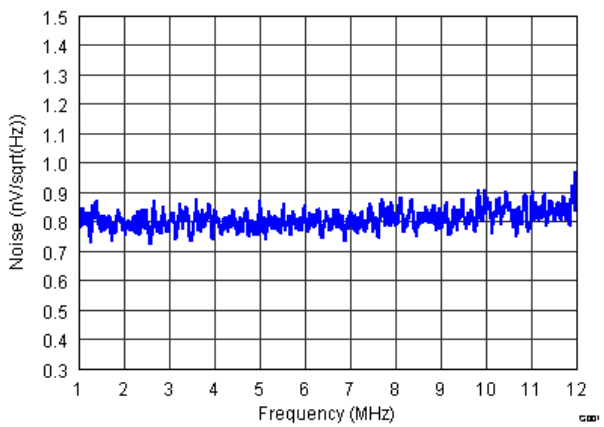


Figure 27. IRN, PGA = 24 dB and Low Noise Mode

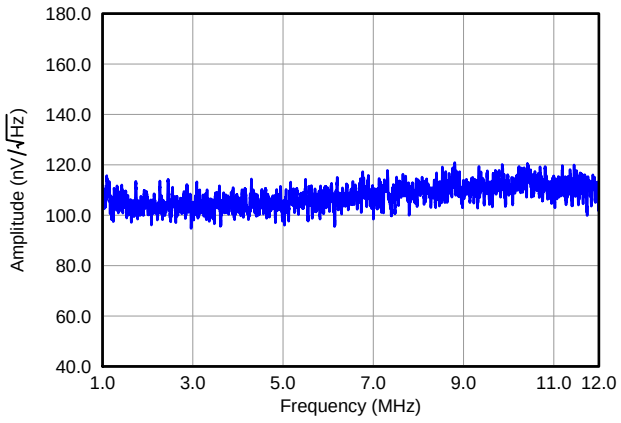


Figure 28. ORN, PGA = 24 dB and Low Noise Mode

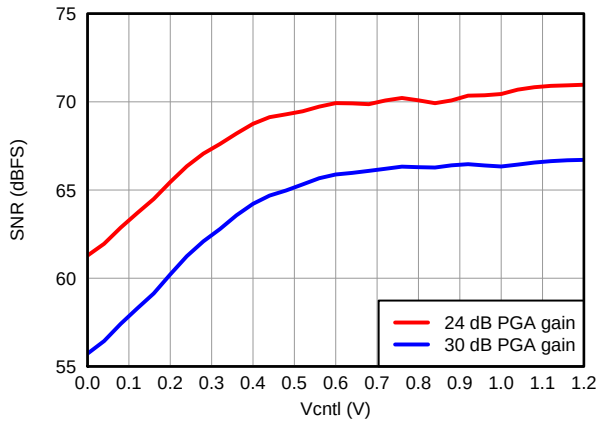


Figure 29. SNR, LNA = 18 dB and Low Noise Mode

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

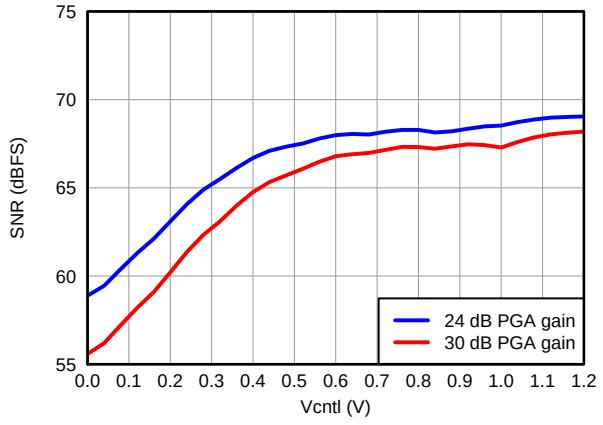


Figure 30. SNR, LNA = 18 dB and Low-Power Mode

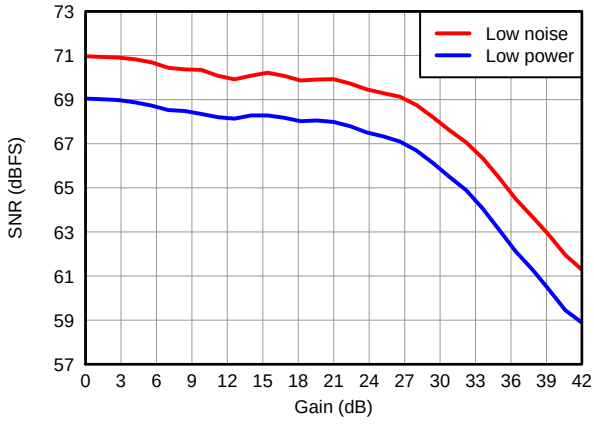


Figure 31. SNR vs Different Power Modes

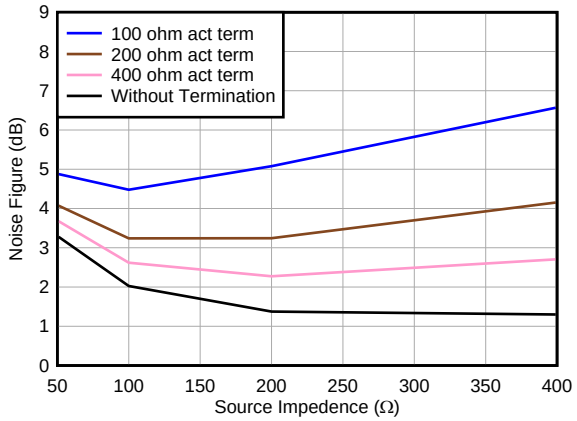


Figure 32. Noise Figure, LNA = 15 dB and Low Noise Mode

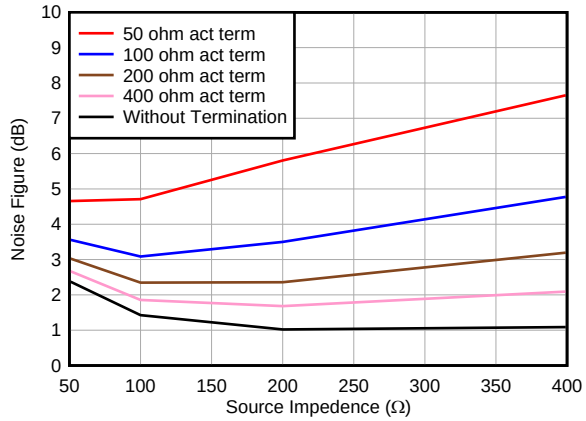


Figure 33. Noise Figure, LNA = 18 dB and Low Noise Mode

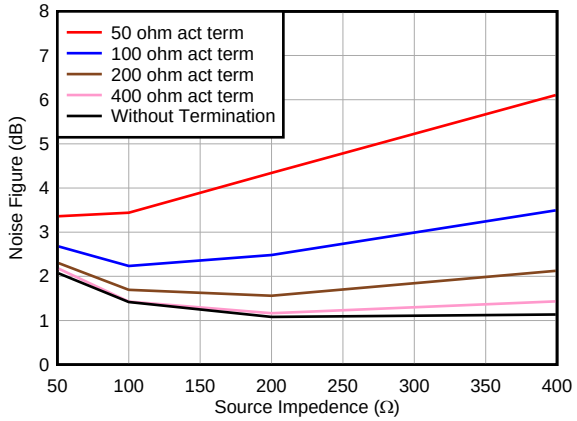


Figure 34. Noise Figure, LNA = 24 dB and Low Noise Mode

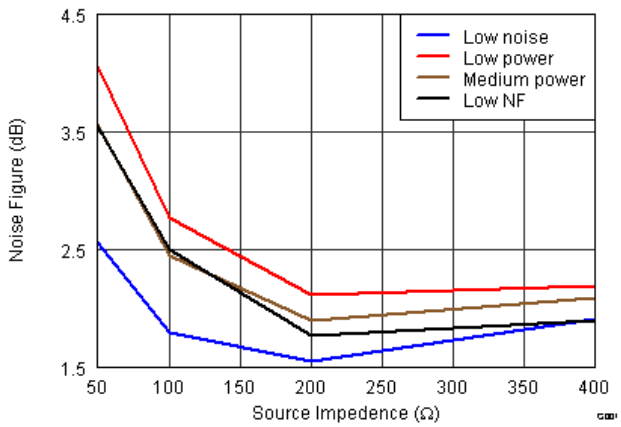


Figure 35. Noise Figure vs Power Modes With 400-Ω Termination

Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

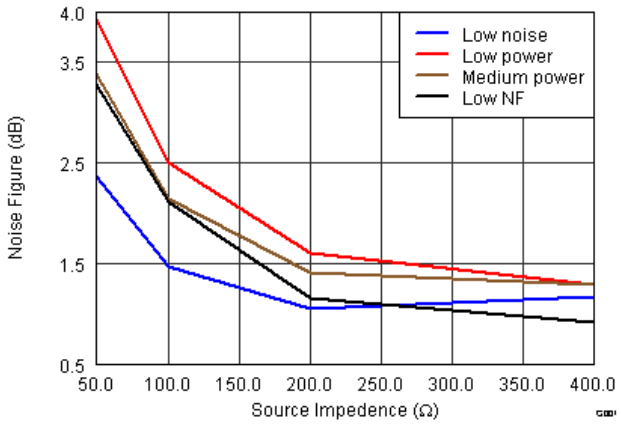


Figure 36. Noise Figure vs Power Modes Without Termination

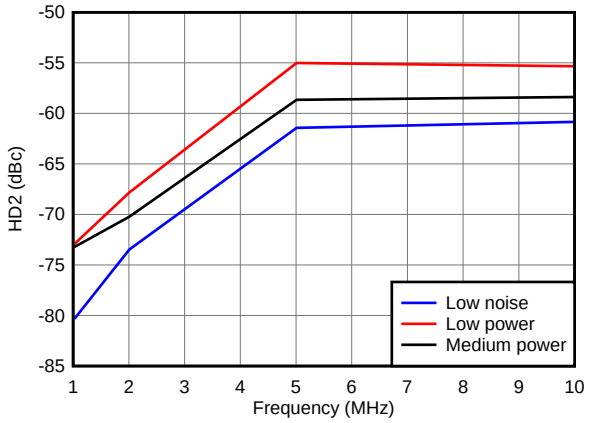


Figure 37. HD2 vs Frequency, V_{IN} = 500 mVpp and V_{OUT} = –1 dBFS

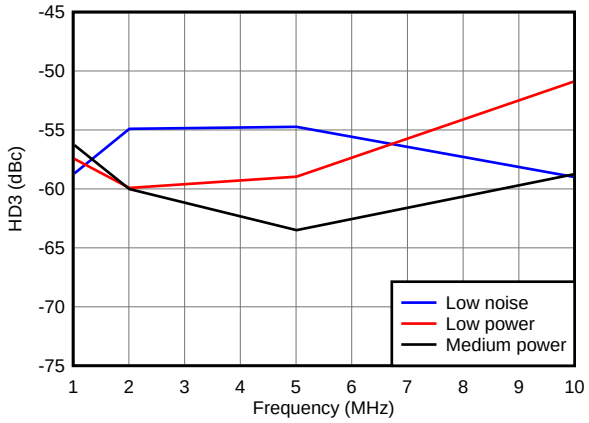


Figure 38. HD3 vs Frequency, V_{IN} = 500 mVpp and V_{OUT} = –1 dBFS

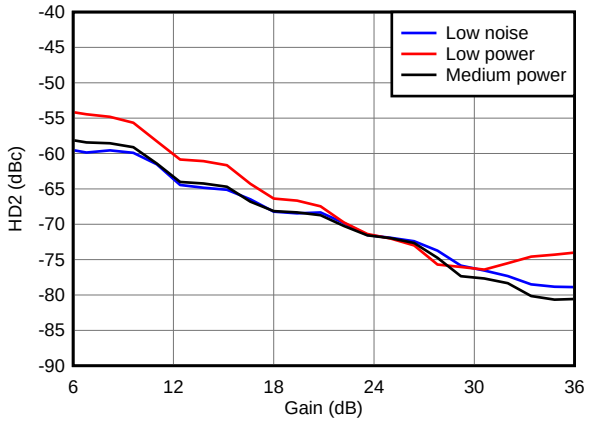


Figure 39. HD2 vs Gain, LNA = 15 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

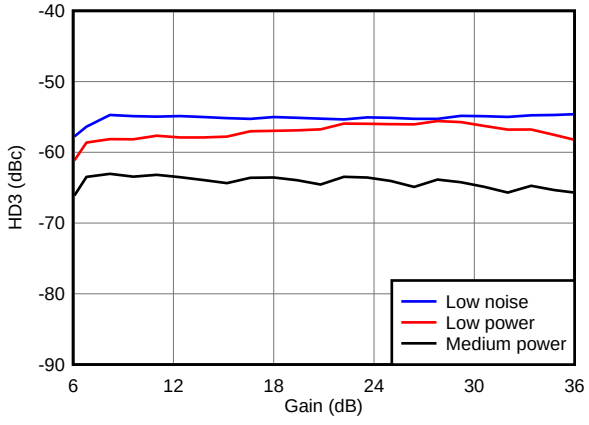


Figure 40. HD3 vs Gain, LNA = 15 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

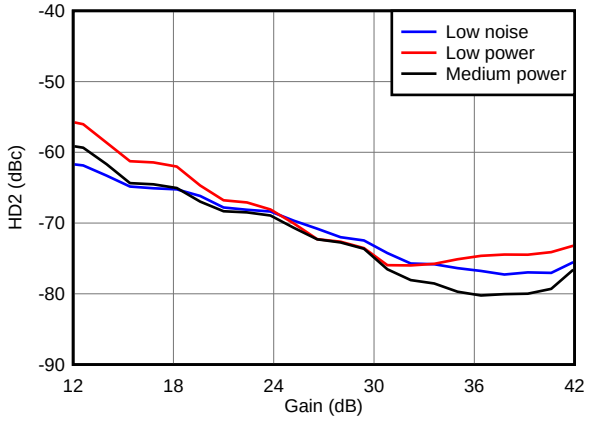


Figure 41. HD2 vs Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

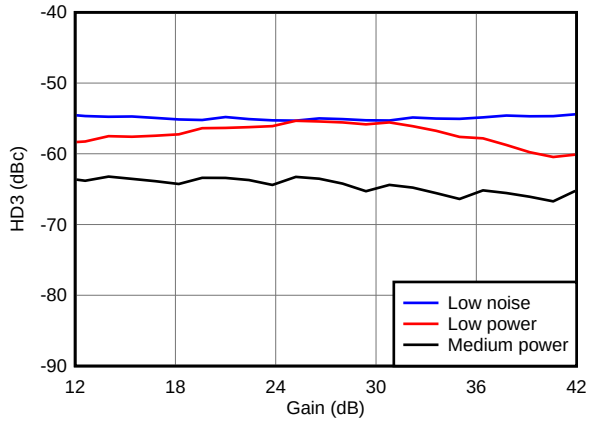


Figure 42. HD3 vs Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

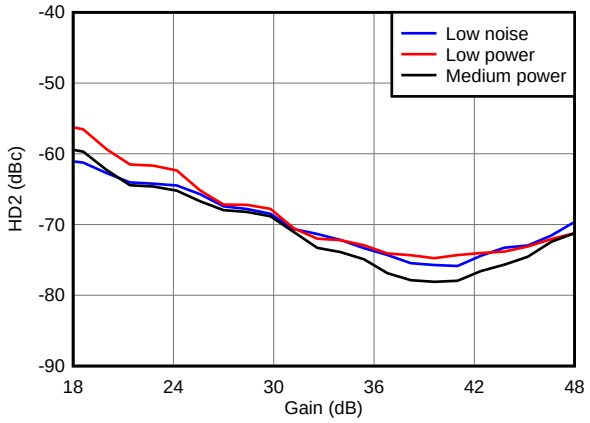


Figure 43. HD2 vs Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

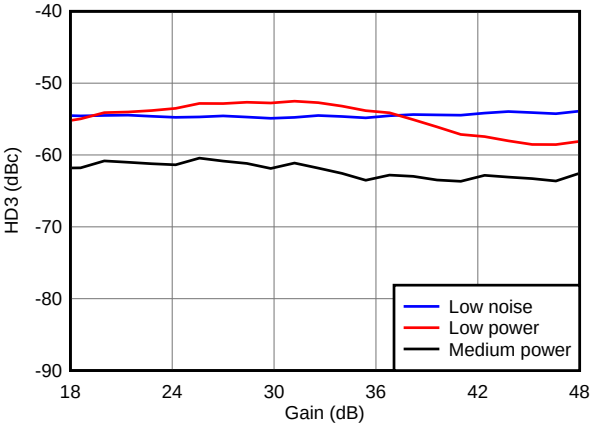


Figure 44. HD3 vs Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

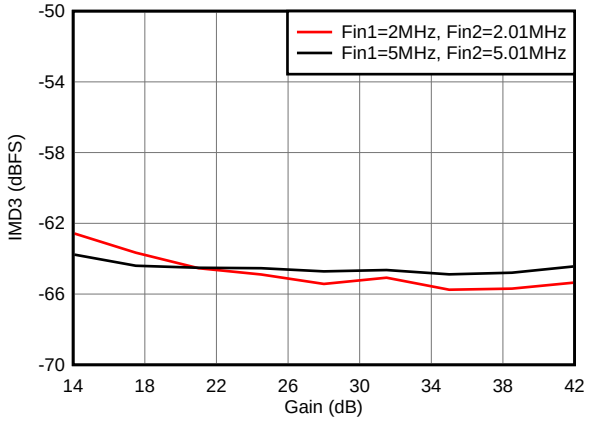


Figure 45. IMD3, Fout1 = –7 dBFS and Fout2 = –21 dBFS

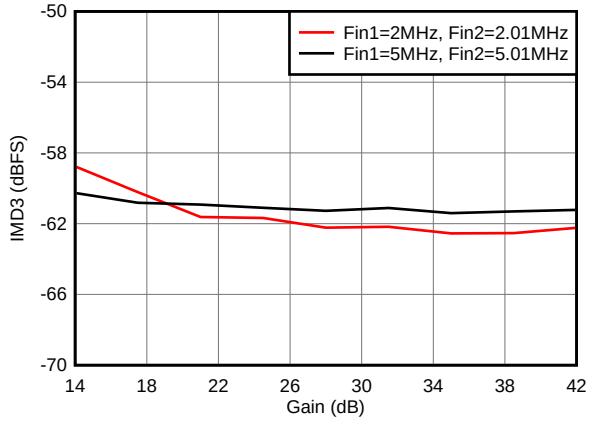


Figure 46. IMD3, Fout1 = –7 dBFS and Fout2 = –7 dBFS

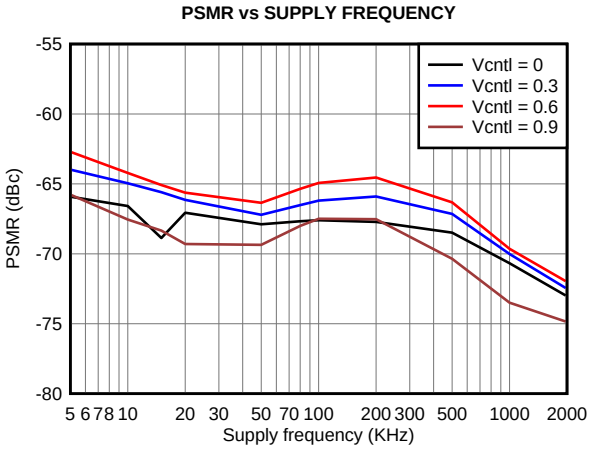


Figure 47. AVDD Power Supply Modulation Ratio, 100 mVpp Supply Noise With Different Frequencies

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

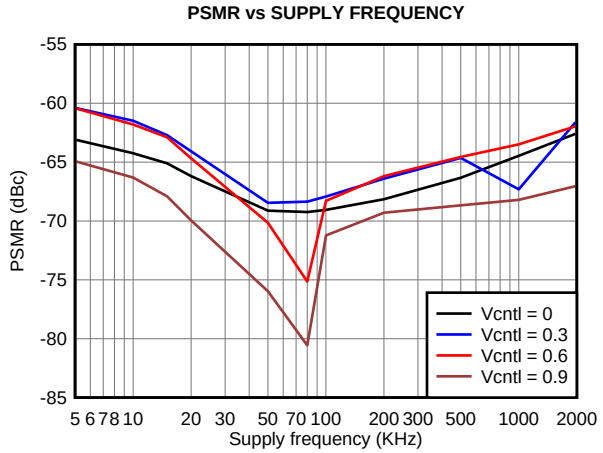


Figure 48. AVDD_5V Power Supply Modulation Ratio, 100 mVpp Supply Noise With Different Frequencies

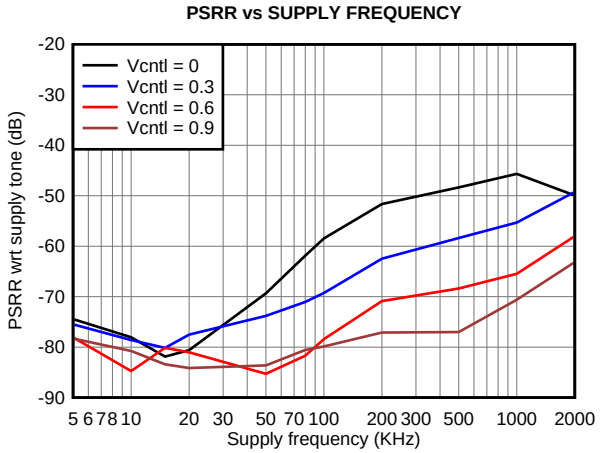


Figure 49. AVDD Power Supply Rejection Ratio, 100 mVpp Supply Noise With Different Frequencies

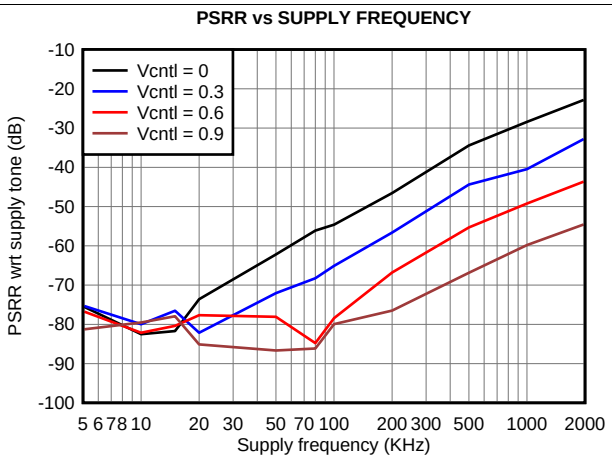


Figure 50. AVDD_5V Power Supply Rejection Ratio, 100 mVpp Supply Noise With Different Frequencies

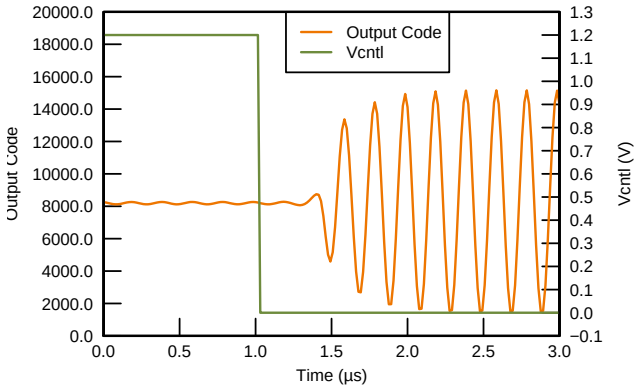


Figure 51. V_{CNTL} Response Time, LNA = 18 dB and PGA = 24 dB

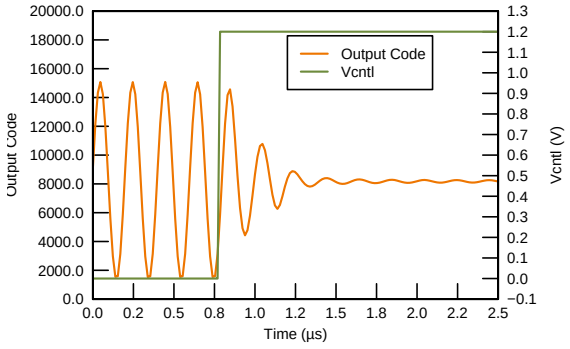


Figure 52. V_{CNTL} Response Time, LNA = 18 dB and PGA = 24 dB

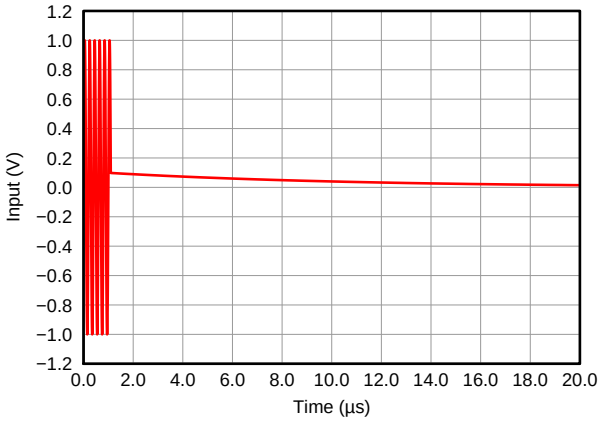


Figure 53. Pulse Inversion Asymmetrical Positive Input

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Typical Characteristics (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1-µF capacitors at INP and 15-nF capacitors at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16× clock, digital demodulator is disabled, at ambient temperature T_A = 25°C, unless otherwise noted.

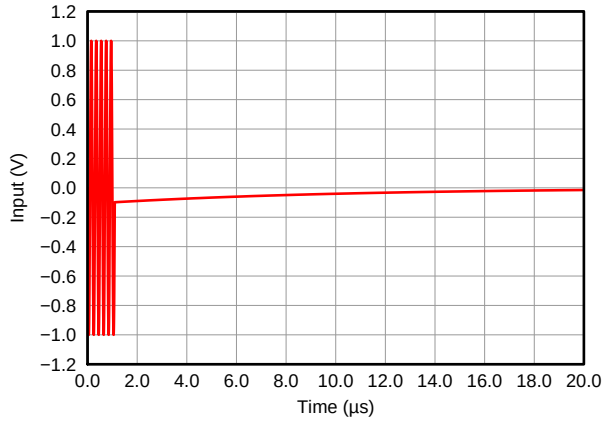


Figure 54. Pulse Inversion Asymmetrical Negative Input

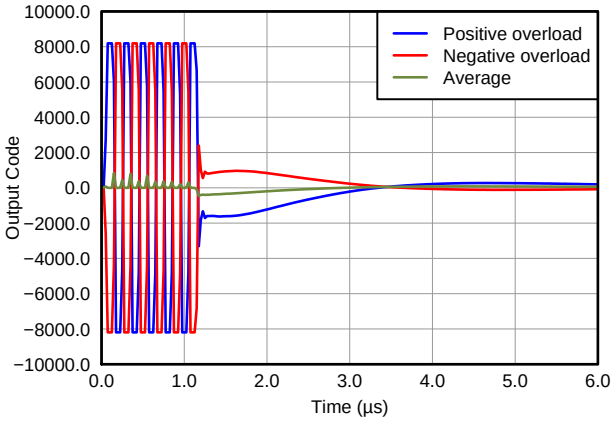


Figure 55. Pulse Inversion, V_{IN} = 2 Vpp, PRF = 1 kHz, Gain = 21 dB

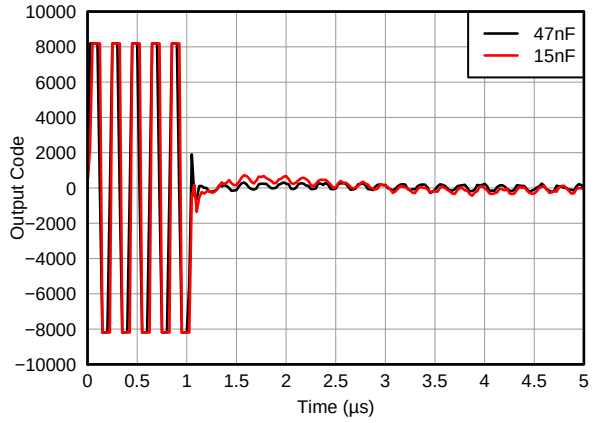


Figure 56. Overload Recovery Response vs INM Capacitor, V_{IN} = 50 mVpp/100 µVpp, Max Gain

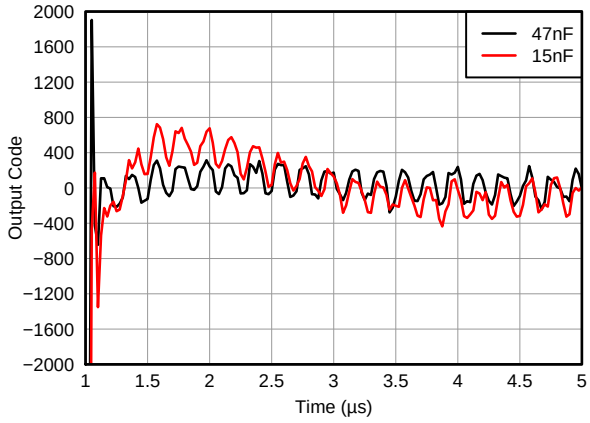


Figure 57. Overload Recovery Response vs INM Capacitor (Zoomed), V_{IN} = 50 mVpp/100 µVpp, Max Gain

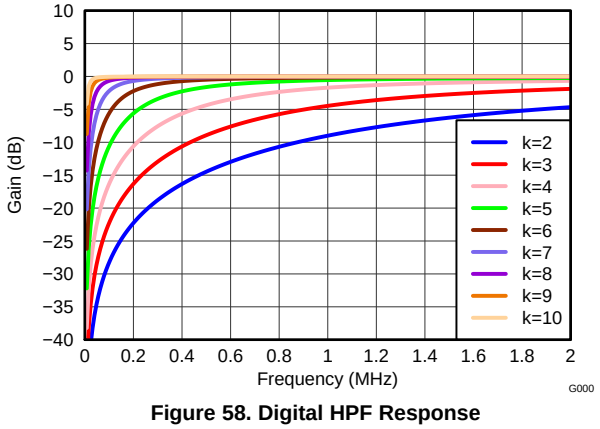


Figure 58. Digital HPF Response

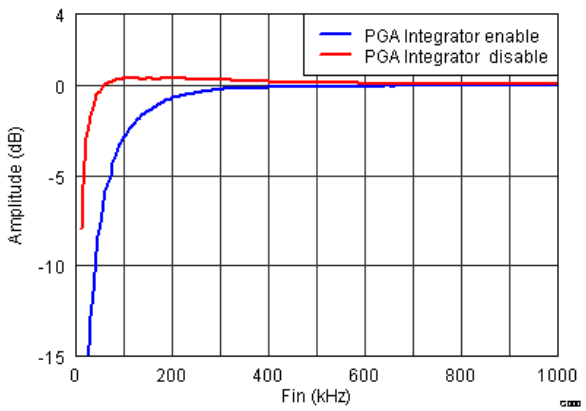


Figure 59. Signal Chain Low Frequency Response With INM Capacitor = 1 µF

10 Detailed Description

10.1 Overview

The AFE5812 is a highly-integrated AFE solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5812 integrates a complete TGC imaging path and a CWD path. It also enables users to select one of various power/noise combinations to optimize system performance. The AFE5812 contains eight channels; each channel includes a LNA, VCAT, PGA, LPF, 14-bit ADC, digital I/Q demodulator, and CW mixer.

Multiple features in the AFE5812 are suitable for ultrasound applications, such as active termination, individual channel control, fast power-up and power-down response, programmable clamp voltage control, and fast and consistent overload recovery. Therefore, the AFE5812 brings premium image quality to ultraportable, handheld systems all the way up to high-end ultrasound systems.

In addition, the signal chain of the AFE5812 can handle ultrasound systems or tranducers with a center frequency from 50 kHz to 50 MHz. This enables the AFE5812 to be used in both sonar and medical applications.

Figure 60 shows a simplified functional block diagram.

10.2 Functional Block Diagram

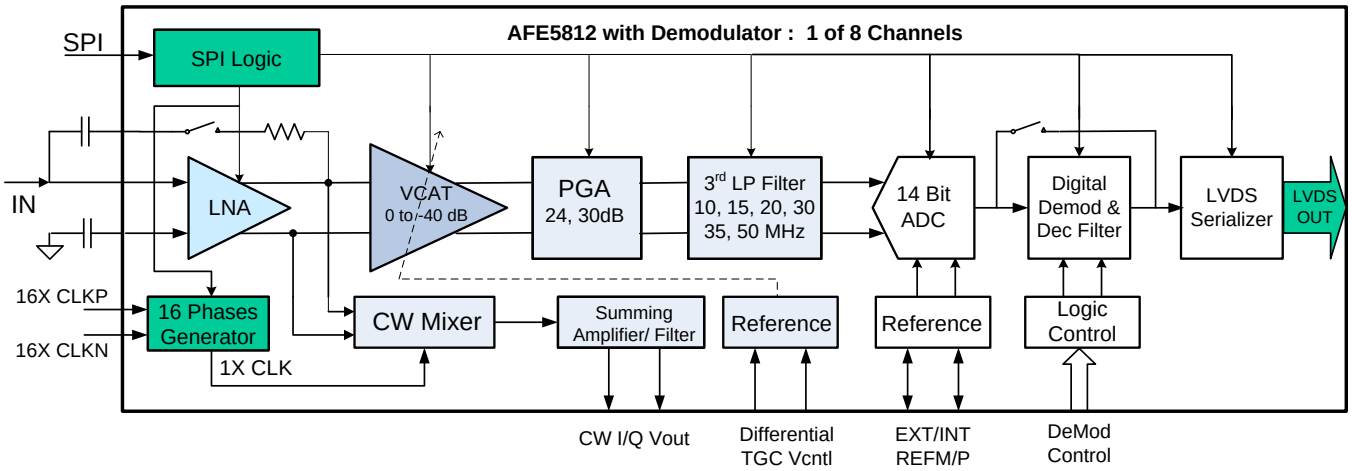


Figure 60. Simplified Functional Block Diagram

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Functional Block Diagram (continued)

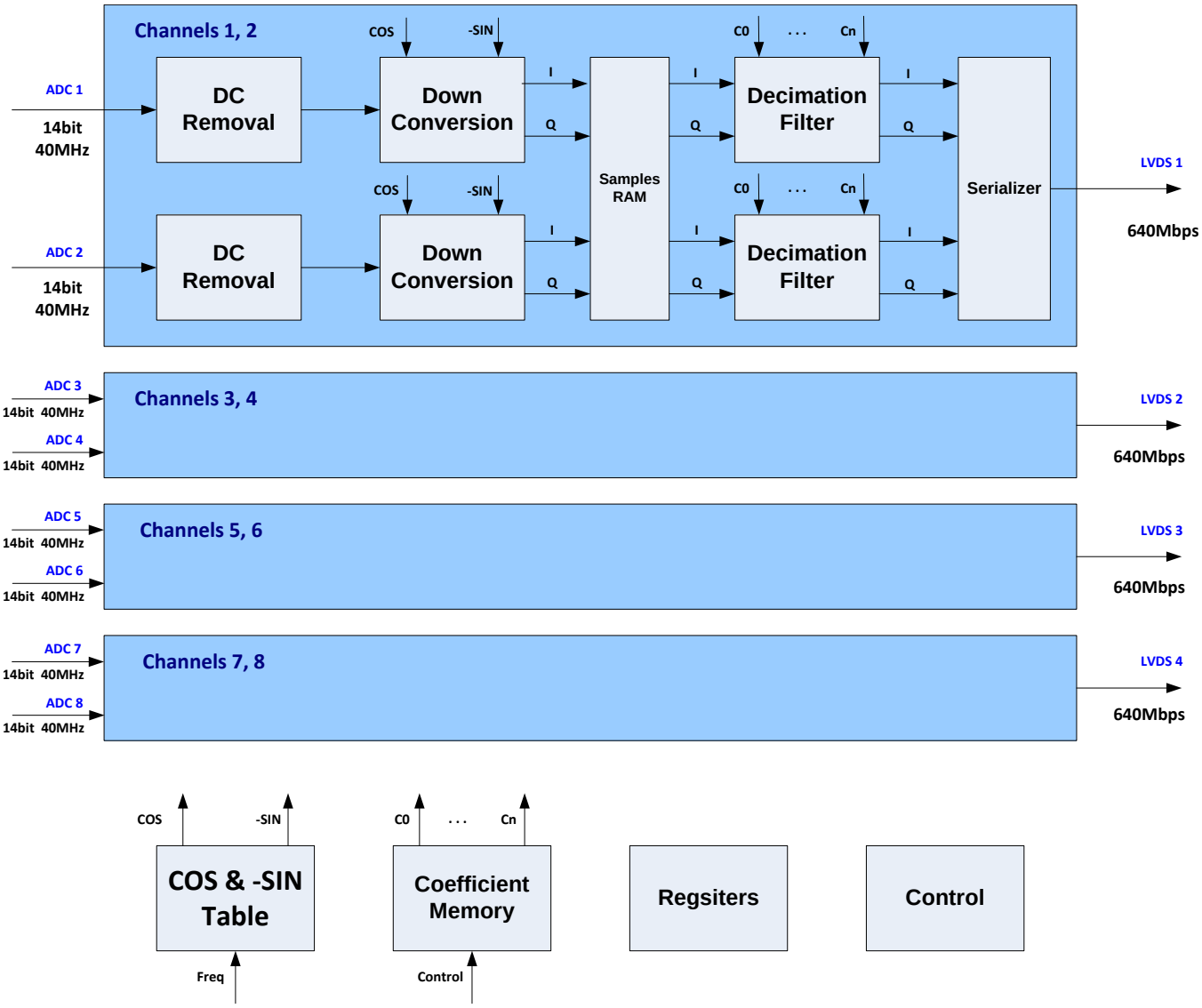


Figure 61. Digital Demodulator Block Diagram, M=4

10.3 Feature Description

10.3.1 LNA

In many high-gain systems, a LNA is critical to achieve overall performance. Using a new proprietary architecture, the LNA in the AFE5812 delivers exceptional low-noise performance, while operating on a low-quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. It is configurable for a programmable gain of 24, 18, or 15 dB and its input-referred noise is only 0.63, 0.7, or 0.9 nV/√Hz, respectively. Programmable gain settings result in a flexible linear input range up to 0.70 Vpp, realizing high-signal handling capability demanded by new transducer technologies. A larger input signal can be accepted by the LNA; however, the signal can be distorted because it exceeds the LNA's linear operation region. Combining the low noise and high-input range, the device consequently achieves a wide-input dynamic range for supporting the high demands from various ultrasound imaging modes.

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Feature Description (continued)

The LNA input is internally biased at approximately 2.2 V; the signal source should be AC-coupled to the LNA input by an adequately-sized capacitor, for example ≥0.1 µF. To achieve low DC offset drift, the AFE5812 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a HPF. The effective corner frequency is determined by the capacitor C_{BYPASS} connected at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filter cut-off frequency, a ≥15-nF capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15 nF gives a corner frequency of approximately 100 kHz, while 47 nF can give an effective corner frequency of 33 kHz. The DC offset correction circuit can also be disabled or enabled through register 52[12]. A large capacitor like 1 µF can be used for setting low corner frequency (<2 kHz) of the LNA DC offset correction circuit. Figure 59 shows the frequency responses for low-frequency applications.

The AFE5812 can be terminated passively or actively. Active termination is preferred in ultrasound applications for reducing reflection from mismatches and achieving better axial resolution without degrading noise figure too much. Active termination values can be preset to 50, 100, 200, and 400 Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 62 shows. On the active termination path, a clamping circuit is also used to create a low-impedance path when overload signal is seen by the AFE5812. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance of the AFE5812. The clamp level can be set to 350 mVpp, 600 mVpp, or 0.825 Vpp automatically depending on the LNA gain settings when register 52[10:9] = 0. Other clamp voltages, such as 0.825 Vpp, 0.6 Vpp, and 1.5 Vpp, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs.

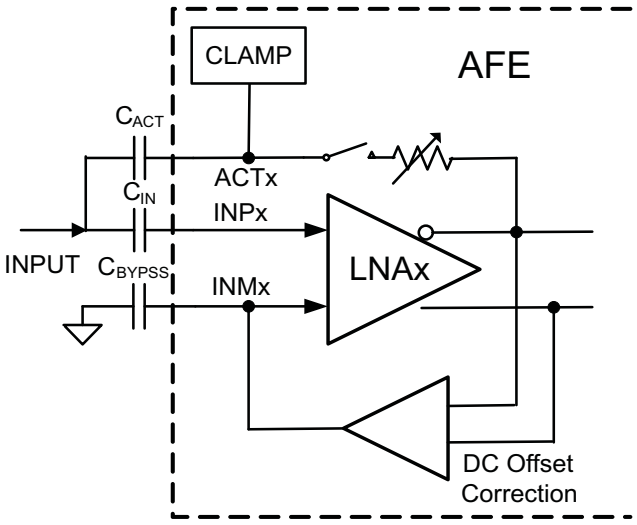


Figure 62. AFE5812 LNA With DC Offset Correction Circuit

10.3.2 Voltage-Controlled Attenuator

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (refer to Figure 2) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 63. A differential control structure is used to reduce common mode noise. Figure 63 and Figure 64 show a simplified attenuator structure.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (RS) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0- to 1.5-V control voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state

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Feature Description (continued)

and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by RS and the parallel FET network.

Additionally, a digitally-controlled TGC (DTGC) mode is implemented to achieve better phase-noise performance in the AFE5812. The attenuator can be controlled digitally instead of the analog control voltage, V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned on by connecting the switches SW1 through SW7. Turning on each of the switches can give approximately 6 dB of attenuation. This can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the V_{CNTL} circuit and ensure better SNR and phase noise for the TGC path.

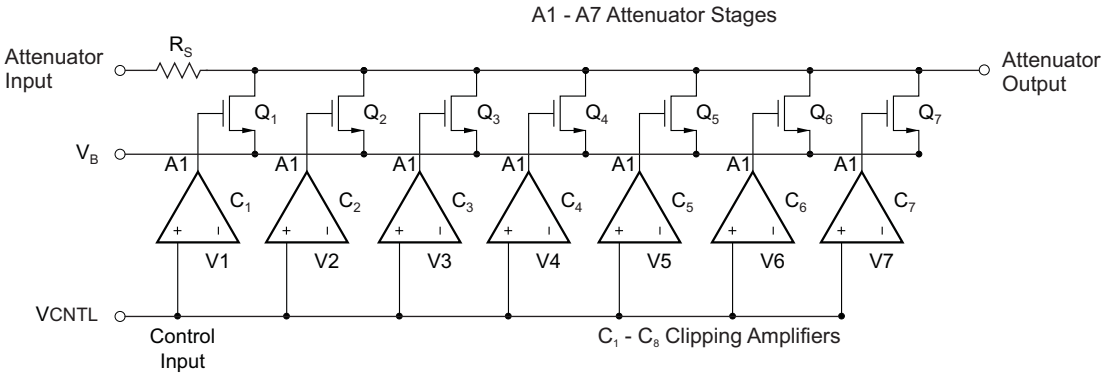


Figure 63. Simplified Voltage-Controlled Attenuator (Analog Structure)

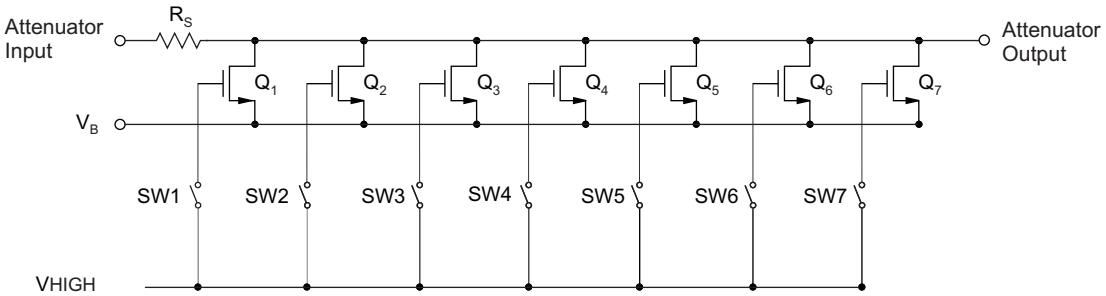


Figure 64. Simplified Voltage-Controlled Attenuator (Digital Structure, DTGC)

The voltage-controlled attenuator's noise follows a monotonic relationship to the attenuation coefficient. At higher attenuation, the input-referred noise is higher and vice-versa. The attenuator's noise is then amplified by the PGA and becomes the noise floor at ADC input. In the attenuator's high-attenuation operating range, that is V_{CNTL} is high, the attenuator's input noise may exceed the LNA output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore, the attenuator noise should be minimized compared to the LNA output noise. The AFE5812 attenuator is designed for achieving very-low noise even at high attenuation (low channel gain) and realizing better SNR in near field. Table 2 lists the input referred noise for different attenuations.

Table 2. Voltage-Controlled-Attenuator Noise versus Attenuation

Attenuation (dB)	Attenuator Input Referred Noise (nV/rtHz)
–40	10.5
–36	10
–30	9

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Table 2. Voltage-Controlled-Attenuator Noise versus Attenuation (continued)

Attenuation (dB)	Attenuator Input Referred Noise (nV/rtHz)
–24	8.5
–18	6
–12	4
–6	3
0	2

10.3.3 PGA

After the voltage-controlled attenuator, a PGA can be configured as 24 or 30 dB with a constant-input referred noise of 1.75 nV/rtHz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, clamping circuits, a transimpedance amplifier with a programmable LPF, and a DC offset correction circuit. Figure 65 shows its simplified block diagram.

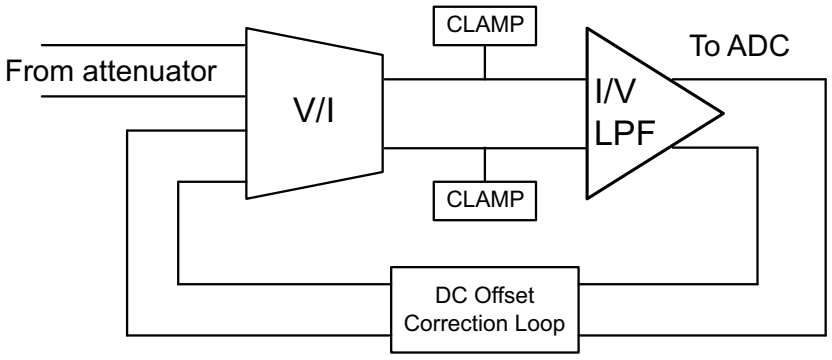


Figure 65. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA, and its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus, 24-dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA clamping circuit can be enabled (register 51) to improve the overload recovery performance of the AFE. If the user measures the standard deviation of the output just after overload, for 0.5 V V_{CNTL}, it is about 3.2 LSBs in normal case, that is, the output is stable in about 1 clock cycle after overload. With the clamp disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the clamp enabled, there will be degradation in HD3 for PGA output levels >–2 dBFS. For example, for a –2-dBFS output level, the HD3 degrades by approximately 3 dB. To maximize the output dynamic range, the maximum PGA output level can be above 2 Vpp even with the clamp circuit enabled; the ADC in the AFE5812 has excellent overload recovery performance to detect small signals right after the overload.

NOTE

In the low-power and medium-power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0.

The AFE5812 integrates an anti-aliasing filter in the form of a programmable LPF in the transimpedance amplifier. The LPF is designed as a differential, active, third-order filter with Butterworth characteristics and a typical 18 dB per octave roll-off. Programmable through the serial interface, the –1-dB frequency corner can be set to one of 10, 15, 20, 30, 35 and 50 MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. It extracts the DC component of the PGA outputs and feeds back to the PGA complementary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80 kHz.

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10.3.4 ADC

The ADC of the AFE5812 employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 14-bit level. The 14 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5812 operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 14× clock required for the serializer is generated internally from the CLKP/M pins. A 7× and 1× clock are also given out in LVDS format, along with the data, to enable easy data capture. The AFE5812 operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices. The nominal values of REFP and REFM are 1.5 and 0.5 V, respectively. Alternatively, the device also supports an external reference mode that can be enabled using the serial interface.

Using serialized LVDS transmission has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital-noise coupling to the analog circuit inside the AFE5812.

10.3.5 Continuous-Wave (CW) Beamformer

CWD is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path needs to handle high dynamic range along with strict phase-noise performance. CW beamforming is often implemented in analog domain due to the strict requirements. Multiple beamforming methods are implemented in ultrasound systems, including passive delay line, active mixer, and passive mixer. Among all of them, the passive mixer approach achieves optimized power and noise. It satisfies the CW processing requirements, such as wide dynamic range, low phase noise, accurate gain and phase matching.

Figure 66 and Figure 67 show a simplified CW path block diagram and an in-phase or quadrature (I/Q) channel block diagram, respectively. Each CW channel includes a LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a LPF, and clocking circuits.

NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on the users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed to get correct blood flow directions.

All blocks include well-matched in-phase and quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than –46 dBc, which is desired in ultrasound systems.

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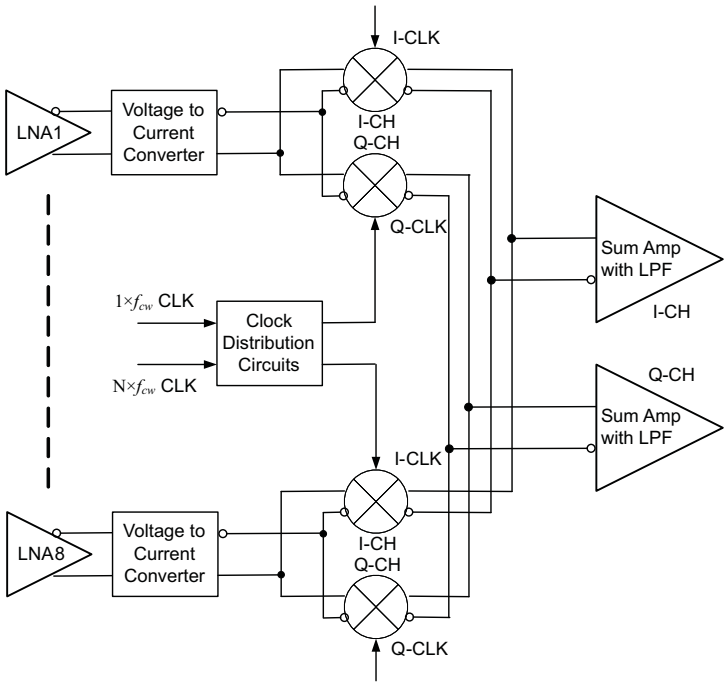
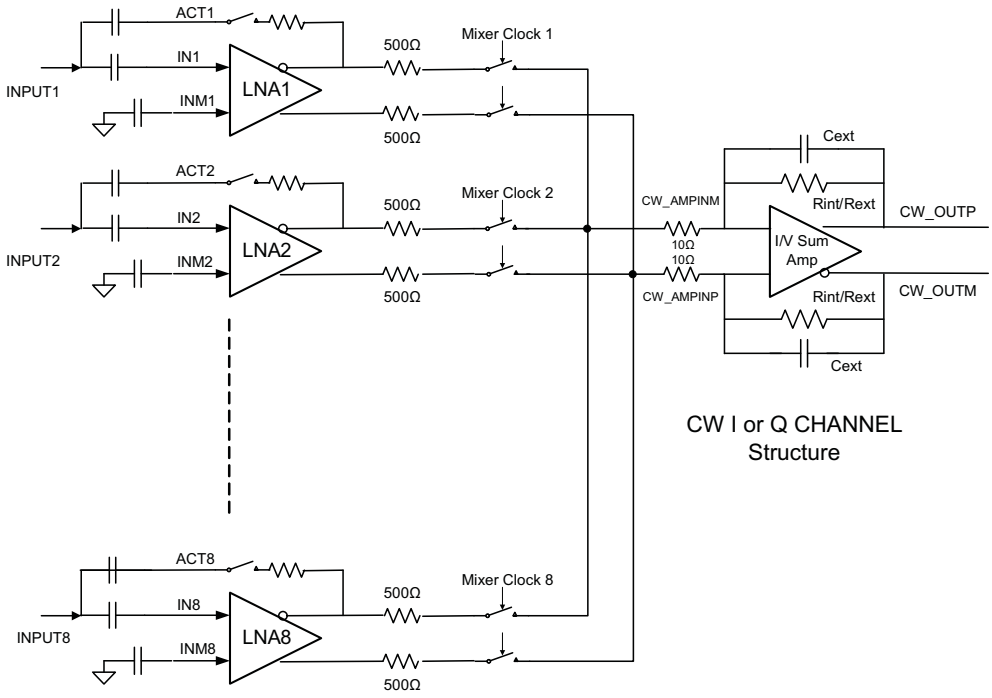


Figure 66. Simplified Block Diagram of CW Path



Note: The approximately 10- to 15-Ω resistors at CW_AMPINM/P are due to internal IC routing and can create slight attenuation.

Figure 67. Complete In-Phase or Quadrature-Phase Channel

The CW mixer in the AFE5812 is passive and switch based; a passive mixer adds less noise than an active mixer. It achieves good performance at low power. Figure 68 and the equations describe the principles of mixer operation, where Vi(t), Vo(t), and LO(t) are input, output, and local oscillator (LO) signals for a mixer respectively. The LO(t) is square-wave based and includes odd harmonic components, as shown in Equation 1.

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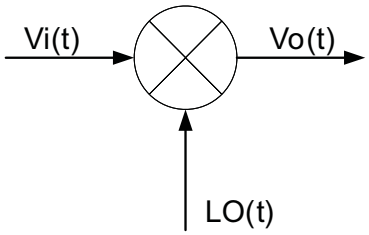


Figure 68. Block Diagram of Mixer Operation

$$Vi(t) = \sin(\omega_0 t + \omega_d t + \varphi) + f(\omega_0 t)$$
$$LO(t) = \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t)...\right]$$
$$Vo(t) = \frac{2}{\pi}\left[\cos(\omega_d t + \phi) - \cos(2\omega_0 t - \omega_d t + \phi)...\right] \quad (1)$$

From Equation 1, the third-order and fifth-order harmonics from the LO can interface with the third-order and fifth-order harmonic signals in the Vi(t), or the noise around the third-order and fifth-order harmonics in the Vi(t). Therefore, the mixer's performance is degraded. To eliminate this side effect due to the square-wave demodulation, a proprietary harmonic-suppression circuit is implemented in the AFE5812. The third- and fifth-harmonic components from the LO can be suppressed by over 12 dB. Thus, the LNA output noise around the third-order and fifth-order harmonic bands is not down-converted to base band. Hence, the device achieves better noise figure. The conversion loss of the mixer is about –4 dB, which is derived from $20\log_{10}\frac{2}{\pi}$.

The mixed current outputs of the eight channels are summed together internally. An internal low-noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low-power consumption, low noise, and ease of use. CW outputs from multiple AFE5812s can be further combined on system board to implement a CW beamformer with more than eight channels. See *Typical Application* for more detailed information.

Multiple clock options are supported in the AFE5812 CW path. Two CW clock inputs are required: N × f_{cw} clock and 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N could be 16, 8, 4, or 1. Users have the flexibility to select the most convenient system clock solution for the AFE5812. In the 16 × f_{cw} and 8 × f_{cw} modes, the third- and fifth-harmonic suppression feature can be supported. Thus, the 16 × f_{cw} and 8 × f_{cw} modes achieve better performance than the 4 × f_{cw} and 1 × f_{cw} modes.

10.3.5.1 16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. It is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16 × f_{cw} generates LO signals with 16 accurate phases. Multiple AFE5812s can be synchronized by the 1 × f_{cw} , that is LO signals in multiple AFEs can have the same starting phase. The phase noise specification is critical only for 16× clock. The 1× clock is for synchronization only and does not require low phase noise. See the phase noise requirement in *Typical Application*.

Figure 69 shows the top-level clock distribution diagram. Each mixer's clock is distributed through a 16 × 8 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1× clock. **TI recommends to align the rising edges of the 1 × f_{cw} and 16 × f_{cw} clocks.**

The cross-point switch distributes the clocks with appropriate phase delay to each mixer. For example, Vi(t) is a received signal with a delay of $\frac{1}{16}T$, a delayed LO(t) should be applied to the mixer to compensate for the $\frac{1}{16}T$ delay. Thus a 22.5º delayed clock, that is $\frac{2\pi}{16}$, is selected for this channel. The mathematic calculation is expressed in the following equations:

$$Vi(t) = \sin\left[\omega_0\left(t + \frac{1}{16f_0}\right) + \omega_d t\right] = \sin\left[\omega_0 t + 22.5^\circ + \omega_d t\right]$$

$$LO(t) = \frac{4}{\pi}\sin\left[\omega_0\left(t + \frac{1}{16f_0}\right)\right] = \frac{4}{\pi}\sin\left[\omega_0 t + 22.5^\circ\right]$$

$$Vo(t) = \frac{2}{\pi}\cos\left(\omega_d t\right) + f\left(\omega_n t\right) \quad (2)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the Doppler signals from N channels are summed, the signal-to-noise ratio improves.

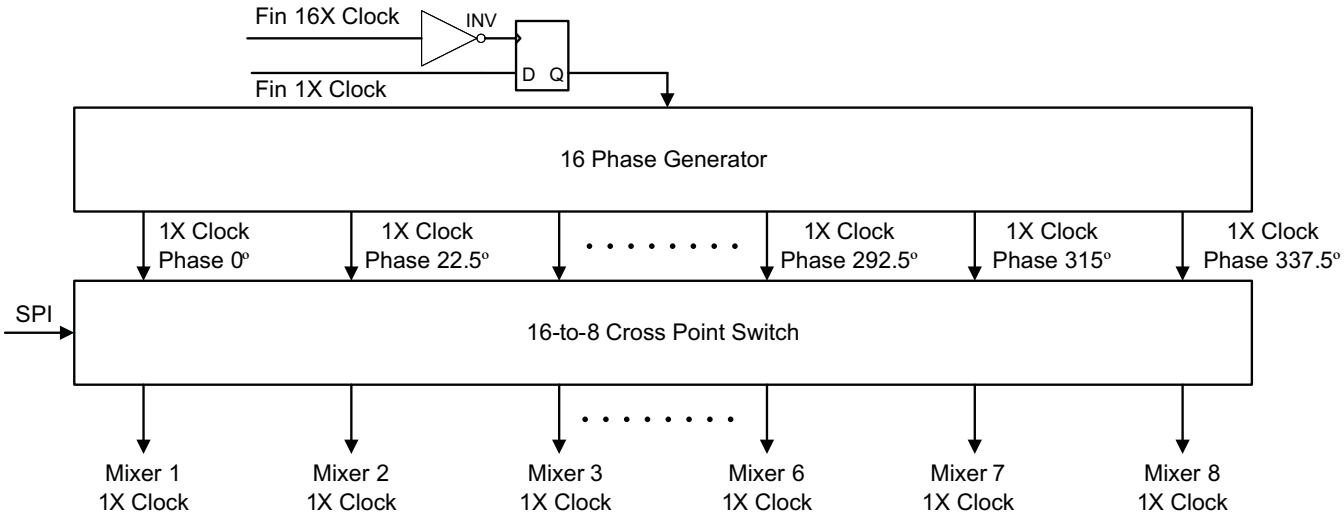


Figure 69.

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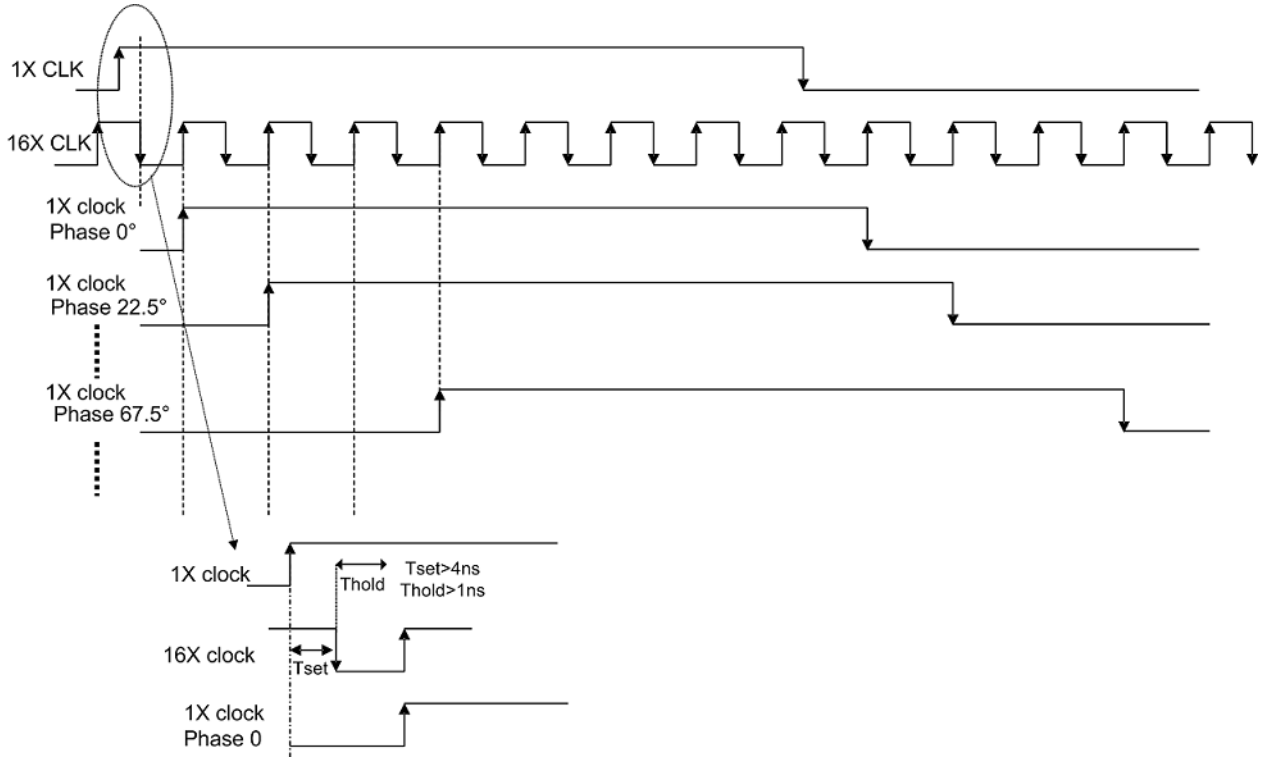


Figure 70. 1× and 16× CW Clock Timing

10.3.5.2 8 × f_{cw} and 4 × f_{cw} Modes

8 × f_{cw} and 4 × f_{cw} modes are alternative modes when a higher frequency clock solution (that is 16 × f_{cw} clock) is not available in system. Figure 71 shows a block diagram of these two modes.

Good phase accuracy and matching are also maintained. Quadrature clock generator is used to create in-phase and quadrature clocks with exactly 90° phase difference. The only difference between 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the third- and fifth-harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, $\frac{1}{16}T$ phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of $\frac{1}{16}T$ or 22.5° is targeted, the weighting coefficients should follow Equation 3, assuming I_{in} and Q_{in} are sin($\omega_0 t$) and cos($\omega_0 t$) respectively.

$$I_{delayed}(t) = I_{in}\cos\left(\frac{2\pi}{16}\right) + Q_{in}\sin\left(\frac{2\pi}{16}\right) = I_{in}\left(t + \frac{1}{16 f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(\frac{2\pi}{16}\right) - I_{in}\sin\left(\frac{2\pi}{16}\right) = Q_{in}\left(t + \frac{1}{16 f_0}\right) \quad (3)$$

Therefore, after I/Q mixers, phase delay in the received signals is compensated. The mixers' outputs from all channels are aligned and added linearly to improve the signal-to-noise ratio. **It is preferred to have the 4 × f_{cw} or 8 × f_{cw} and 1 × f_{cw} clocks both aligned at the rising edge.**

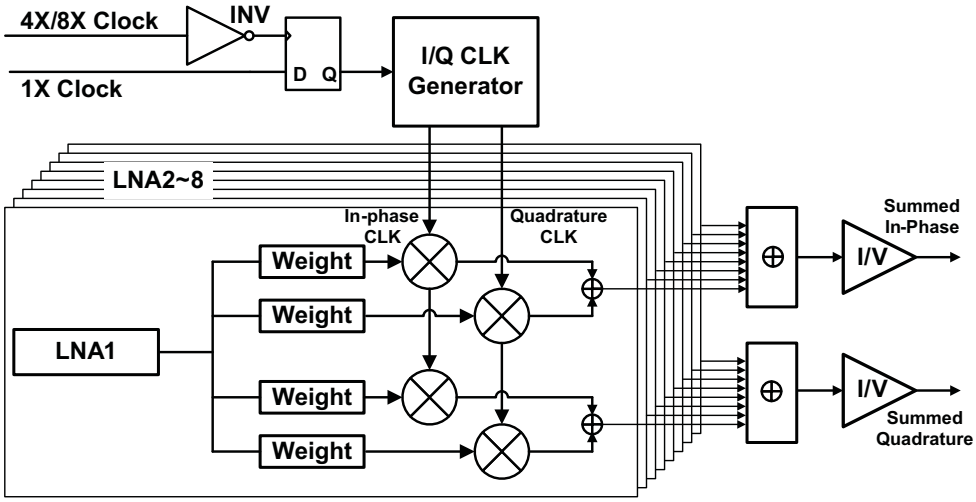


Figure 71. 8 × f_{cw} and 4 × f_{cw} Block Diagram

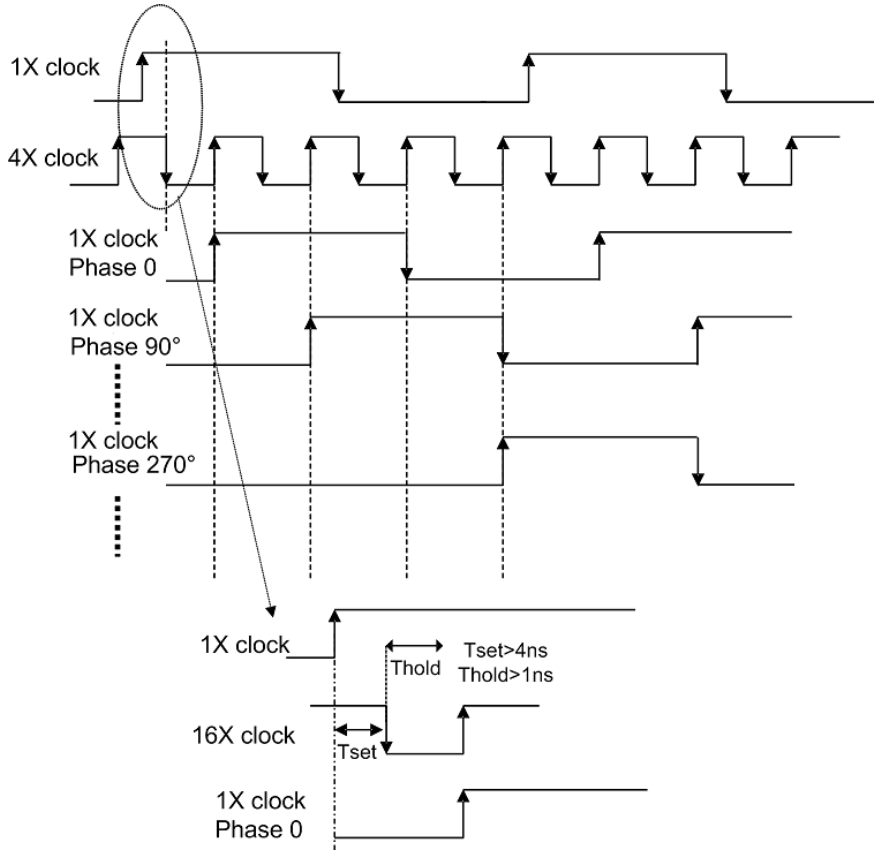


Figure 72. 8 × f_{cw} and 4 × f_{cw} Timing Diagram

10.3.5.3 1 × f_{cw} Mode

The 1 × f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. The $\frac{1}{16}T$ phase delay resolution is also achieved by weighting the in-phase and quadrature signals as described in the 8 × f_{cw} and 4 × f_{cw} modes.

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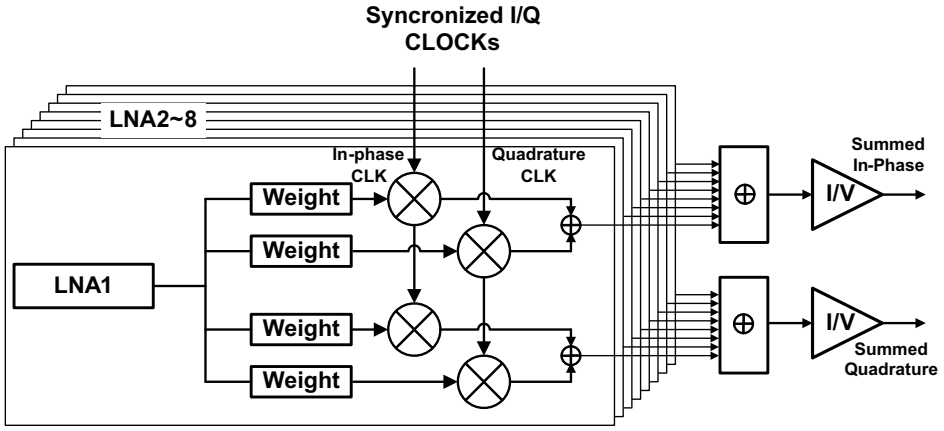


Figure 73. Block Diagram of 1 x f_{cw} mode

10.3.6 Digital I/Q Demodulator

AFE5812 also includes a digital in-phase and quadrature (I/Q) demodulator and a low-pass decimation filter. The main purpose of the demodulation block is to reduce the LVDS data rate and improve overall system power efficiency. The I/Q demodulator accepts ADC output with up to 65 MSPS sampling rate and 14-bit resolution. For example, after digital demodulation and 4× decimation filtering, the data rate for either in-phase or quadrature output is reduced to 16.25 MSPS, and the data resolution is improved to 16 bits consequently. Hence, the overall LVDS trace reduction can be a factor of 2. This demodulator can be bypassed and powered down completely if it is not needed.

The digital demodulator block given in AFE5812 is designed to do down-conversion followed by decimation. The top-level block is divided into two exactly similar blocks: (1) subchip0 and (2) subchip1. Both subchips share four channels each, that is, subchip0 (ADC.1, ADC.2, ADC.3, and ADC.4) and subchip1 (ADC.5, ADC.6, ADC.7, and ADC.8).

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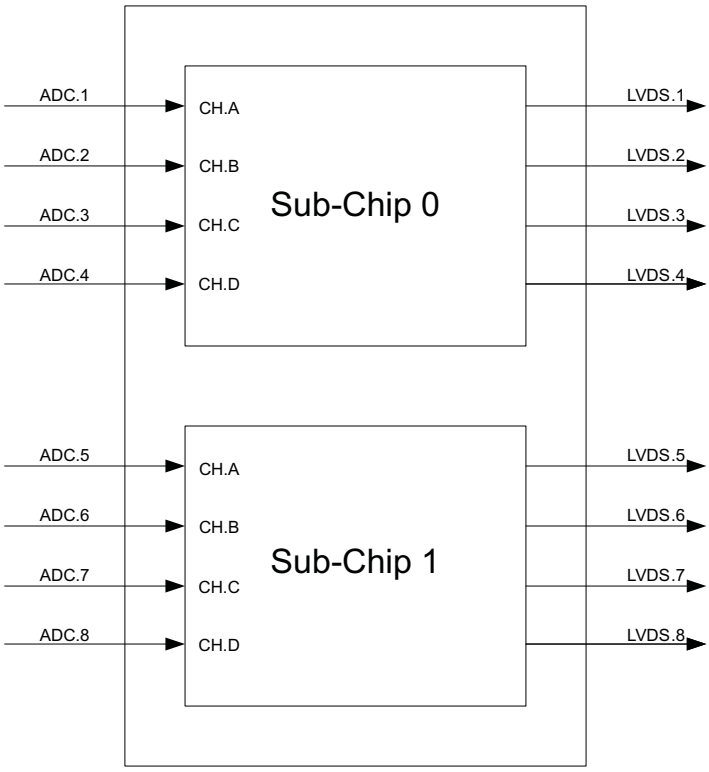


Figure 74. Subchip

The following four functioning blocks are given in each demodulator. Every block can be bypassed.

- DC removal block
- Down conversion
- Decimator
- Channel multiplexing

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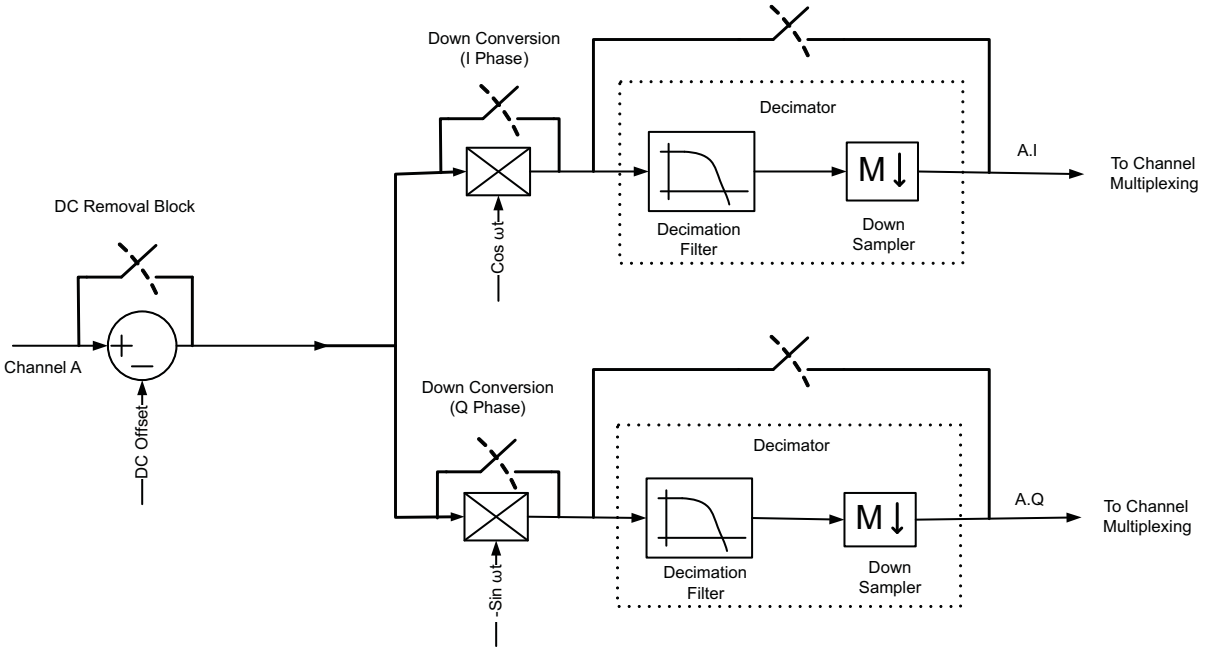


Figure 75. Digital Demodulator Block

1. DC removal block is used to remove DC offset. An offset value can be given to a specific register.
2. Down conversion or demodulation of signal is done by multiplying signal by $\cos(\omega_0 t)$ and by $-\sin(\omega_0 t)$ to give out I phase and Q phase, respectively. $\cos(\omega t)$ and $-\sin(\omega t)$ are 14-bit wide plus a sign bit. $\omega = 2\pi f$, f can be set with resolution Fs / 2^{16}, where Fs is the ADC sampling frequency.

NOTE

The digital demodulator is based on a conventional down converter, that is, $-\sin(\omega_0 t)$ is used for Q phase.

3. The decimator block has two functions: decimation filter and down sampler. Decimation filter is a variable coefficient symmetric FIR filter and its coefficients can be given using coefficient RAM. Number of taps of FIR filter is 16× decimation factor (M). For decimation factor of M, 8M coefficients have to be stored in the coefficient bank. Each coefficient is 14-bit wide. Down-sampler gives out 1 sample followed by M – 1 samples zeros.
4. In Figure 76, channel multiplexing is implemented for flexible data routing:

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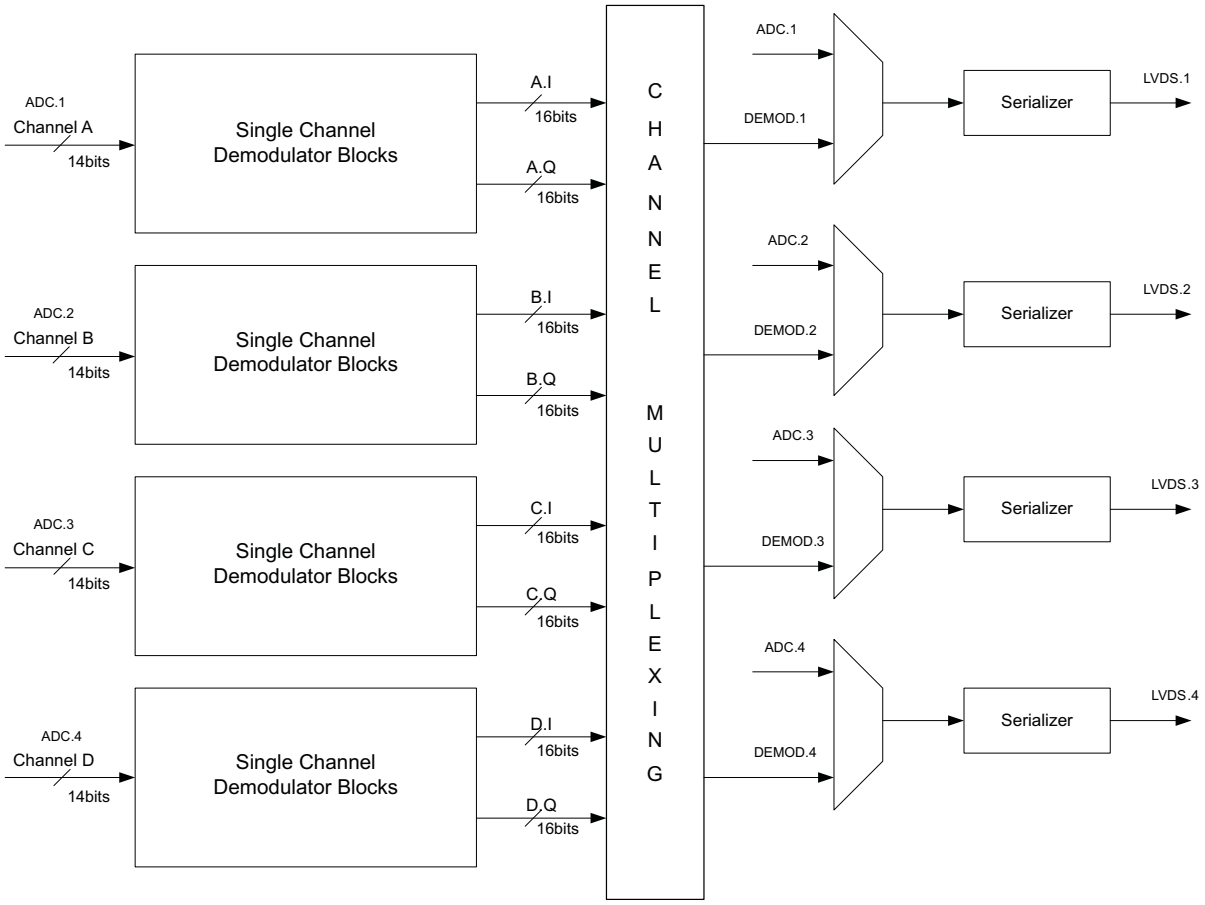


Figure 76. Channel Multiplexing

10.3.7 Equivalent Circuits

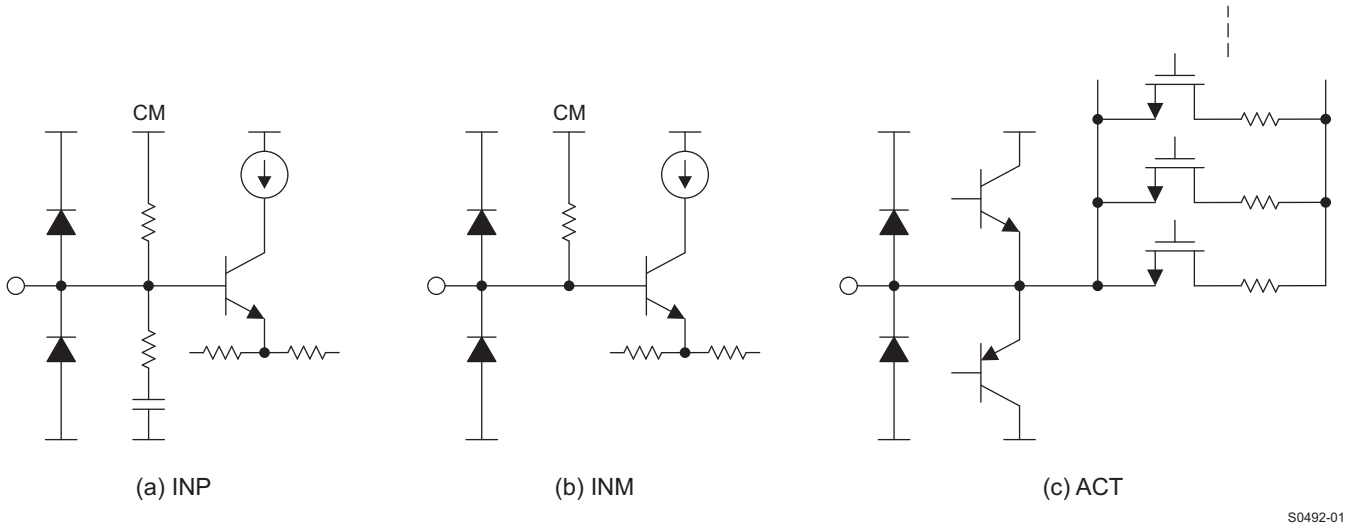


Figure 77. Equivalent Circuits of LNA Inputs

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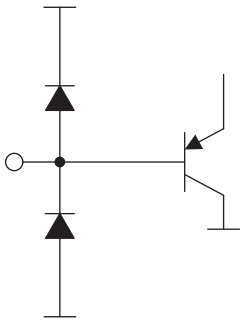


Figure 78. Equivalent Circuits of $V_{CNTLP/M}$

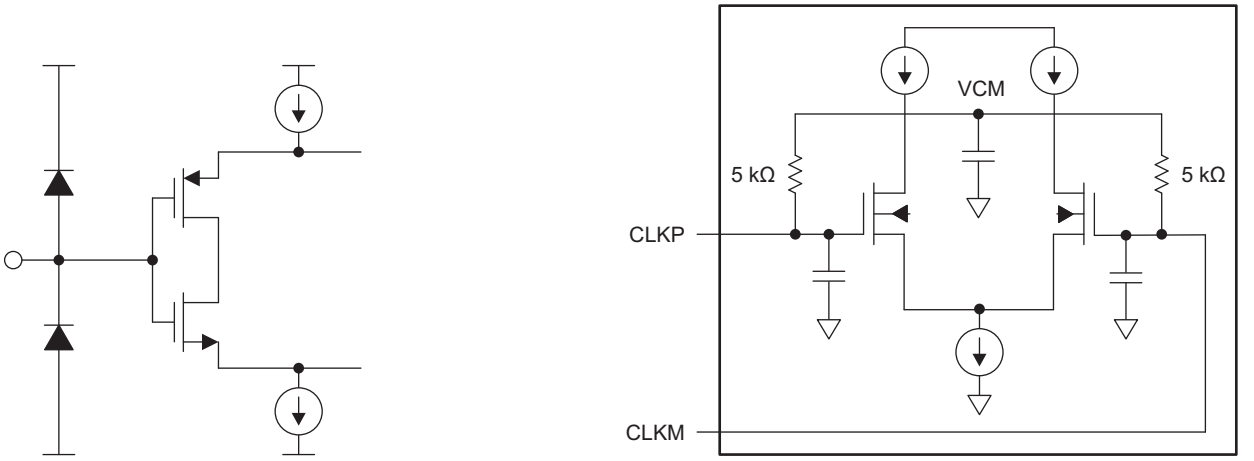


Figure 79. Equivalent Circuits of Clock Inputs

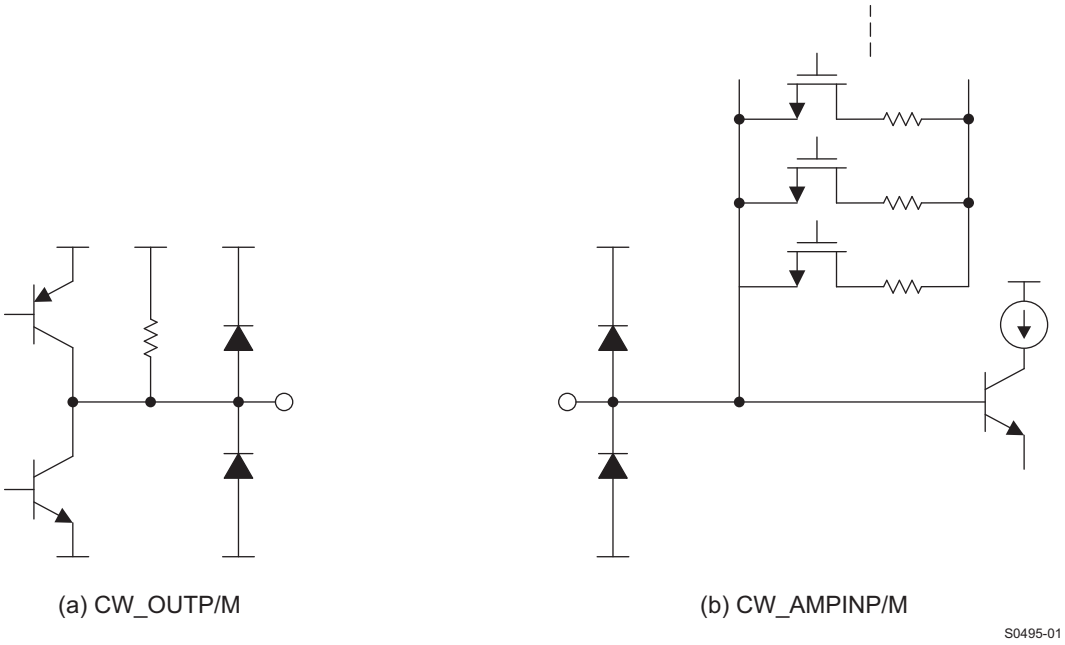


Figure 80. Equivalent Circuits of CW Summing Amplifier Inputs and Outputs

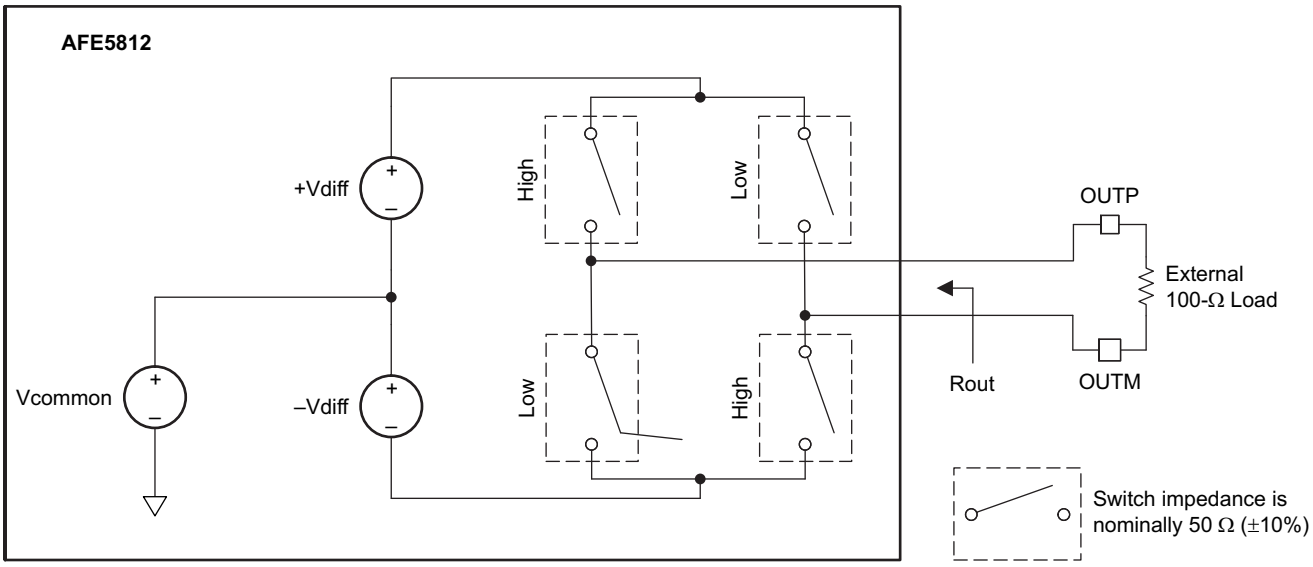


Figure 81. Equivalent Circuits of LVDS Outputs

10.3.8 LVDS Output Interface Description

AFE5812 has a LVDS output interface, which supports multiple output formats. The ADC resolutions can be configured as 12 bit or 14 bit as shown in the LVDS timing diagrams (Figure 1). The ADCs in the AFE5812 are running at 14 bits; 2 LSBs are removed when 12-bit output is selected; and two zeros are added at LSBs when 16-bit output is selected. Appropriate ADC resolutions can be selected for optimizing system-performance cost effectiveness. When the devices run at 16-bit mode, higher-end FPGAs are required to process the higher rate of LVDS data. Corresponding register settings are listed in Table 5.

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10.4 Device Functional Modes

10.4.1 TGC Mode

By default, after reset the AFE is configured in TGC mode. Depending upon the system requirements, the device can be programmed in a suitable power mode using the register bits shown in *VCA Register Map*. In the TGC mode, the digital demodulator after ADC can be enabled as well for further digital processing.

10.4.2 CW Mode

To configure the device in CW mode, set the CW_TGC_SEL (0x36[8]) register bit to 1. To save power, the voltage-controlled attenuator and programmable gain amplifier in the TGC path can be disabled by setting the 0x35[12] to 1. Also, the ADC can be powered down completely using the 0x1[0] . Usually only half the number of channels in a system are active in the CW mode. Thus, the individual channel control can power-down unused channels and save power; see register 0x1[9:2] and 0x35[7:0] and *Power Saving in CW Mode*.

10.4.3 TGC + CW Mode

In systems that require fast switching between the TGC and CW modes, either mode can be selected simply by setting the CW_TGC_SEL register bit.

10.4.4 Test Modes

The AFE5812 includes multiple test modes to accelerate system development.

10.4.4.1 ADC Test Modes

The AFE5812 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13] = 111 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all 0s by setting Register 2[15:13] = 110.
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13] = 100.
4. **Deskew Pattern:** When 2[15:13] = 010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13] = 001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13] = 101, the normal ADC output is alternating between 1s and 0s. The start state of ADC word can be either 1s or 0s.
7. **Custom Pattern:** It can be enabled when 2[15:13] = 011. Users can write the required VALUE into register bits <CUSTOM PATTERN>, which is Register 5[13:0]. Then, the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24^{th} rising edge of SCLK. So, the time taken to write one value is 24 SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern takes approximately 128 × (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

Only one of the above ADC patterns can be active at any given instant.

Digital demodulator should be disabled, i.e. 0x16=1.

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Device Functional Modes (continued)

10.4.4.2 VCA Test Mode

The VCA has a test mode in which the CH7 and CH8 PGA outputs can be brought to the CW pins. By monitoring these PGA outputs, the functionality of VCA operation can be verified. The PGA outputs are connected to the virtual ground pins of the summing amplifier (CW_IP_AMPINM/P, CW_QP_AMPINM/P) through 5-kΩ resistors. The PGA outputs can be monitored at the summing amplifier outputs when the LPF capacitors C_{EXT} are removed. Note that the signals at the summing amplifier outputs are attenuated due to the 5-kΩ resistors. The attenuation coefficient is $R_{INT/EXT}$ / 5 kΩ.

If users would like to check the PGA outputs without removing C_{EXT}, an alternative way is to measure the PGA outputs directly at the CW_IP_AMPINM/P and CW_QP_AMPINM/P when the CW summing amplifier is powered down.

Some registers are related to this test mode, PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0]. Based on the buffer amplifier configuration, the registers can be set in different ways:

- Configuration 1
  - In this configuration, the test outputs can be monitored at CW_AMPINP/M.
  - Reg59[9] = 1; test mode enabled
  - Reg59[8] = 0; buffer amplifier powered-down
- Configuration 2
  - In this configuration, the test outputs can be monitored at CW_OUTP/M.
  - Reg59[9] = 1; test mode enabled
  - Reg59[8] = 1; buffer amplifier powered on
  - Reg54[4:0] = 10H; internal feedback 2-kΩ resistor enabled. Different values can be used as well.

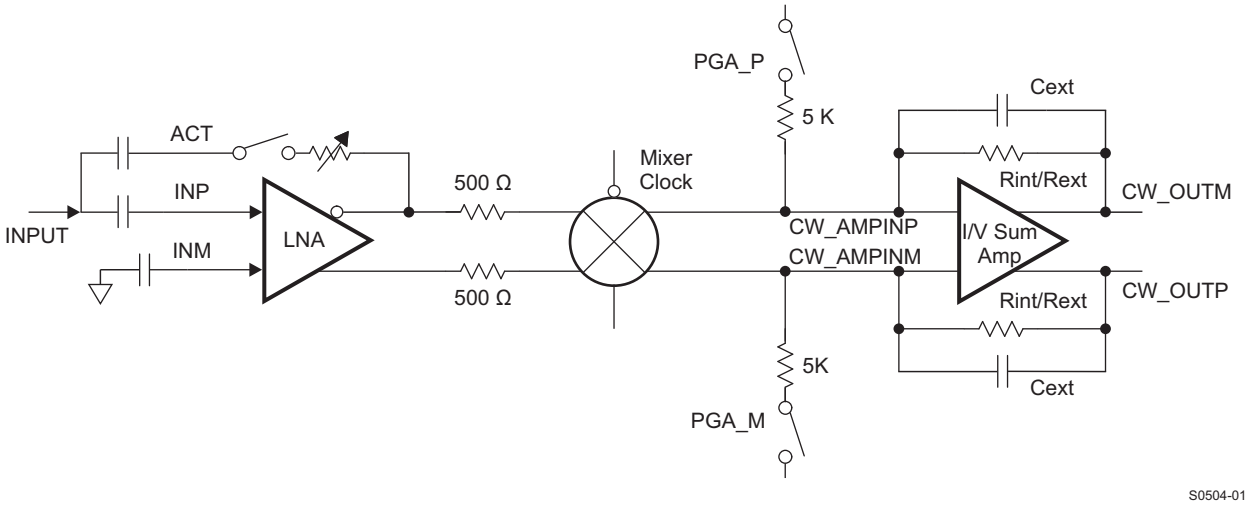


Figure 82. AFE5812 PGA Test Mode

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10.5 Programming

10.5.1 Serial Peripheral Interface (SPI) Operation

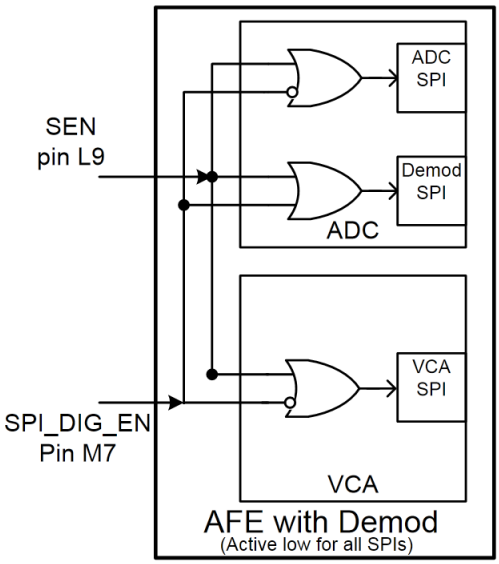


Figure 83. SPI Interface in the AFE5812

Figure 83 shows the block diagram of SPI inerface in the AFE5812. SPI_DIG_EN and SEN are used to access ADC/VCA SPI or Demod SPI. After reset and SPI_DIG_EN pin is floating or SPI_DIG_EN = 1, the ADC/VCA SPI is accessiable. When SEN and SPI_DIG_EN are pulled down simultaneously, the demod SPI is accessiable.

10.5.1.1 Serial Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and RESET. All these pins have a pulldown resistor to GND of 20 kΩ. Serial shift of bits into the device is enabled when SEN is low. Serial data, SDATA, is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (an internal counter counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz to low speeds (of a few Hertz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits), to load on the addressed register. When writing to a register with unused bits, set these to 0. Figure 84 shows this process.

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Programming (continued)

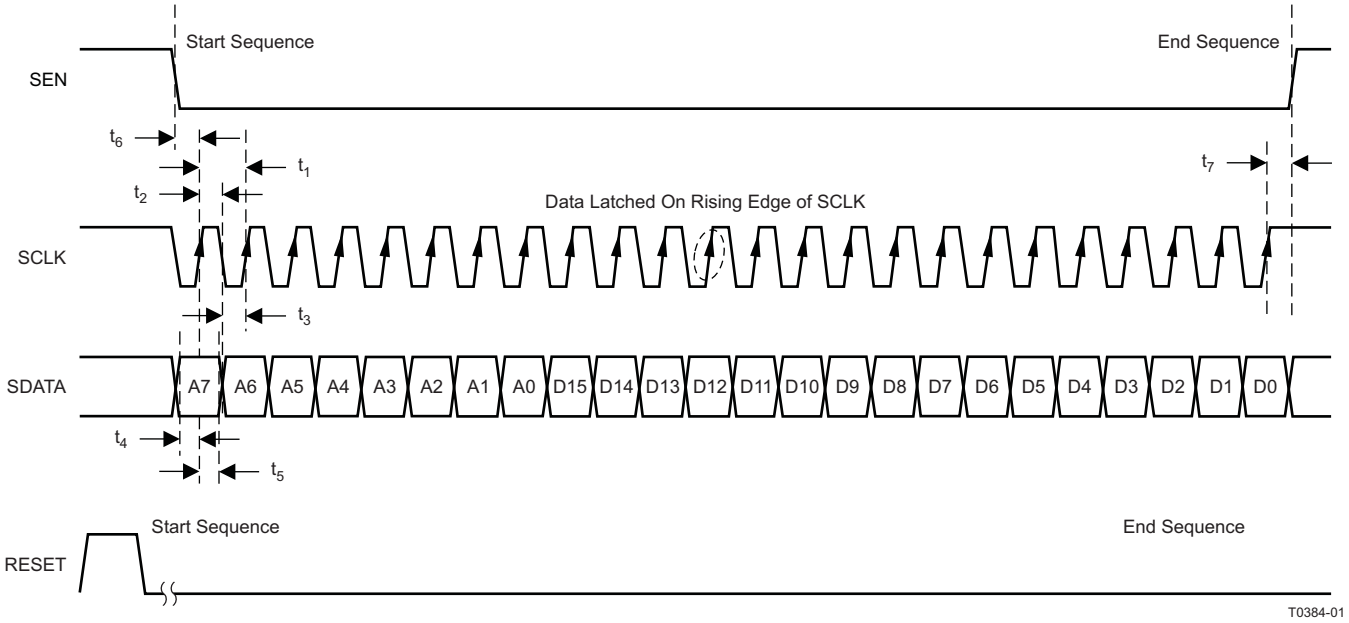


Figure 84. SPI Timing

NOTE

TI recommends to synchronize SCLK to ADC CLK. Typically, SCLK can be generated by dividing ADC CLK by an integer factor of N. In a system with multiple AFEs, SCLKs may not reach all AFEs simultaneously due to routing. To compensate routing differences and ensure AFEs' outputs are aligned, SCLK can be adjusted to toggle on either the falling edge of ADCLK or the rising edge of ADC CLK (ensuring new register settings are loaded before next ADC sampling clock).

ADC CLK is required to access the demodulation registers.

Refer to *SPI Timing Characteristics* for the timing characteristics of t1~t8.

10.5.1.2 Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to 1. Then, the user should initiate a serial interface cycle specifying the address of the register (A7 through A0) whose content has to be read. The data bits are don't care. The device outputs the contents (D15 through D0) of the selected register on the SDOUT pin. SDOUT has a typical delay, t_8, of 20 ns from the falling edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK, for example, if the SCLK period is less than 60 ns, it is better to latch the SDOUT at the next falling edge of SCLK. Figure 85 shows this operation. In the readout mode, users still can access the <REGISTER READOUT ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to 0.

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Programming (continued)

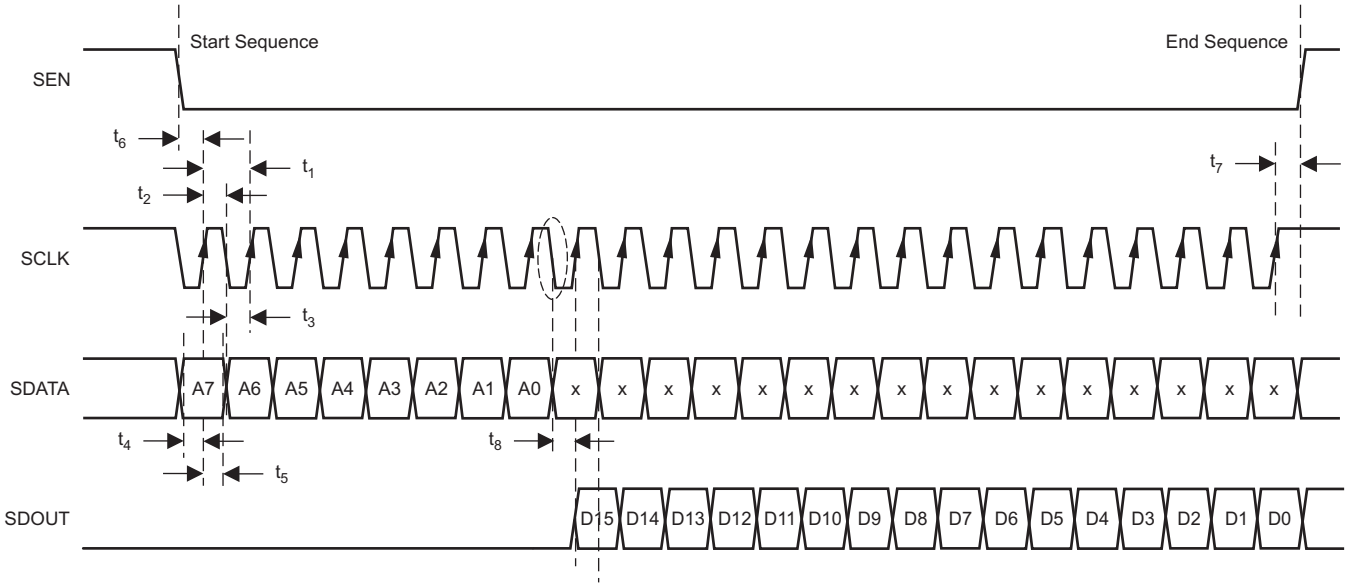


Figure 85. Serial Interface Register Read

The AFE5812 SDOUT buffer is tri-stated and gets enabled only when 0[1] (REGISTER READOUT ENABLE) is enabled. SDOUT pins from multiple AFE5812s can be tied together without any pullup resistors. Level shifter SN74AUP1T04 can be used to convert 1.8-V logic to 2.5-V/3.3-V logics if needed.

10.5.1.3 SPI for Demodulator

Demodulator is enabled after a software or hardware reset. It can be disabled by setting the LSB of register 0x16 as 1. This is done using the ADC SPI interface, that is, SPI_DIG_EN = 1. The demodulator SPI interface is independent from the ADC/VCA SPI interface as shown in Figure 83.

To access the specific demodulator registers:

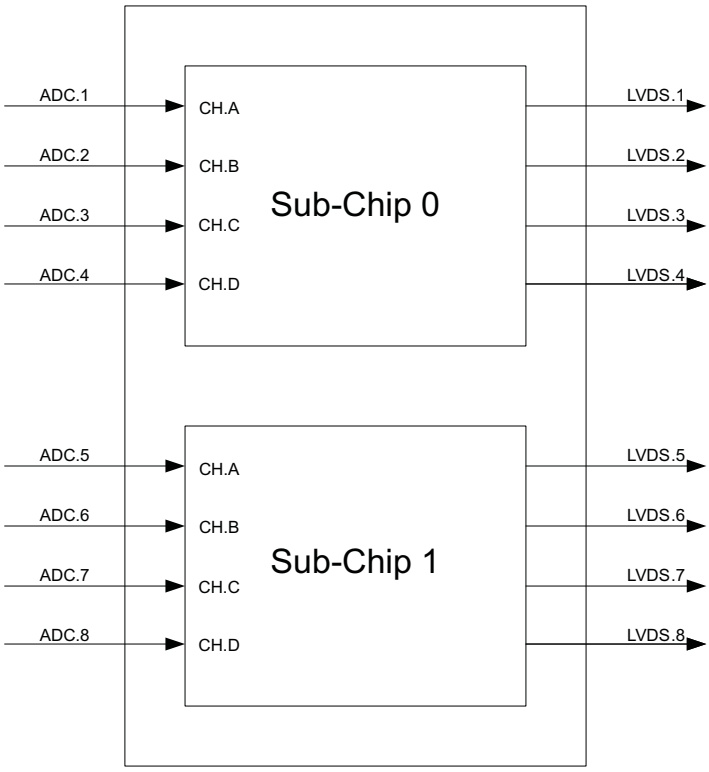
1. SPI_DIG_EN pin is required to be set as 0 during SPI transactions to demodulator registers. Meanwhile, ADC SEN needs to be set as 0 during demodulator SPI programming.
2. The SPI register address is 8 bits and is made of 2 subchip select bits and 6 register address bits. SPI register data is 16 bits.
3. **ADC CLK and DVDD_LDO1/2 are required to access the demodulation registers.**

Table 3. Register Address Bit Description

Bit7	Bit6	Bit 5:0
SCID1_SEL	SCID0_SEL	Register address <5:0>

4. SCID0_SEL enables configuration of channels 1 through 4. SCID1_SEL enables configuration of channels 5 through 7. When performing demodulator SPI write transactions, these SCID bits can be individually or mutually used with a specific register address.
5. Register configuration is normally shared by both subchips (both SCID bits should be set as 1). An exception to this rule would be the DC OFFSET registers (0x14 through 0x17) for which specific channel access is expected.

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A. Each of two subchips supports four channels.

B. Each of two demodulators has four channels named as A, B, C, and D.

Figure 86. Subchip 0 and Subchip 1

6. Demodulator register readout follows these procedures:
   - Write 1 to register 0x0[1]; pin SPI_DIG_EN should be 0 while writing. This is the readout enable register for demodulator.
   - Write 1 to register 0x0[1]; pin SPI_DIG_EN should be 1 while writing. This is the readout enable register for ADC and VCA.
   - Set SPI_DIG_EN as 0 and write anything to the register whose stored data needs to be known. Device finds the address of the register and sends its stored data at the SDOUT pin serially.

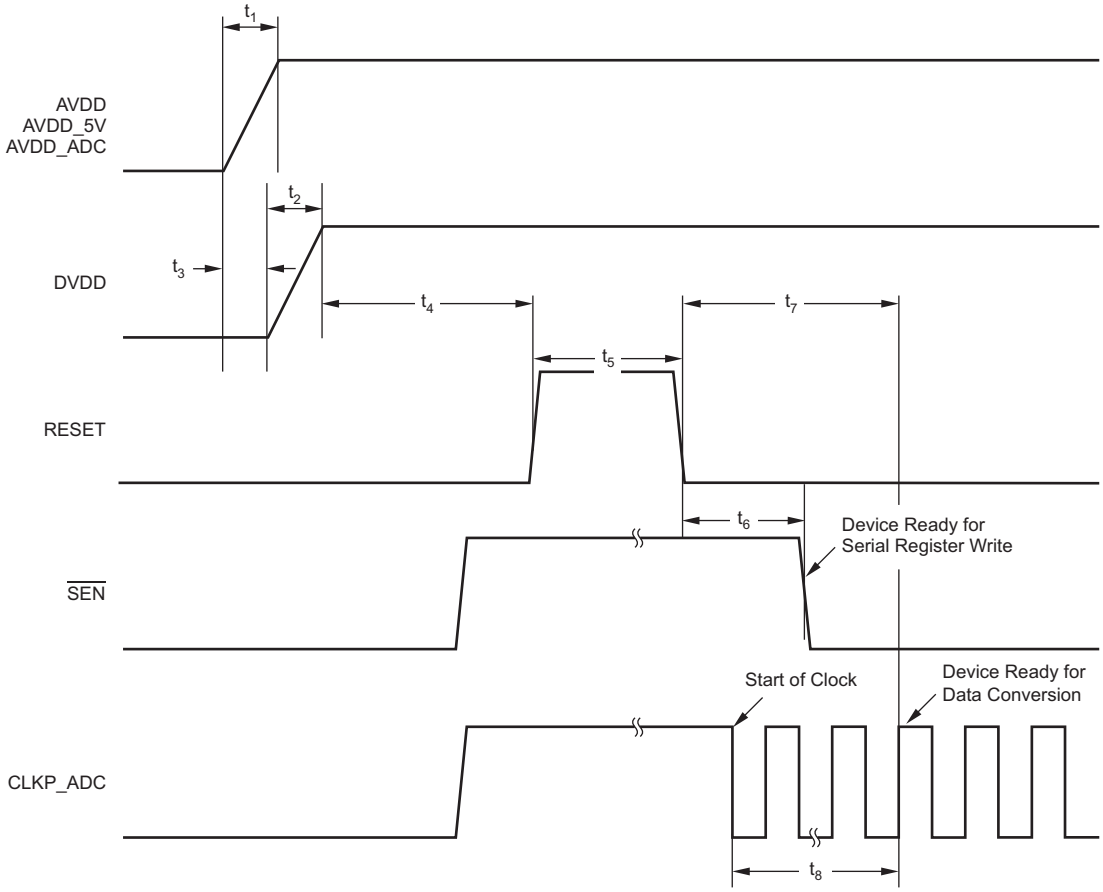
NOTE

After enabling the register 0x0[1] REGISTER_READOUT_ENABLE, data cannot be written to the register (whose data needs to be known), but stored data would come serially at the SDOUT pin.

   - To disable the register readout, first write 0 to register 0x0[1] while SPI_DIG_EN is 1; then write 0 to register 0x0[1] while SPI_DIG_EN is 0.

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10.5.2 POWER UP SEQUENCE



A. 10 µs < t_1 < 50 ms, 10 µs < t_2 < 50 ms, –10 ms < t_3 < 10 ms, t_4 > 10 ms, t_5 > 100 ns, t_6 > 100 ns, t_7 > 10 ms, and t_8 > 100 µs. **When the demodulator power DVDD_LDO1 and DVDD_LDO2 are supplied externally, it should be powered up 1ms after DVDD. LDOs for external DVDD_LDO1 and DVDD_LDO2 can be powered down if the demodualtor is not used.**

B. The AVDDx and DVDD power-on sequence does not matter as long as –10 ms < t_3 < 10 ms. Similar considerations apply while shutting down the device.

Figure 87. Recommended Power-Up Sequencing with Internally Generated 1.4V Demod Supply

10.6 Register Maps

10.6.1 ADC and VCA Register Description

A reset process is required at the AFE5812 initialization stage. Initialization can be done in one of two ways:

- Through a hardware reset, by applying a positive pulse in the RESET pin.
- Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros), and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

NOTE

After reset, all ADC and VCA registers are set to 0, that is default setting. During register programming, all unlisted register bits need to be set as 0.

Some demodulator registers are set as 1 after reset. During register programming, all unlisted register bits need to be set as 0. In addition, the demodulator registers can be reset when 0x16[0] is set as 0. Thus, it is required to reconfigure the demodulator registers after toggling the 0x16[0] from 1 to 0.

10.6.1.1 ADC Register Map

Address (DEC)	Address (HEX)	Default Value	Function	Description
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation 1: Resets the device and self-clears the bit to 0. Note: Register 0 is a write only register.
0[1]	0x0[1]	0	REGISTER_READOUT_ENABLE	0:Disables readout 1: Enables readout of register at SDOUT pin. Note: When this bit is set to 0, the device always operates in write mode and when it is set to 1, device will be in read mode. Multiple reading or writing events can be performed when this bit is set to 1 or 0 correspondingly. Register 0 is a write-only register.
1[0]	0x1[0]	0	ADC_COMPLETE_PDN	0: Normal 1: Complete power down. Note: When the complete power-down mode is enabled, the digital demodulator may lose register settings. Therefore, it is required to reconfigure the demodulator registers, filter coefficient memory, and profile memory after exiting the complete power-down mode.
1[1]	0x1[1]	0	LVDS_OUTPUT_DISABLE	0: Output enabled 1: Output disabled
1[9:2]	0x1[9:2]	0	ADC_PDN_CH<7:0>	0: Normal operation 1: Power down. Power down individual ADC channels. 1[9] → CH8…1[2] → CH1
1[10]	0x1[10]	0	PARTIAL_PDN	0: Normal operation 1: Partial power down ADC
1[11]	0x1[11]	0	LOW_FREQUENCY_ NOISE_SUPPRESSION	0: No suppression 1: Suppression enabled
1[13]	0x1[13]	0	EXT_REF	0: Internal reference 1: External reference. VREF_IN is used. Both 3[15] and 1[13] should be set as 1 in the external reference mode
1[14]	0x1[14]	0	LVDS_OUTPUT_RATE_2X	0: 1× rate 1: 2× rate. Combines data from 2 channels on 1 LVDS pair. When ADC clock rate is low, this feature can be used.
1[15]	0x1[15]	0	SINGLE-ENDED_CLK_MODE	0: Differential clock input 1: Single-ended clock input
2[2:0]	0x2[2:0]	0	RESERVED	Set to 0
2[10:3]	0x2[10:3]	0	POWER-DOWN_LVDS	0: Normal operation 1: PDN individual LVDS outputs. 2[10] → CH8…2[3] → CH1
2[11]	0x2[11]	0	AVERAGING_ENABLE	0: No averaging 1: Average two channels to increase SNR
2[12]	0x2[12]	0	LOW_LATENCY	0: Default latency with digital features supported 1: Low latency with digital features bypassed

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Register Maps (continued)

Address (DEC)	Address (HEX)	Default Value	Function	Description
2[15:13]	0x2[15:13]	0	TEST_PATTERN_MODES	000: Normal operation 001: Sync 010: De-skew 011: Custom 100:All 1's 101: Toggle 110: All 0's 111: Ramp. Note: Reg.0x16 should be set as 1, i.e. demodulator is disabled.
3[7:0]	0x3[7:0]	0	INVERT_CHANNELS	0: No inverting 1: Invert channel digital output. 3[7] → CH8;3[0] → CH1. Note: Suppose that the device is giving digital output of 11001100001111. After enabling this bit, output of device becomes 00110011110000. Note: This function is not applicable for ADC test patterns and in demod mode.
3[8]	0x3[8]	0	CHANNEL_OFFSET_ SUBSTRACTION_ENABLE	0: No offset subtraction 1: Offset value subtract enabled
3[9:11]	0x3[9:11]	0	RESERVED	Set to 0
3[12]	0x3[12]	0	DIGITAL_GAIN_ENABLE	0: No digital gain 1: Digital gain enabled
3[14:13]	0x3[14:13]	0	SERIALIZED_DATA_RATE	Serialization factor 00: 14× 01: 16× 10: Reserved 11: 12× When 4[1] = 1, in the 16× serialization rate, two zeros are filled at two LSBs (see Table 5). Note: Make sure the settings aligning with the demod register 0x3[14:13]. Be aware that the same setting, for example, 00, in these two registers can represent different LVDS data rates respectively.
3[15]	0x3[15]	0	ENABLE_EXTERNAL_ REFERENCE_MODE	0: Internal reference mode 1: Set to external reference mode Note: Both 3[15] and 1[13] should be set as 1 when configuring the device in the external reference mode.
4[1]	0x4[1]	0	ADC_RESOLUTION_SELECT	0: 14 bit 1: 12 bit
4[3]	0x4[3]	0	ADC_OUTPUT_FORMAT	0: 2's complement 1: Offset binary **Note: When the demodulation feature is enabled, only 2's complement format can be selected.**
4[4]	0x4[4]	0	LSB_MSB_FIRST	0: LSB first 1: MSB first
5[13:0]	0x5[13:0]	0	CUSTOM_PATTERN	Custom pattern data for LVDS output (2[15:13] = 011)
10[8]	0xA[8]	0	SYNC_PATTERN	0: Test pattern outputs of 8 channels are not synchronized. 1: Test pattern outputs of 8 channels are synchronized.
13[9:0]	0xD[9:0]	0	OFFSET_CH1	Value to be subtracted from channel 1 code
13[15:11]	0xD[15:11]	0	DIGITAL_GAIN_CH1	0 to 6 dB in 0.2-dB steps
15[9:0]	0xF[9:0]	0	OFFSET_CH2	Value to be subtracted from channel 2 code
15[15:11]	0xF[15:11]	0	DIGITAL_GAIN_CH2	0 to 6 dB in 0.2-dB steps
17[9:0]	0x11[9:0]	0	OFFSET_CH3	Value to be subtracted from channel 3 code
17[15:11]	0x11[15:11]	0	DIGITAL_GAIN_CH3	0 to 6 dB in 0.2-dB steps
19[9:0]	0x13[9:0]	0	OFFSET_CH4	Value to be subtracted from channel 4 code
19[15:11]	0x13[15:11]	0	DIGITAL_GAIN_CH4	0 to 6 dB in 0.2-dB steps
21[0]	0x15[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH1-4	0: Disable the digital HPF filter; 1: Enable for 1 to 4 channels Note: This HPF feature is only available when the demodulation block is disabled.
21[4:1]	0x15[4:1]	0	DIGITAL_HPF_FILTER_K_CH1-4	Set K for the HPF (k from 2 to 10, that is 0010B to 1010B). This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 4)

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Register Maps (continued)

Address (DEC)	Address (HEX)	Default Value	Function	Description
22[0]	0x16[0]	0	DIS_DEMOD	0: Digital demodulator is enabled 1: Digital demodulator is disabled Note: The demodulator registers can be reset when 0x16[0] is set as 0. Thus, it is required to reconfigure the demodulator registers after toggling the 0x16[0].
25[9:0]	0x19[9:0]	0	OFFSET_CH8	Value to be subtracted from channel 8 code
25[15:11]	0x19[15:11]	0	DIGITAL_GAIN_CH8	0 to 6-dB in 0.2-dB steps
27[9:0]	0x1B[9:0]	0	OFFSET_CH7	Value to be subtracted from channel 7 code
27[15:11]	0x1B[15:11]	0	DIGITAL_GAIN_CH7	0 to 6-dB in 0.2-dB steps
29[9:0]	0x1D[9:0]	0	OFFSET_CH6	Value to be subtracted from channel 6 code
29[15:11]	0x1D[15:11]	0	DIGITAL_GAIN_CH6	0 to 6-dB in 0.2-dB steps
31[9:0]	0x1F[9:0]	0	OFFSET_CH5	Value to be subtracted from channel 5 code
31[15:11]	0x1F[15:11]	0	DIGITAL_GAIN_CH5	0 to 6-dB in 0.2-dB steps
33[0]	0x21[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH5-8	0: Disable the digital HPF filter 1: Enable for 5 to 8 channels Note: This HPF feature is only available when the demodulation block is disabled.
33[4:1]	0x21[4:1]	0	DIGITAL_HPF_FILTER_K_CH5-8	Set K for the HPF (k from 2 to 10, 0010B to 1010B) This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k / (2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 4)

10.6.1.2 AFE5812 ADC Register/Digital Processing Description

The ADC in the AFE5812 has extensive digital processing functionality, which can be used to enhance ultrasound system performance. The digital processing blocks are arranged as in Figure 88.

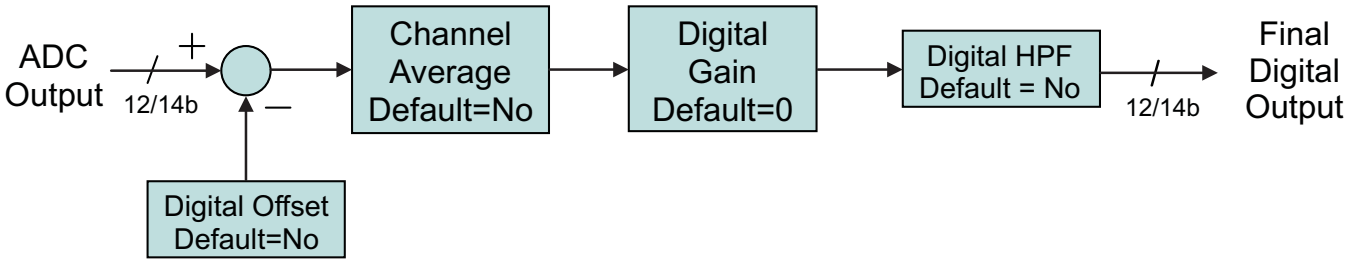


Figure 88. ADC Digital Block Diagram

NOTE

These digital processing features are only available when the demodulation block is disabled. ADC output data directly enter the digital demodulator when the demod is enabled.

10.6.1.2.1 AVERAGING_ENABLE: Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3
- Channel 3 + channel 4 comes out on channel 4
- Channel 5 + channel 6 comes out on channel 5
- Channel 7 + channel 8 comes out on channel 6

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10.6.1.2.2 ADC_OUTPUT_FORMAT: Address: 4[3]

The ADC output, by default, is in 2's-complement mode. Programming the ADC_OUTPUT_FORMAT bit to 1 inverts the MSB, and the output becomes straight-offset binary mode. **When the demodulation feature is enabled, only 2's complement format can be selected**.

10.6.1.2.3 ADC Reference Mode: Address 1[13] and 3[15]

The following shows the register settings for the ADC internal reference mode and external reference mode.

- 0x1[13] 0x3[15] = 00: ADC internal reference mode, VREF_IN floating (pin M3)
- 0x1[13] 0x3[15] = 01: N/A
- 0x1[13] 0x3[15] = 10: N/A
- 0x1[13] 0x3[15] = 11: ADC external reference mode, VREF_IN = 1.4 V (pin M3)

10.6.1.2.4 DIGITAL_GAIN_ENABLE: Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by DIGTAL_GAIN_CHi <15:11>. The gain is given as 0dB + 0.2dB × DIGTAL_GAIN_CHi<15:11>. For instance, if DIGTAL_GAIN_CH5<15:11> = 3, channel 5 is increased by 0.6-dB gain. DIGTAL_GAIN_CHi <15:11> = 31 produces the same effect as DIGTAL_GAIN_CHi <15:11> = 30, setting the gain of channel i to 6 dB.

10.6.1.2.5 DIGITAL_HPF_ENABLE

- CH1 to CH4: Address 21[0]
- CH5 to CH8: Address 33[0]

10.6.1.2.6 DIGITAL_HPF_FILTER_K_CHX

- CH1 to CH4: Address 21[4:1]
- CH5 to CH8: Address 33[4:1]

This group of registers controls the characteristics of a digital high-pass transfer function applied to the output data, following Equation 4.

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right] \quad (4)$$

These digital HPF registers (one for the first four channels and one for the second group of four channels) describe the setting of K. The digital HPF can be used to suppress low frequency noise, which commonly exists in ultrasound echo signals. The digital filter can significantly benefit near-field recovery time due to T/R switch low-frequency response. Table 4 shows the cut-off frequency versus K.

Table 4. Digital HPF –1-dB Corner Frequency versus K and Fs

k	40 MSPS	50 MSPS	65 MSPS
2	2780 kHz	3480 kHz	4520 kHz
3	1490 kHz	1860 kHz	2420 kHz
4	770 kHz	960 kHz	1250 kHz

10.6.1.2.7 LOW_FREQUENCY_NOISE_SUPPRESSION: Address: 1[11]

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0 to 1 MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5812 to approximately Fs / 2, thereby moving the noise floor around dc to a much lower value. Register bit 1[11] is used for enabling or disabling this feature. When this feature is enabled, power consumption of the device is increased slightly by approximately 1 mW/CH.

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10.6.1.2.8 LVDS_OUTPUT_RATE_2X: Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1× (LVDS_OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, in this way lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination should be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first.

10.6.1.2.9 CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8]

Setting this bit to 1 enables the subtraction of the value on the corresponding OFFSET_CHx<9:0> (offset for channel i) from the ADC output. The number is specified in 2's complement format. For example, OFFSET_CHx<9:0> = 11 1000 0000 means subtract –128. For OFFSET_CHx<9:0> = 00 0111 1111 the effect is to subtract 127. In effect, both addition and subtraction can be performed. Note that the offset is applied before the digital gain (see DIGITAL_GAIN_ENABLE). The whole data path is 2's complement throughout internally, with digital gain being the last step. Only when ADC_OUTPUT_FORMAT = 1 (straight binary output format) is the 2's complement word translated into offset binary at the end.

10.6.1.2.10 SERIALIZED_DATA_RATE: Address: 3[14:13]

See Table 5 for detailed description.

Table 5. Corresponding Register Settings

LVDS Rate	12 bit (6× DCLK)	14 bit (7× DCLK)	16 bit (8× DCLK)
Register 3 [14:13]	11	00	01
Register 4 [2:0]	010	000	000
Description	2 LSBs removed	N/A	2 zeroes added at LSBs

10.6.1.2.11 TEST_PATTERN_MODES: Address: 2[15:13]

The AFE5812 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13] = 111 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all 0s by setting Register 2[15:13] = 110.
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13] = 100.
4. **Deskew Pattern:** When 2[15:13] = 010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13] = 001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13] = 101, the normal ADC output is alternating between 1s and 0s. The start state of ADC word can be either 1s or 0s.
7. **Custom Pattern:** It can be enabled when 2[15:13] = 011. Users can write the required VALUE into register bits <CUSTOM PATTERN>, which is Register 5[13:0]. Then, the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24 SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern takes approximately 128 × (24 SCLK clock cycles + 4 ADC clock cycles).

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NOTE

Only one of the above patterns can be active at any given instant.

Digital demodulator should be disabled, i.e. Register 0x16=1.

10.6.1.2.12 SYNC_PATTERN: Address: 10[8]

By enabling this bit, all channels' test pattern outputs are synchronized. When 10[8] is set as 1, the ramp patterns of all 8 channels start simultaneously.

10.6.1.3 VCA Register Map

Address (DEC)	Address (HEX)	Default Value	Function	Description
51[0]	0x33[0]	0	RESERVED	Set to 0
51[3:0]	0x33[3:0]	0	LPF_PROGRAMMABILITY	1000: 10 MHz 0000: 15MHz, 0100: 20 MHz, 0110: 30MHz, 0101: 35 MHz 0111: 50 MHz Note: 0x3D[14], that is, 5 MHz LPF, should be set as 0.
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disable offset integrator for PGA. See the explanation for the PGA integrator function in the *Application Information* section
51[7:5]	0x33[7:5]	0	PGA_CLAMP_LEVEL	Low-noise mode: 53[11:10] = 00 000: –2 dBFS 010: 0 dBFS 1XX: Clamp is disabled Low-power/medium-power mode; 53[11:10] = 01/10 100: –2 dBFS 110: 0 dBFS 0XX: clamp is disabled Note: The clamp circuit makes sure that PGA output is in linear range. For example, at 000 setting, PGA output HD3 will worsen by 3 dB at –2-dBFS ADC input. In normal operation, clamp function can be set as 000 in the low-noise mode. The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled. Note: In the low-power and medium-power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0. . Note: Register 61[15] should be set as 0; otherwise, PGA_CLAMP_LEVEL is affected by Register 61[15].
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24 dB 1:30 dB
51[15:14]	0x33[15:14]	0	RESERVED	Set to 0
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	See Table 7. Register 52[5] should be set as 1 to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disable 1: Enable internal active termination individual resistor control

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Address (DEC)	Address (HEX)	Default Value	Function	Description
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50 Ω 01: 100 Ω 10: 200 Ω 11: 400 Ω Note: The device adjusts resistor mapping (52[4:0]) automatically. 50-Ω active termination is not supported in 15-dB LNA setting. Instead, 00 represents high-impedance mode when LNA gain is 15 dB.
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disable 1: Enable active termination
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting 01: 1.5 Vpp 10: 0.825 Vpp 11: 0.6 Vpp
52[11]	0x34[11]	0	RESERVED	Set to 0
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enable 1: Disable offset integrator for LNA. See the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18 dB 01: 24 dB 10: 15 dB 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable 1: Enable LNA individual channel control. See Register 57 for details
53[7:0]	0x35[7:0]	0	VCA_PDN_CH<7:0>	0: Normal operation 1: Powers down corresponding channels. Bit7 → CH8, Bit6 → CH7…Bit0 → CH1. PDN_CH shuts down whichever blocks are active depending on TGC mode or CW mode.
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	LOW_NF	0: Normal operation 1: Enable low-noise figure mode for high-impedance probes
53[11:10]	0x35[11:10]	0	POWER_MODES	00: Low noise mode 01: Set to low-power mode. At 30-dB PGA, total chain gain may slightly change. See *Typical Characteristics*. 10: Set to medium-power mode. At 30-dB PGA, total chain gain may slightly change. See *Typical Characteristics*. 11: Reserved
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation 1: Powers down VCAT and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation 1: Powers down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation 1: Powers down LNA, VCAT, and PGA partially (fast-wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation 1: Power down LNA, VCAT, and PGA completely (slow-wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	CW_SUM_AMP_GAIN_CNTL	Select feedback resistor for the CW amplifier as per Table 7
54[5]	0x36[5]	0	CW_16X_CLK_SEL	0: Accept differential clock 1: Accept CMOS clock

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Address (DEC)	Address (HEX)	Default Value	Function	Description
54[6]	0x36[6]	0	CW_1X_CLK_SEL	0: Accept CMOS clock 1: Accept differential clock
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	CW_TGC_SEL	0: TGC mode 1 : CW mode Note : VCAT and PGA are still working in CW mode. They should be powered down separately through 53[12].
54[9]	0x36[9]	0	CW_SUM_AMP_ENABLE	0: Enable CW summing amplifier 1: Disable CW summing amplifier Note: 54[9] is only effective in CW mode.
54[11:10]	0x36[11:10]	0	CW_CLK_MODE_SEL	00: 16× mode 01: 8× mode 10: 4× mode 11: 1× mode
54[15:12]	0x36[15:12]	0	RESERVED	Set to 0
55[3:0]	0x37[3:0]	0	CH1_CW_MIXER_PHASE	0000 → 1111, 16 different phase delays, see Table 11
55[7:4]	0x37[7:4]	0	CH2_CW_MIXER_PHASE	
55[11:8]	0x37[11:8]	0	CH3_CW_MIXER_PHASE	
55[15:12]	0x37[15:12]	0	CH4_CW_MIXER_PHASE	
56[3:0]	0x38[3:0]	0	CH5_CW_MIXER_PHASE	
56[7:4]	0x38[7:4]	0	CH6_CW_MIXER_PHASE	
56[11:8]	0x38[11:8]	0	CH7_CW_MIXER_PHASE	
56[15:12]	0x38[15:12]	0	CH8_CW_MIXER_PHASE	
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18 dB 01: 24 dB 10: 15 dB 11: Reserved REG52[15] should be set as 1.
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18 dB 01: 24 dB 10: 15 dB 11: Reserved REG52[15] should be set as 1.
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[1:0]	0x3B[1:0]	0	RESERVED	Set to 0
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100 kHz 01: 50 kHz 10: 200 kHz 11: 150 kHz with 0.015 µF on INMx
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0-dB attenuation 001: 6-dB attenuation N: About N × 6 dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: Disable digital TGC attenuator 1: Enable digital TGC attenuator
59[8]	0x3B[8]	0	CW_SUM_AMP_PDN	0: Power down 1: Normal operation Note: 59[8] is only effective in TGC test mode.
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal CW operation 1: PGA outputs appear at CW outputs.
59[15:10]	0x3B[15:10]	0	RESERVED	Set to 0
61[12:0]	0x3D[12:0]	0	RESERVED	Set to 0

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Address (DEC)	Address (HEX)	Default Value	Function	Description
61[13]	0x3D[13]	0	V2I_CLAMP	0: Clamp disabled 1: Clamp enabled at the V2I input. An additional voltage clamp at the V2I input. This limits the amount of overload signal the PGA sees.
61[14]	0x3D[14]	0	5MHz_LPF	0: 5-MHz LPF disabled 1: 5-MHz LPF enabled. Suppress signals >5 MHz or high-order harmonics. **The LPF Register 51[3:1] needs to be set as 100, that is, 10 MHz.**
61[15]	0x3D[15]	0	PGA_CLAMP_-6dBFS	0: Disable the –6-dBFS clamp. PGA_CLAMP is set by Reg51[7:5]. 1: Enable the –6-dBFS clamp. **PGA_CLAMP Reg51[7:5] should be set as 000 in the low-noise mode or 100 in the low-power/medium-power mode.** In this setting, PGA output HD3 will be worsen by 3 dB at –6-dBFS ADC input. The actual PGA output is reduced to approximately 1.5 Vpp, about 2.5 dB below the ADC full-scale input 2 Vpp . As a result, AFE5812's LPF is not saturated, and it can suppress harmonic signals better at PGA output. Due to PGA output reduction, the ADC output dynamic range is impacted. **Note: This bit is ONLY valid when PGA=24dB.**

10.6.1.4 VCA Register Description

10.6.1.4.1 LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 6 describes the relationship between LNA gain and 52[4:0] settings. The input impedance settings are the same for both TGC and CW paths.

The AFE5812 also has four preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

Table 6. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450-Ω feedback resistor
00010	Enables 900-Ω feedback resistor
00100	Enables 1800-Ω feedback resistor
01000	Enables 3600-Ω feedback resistor
10000	Enables 4500-Ω feedback resistor

The input impedance of AFE can be programmed through Register 52[8:0]. Each bit of Register 52[4:0] controls one active termination resistor. The following tables indicate the nominal impedance values when individual active termination resistors are selected. See *Active Termination* for more details. Table 7 shows the corresponding impedances under different Register 52[4:0] values, while Table 8 shows the Register 52[4:0] settings under different impedances.

NOTE

Table 7 and Table 8 show nominal input impedance values. Due to silicon process variation, the actual values can vary.

Table 7. Register 52[4:0] versus LNA Input Impedances

52[4:0]/0x34[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
LNA:15dB	High Z	118 Ω	236 Ω	79 Ω	472 Ω	94 Ω	157 Ω	67 Ω

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Table 7. Register 52[4:0] versus LNA Input Impedances (continued)

52[4:0]/0x34[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	01000	01001	01010	01011	01100	01101	01110	01111
LNA:15dB	944 Ω	105 Ω	189 Ω	73 Ω	315 Ω	86 Ω	135 Ω	63 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	10000	10001	10010	10011	10100	10101	10110	10111
LNA:15dB	1181 Ω	107 Ω	197 Ω	74 Ω	337 Ω	87 Ω	139 Ω	64 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	11000	11001	11010	11011	11100	11101	11110	11111
LNA:15dB	525 Ω	96 Ω	163 Ω	68 Ω	249 Ω	80 Ω	121 Ω	60 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

Table 8. LNA Input Impedances versus Register 52[4:0]

Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB
25			11111	67	00111	10101		139	10110		
27			10111/01111	68	11011			143			10100
29			00111/11011	69			11010	144		01010	
31			01011/10011	72		00101		150		10010	
33			00011	73	01011	11001		157	00110		
34			11101	74	10011			163	11010		
36			01101	79	00011			176			
37			10101	80	11101	01001	01010	180		00010	
40			00101	81				189	01010	11100	
41			11001	82		10001		197	10010		
44			01001	83			10010	200			00100
45			10001	86	01101			222			11000
46		11111		87	10101			236	00010		
48		01111		90		00001		240		01100	
49		10111		92		11110		249	11100		
50			00001	94	00101			257		10100	
51			00111/11110	96	11001			315	01100		
52		11011		100			00010	337	10100		
55		01011		103		01110		360		00100	
56		10011		105	01001		11100	400		11000	01000
57			01110	106		10110		472	00100		
59			10110	107	10001			500			10000
60	11111	00011		118	00001			525	11000		
61		11101		120		00110		667			
63	01111			121	11110			720		01000	
64	10111			122				900		10000	

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Table 8. LNA Input Impedances versus Register 52[4:0] (continued)

Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:15dB	LNA:18dB	LNA:24dB
65		01101		124		11010		944	01000		
66.7			00110	133			01100	1181	10000		
				135	01110						

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10.6.1.4.2 Programmable Gain for CW Summing Amplifier

Different gain can be configured for the CW summing amplifier through the register 54[4:0]. By enabling and disabling the feedback resistors between the summing amplifier inputs and outputs, the gain is adjustable accordingly to maximize the dynamic range of CW path. Table 9 describes the relationship between the summing amplifier gain and 54[4:0] settings.

Table 9. Register 54[4:0] Description

54[4:0]/0x36[4:0]	FUNCTION
00000	No feedback resistor
00001	Enables 250-Ω feedback resistor
00010	Enables 250-Ω feedback resistor
00100	Enables 500-Ω feedback resistor
01000	Enables 1000-Ω feedback resistor
10000	Enables 2000-Ω feedback resistor

Table 10. Register 54[4:0] vs Summing Amplifier Gain

54[4:0]/0x36[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
CW I/V Gain	N/A	0.50	0.50	0.25	1.00	0.33	0.33	0.20
54[4:0]/0x36[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
CW I/V Gain	2.00	0.40	0.40	0.22	0.67	0.29	0.29	0.18
54[4:0]/0x36[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
CW I/V Gain	4.00	0.44	0.44	0.24	0.80	0.31	0.31	0.19
54[4:0]/0x36[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
CW I/V Gain	1.33	0.36	0.36	0.21	0.57	0.27	0.27	0.17

10.6.1.4.3 Programmable Phase Delay for CW Mixer

Accurate CW beamforming is achieved through adjusting the phase delay of each channel. In the AFE5812, 16 different phase delays can be applied to each LNA output. It meets the standard requirement of typical ultrasound beamformer, that is, $\frac{1}{16}\lambda$ beamformer resolution. Table 9 describes the relationship between the phase delays and the register 55 and 56 settings.

Table 11. CW Mixer Phase Delay vs Register Settings
CH1 to 55[3:0], CH2 to 55[7:4], CH3 to 55[11:8], CH4 to 55[15:12], CH5 to 56[3:0], CH6 to 56[7:4], CH7 to 56[11:8], CH8 to 56[15:12]

Phase Delay	Register Settings							
CHX_CW_MIXER_PHASE	0000	0001	0010	0011	0100	0101	0110	0111
PHASE SHIFT	0	22.5°	45°	67.5°	90°	112.5°	135°	157.5°
CHX_CW_MIXER_PHASE	1000	1001	1010	1011	1100	1101	1110	1111
PHASE SHIFT	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°

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10.6.2 Digital Demodulator Register Description

Table 12. Digital Demodulator Register Map(1)(2)(3)

Register Name	Address (HEX) BIT [5:0]	Address (DEC) BIT [5:0]	Default	Description
MANUAL_TX_TRIG	00[2]	00[2]	0	1: Generate internal TX_TRIG (self clear, write only). This is an alternative for TX_SYNC hardware pulse.
REGISTER_READOUT_ENABLE	00[1]	00[1]	0	1: Enables readout of register at SDOUT pin (write only)
CHIP_ID	01[4:0]	01[4:0]	0	Unique chip ID
OUTPUT_MODE	02[15:13]	02[15:13]	0	000 = Normal operation 011 = Custom pattern (set by register 05) Note: LSB always comes out first regardless of whether 0x04[4] = 0 or 1. 111 = chipID + ramp test pattern. ChipID (5 bit) and subchip information (3 bit) are the 8 LSBs and the ramp pattern is in the rest MSBs. (0x0A[9] = 1). Note: Valid only when the demodulator is enabled, i.e. ADC register 0x16=0.
SERZ_FACTOR	03[14:13]	03[14:13]	11	Serialization factor (output rate) 00 = Reserved 01 = 12x 10 = 14x 11 = 16x Note: This register is different from the ADC SERIALIZED_DATA_RATE. The demod and ADC serialization factors must be matched.
OUTPUT_RESOLUTION	03[11:9]	03[11:9]	0	Output resolution of the demodulator. It refers to the ADC resolution when the demodulator is bypassed. 100 = 16 bit (demod only) 000 = 14 bit 001 = 13 bit 010 = 12 bit
MSB_FIRST	04[4]	04[4]	0	0 = LSB first 1 = MSB first This bit does not affect the test mode: customer pattern, that is, 02[15:13] = 011B. Note: in the CUSTOM_PATTERN mode, the output is always set as LSB first regardless of this bit setting.
CUSTOM_PATTERN	05[15:0]	05[15:0]	0000	Custom data pattern for LVDS (0x02[15:13] = 011)
COEFF_MEM_ADDR_WR	06[7:0]	06[7:0]	0	Write address offset to coefficient memory (auto increment)
COEFF_BANK	07[111:0]	07[111:0]	—	Writes chunks of 112 bits to the coefficient memory. This RAM does not have default values, so it is necessary to write required values to the RAM. TI recommends to configure the RAM before other registers.
PROFILE_MEM_ADDR_WR	08[4:0]	08[4:0]	0	Write address offset to profile memory (auto increment)
PROFILE_BANK	09 [63:0]	09 [63:0]	—	Writes chunks of 64 bits to the profile memory (effective 62 bits because two LSBs are ignored). This RAM does not have default values, so it is necessary to write required values to the RAM. TI recommends to configure the RAM before other registers.
RESERVED	0A[15]	10[15]	0	**Must set to 0**
MODULATE_BYPASS	0A[14]	10[14]	0	Arrange the demodulator output format for I/Q data. See Table 11.
DEC_SHIFT_SCALE	0A[13]	10[13]	0	0 = No additional shift applied to the decimation filter output. 1 = Shift the decimation filter output by 2 bits additionally, that is apply 12-dB additional digital gain.

(1) When programming the SPI, 8-bit address is required. This table and the following sections only list the Add_Bit5 to Add_Bit0. The Add_Bit7 = SCID1_SEL and Add_Bit6 = SCID0_SEL need to be appended as 11, 10, or 01, which determines if SubChip1 or SubChip0 is being programmed. If SCID1_SEL,SCID0_SEL = 11, then both subchips get written with the same register value. See Table 3.
(2) Reserved register bits must be programmed based on their descriptions.Unlisted register bits must be programmed as zeros.
(3) ADC CLK is required to access the demodulation registers.

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Table 12. Digital Demodulator Register Map(1)(2)(3) (continued)

Register Name	Address (HEX) BIT [5:0]	Address (DEC) BIT [5:0]	Default	Description
DHPF	0A[12]	10[12]	1	0 = Enable first-order digital HPF. –3 dB cut off frequency is at 0.0225 × Fs / 2. Its transfer function equation is h(n) = a / b, where a = [1 – 7569 / 2^{13}] and b = [1 –1]; 1 = Disable first-order digital HPF.
OUTPUT_CHANNEL_SEL	0A[11]	10[11]	0	Swap channel pairs. It is used in 4 LVDS bypass configuration to select which of the two possible data streams to pass on. See Table 11.
SIN_COS_RESET_ON_TX_TRIG	0A[10]	10[10]	1	0 = Continuous phase 1 = Reset down conversion phase on TX_TRIG
FULL_LVDS_MODE	0A[9]	10[9]	0	0 = Use 4 LVDS lines (1, 3, 5, 7) 1 = Use 8 LVDS lines (1 through 8) Note: 4 LVDS mode valid only for decimation factors ≥4. See Table 14.
RESERVED	0A[8:5]	10[8:5]	0	**Must set to 0**
RESERVED	0A[4]	10[4]	0	**Must set to 1**
DEC_BYPASS	0A[3]	10[3]	0	0 = Enable decimation filter 1 = Bypass decimation filter
DWN_CNV_BYPASS	0A[2]	10[2]	0	0 = Enable down conversion block 1 = Bypass down conversion block. Note: the decimation filter can still be used when the down conversion block is bypassed.
RESERVED	0A[1]	10[1]	1	**Must set to 1**
DC_REMOVAL_BYPASS	0A[0]	10[0]	0	0 = Enable DC removal block 1 = Bypass DC removal block
SYNC_WORD	0B[15:0]	11[15:0]	0x2772	LVDS sync word. When MODULATE_BYPASS = 1, there is no sync word output.
PROFILE_INDX	0E[15:11]	14[15:11]	0	Profile word selector. The Profile Index register is a special 5-bit data register. Read value still uses 16-bit convention, which means data will be available on LSB 0e[4:0])
DC_REMOVAL_1_5	14[13:0]	20[13:0]	0	54[13:0] → DC offset for channel 1, SCID1_SEL,SCID0_SEL = 01 94[13:0] → DC offset for channel 5, SCID1_SEL,SCID0_SEL = 10 Note: Considering the CH-to-CH DC offset variation, the offset value must be set individually. Therefore, SCID1_SEL,SCID0_SEL should not be set as 11. Note: DC_REMOVAL_X_X registers are write-only.
DC_REMOVAL_2_6	15[13:0]	21[13:0]	0	55[13:0] → DC offset for channel 2, SCID1_SEL,SCID0_SEL = 01 95[13:0] → DC offset for channel 6, SCID1_SEL,SCID0_SEL = 10 Note: Considering the CH-to-CH DC offset variation, the offset value must be set individually. Therefore, SCID1_SEL,SCID0_SEL should not be set as 11. Note: DC_REMOVAL_X_X registers are write-only.
DC_REMOVAL_3_7	16[13:0]	22[13:0]	0	56[13:0] → DC offset for channel 3, SCID1_SEL,SCID0_SEL=01 96[13:0] → DC offset for channel 7, SCID1_SEL,SCID0_SEL=10 Note: Considering the CH-to-CH DC offset variation, the offset value must be set individually. Therefore, SCID1_SEL,SCID0_SEL should not be set as 11. Note: DC_REMOVAL_X_X registers are write-only.
DC_REMOVAL_4_8	17[13:0]	23[13:0]	0	57[13:0] → DC offset for channel 4, SCID1_SEL,SCID0_SEL = 01 97[13:0] → DC offset for channel 8, SCID1_SEL,SCID0_SEL = 10 Note: Considering the CH-to-CH DC offset variation, the offset value must be set individually. Therefore, SCID1_SEL,SCID0_SEL should not be set as 11. Note: DC_REMOVAL_X_X registers are write-only.
DEC_SHIFT_FORCE_EN	1D[7]	29[7]	0	0 = Profile vector specifies the number of bit to shift for the decimation filter output. 1 = Register 1D[6:4] specifies the number of bit to shift for the decimation filter output.

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Table 12. Digital Demodulator Register Map[1][2][3] (continued)

Register Name	Address (HEX) BIT [5:0]	Address (DEC) BIT [5:0]	Default	Description
DEC_SHIFT_FORCE	1D[6:4]	29[6:4]	0	Specify that the decimation filter output is right-shifted by (20 – N) bit, N = 0x1D[6:4]. N = 0, minimal digital gain; N = 7 maximal digital gain; additional 12-dB digital gain can be applied by setting DEC_SHIFT_SCALE = 1, that is, 0x0A[13] = 1
TM_COEFF_EN	1D[3]	29[3]	0	1 = Set coefficient output test mode
TM_SINE_EN	1D[2]	29[2]	0	1 = Set sine output mode; the sine waveform specifications can be configured through register 0x1E.
RESERVED	1D[1]	29[1]	0	**Must set to 0**
RESERVED	1D[0]	29[0]	0	**Must set to 0**
TM_SINE_DC	1E[15:9]	30[15:9]	0	7-bit signed value for sine wave DC offset control.
TM_SINE_AMP	1E[8:5]	30[8:5]	0	4-bit unsigned value, controlling the sine wave amplitude (powers of two), from unity to the full scale of 14 bit, including saturation. 0 = No sine (only DC)
TM_SINE_STEP	1E[4:0]	30[4:0]	0	5-bit unsigned value, controlling the sine wave frequency with resolution of Fs / 2^6, which is 0.625 MHz for 40-MHz ADC clock.
MANUAL_COEFF_START_EN	1F[15]	31[15]	0	0 = The starting address of the coefficient RAM is set by the profile vector, that is, the starting address is set manually. 1 = The starting address of the coefficient RAM is set by the register 0x1F[14:7].
MANUAL_COEFF_START_ADDR	1F[14:7]	31[14:7]	0	When 0x1F[15] is set, the starting address of coefficient RAM is set by these 8 bits.
MANUAL_DEC_FACTOR_EN	1F[6]	31[6]	0	0 = The decimation factor is set by profile vector. 1 = The decimation factor is set by the register 0x1F[5:0].
MANUAL_DEC_FACTOR	1F[5:0]	31[5:0]	0	When 0x1F[6] is set, the decimation factor is set by these 6 bits. Note: It is from 1 to 32.
MANUAL_FREQ_EN	20[0]	32[0]	0	0 = The down convert frequency is set by profile vector. 1 = The down convert frequency is set by the register 0x21[15:0].
MANUAL_FREQ	21[15:0]	33[15:0]	0	When 0x20[0] is set, the value of manual down convert frequency is calculated as N × Fs / 2^{16}

Table 13. Configuring Data Output:

Register Name	SPI Address
SERZ_FACTOR	0x03[14:13]
OUTPUT_RESOLUTION	0x03[11:9]
MSB_FIRST	0x04[4]
OUT_MODE	0x02[15:13]
CUSTOM_PATTERN	0x05[15:0]
OUTPUT_CHANNEL_SEL	0x0A[11]
MODULATE_BYPASS	0x0A[14]
FULL_LVDS_MODE	0x0A[9]

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1. Serializer configuration:
   - Serialization Factor 0x03[14:13]: It can be set using demodulator register SERZ_FACTOR. Default serialization factor for the demodulator is 16×. However, the actual LVDS clock speed can be set by the serialization factor in the ADC SPI interface as well; the ADC serialization factor is adjusted to 14× by default. Therefore, it is necessary to sync these two settings when the demodulator is enabled, that is, set the ADC register 0x03[14:13] = 01.
   - Output Resolution 0x03[11:9]: In the default setting, it is 14 bits. The demodulator output resolution depends on the decimation factor. 16-bit resolution can be used when higher decimation factor is selected.
   - For RF mode (passing 14 bits only), demodulator serialization factor can be changed to 14× by setting demodulator register 0xC3[14:13] to 10.
2. Channel selection:
   - Using register MODULATE_BYPASS 0x0A[14], channel output mode can be selected as IQ modulated or single-channel I or Q output.
   - Channel output is also selected using registers OUTPUT_CHANNEL_SEL 0x0A[11] and FULL_LVDS_MODE 0x0A[9] and decimation factor.
   - Each of the two demodulator subchips in a device has four channels named A, B, C, and D.

NOTE

After decimation, the LVDS FCLK rate keeps the same as the ADC sampling rate. Considering the reduced data amount, zeros are appended after I and Q data and ensure the LVDS data rate matches the LVDS clock rate. For detailed information about channel multiplexing, see Table 14. In the table, A.I refers to CHA in-phase output, and A.Q refers to CHA quadrature output. For example, M = 3, the valid data output rate is Fs / 3 for both I and Q channels, that is 2 × Fs / 3 bandwidth is occupied. The left Fs / 3 bandwidth is then filled by M-2 zeros. As a result, the demod LVDS output data are A.I, A.Q, 0, A.I A.Q 0 after SYNC_WORD, FCLK = Fs and DCLK = Fs × 8. When two ADC CHs' data are transferred by one LVDS lane, M-4 zeros are filled after A.I, A.Q, B.I, and B.Q. See more details in Table 14 and Figure 89.

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Table 14. Channel Selection(1)

Decimation Factor (M)	Modulate Bypass	Output Channel Select	Full LVDS Mode	Decimation Factor M	LVDS Output Description
M ≥ 2	0	0	0	M < 4	LVDS1: A.I, A.Q, (zeros)
					LVDS2: B.I, B.Q, (zeros)
					LVDS3: C.I, C.Q, (zeros)
					LVDS4: D.I, D.Q, (zeros)
				M ≥ 4	LVDS1: A.I, A.Q, B.I, B.Q, (zeros) LVDS2: idle
					LVDS3: C.I, C.Q, D.I, D.Q, (zeros) LVDS4: idle
			1	X	LVDS1: A.I, A.Q, (zeros)
					LVDS2: B.I, B.Q, (zeros)
					LVDS3: C.I, C.Q, (zeros)
					LVDS4: D.I, D.Q, (zeros)
		1	0	M < 4	LVDS1: B.I, B.Q, (zeros)
					LVDS2: A.I, A.Q, (zeros)
					LVDS3: D.I, D.Q, (zeros)
					LVDS4: C.I, C.Q, (zeros)
				M ≥ 4	LVDS1: B.I, B.Q, A.I, A.Q, (zeros)
					LVDS2: idle
					LVDS3: D.I, D.Q, C.I, C.Q, (zeros)
					LVDS4: idle
			1	X	LVDS1: B.I, B.Q, (zeros)
					LVDS2: A.I, A.Q, (zeros)
					LVDS3: D.I, D.Q, (zeros)
					LVDS4: C.I, C.Q, (zeros)
M ≥ 2	1	0	X	X	LVDS1: A.I; Note: the same A.I is repeated by M times.
					LVDS2: A.Q; Note: the same A.Q is repeated by M times.
					LVDS3: C.I; Note: the same C.I is repeated by M times.
					LVDS4: C.Q; Note: the same C.Q is repeated by M times.
		1	X	X	LVDS1: B.I; Note: the same B.I is repeated by M times.
					LVDS2: B.Q; Note: the same B.Q is repeated by M times.
					LVDS3: D.I; Note: the same D.I is repeated by M times.
					LVDS4: D.Q; Note: the same D.Q is repeated by M times.
M = 1	0	0	X	1	LVDS1: A.I; LVDS2: B.I; LVDS3: C.I; LVDS4: D.I
M = 1	0	1	X	1	LVDS1: B.I; LVDS2: A.I; LVDS3: D.I; LVDS4: C.I
M = 1	1	0	X	1	LVDS1: A.I; LVDS2: A.Q; LVDS3: C.I; LVDS4: C.Q
M = 1	1	1	X	1	LVDS1: B.I; LVDS2: B.Q; LVDS3: D.I; LVDS4: D.Q

(1) This table refers to individual demodulator subchip, which has four LVDS outputs, that is LVDS1 through LVDS4; and four input CHs, that is CH.A to CH.D. See Figure 86.

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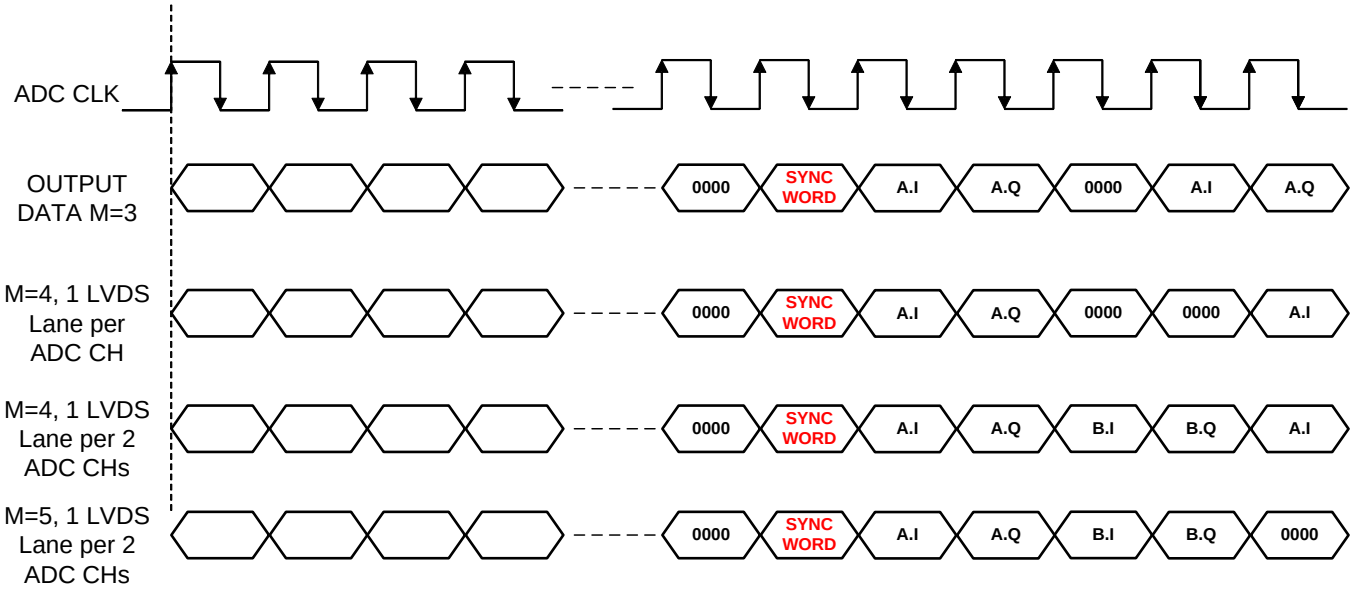


Figure 89. Output Data Format at M = 3~5

3. Output mode:
   - Using register OUT_MODE, ramp pattern and custom pattern can be enabled.
   - Custom pattern: In the case of a custom pattern, custom pattern value can be set using register CUSTOM_PATTERN. Note: LSB always comes out first regardless of whether 0x04[4] = 0 or 1, that is, MSB_FIRST = 0 or 1.
   - Ramp pattern: Demodulator generated ramp pattern includes information of chip_id as well. 8 MSB (that is, Data[15..8]) bits are ramp pattern. Next 5 bits (that is, Data[3..7]) gives value of chip ID. Data[2] corresponds to subchip ID, 0 or 1; Data[1:0] are filled with zeros.

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10.6.2.1 Common Demod Registers

Table 15. DC Removal Block

Register Name	SPI Address
DC_REMOVAL_BYPASS	0x0A[0]
DC_REMOVAL_1_5	0x14[13:0]
DC_REMOVAL_2_6	0x15[13:0]
DC_REMOVAL_3_7	0x16[13:0]
DC_REMOVAL_4_8	0x17[13:0]

- DC removal block can be bypassed using the register bit DC_REMOVAL_BYPASS.
- DC removal is designed to be done manually.
- Manual DC offset removal: Registers DC_REMOVAL_1_5, DC_REMOVAL_2_6, DC_REMOVAL_3_7, and DC_REMOVAL_4_8 can be used to give manual offset. Value should be given in 2's complement format. In the case of these registers, SCID values should be given accordingly (see *SPI for Demodulator* for more information). Example: For DC offset of channel 5, the address of the register would be 0x91 (in hex). Here SCID0 is 0 and SCID1 is 1.

Table 16. Down Conversion Block

Register Name	SPI Address
DWN_CNV_BYPASS	0x0A[2]
SIN_COS_RESET_ON_TX_TRIG	0x0A[10]
MANUAL_FREQ_EN	0x20 [0]
MANUAL_FREQ	0x21[15:0]

- Down conversion block can be bypassed using register DWN_CNV_BYPASS.
- Down conversion frequency can be given using the down conversion frequency (f) parameter of the profile vector. Alternatively, manual registers MANUAL_FREQ_EN and MANUAL_FREQ can be used to provide down conversion frequency.
- Down conversion frequency (f): 'f' can be set with resolution Fs / 2^{16} (where Fs is the sampling frequency). An integer value of '$2^{16}f$ / Fs' is given to the profile vector or respective register.
- Down conversion signal can be configured to be reset at each TX_TRIG pulse. This facility can be enabled using SIN_COS_RESET_ON_TX_TRIG.

Table 17. Decimation Block

Register Name	SPI Address
DEC_BYPASS	0x0A[3]
MANUAL_DEC_FACTOR_EN	0x1F [6]
MANUAL_DEC_FACTOR	0x1F[5:0]
MANUAL_COEFF_START_EN	0x1F[15]
MANUAL_COEFF_START_ADDR	0x1F[14:7]
DEC_SHIFT_FORCE_EN	0x1D[7]
DEC_SHIFT_FORCE	0x1D[6:4]
DEC_SHIFT_SCALE	0x0A[13]

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- Decimation block can be bypassed using register DEC_BYPASS.
- Decimation factor: This can be set using the decimation factor (M) parameter of the profile vector. Alternatively, it can be set using registers MANUAL_DEC_FACTOR_EN and MANUAL_DEC_FACTOR.
- Filter coefficients: Filter coefficients should be written to coefficient RAM (see *Profile RAM and Coefficient RAM*). The format of the filter coefficient is 2's complement. Its address pointer should be given in profile vector, or alternatively, registers MANUAL_COEFF_START_EN and MANUAL_COEFF_START_ADDR can be used.
- Filter digital gain: Decimation block takes 14-bit input data and 14-bit input coefficients and gives 36-bit output internally. While implementing this FIR filter, after multiplication and addition, the 36-bit internal filter output should be scaled approximately to make the final demod output as 16 bit, that is, applying digital gain or attenuation. Filter gain or attenuation depends on two parameters: decimation shift scale and gain compensation factor.
- Decimation shift scale can be chosen using register DEC_SHIFT_SCALE. The gain compensation factor can be given to the gain compensation factor (G) parameter of the profile vector, or can be given using registers DEC_SHIFT_FORCE_EN and DEC_SHIFT_FORCE.
- The internal 36-bit filter output is right-shifted by N bits, where N equals:
  - 20-G when Dec_Shift_Scale = 0
  - 20-G-2 when Dec_Shift_Scale = 1

  The minimal gain occurs when G = 0 and DEC_SHIFT_SCALE = 0. The total scaling range can be a factor of 2^9, that is, approximately 54 dB.

Table 18. Test Modes

Register Name	SPI Address
TM_SINE_DC	0x1E[15:9]
TM_SINE_AMP	0x1E[8:5]
TM_SINE_STEP	0x1E[4:0]
TM_SINE_EN	0x1D[2]
TM_COEFF_EN	0x1D[3]

1. Sine test mode:

   The normal ADC output can be replaced by:

$$x_n = C + 2^k \sin\left(\frac{\pi N n}{2^5}\right) \quad (5)$$

   - N is a 5-bit unsigned value, controlling the sine wave frequency with resolution of $F_S / 2^6$, which is 0.625 MHz for 40-MHz ADC clock.
   - k is 4-bit unsigned value, controlling the wave amplitude, from unity to the full scale of 14 bits, including saturation.
   - C is 7-bit signed value for DC offset control.

   The controlling values fit into one 16-bit register. This test pattern shall allow testing of demodulation, decimation filter, DC removal, gain control, and so on.
2. Coefficient output test mode:
   - The input to the decimating filter can be replaced with a sequence of one impulse and zero samples, where one impulse (0x4000) is followed by (16 × M) zeros (that is, 0 × 0000).
   - This mode is useful to check decimation filter coefficients.
   - This mode can be enabled using register TM_COEFF_EN.
3. RF mode:

   RF mode allows for the streaming of ADC data through the demodulator to the LVDS. Note: Test pattern from the ADC output stage cannot be sent to the demodulator (it can only be sent to the LVDS when the demodulator is off). RF mode without sync word can be set by the following:
   (a) Configure the ADC Serialization rate as 16bit, by setting ADC register 03[14:13]=01B.
   (b) Write 0x0041 to demod register 0xDF; that is MANUAL_DEC_FACTOR_EN = 1 and MANUAL_DEC_FACTOR = 1.

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(c) Write 0x121F to demod register 0xCA, that is, MODULATE_BYPASS = 0, FULL_LVDS_MODE = 1, DC_REMOVAL_BYPASS = 1, DWN_CNV_BYPASS = 1. DEC_BYPASS = 1, SYN_COS_RESET_ON_TX_TRIG = 0.
(d) Write 0x6800 to demod register 0xC3, that is, SERZ_FACTOR = 16×, OUTPUT_RESOLUTION = 16×,
(e) Write 0x0010 to demod register 0xC4, that is, MSB_FIRST = 1
(f) Provide TX_TRIG pulse or set demod register 0xC0[2] MANUAL_TX_TRIG
(g) Note: For RF mode (passing 14 bits only), demodulator serialization factor can be changed to 14× by setting demodulator register 0xC3[14:13] to 10B and ADC register 03[14:13]=0.

10.6.2.2 Profile RAM and Coefficient RAM

Writing data to profile RAM and coefficient RAM is similar to registers. Both RAMs do not get reset after resetting the device. RAM does not have default values, so it is necessary to write required values to RAM. RAM address values need to be given to the pointer register that points to the location wherever data needs to be written. Because both RAMs are part of the demodulator, SPI_DIG_EN should be low while writing.

NOTE

TI recommends to program the RAMs before configuring other registers.

PROFILE_INDX Reg.0x0E[15:11] must be reprogrammed in order to make profile and filter RAM correctly loaded.

A trigger is required to make new settings effective, such as profile RAM, coefficient RAM, and PROFILE_INDX Reg.0x0E[15:11] —either an external trigger event through the TX_SYNC_IN pin or a manual trigger event through Register 0[2].

ADC CLK is required during demod register, profile and coefficent RAM programming.

Table 19. Profile Related Registers

Register Name	SPI Address
PROFILE_MEM_ADDR_WR	0x08[4:0]
PROFILE_BANK	0x09[63:0]
PROFILE_INDEX	0x0E[15:11]

- Profile RAM can store up to 32 vectors/profiles. Each vector/profile has 64 bits.
- Pointer value should be given to the register PROFILE_MEM_ADDR_WR before writing to RAM.
- The 64 bits of each vector/profile are arranged as follows:

Table 20. Profile RAM(1)(2)

Name of Parameter	Address	Description
Reserved	RAM[63:50]	Set as 0
Reserved	RAM[49:36]	Set as 0
Pointer to coeff memory (P)(3)	RAM[35:28]	A pointer to filter coefficient memory (8 bits), pointing to 8 coefficient blocks. The relevant coefficients start from address P × 8 in the coefficients memory and will continue for M blocks.
Decimation Factor (M)(3)	RAM[27:22]	Decimation factor for decimation block
Down conversion frequency (f)(3)	RAM[21:6]	Down conversion frequency for down conversion block
Reserved	RAM[5]	Set as 0
Gain compensation factor (G)(3)	RAM[4:2]	Gain compensation factor parameter for decimation block
2 LSBs	RAM[1:0]	Set as 0

(1) 2 LSB's (that is, RAM[1:0]) are ignored and can be set as zeros.
(2) A particular profile vector can be activated using register PROFILE_INDEX. Address pointing to the location of particular vector is to be given in PROFILE_INDEX.
(3) Alternative manual register is available

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10.6.2.2.1 Programming the Profile RAM

1. Set SEN and SPI_DIG_EN as 0.
2. Set SPI address 0xC8[4:0] with the base address, for example 0x0000. 0xC8 means both demodulator subchips are enabled.
3. The 64 profile vector bits are arranged as following:
   - RAM[63:50] = 0 (reserved)
   - RAM[49:36] = 0 (reserved)
   - RAM[35:28] = Pointer to coeff memory (8 bit)
   - RAM[27:22] = Decimation factor (6 bit)
   - RAM[21:6] = Demodulation frequency (16 bit)
   - RAM[5] = 0
   - RAM[4:2] = Gain compensation factor (3 bit)
   - RAM[1:0] = 2 LSBs are ignored, can be set as zeros.
4. Write the above 64 bits to SPI address 0xC9 (MSB first).
5. Repeat steps 3 and 4 for the following profile entries (the address in register 0xC8 auto increments).
6. Set SEN and SPI_DIG_EN as 1.

10.6.2.2.2 Procedure for Configuring Next Vector

1. Write profile index (5 bits) to SPI address 0xCE[15:11]. 0xCE means both demodulator subchips are enabled.

Table 21. Filter Coefficient RAM

Register Name	SPI Address
COEFF_MEM_ADDR_WR	0x06[7:0]
COEFF_BANK	0x07[111:0]
MANUAL_COEFF_START_ADDR	0x1F[14:7]
MANUAL_COEFF_START_EN	0x1F[15]

- Coefficient RAM can store up to 256 coefficient memory blocks. The size of each block is 112 bits.
- Pointer value should be given to the register COEFF_MEM_ADDR_WR before writing to RAM.
- Write 112 bits to SPI address 0xC7 (MSB first). Each coefficient memory block consists of eight 14-bit coefficients which are aligned in the following manner: coefficient order from right to left and bit order from right to left).
- **Note: The coefficients are in 2's complement format.**

Table 22. Coefficient RAM Mapping(1)

Coeff 7[13:0]	Coeff 6[13:0]	Coeff 5[13:0]	Coeff 4[13:0]	Coeff 3[13:0]	Coeff 2[13:0]	Coeff 1[13:0]	Coeff 0[13:0]
111:98	97:84	83:70	69:56	55:42	41:28	27:14	13:0

(1) Note that SPI serialization is done from left to right (0xCoeff 7[13] first and 0xCoeff 0[0] last).

- Because the decimation block uses 16 × M tap FIR filter and filter coefficients are symmetric, only half (that is 8 × M) filter coefficients are necessary to be stored (M is the decimation factor). Each 8 coefficient block that is written to the memory represents a single phase of a polyphase filter. Therefore, the relation between the filter coefficients Cn and their index (i,j) in the coefficients memory is given by:

$$n = M \times (1 + I) - (1 + j) \quad (6)$$

where

- I is the index in the coefficients block, from 0 to 7.
- j is the block index, from 0 to (M – 1).

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Example for M = 4

Table 23. Coefficient RAM Mapping

j\I	7	6	5	4	3	2	1	0
0	Coeff 31	Coeff 27	Coeff 23	Coeff 19	Coeff 15	Coeff 11	Coeff 7	Coeff 3
1	Coeff 30	Coeff 26	Coeff 22	Coeff 18	Coeff 14	Coeff 10	Coeff 6	Coeff 2
2	Coeff 29	Coeff 25	Coeff 21	Coeff 17	Coeff 13	Coeff 9	Coeff 5	Coeff 1
3	Coeff 28	Coeff 24	Coeff 20	Coeff 16	Coeff 12	Coeff 8	Coeff 4	Coeff 0

- Coefficient start address can be given using the Pointer to Coeff Memory (P) parameter of profile RAM. Alternatively, the start address can be given using register MANUAL_COEFF_START_ADDR. (While using this register, register enable bit MANUAL_COEFF_START_EN should be set to 1.)

10.6.2.2.3 Programming the Coefficient RAM

1. Set SPI address 0xC6[7:0] with the base address, for example 0x0000. 0xC6 means both demodulator subchips are enabled.
2. Write 112 bits to SPI address 0xC7 (MSB first). Each coefficient memory word consists of eight 14-bit coefficients, which are aligned in the following manner: coefficient order from right to left and bit order from right to left. **Note: The coefficients are in 2's complement format.**

Figure 90.

Coeff 7[13:0]	Coeff 6[13:0]	Coeff 5[13:0]	Coeff 4[13:0]	Coeff 3[13:0]	Coeff 2[13:0]	Coeff 1[13:0]	Coeff 0[13:0]
111:98	97:84	83:70	69:56	55:42	41:28	27:14	13:0

NOTE

Note that SPI serialization is done from left to right (Coeff 7[13] first and Coeff 0[0] last).

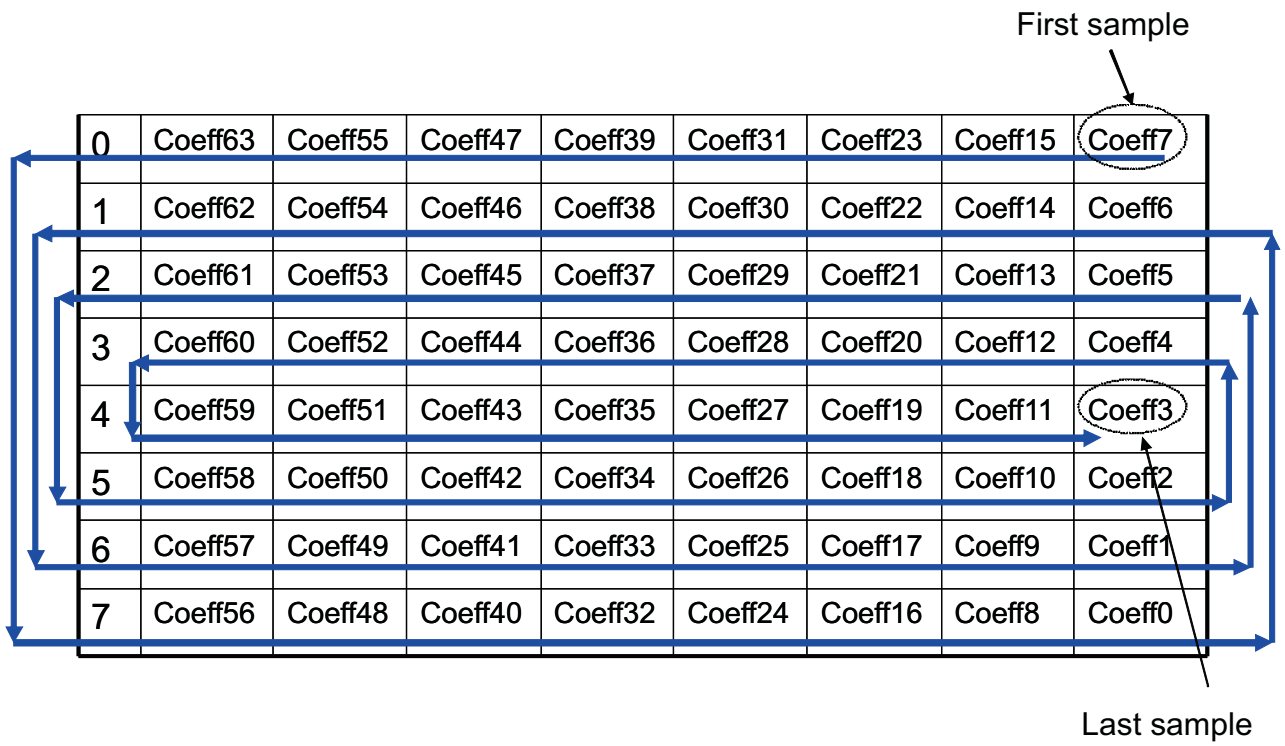
3. Repeat the previous step for the following coefficient bulk entries (the address in register 0xC6 auto increments).

10.6.2.2.4 Filter Coefficent Test Mode

Coefficient test mode allows for the streaming of coefficients through the demodulator to the LVDS. Filter coefficient test mode can be set by the following:

1. Enable TM_COEFF_EN.
2. Write OUTPUT_RESOLUTION (0x03[11:9]) = 0b100, that is, 16-bit output. (Note that output bit resolution of 14 bits will not give proper result.)
3. Write DC_REMOVAL_BYPASS (0x0A[0]) = 1, DWN_CNV_BYPASS (0x0A[2]) = 1.
4. Write DC_DEC_SHIFT_FORCE_EN (0x1D[7]) = 1, DEC_SHIFT_FORCE (0x1D[6:4] = 0b110, and DEC_SHIFT_SCALE (0x0a[13]) = 1.
5. Write MODULATE_BYPASS (0x0A[14]) = 1. After writing all of the above settings, coefficients come at the output in the sequence as follow.
6. M = 2
   - Address 0: C15 C13 C11 C09 C07 C05 C03 C01; Address 1: C14 C12 C10 C08 C06 C04 C02 C00
   - The order in which coefficients come at the output will be: 0 C01 C03 C05 C07 C09 C11 C13 C15 C14 C12 C10 C08 C06 C04 C02 C00 C00 C02 C04 C06 C08 C10 C12 C14 C15 C13 C11 C09 C07 C05 C03 C01 0
7. M = 8
   - The coefficients come to the output as shown in Figure 91.

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NOTE: When it reaches the last sample, it starts giving coefficients in the reverse direction until it reaches the point it started.

Figure 91. Coefficient Readout Sequence

10.6.2.2.5 TX_SYNC and SYNC_WORD Timing

As shown in Figure 92, hardware TX_SYNC is latched at the next negative edge of the ADC Clock after 0 to 1 transition of TX_SYNC. The time gap between latched edge and the start of the LVDS SYNC_WORD is kT ns where T is the time period of ADC clock and k = 16 + decFactor + 1. t_{SETUP} and t_{HOLD} can be considered as 1.5 ns in the normal condition. Both are at the negative edge of the ADC clock.

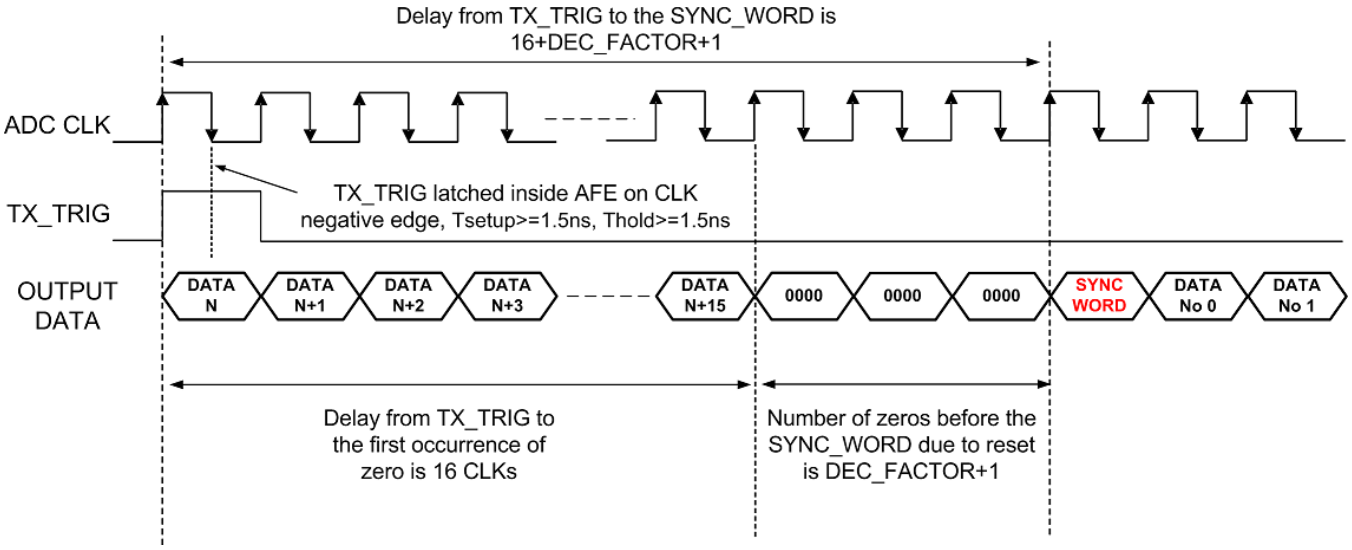


Figure 92. Sync Word Generation With Respect to TX_TRIG when DC_REMOVAL_BYPASS 10[0] = 0

10.6.2.2.6 FIR Filter Delay versus TX_TRIG Timing

AFE5812's decimation filter is a symmetric M×16-order FIR filter, where M is the decimation factor from 1 to 32. Half of the M×16 coefficients are stored in the filter coefficient memory.

For a discrete-time FIR filter, its output is a weighted sum of the current and a finite number of previous values of the input as Equation 7 shows.

$$Y[n] = C0 \times X[n] + C1 \times X[n-1] ... + C_N \times X[n-N] \quad (7)$$

where

- X[n] is the input signal.
- Y[n] is the output signal.
- CN is the filter coefficients.
- N is the filter order.

Therefore, the delay of AFE5812 output is related to decimation factor, M. The TX_TRIG timing also plays a role in this. In the following description, M = 1 and M = 2 are used as examples to derive a generic timing relationship among TX_TRIG, AFE input, and AFE output.

The following register settings were used when the delay relationship was measured:

Table 24. Settings for evaluating FIR Filter Delay versus TX_TRIG Timing

Register Setting	Register Setting (HEX)	Description
22[0] = 0	0x16[0] = 0	Enable demodulator. 0x16 belongs to ADC register
Profile RAM	Profile RAM	Set different decimation factor and other settings in profile RAM.
Coeff RAM	Coeff RAM	Write filter coefficients in coefficient memory.
29[7] = 1	0x1D[7] = 1	Set DEC_SHIFT_FORCE_EN
10[13] = 1	0xA[13] = 1	Set DEC_SHIFT_SCALE
29[6:4] = 6	0x1D[6:4] = 6	Set DEC_SHIFT_FORCE
10[15] = 0, 10[12] = 1, 10[4] = 1, 10[1] = 1;	0xA[15] = 0, 0xA[12] = 1, 0xA[4] = 1, 0xA[1] = 1	RESERVED bits
10[0] = 1	0x0A[0] = 1	Set DC_REMOVAL_BYPASS
10[10] = 1	0x0A[10] = 1	Reset down conversion phase on TX_TRIG
03[14:13] = 11	03[14:13] = 11	SERZ_FACTOR 16X
03[11:9] = 100	03[11:9] = 100	OUTPUT_RESOLUTION 16X
04[4] = 1	04[4] = 1	MSB_FIRST
11[15:0]	0xB[15:0]	Set custom SYNC_WORD value if needed
10[2]=0	0x0A[2]=0	Down conversion is enabled.
Profile RAM[21:6]=0	Profile RAM[21:6]=0	Down convert frequency set to 0, that is, multiply input signal with DC.
Note: Even if this frequency is set to a non-zero value, it will not change the demod latency. For experiment ease, mixing with DC is performed. ADC sampling frequency and VCA LPF settings were kept such that the AFE5812's demod sees a single pulse.		

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When M = 1, 8 filter coefficients written in the memory are C0, C1 to C7. An impulse signal is applied at both VCA input and TX_TRIG. Due to the impulse input, coefficients start coming at the output according to timing diagram shown in Figure 93, where 20-cycle delay is observed.

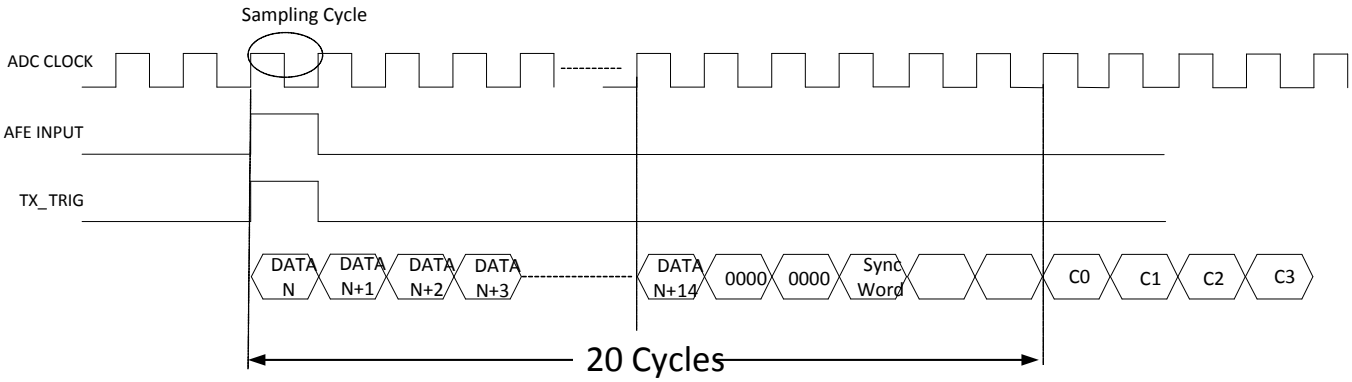


Figure 93. Expected Latency Timing When M = 1

By adjusting the timing between AFE input and TX_TRIG, the user can obtain a timing diagram similar to Figure 93.

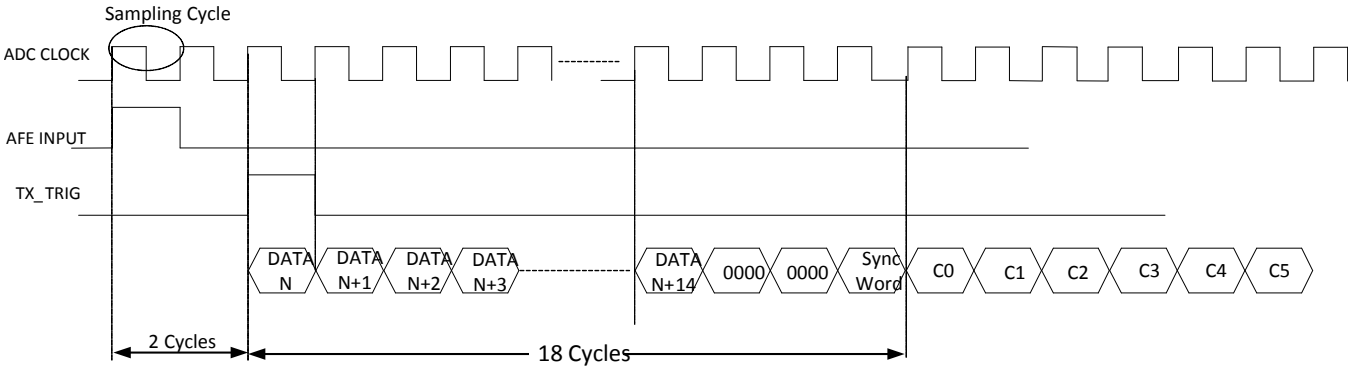


Figure 94. Measured Latency Timing When M = 1

By adjusting the timing between AFE input and TX_TRIG, the user can obtain a timing diagram similar to Figure 94.

When M = 2, if the impulse is given one clock before TX_TRIG signal, then the sample followed after the sync word gives impulse response of the filter as shown in Figure 95.

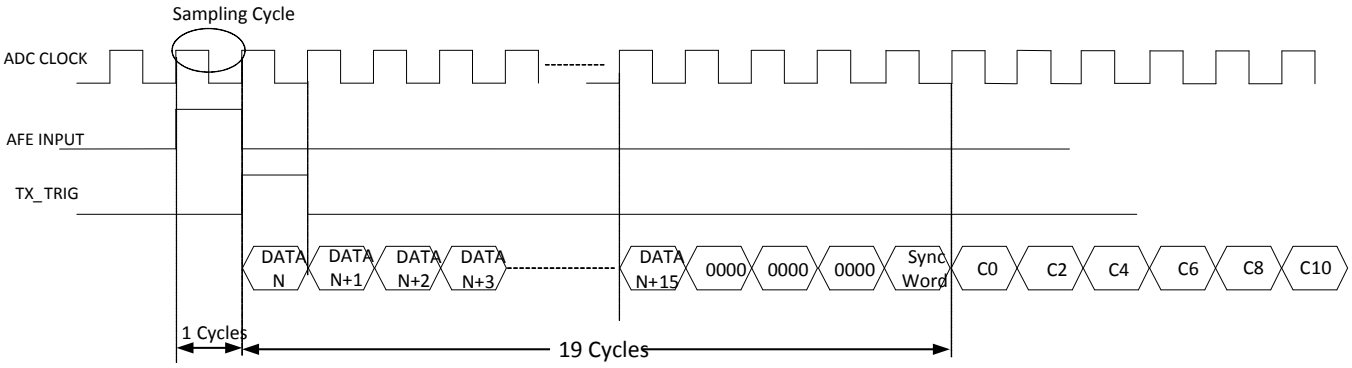


Figure 95. Measured Latency Timing When M = 2

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Figure 96 shows a generic timing diagram. The number of zeros comes before the sync word is equal to Z. The sync word comes after S number of cycles, impulse response starts coming after L number of cycles, and input impulse is given after IP cycles with respect to TX_TRIG signal. Therefore, for different decimation factor (M), values of these numbers are listed in Table 25 and Figure 96.

Table 25. Generic Latency versus Decimation Factor M(1)(2)

M	Number of Zeros (ZNo)	Sync Word Latency (S)	Data Latency (L)	Input Impulse (IP)(3)
1	2	17	18	–2
2	3	18	19	–1
3	4	19	20	0
4	5	20	21	1
5	6	21	22	2
6	7	22	23	3
7	8	23	24	4
8	9	24	25	5
M	M + 1	16 + M	17 + M	M – 3

(1) When DC_REMOVAL_BYPASS 10[0] = 0 or 0xA[0] = 0, the sync word latency and data latency becomes 17 + M and 18 + M
(2) ADC's low latency mode enabled by register 0x2[12] does not impact S and L.
(3) Negative number represents input is given in advance with respect to TX_TRIG signal.

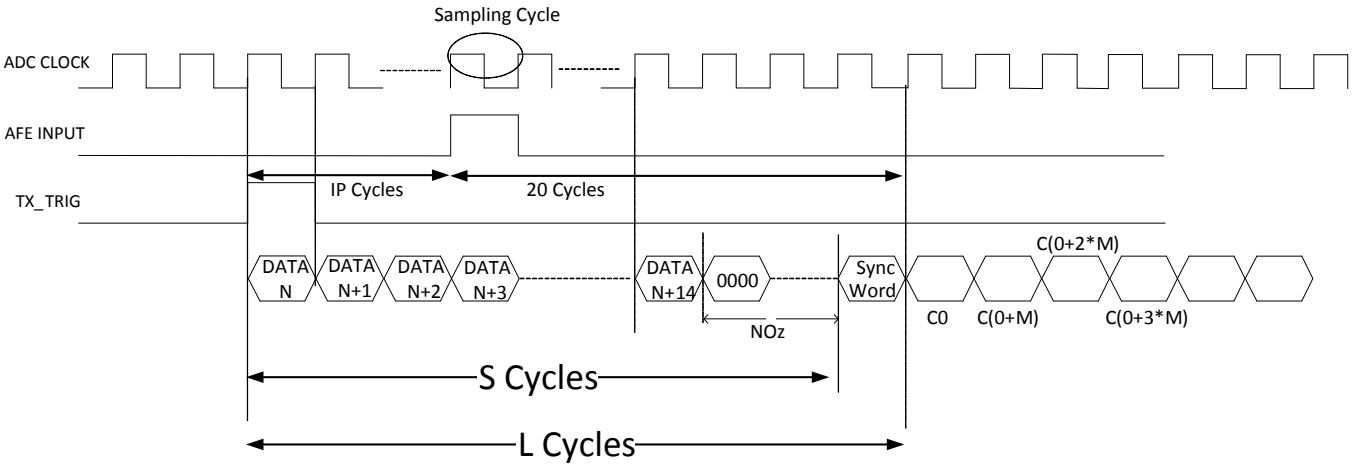


Figure 96. Measured Latency Timing at Any M

10.6.2.2.6.0.1 Expression of Decimation Filter Response

Based on Table 25, the decimation filter's response is formulated. Figure 97 indicates that the Tx_Trig sample is considered as the reference for time scale. So, the input to the device at Tx_Trig clock will be expressed as X[0], the next sample input as X[1], and so on. Similarly, the output of the device followed by the AFE5812's demodulator will be expressed as Y[0] at the instant of Tx_Trig, Y[1] at the next clock, and so on; Cn or C(n) indicates the coefficient of n^{th} index.

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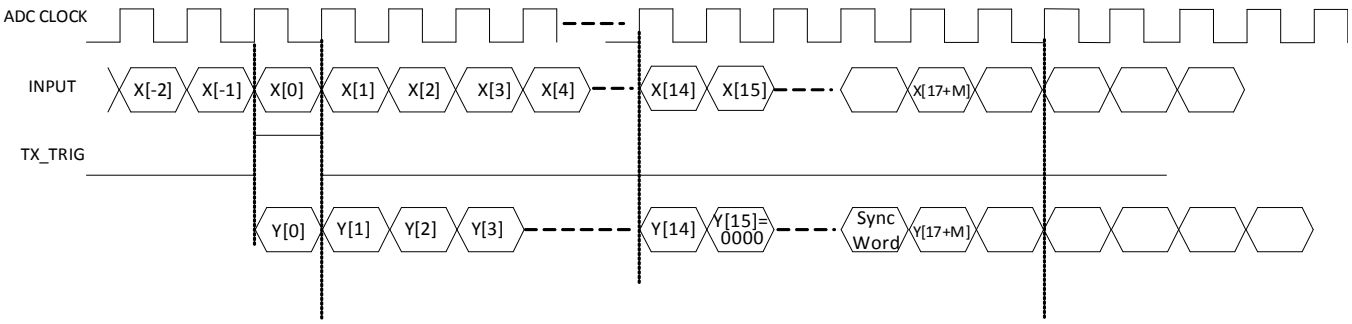


Figure 97. Typical Timing Expression Among ADC CLK, Input, TX_TRIG, and Output

For M = 1, the number of zeros, ZNo = 2; Sync word latency S = 17. So, the output values from sample 18 are relevant and the first few samples are:

- Y[18] = C0×X[-2]+C1×X[-3]+C2×X[-4]+…+C7×X[-9]+C7×X[-10]+…+C[0]×X[-17]
- Y[19] = C0×X[-1]+C1×X[-2]+C2×X[-3]+…+C7×X[-8]+C7×X[-9]+…+C[0]×X[-16]
- Y[20] = C0×X[0]+C1×X[-1]+C2×X[-2]+…+C7×X[-7]+C7×X[-8]+…+C[0]×X[-15]

All these samples appear at the output because no samples are dropped for decimation factor = 1.

For M = 2, the number of zeros, ZNo = 3; Sync word latency S = 18. So, the output values from sample 19 are relevant and the first few samples are described as:

- Y[19] = C0×X[-1]+C1×X[-2]+C2×X[-3]+…+C15×X[-16]+C15×X[-17]+…+C[0]×X[-32]
- Y[20] = C0×X[0]+C1×X[-1]+C2×X[-2]+…+C15×X[-15]+C15×X[-16]+…+C[0]×X[-31]
- Y[21] = C0×X[1]+C1×X[0]+C2×X[-1]+…+C15×X[-14]+C15×X[-15]+…+C[0]×X[-30]

But for M = 2, every alternate sample must be dropped. The decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case, Y[19], Y[21], Y[23], and so forth are retained and Y[20], Y[22], Y[24], and so forth are dropped.

For M = 3, the number of zeros, ZNo = 4; Sync word latency S = 19. So, the output values from sample 20 are relevant and the first few samples are described as:

- Y[20] = C0×X[0]+C1×X[-1]+C2×X[-2]+…+C23×X[-23]+C23×X[-24]+…+C[0]×X[-47]
- Y[21] = C0×X[1]+C1×X[0]+C2×X[-1]+…+C23×X[-22]+C23×X[-23]+…+C[0]×X[-46]
- Y[22] = C0×X[2]+C1×X[1]+C2×X[0]+…+C23×X[-21]+C23×X[-22]+…+C[0]×X[-45]
- Y[23] = C0×X[3]+C1×X[2]+C2×X[1]+…+C23×X[-20]+C23×X[-21]+…+C[0]×X[-44]

But for M = 3, the last two of every three samples must be dropped. The decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case, Y[20], Y[23], Y[26], and so forth are retained and Y[21], Y[22], Y[24], Y[25], and so forth are dropped.

For any M, this pattern can be generalized for a decimation factor of M. The number of ZNo = M + 1, Sync word latency S = 16 + M. So, the output values from sample (17 + M) are relevant and the first few samples are described as:

- Y[17+M] = C0×X[M-3]+C1×X[M-4]+C2×X[M-5]+…+C(8M-1)×X[-7M-2]+C(8M-1)×X[-7M-3]+ … +C[0]×X[-15M-2]
- Y[18+M] = C0×X[M-2]+C1×X[M-3]+C2×X[M-4]+…+C(8M-1)×X[-7M-1]+C(8M-1)×X[-7M-2]+ … +C[0]×X[-15M-1]

For a decimation factor of M which is not 1, the decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case, Y[17 + M], Y[17 + 2M], Y[17 + 3M], and so forth are retained and the rest of samples between these, that is, Y[18 + M], Y[19 + 2M],…, Y[16 + 2M] are dropped.

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

Figure 98 lists a typical application circuit diagram. The configuration for each block is discussed in the following sections. Table 26 lists companion TI devices that are used to complete the analog signal chain in a system.

Table 26. Application Companion Devices

Part Number	Part Description	Functions
THS4130,SLOS318	Fully Differential Input/Output Low Noise Amplifier With Shutdown	TGC Vcntl Opamp, CW summing amplifier and active filter
OPA1632, SBOS286	Fully Differential I/O Audio Amplifier	TGC Vcntl amplifier, CW summing amplifier and active filter
OPA2211A, SBOS377	1.1nV/rtHz Noise, Low Power, Precision Operational Amplifier	CW summing amplifier and active filter
LME49990, SNOSB16	Ultra-low Distortion, Ultra-low Noise Operational Amplifier	CW summing amplifier and active filter
LMH6629, SNOSB18	Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown	CW summing amplifier and active filter
ADS8413,SLAS490	16-bit, Unipolar Diff Input, 2MSPS Sampling rate, 4.75V to 5.25V ADC with LVDS Serial Interface	CW Audio ADC
ADS8881, SBAS547	18-Bit, 1-MSPS, Serial Interface, microPower, Truly-Differential Input, SAR ADC	CW Audio ADC
DAC7811, SBAS337	12-Bit, Serial Input, Multiplying Digital to Analog Converter	TGC Vcntl Digital to Analog Converter
LMK04803, SNAS489	Low Noise Clock Jitter Cleaner With Dual Cascaded PLLs and Integrated 1.9 GHz VCO	Jitter cleaner and clock synthesizer
CDCM7005,SCAS793	High Performance, Low Phase Noise, Low Skew Clock Synchronizer	Jitter cleaner and clock synthesizer
CDCE72010,SLAS490	10 Outputs Low Jitter Clock Synchronizer and Jitter Cleaner	Jitter cleaner and clock synthesizer
CDCLVP1208, SCAS890	Low Jitter, 2-Input Selectable 1:8 Universal-to-LVPECL Buffer	Clock buffer
LMK00308, SNAS576	3.1-GHz Differential Clock Buffer/Level Translator	Clock buffer
LMK01000, SNAS437	1.6 GHz High Performance Clock Buffer, Divider, and Distributor	Clock buffer
SN74AUP1T04,SCES800	Low Power, 1.8/2.5/3.3-V Input, 3.3-V CMOS Output, Single Inverter Gate	1.8V/2.5V/3.3V Level shifter for SPI
UCC28250 SLUSA29	Advanced PWM Controller with Pre-Bias Operation	Synchronized DC-DC power supply controller

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11.2 Typical Application

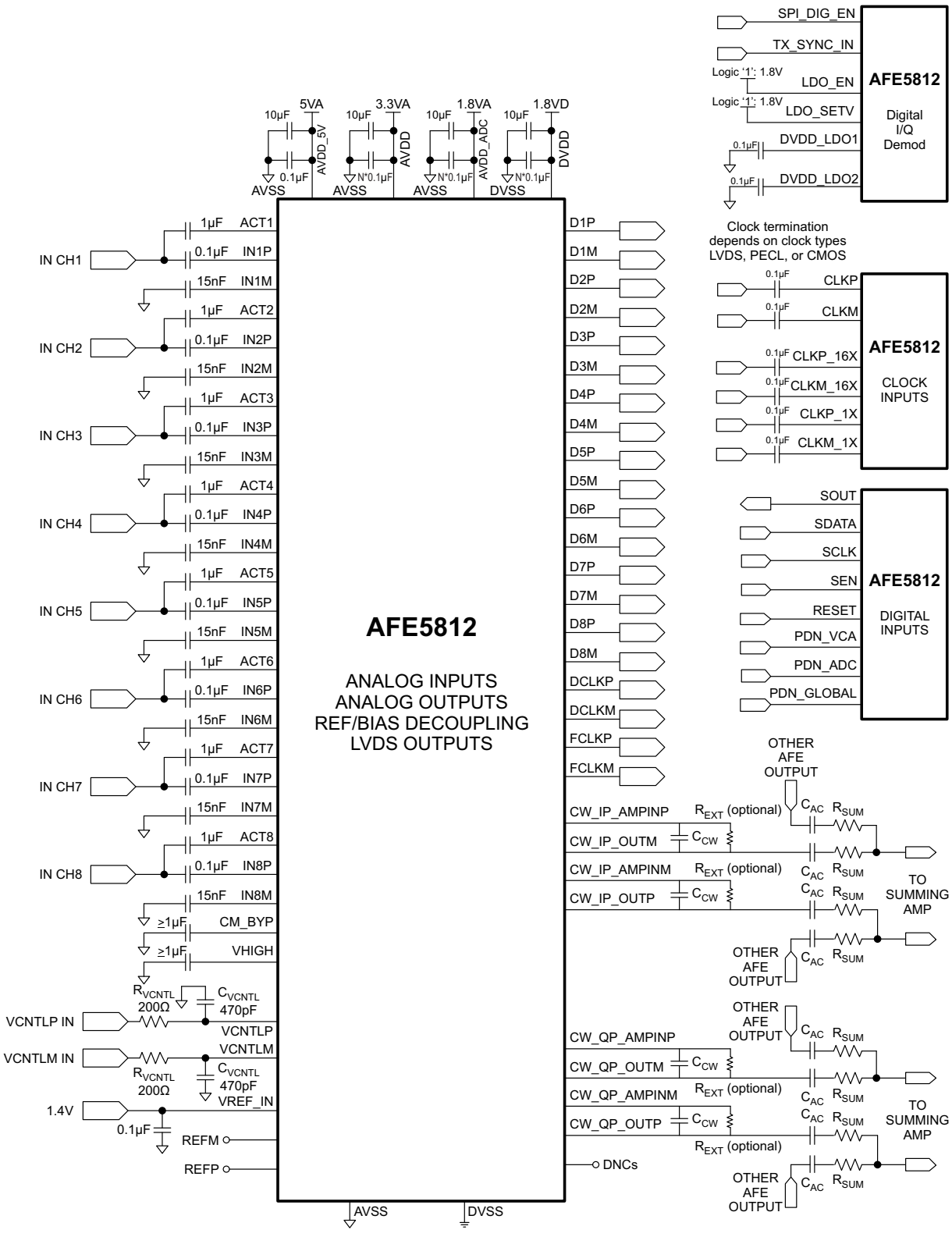


Figure 98. Application Circuit with Internally Generated 1.4V Demod Supply

Typical Application (continued)

11.2.1 Design Requirement

The AFE5812 is a highly integrated analog front-end solution. In order to maximize its performance, users must carefully optimize its surrounding circuits, such as T/R switch, Vcntl circuits, audio ADCs for CW path, clock distribution network, synchronized power supplies and digital processors. Some common practices are described below.

Typical requirements for a traditional medical ultrasound imaging system are shown in Table 27.

Table 27. Design Parameters

PARAMETER	EXAMPLE VALUES
Signal center frequency (f_0)	1~20 MHz
Signal Bandwidth (BW)	10~100% of f_0
Overloaded signals due to T/R switch leakage	~2 Vpp
Maximum input signal amplitude	100 mVpp to 1 Vpp
Transducer noise level	1 nV/rtHz
Dynamic range	151 dBc/Hz
Time gain compensation range	40 dB
Total harmonic distortion	40 dBc @ 5MHz

11.2.2 Detailed Design Procedure

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. The concept of focal imaging provides the ability to focus on a single point in the scan region. By subsequently focusing at different points, an image is assembled.

When initiating an imaging, a pulse is generated and transmitted from each of the 64 transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1MHz to 15 MHz. The sound waves are attenuated as they travel through the objects being imaged, and the attenuation coefficients α are about 0.54 dB/(MHz×cm) in soft tissue and 6~10 dB/(MHz×cm) in bone (source: http://en.wikipedia.org/wiki/Attenuation). Most medical ultrasound systems use the reflection imaging mode and the total signal attenuation is calculated by $2\times depth\times\alpha\times f_0$. As the signal travels, portions of the wave front energy are reflected. Signals that are reflected immediately after transmission are very strong because they are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because they are reflecting from deep in the body. As a result of the limitations on the amount of energy that can be put into the imaging object, the industry developed extremely sensitive receive electronics with wide dynamic range.

Receive echoes from focal points close to the surface require little, if any, amplification. This region is referred to as the near field. However, receive echoes from focal points deep in the body are extremely weak and must be amplified by a factor of 100 or more. This region is referred to as the far field. In the high-gain (far field) mode, the limit of performance is the sum of all noise sources in the receive chain. In high-gain (far field) mode, system performance is defined by its overall noise level, which is limited by the noise level of the transducer assembly and the receive low-noise amplifier (LNA). However in the low-gain (near field) mode, system performance is defined by the maximum amplitude of the input signal that the system can handle. The ratio between noise levels in high-gain mode and the signal amplitude level in low-gain mode is defined as the dynamic range of the system. The high integration and high dynamic range of the device make it ideally suited for ultrasound imaging applications.

The device includes an integrated LNA and VCAT (which use the gain that can be changed with enough time to handle both near- and far-field systems), a low-pass antialiasing filter to limit the noise bandwidth, an ADC with high SNR performance, and a CW mixer. Figure 98 illustrates an application circuit of the device.

Use the following steps to design medical ultrasound imaging systems:

1. Use the signal center frequency and signal bandwidth to select an appropriate ADC sampling frequency.

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2. Use the time gain compensation range to select the range of the VCNTL signal.

3. Use the transducer noise level and maximum input signal amplitude to select the appropriate LNA gain. The device input-referred noise level reduces with higher LNA gain. However, higher LNA gain leads to lower input signal swing support.

4. Select different passive components for different device pins as shown in Figure 98.

5. Select the appropriate input termination configuration as discussed in Active Termination.

6. Select the clock configuration for the ADC and CW clocks as discussed in CW Clock Selection and ADC Clock Configurations.

11.2.2.1 LNA Configuration

11.2.2.1.1 LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.2 V and AC coupling is required. Figure 99 shows a typical input configuration. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. The recommended values for C_{ACT} is ≥1 µF and C_{IN} is ≥0.1 µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (for example: the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

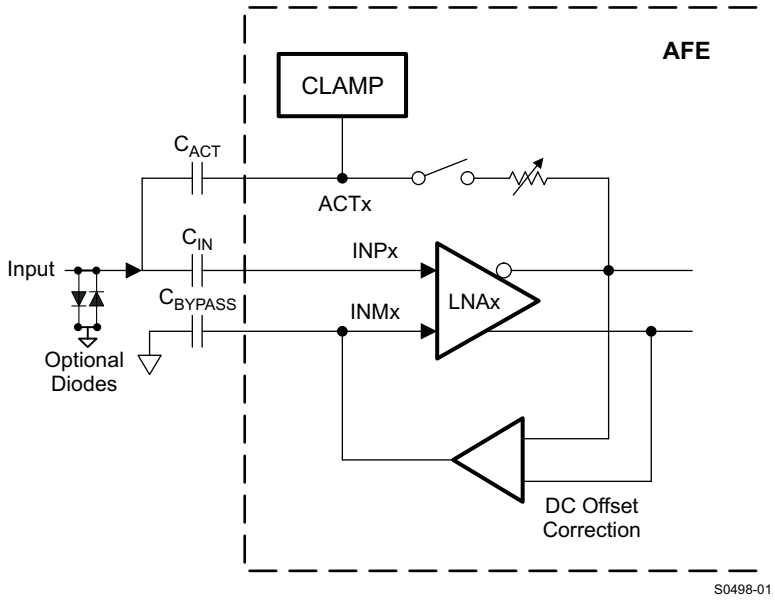


Figure 99. LNA Input Configurations

This architecture minimizes any loading of the signal source that may lead to a frequency-dependent voltage divider. The closed-loop design yields low offsets and offset drift. C_{BYPASS} (≥0.015 µF) is used to set the HPF cut-off frequency and decouple the complementary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value. The HPF cut-off frequency can be adjusted through the register 59[3:2] Table 28 lists. Low-frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal-processing unit includes digital HPFs or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. In addition, a digital HPF is also available in the AFE5812 ADC or digital demodulator. If low-frequency signal detection is desired in some applications, the LNA HPF can be disabled.

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Table 28. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	Frequency (kHz)
00	100
01	50
10	200
11	150

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥1-µF capacitors. Bigger bypassing capacitors (>2.2 µF) may be beneficial if low-frequency noise exists in the system.

11.2.2.1.2 LNA Noise Contribution

The noise specification is critical for LNA and it determines the dynamic range of the entire system. The LNA of the AFE5812 achieves low power and an exceptionally low-noise voltage of 0.63~0.9 nV/√Hz, and a low current noise of 2~2.7 pA/√Hz.

Typical ultrasonic transducer's impedance, R_S, varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (R_S) generates additional voltage noise.

$$LNA_Noise_{total} = \sqrt{V_{LNAnoise}^2 + R_s^2 \times I_{LNAnoise}^2} \quad (8)$$

The AFE5812 achieves low-noise figure (NF) over a wide range of source resistances as shown in Figure 32, Figure 33, and Figure 34.

11.2.2.1.3 Active Termination

In ultrasound applications, signal reflection exists due to long cables between the transducer and system. The reflection results in extra ringing added to echo signals in PW mode. Because the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Therefore, either passive termination or active termination is preferred if good axial resolution is desired. Figure 100 shows three termination configurations.

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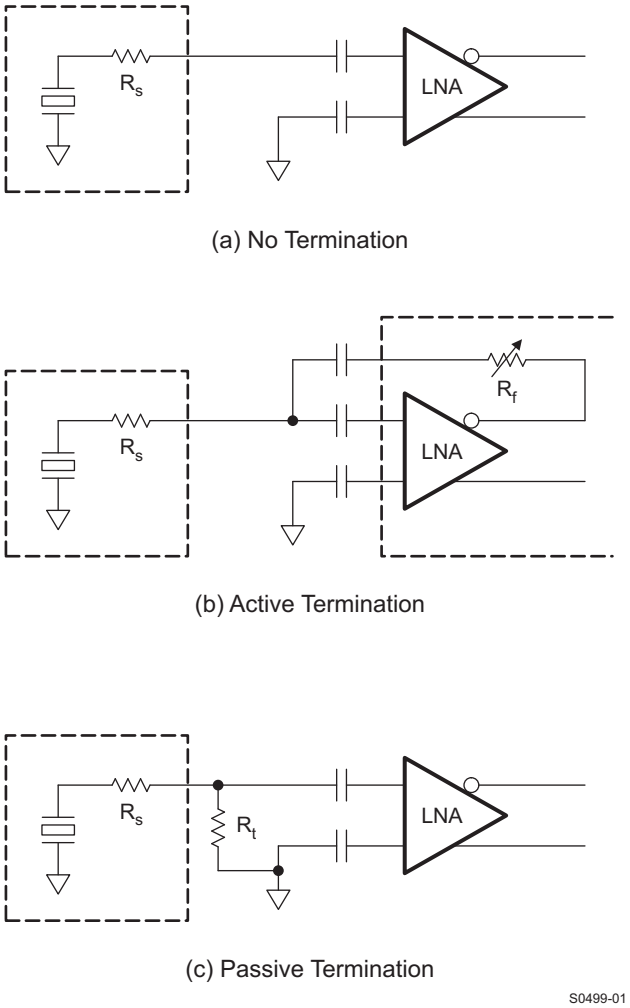


Figure 100. Termination Configurations

Under the no termination configuration, the input impedance of the AFE5812 is about 6 kΩ (8 K//20 pF) at 1 MHz. Passive termination requires external termination resistor R_t, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 101 .

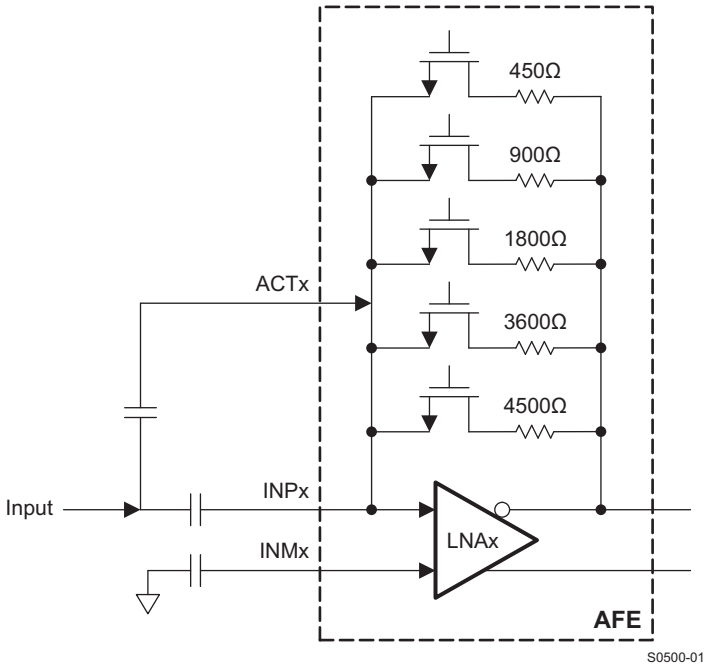


Figure 101. Active Termination Implementation

The AFE5812 has four pre-settings 50, 100, 200, and 400 Ω, which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 101. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \quad (9)$$

Table 6 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 10 where R_{IN} (8 kΩ) and C_{IN} (20 pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \,//\, C_{IN} \,//\, R_{IN} \quad (10)$$

Therefore, the Z_{IN} is frequency dependent, and it decreases as frequency increases as shown in Figure 10. Because 2 to 10 MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect does not impact system performance greatly. Active termination can be applied to both CW and TGC modes. Because each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 32, Figure 33, and Figure 34 show the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus, termination topology should be carefully selected based on each use scenario in ultrasound.

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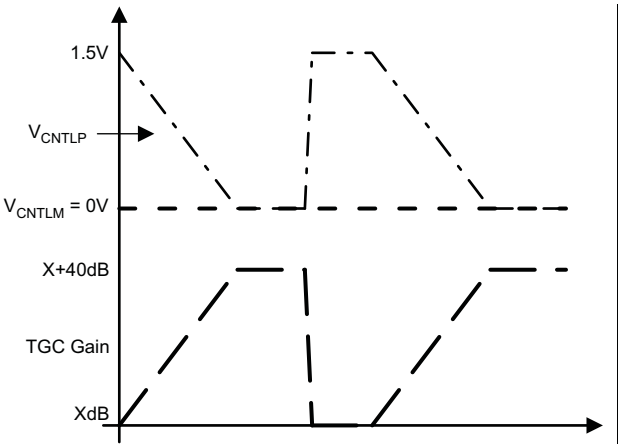
11.2.2.1.4 LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. In addition, the signal chain needs about 14 µs to settle after the LNA gain change. Thus, LNA gain switching may not be preferred when switching time or settling time for the signal chain is limited.

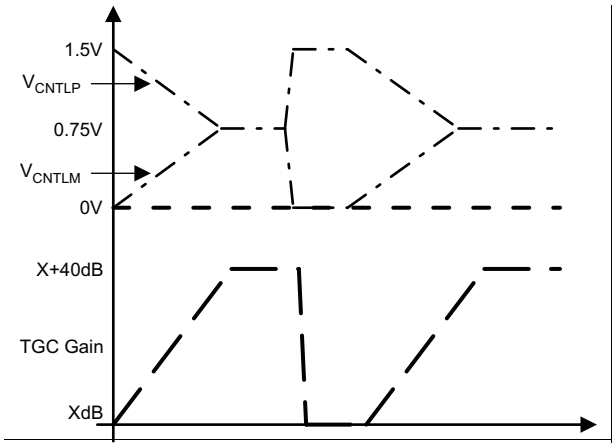
11.2.2.2 Voltage-Controlled Attenuator

The attenuator in the AFE5812 is controlled by a pair of differential control inputs, the $V_{CNTLM,P}$ pins. The differential control voltage spans from 0 to 1.5 V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. Its maximum attenuation (minimum channel gain) appears at $V_{CNTLP} - V_{CNTLM}$ = 1.5 V and minimum attenuation (maximum channel gain) occurs at $V_{CNTLP} - V_{CNTLM}$ = 0. The typical gain range is 40 dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5-Vpp signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground; As Figure 102 show, the TGC gain curve is inversely proportional to the $V_{CNTLP} - V_{CNTLM}$.



(a) Single-Ended Input at V_{CNTLP}



(b) Differential Inputs at V_{CNTLP} and V_{CNTLM}

W0004-01

Figure 102. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5 dB.

The control voltage input ($V_{CNTLM,P}$ pins) represents a high-impedance input. The $V_{CNTLM,P}$ pins of multiple AFE5812 devices can be connected in parallel with no significant loading effects. When the voltage level ($V_{CNTLP} - V_{CNTLM}$) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level, respectively. TI recommends to limit the voltage from –0.3 to 2 V.

When the AFE5812 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, TI recommends to power down the VCA using the PDN_VCA register bit. In this case, $V_{CNTLP} - V_{CNTLM}$ voltage does not matter.

The AFE5812 gain-control input has a –3-dB bandwidth of approximately 800 kHz. This wide bandwidth, although useful in many applications (for example, fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM,P}$ pins as Figure 81 shows. However, the external filter's cutoff frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of 1 VPP (–6-dBFS) output as indicated in Figure 51 and Figure 52.

Typical $V_{CNTLM,P}$ signals are generated by an 8- to 12-bit 10-MSPS digital-to-analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10 MSPS/12 bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (that is, THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low-frequency noise. The $V_{CNTLM/P}$ circuit achieves low noise to prevent the $V_{CNTLM/P}$ noise being modulated to RF signals. TI recommends that $V_{CNTLM/P}$ noise for one AFE is below 25 nV/rtHz at 1 kHz and 5 nV/rtHz at 50 kHz. In high-channel count premium systems, the $V_{CNTLM/P}$ noise requirement is higher as shown below.

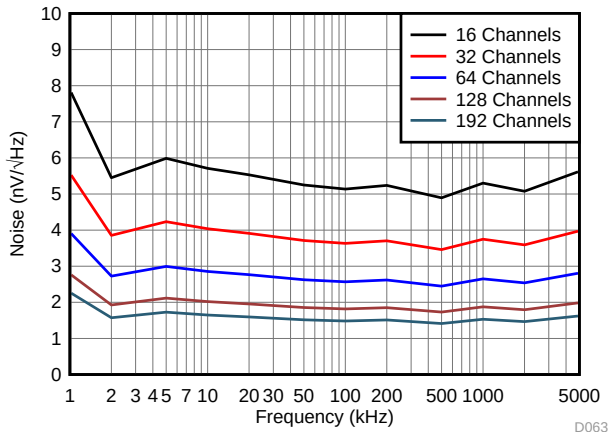


Figure 103. Allowed Noise on the VCNTL Signal Across Frequency and Different Channels

More information can be found in the literatures SLOS318 and SBAA150. See Figure 2 for the V_{CNTL} vs Gain curves. Table 29 also shows the absolute gain vs V_{CNTL}, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. DTGC feature is implemented to address this need in the AFE5812. In the DTGC mode, no external V_{CNTL} is needed. Refer to Figure 64.

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Table 29. V_{CNTLP} – V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low-Noise Mode)

V_{CNTLP} – V_{CNTLM} (V)	Gain (dB) LNA = 15 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 15 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	39.45	42.45	48.45	45.25	48.25	54.25
0.1	36.91	39.91	45.91	42.71	45.71	51.71
0.2	33.78	36.78	42.78	39.58	42.58	48.58
0.3	30.39	33.39	39.39	36.19	39.19	45.19
0.4	26.74	29.74	35.74	32.54	35.54	41.54
0.5	23.69	26.69	32.69	29.49	32.49	38.49
0.6	20.11	23.11	29.11	25.91	28.91	34.91
0.7	16.54	19.54	25.54	22.34	25.34	31.34
0.8	13.27	16.27	22.27	19.07	22.07	28.07
0.9	9.48	12.48	18.48	15.28	18.28	24.28
1.0	6.16	9.16	15.16	11.96	14.96	20.96
1.1	2.65	5.65	11.65	8.45	11.45	17.45
1.2	0.52	3.52	9.52	6.32	9.32	15.32
1.3	–0.58	2.42	8.42	5.22	8.22	14.22
1.4	–1.01	1.99	7.99	4.79	7.79	13.79
1.5	–1	2	8	4.8	7.8	13.8

11.2.2.3 CW Operation

11.2.2.3.1 CW Summing Amplifier

To simplify CW system design, a summing amplifier is implemented in the AFE5812 to sum and convert 8-channel mixer current outputs to a differential voltage output. Low noise and low power are achieved in the summing amplifier while maintaining the full dynamic range required in CW operation.

This summing amplifier has five internal gain adjustment resistors which can provide 32 different gain settings (register 54[4:0], Figure 101 and Table 9). System designers can easily adjust the CW path gain depending on signal strength and transducer sensitivity. For any other gain values, an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 500-Ω resistors after LNA and the internal or external resistor network $R_{EXT/INT}$. Thus, the matching between these resistors plays a more important role than absolute resistor values. Better than 1% matching is achieved on chip. Due to process variation, the absolute resistor tolerance could be higher. If external resistors are used, the gain error between I/Q channels or among multiple AFEs may increase. TI recommends to use internal resistors and low tolerance capacitor $C_{EXT}$to set the gain in order to achieve better gain matching (across channels and multiple AFEs). This summing amplifier has first-order LPF response to remove high-frequency components from the mixers, such as 2f0±fd. Its cut-off frequency is determined by:

$$f_{HP} = \frac{1}{2\pi R_{INT/EXT} C_{EXT}} \quad (11)$$

Note that when different gain is configured through Register 54[4:0], the LPF response varies as well.

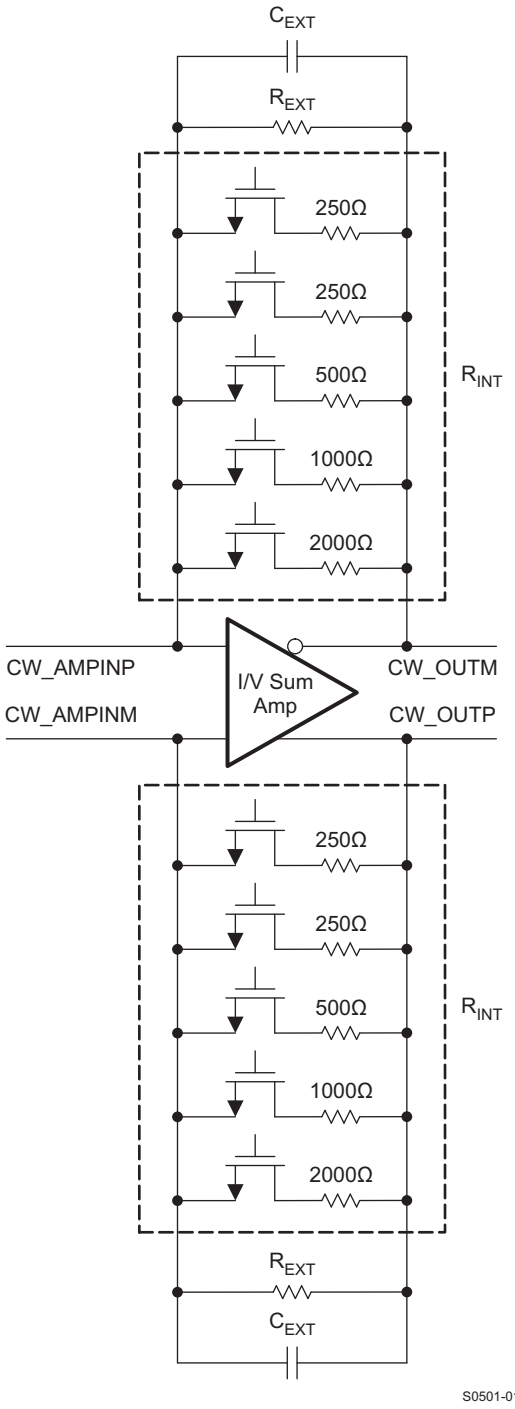


Figure 104. CW Summing Amplifier Block Diagram

Multiple AFE5812s are usually used in parallel to expand CW beamformer channel count. The AFE5812 CW's voltage outputs can be summed and filtered externally further to achieve desired gain and filter response. AC-coupling capacitors C_{AC} are required to block the DC component of the CW carrier signal. C_{AC} can vary from 1 to 10 µF depending on the desired low-frequency Doppler signal from slow blood flow. Multiple AFE5812s' I/Q outputs can be summed together with a low-noisel differential amplifiers before 16, 18-bit differential audio ADCs. The TI ultra-low noise differential precision amplifier OPA1632 and THS4130 are suitable devices.

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Figure 106 shows an alternative current summing circuit. However, this circuit only achieves good performance when a lower-noise operational amplifier is available compared to the AFE5812's internal summing differential amplifier.

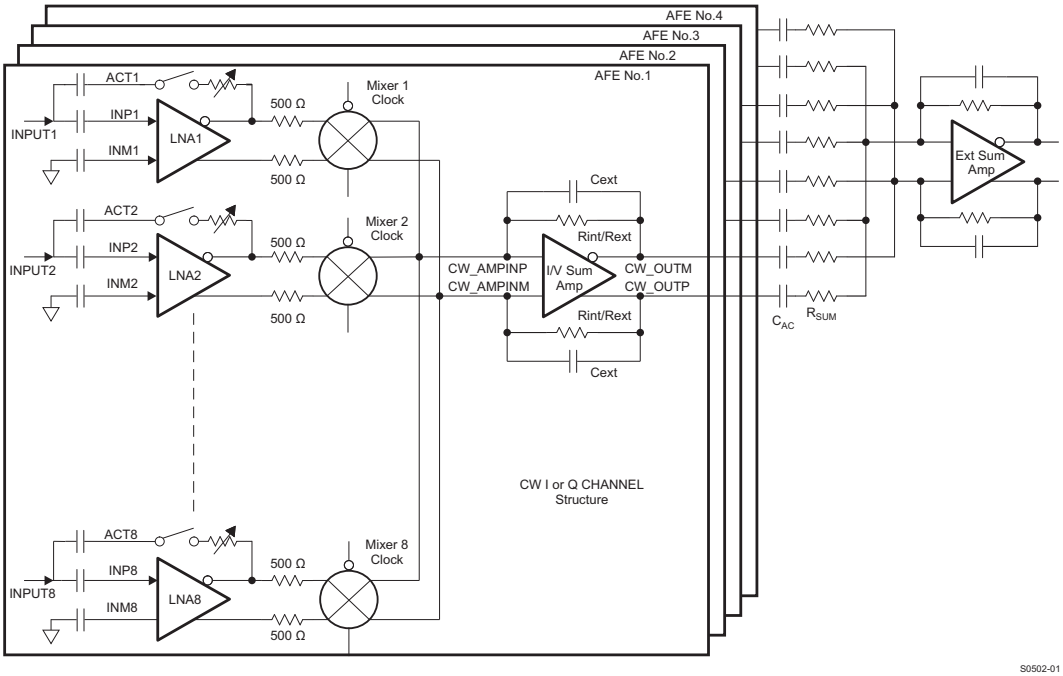


Figure 105. CW Circuit With Multiple AFE5812s (Voltage Output Mode)

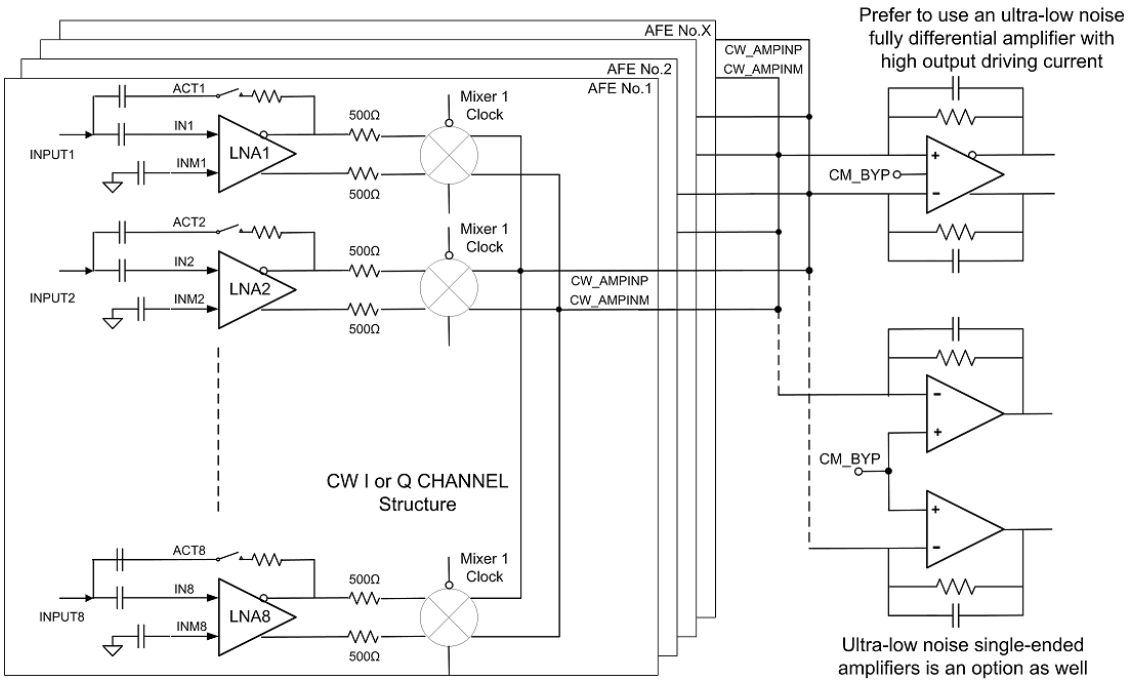


Figure 106. CW Circuit With Multiple AFE5812s (Current Output Mode, CM_BYP=1.5V)

The CW I/Q channels are well matched internally to suppress image frequency components in the Doppler spectrum. Low-tolerance components(R and C) and precise operational amplifiers should be used for achieving good matching in the external circuits as well.

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NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH, respectively. Depending on the users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed to get correct blood flow directions.

11.2.2.3.2 CW Clock Selection

The AFE5812 can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended CMOS clock. An internally generated VCM of 2.5 V is applied to CW clock inputs, that is, CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X. Because this 2.5-V VCM is different from the one used in standard LVDS or LVPECL clocks, AC coupling is required between clock drivers and the AFE5812 CW clock inputs. When the CMOS clock is used, CLKM_1X and CLKM_16X should be tied to ground. Figure 107 shows common clock configurations. TI recommends appropriate termination to achieve good signal integrity.

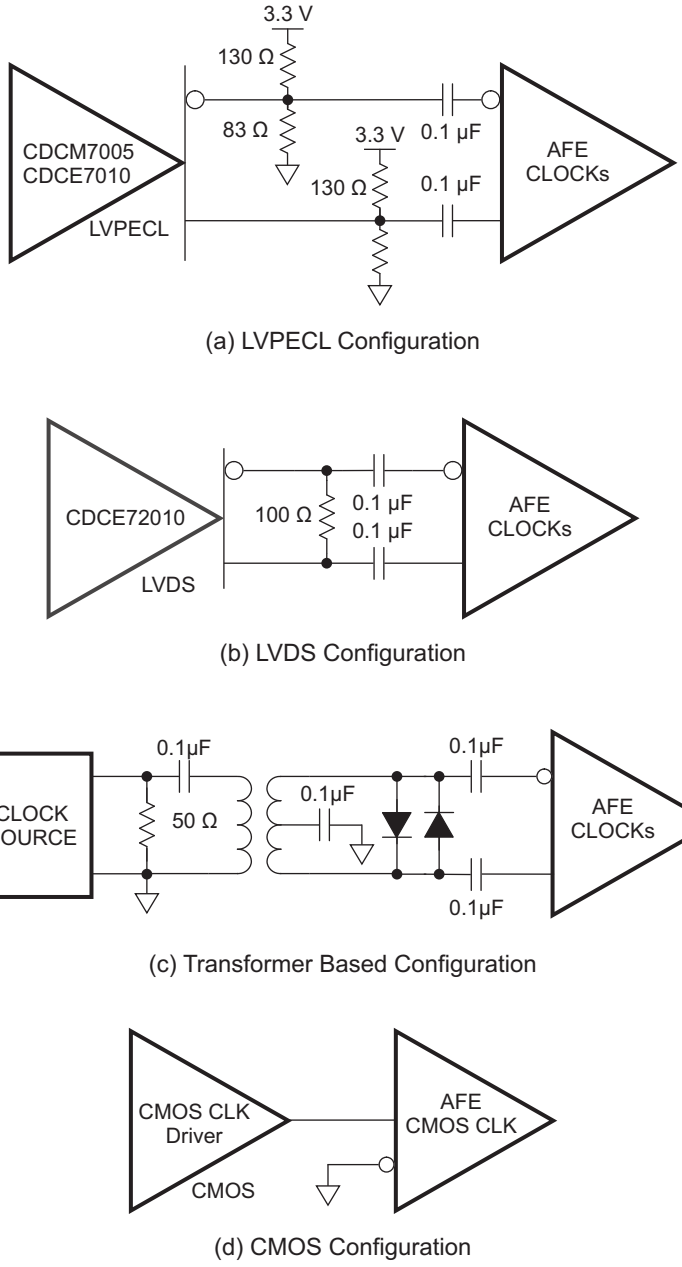


Figure 107. Clock Configurations

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The combination of the clock noise and the CW path noise can degrade the CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the AFE5812 CW path is better than 155 dBc/Hz at 1-kHz offset. Consequently, the phase noise of the mixer clock inputs needs to be much better than 155 dBc/Hz.

In the 16/8/4 × f_{cw} operations modes, low phase noise clock is required for 16, 8, 4 × f_{cw} clocks (that is, CLKP_16X/ CLKM_16X pins) to maintain good CW phase noise performance. The 1 × f_{cw} clock (that is, CLKP_1X/ CLKM_1X pins) is only used to synchronize the multiple AFE5812 chips and is not used for demodulation. Thus, 1 × f_{cw} clock's phase noise is not a concern. However, in the 1 × f_{cw} operation mode, low-phase noise clocks are required for both CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X pins because both of them are used for mixer demodulation. In general, a higher slew rate clock has lower phase noise; thus, clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, a 5-V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider's phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of 20logN dB where N is the dividing factor of 16, 8, or 4. If the target phase noise of mixer LO clock 1 × f_{cw} is 160 dBc/Hz at 1 kHz off carrier, the 16 × f_{cw} clock phase noise should be better than 160 – 20log16 = 136 dBc/Hz. TI's jitter cleaners LMK048X/CDCM7005/CDCE72010 exceed this requirement and can be selected for the AFE5812. In the 4×/1× modes, higher-quality input clocks are expected to achieve the same performance because N is smaller. Thus, the 16× mode is a preferred mode because it reduces the phase noise requirement for system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit. Note in the 16× operation mode, the CW operation range is limited to 8 MHz due to the 16× CLK. The maximum clock frequency for the 16× CLK is 128 MHz. In the 8×, 4×, and 1× modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, for example, the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz.

As the channel number in a system increases, clock distribution becomes more complex. It is not preferred to use one clock driver output to drive multiple AFEs because the clock buffer's load capacitance increases by a factor of N. As a result, the falling and rising time of a clock signal is degraded. A typical clock arrangement for multiple AFE5812s is shown in Figure 108. Each clock buffer output drives one AFE5812 in order to achieve the best signal integrity and fastest slew rate, that is, better phase noise performance. When clock phase noise is not a concern, for example, the 1 × f_{cw} clock in the 16, 8, 4 × f_{cw} operation modes, one clock driver output may excite more than one AFE5812. Nevertheless, special considerations should be applied in such a clock distribution network design. In typical ultrasound systems, it is required that all clocks are generated from a same clock source, such as 16 × f_{cw} , 1 × f_{cw} clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock, and so on. By doing this, interference due to clock asynchronization can be minimized.

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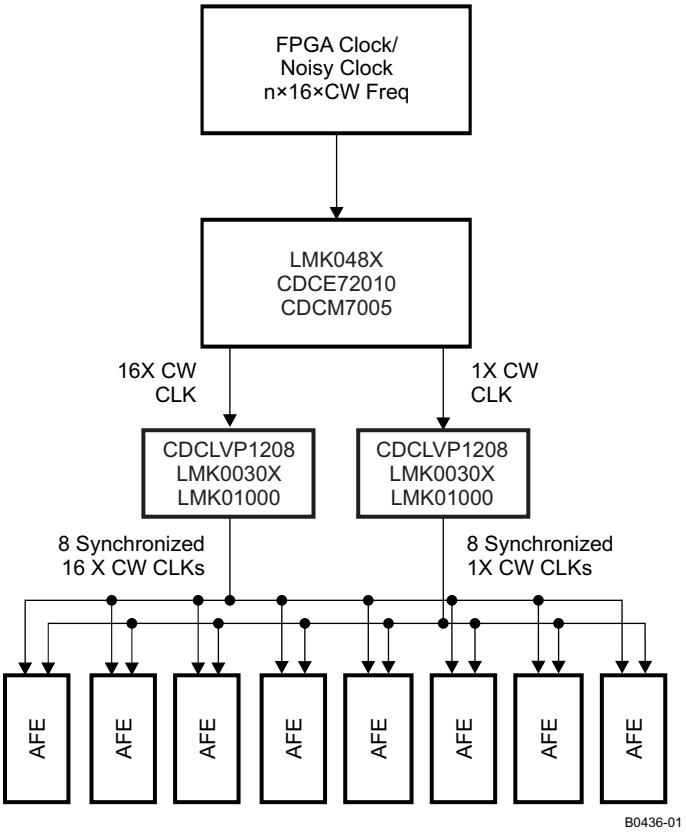


Figure 108. CW Clock Distribution

11.2.2.3.3 CW Supporting Circuits

As a general practice in CW circuit design, in-phase and quadrature channels should be strictly symmetrical by using well-matched layout and high-accuracy components.

In systems, additional high-pass wall filters (20 to 500 Hz) and low-pass audio filters (10 to 100 kHz) with multiple poles are usually needed. Because the CW Doppler signal ranges from 20 Hz to 20 kHz, noise under this range is critical. Consequently, low-noise audio operational amplifiers are suitable to build these active filters for CW post-processing, that is, OPA1632 or OPA2211. To find more filter design techniques, see www.ti.com. For the TI active filter design tool, see http://focus.ti.com/docs/toolsw/folders/print/filter-designer.html.

The filtered audio CW I/Q signals are sampled by audio ADCs and processed by DSP or PC. Although CW signal frequency is from 20 Hz to 20 kHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Due to the large dynamic range of CW signals, high resolution ADCs (≥16 bit) are required, such as ADS8881(18bit, 1MSPS), ADS8413 (2 MSPS, 16-bit, 92-dBFS SNR) and ADS8472 (1 MSPS, 16-bit, 95-dBFS SNR). ADCs for in-phase and quadrature-phase channels must be strictly matched, not only amplitude matching but also phase matching, in order to achieve the best I/Q matching. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

11.2.2.4 Low Frequency Support

In addition, the signal chain of the AFE5812 can handle signal frequency lower than 100 kHz, which enables the AFE5812 to be used in both sonar and medical applications. The PGA integrator has to be turned off in order to enable the low frequency support. Meanwhile, a large capacitor like 1 µF can be used for setting low corner frequency of the LNA DC offset correction circuit as shown in Figure 62. See Figure 59 to find AFE5812's low frequency response.

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11.2.2.5 ADC Operation

11.2.2.5.1 ADC Clock Configurations

To ensure that the aperture delay and jitter are the same for all channels, the AFE5812 uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

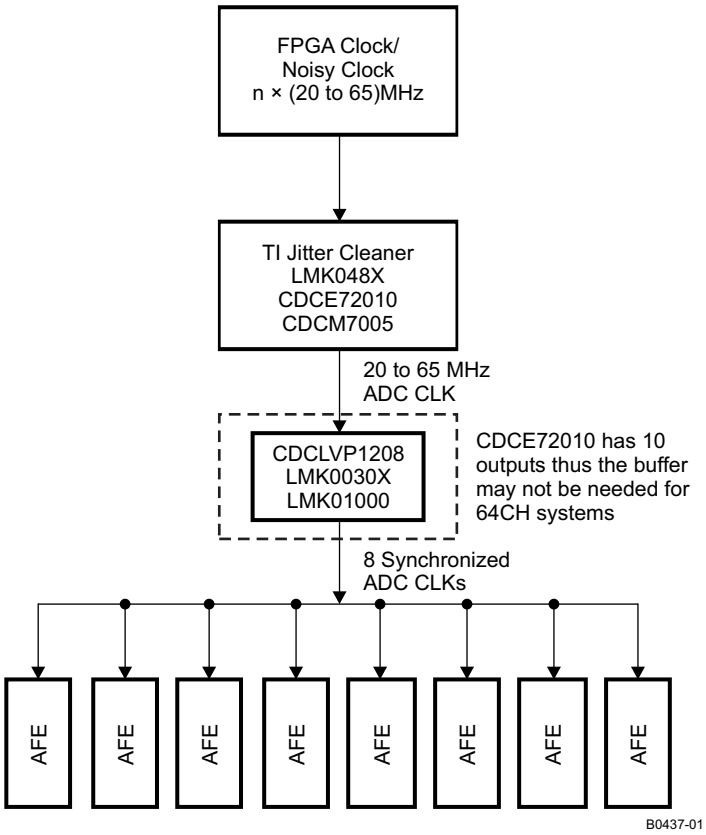


Figure 109. ADC Clock Distribution Network

The AFE5812 ADC clock input can be driven by differential clocks (sine wave, LVPECL, or LVDS) or singled clocks (LVCMOS) similar to CW clocks as shown in Figure 107. In the single-end case, TI recommends that the use of low jitter square signals (LVCMOS levels, 1.8-V amplitude). See TI document SLYT075 for further details on the theory.

The jitter cleaner LMK048x, CDCM7005 or CDCE72010 is suitable to generate the AFE5812's ADC clock and ensure the performance for the14-bit ADC with 77-dBFS SNR. Figure 109 shows a clock distribution network.

11.2.2.5.2 ADC Reference Circuit

The ADC's voltage reference can be generated internally or provided externally. When the internal reference mode is selected, the REFP/M become output pins and should be floated. When 3[15] = 1 and 1[13] = 1, the device is configured to operate in the external reference mode in which the VREF_IN pin should be driven with a 1.4-V reference voltage and REFP/M must be left open. Because the input impedance of the VREF_IN is high, no special drive capability is required for the 1.4-V voltage reference

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The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips. When the external reference mode is used, a solid reference plane on a PCB can ensure minimal voltage variation across devices. More information on voltage reference design can be found in the document SLYT339.

The dominant gain variation in the AFE5812 comes from the VCA gain variation. The gain variation contributed by the ADC reference circuit is much smaller than the VCA gain variation. Hence, in most systems, using the ADC internal reference mode is sufficient to maintain good gain matching among multiple AFE5812s. In addition, the internal reference circuit without any external components achieves satisfactory thermal noise and phase noise performance.

11.2.3 Application Curves

Figure 110 show the output SNR of one AFE channel from VCNTL = 0 V and VCNTL = 1.2 V, respectively, with an input signal at 5 MHz captured at a sample rate of 50 MHz. VCNTL = 0 V represents far field while VCNTL = 1.2 V represents near field. Figure 111 shows the CW phase noise or dyanmic range of a singe AFE channel.

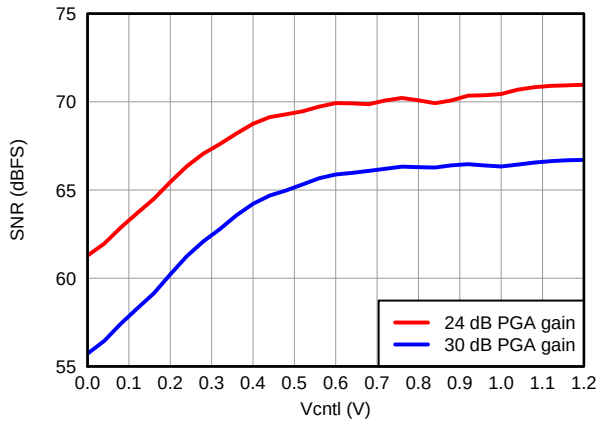


Figure 110. SNR vs. Vcntl at 18dB LNA

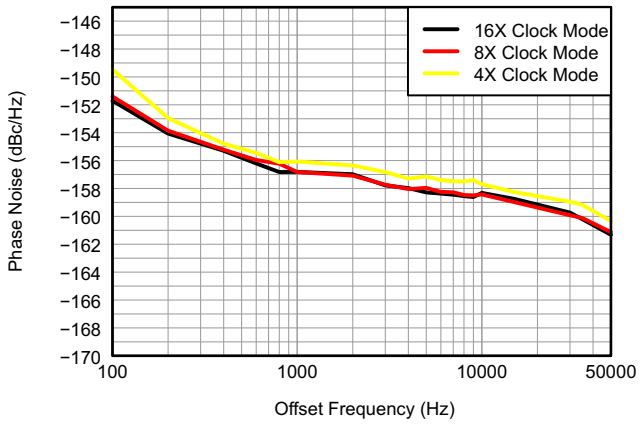


Figure 111. CW Phase Noise at Fin=2MHz

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11.3 Do's and Don'ts

11.3.1 Driving the inputs (analog or digital) beyond the power-supply rails

For device reliability, an input must not go more than 300 mV below the ground pins or 300 mV above the supply pins as suggested in the *Absolute Maximum Ratings* table. Exceeding these limits, even on a transient basis, can cause faulty or erratic operation and can impair device reliability.

11.3.2 Driving the device signal input with an excessively high level signal

The device offers consistent and fast overload recovery with a 6-dB overloaded signal. For very large overload signals (> 6 dB of the linear input signal range), TI recommends back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal. Refer to the *LNA Input Coupling and Decoupling* section for more details.

11.3.3 Driving the VCNTL signal with an excessive noise source

Noise on the VCNTL signal gets directly modulated with the input signal and causes higher output noise and reduction in SNR performance. Maintain a noise level for the VCNTL signal as discussed in the *Voltage-Controlled Attenuator* section.

11.3.4 Using a clock source with excessive jitter, an excessively long input clock signal trace, or having other signals coupled to the ADC or CW clock signal trace

These situations cause the sampling interval to vary, causing an excessive output noise and a reduction in SNR performance. For a system with multiple devices, the clock tree scheme must be used to apply an ADC or CW clock. Refer to the *ADC Clock Configurations* section for clock mismatch between devices, which can lead to latency mismatch and reduction in SNR performance. Clocks generated by FPGA may include excessive jitter and must be evaluated carefully before driving ADC or CW circuits.

11.3.5 LVDS routing length mismatch

The routing length of all LVDS lines routing to the FPGA must be matched to avoid any timing related issue. For systems with multiple devices, the LVDS serialized data clock (DCLKP, DCLKM) and the frame clock (FCLKP, FCLKM) of each individual device must be used to deserialize the corresponding LVDS serialized data (DnP, DnM).

11.3.6 Failure to provide adequate heat removal

Use the appropriate thermal parameter listed in the *Thermal Information* table and an ambient, board, or case temperature in order to calculate device junction temperature. A suitable heat removal technique must be used to keep the device junction temperature below the maximum limit of 105°C.

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12 Power Supply Recommendations

12.1 Power/Performance Optimization

The AFE5812 has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. Refer to characteristics information listed in the *Electrical Characteristics* as well as the *Typical Characteristics*.

12.2 Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The AFE5812 has fast and flexible power-down and power-up control which can maximize battery life. The AFE5812 can be powered down or up through external pins or internal registers. Table 30 indicates the affected circuit blocks and priorities when the power management is invoked. The higher priority controls can overwrite the lower priority controls.

In the device, all the power-down controls are logically ORed to generate final power down for different blocks. The higher priority controls can cover the lower priority controls.

Table 30. Power Management Priority

	Name	Blocks	Priority
Pin	PDN_GLOBAL	All	High
Pin	PDN_VCA	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Pin	PDN_ADC	ADC	Medium
Register	ADC_PARTIAL_PDN	ADC	Low
Register	ADC_COMPLETE_PDN	ADC	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

12.3 Partial Power-Up and Power-Down Mode

The partial power-up and power-down mode is also called fast power-up and power-down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active as well as the LVDS clock circuit, that is, the LVDS circuit still generates its frame and bit clocks.

The partial power-down function allows the AFE5812 to wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus, a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power-down duration, whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, because the wake-up time is the time required to recharge the capacitors to the desired operating voltages. 0.1 µF at INP and 15 nF at INM can give a wake-up time of 2.5 ms. For larger capacitors, this time will be longer. The ADC wake-up time is about 1 µs. Thus, the AFE5812 wake-up time is more dependent on the VCA wake-up time. This also assumes that the ADC clock has been running for at least 50 µs before normal operating mode resumes. The power-down time is instantaneous, less than 1 µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of an ultrasound system could vary from 50 kHz to 500 Hz, while the imaging depth (that is, the active period for a receive path) varies from 10 µs to hundreds of µs. The power saving can be significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimal impact to FPGAs.

In the partial power-down mode, the AFE5812 typically dissipates only 26 mW/ch, representing an 80% power reduction compared to the normal operating mode. This mode can be set using either pins (PDN_VCA and PDN_ADC) or register bits (VCA_PARTIAL_PDN and ADC_PARTIAL_PDN).

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12.4 Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the AFE5812 can be placed into a complete power-down mode. This mode is controlled through the registers ADC_COMPLETE_PDN, VCA_COMPLETE_PDN, or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the AFE5812 are powered down, and the capacitors connected to the AFE5812 are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the AFE5812 spends in shutdown mode. 0.1 µF at INP and 15 nF at INM can give a wake-up time close to 2.5 ms.

NOTE

When the complete power-down mode is enabled, the digital demodulator may lose register settings. Therefore, it is required to reconfigure the demodulator registers, filter coefficient memory, and profile memory after exiting the complete power-down mode.

12.5 Power Saving in CW Mode

Usually, only half the number of channels in a system are active in the CW mode. Thus, the individual channel control through ADC_PDN_CH <7:0> and VCA's PDN_CH <7:0> can power down unused channels and save power consumption greatly. Under the default register setting in CW mode, the voltage controlled attenuator, PGA, and ADC are still active. During the debug phase, both the PW and CW paths can run simultaneously. In real operation, these blocks need to be powered down manually.

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13 Layout

13.1 Layout Guidelines

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5812 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement. To maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design. In addition, all LVDS trace lengths should be equal and symmetrical; TI recommends to keep trace length variations less than 150 mil (0.150 inch or 3.81 mm).

To avoid noise coupling through supply pins, it is recommended to keep sensitive input net classes, such as INM, INP, ACT pins, away from AVDD 3.3 V, AVDD_5V, DVDD, AVDD_ADC, DVDD_LDO1/2 nets or planes. For example, vias connected to these pins should NOT be routed across any supply plane. That is to avoid power planes under INM, INP, and ACT pins.

In addition, appropriate delay matching should be considered for the CW clock path, especially in systems with high channel count. For example, if clock delay is half of the 16× clock period, a phase error of 22.5° could exist. Thus, the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on BGA PCB layout techniques can be found in the TI application report *MicroStar BGA Packaging Reference Guide* (SSYZ015), which can be downloaded from www.ti.com.

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13.2 Layout Example

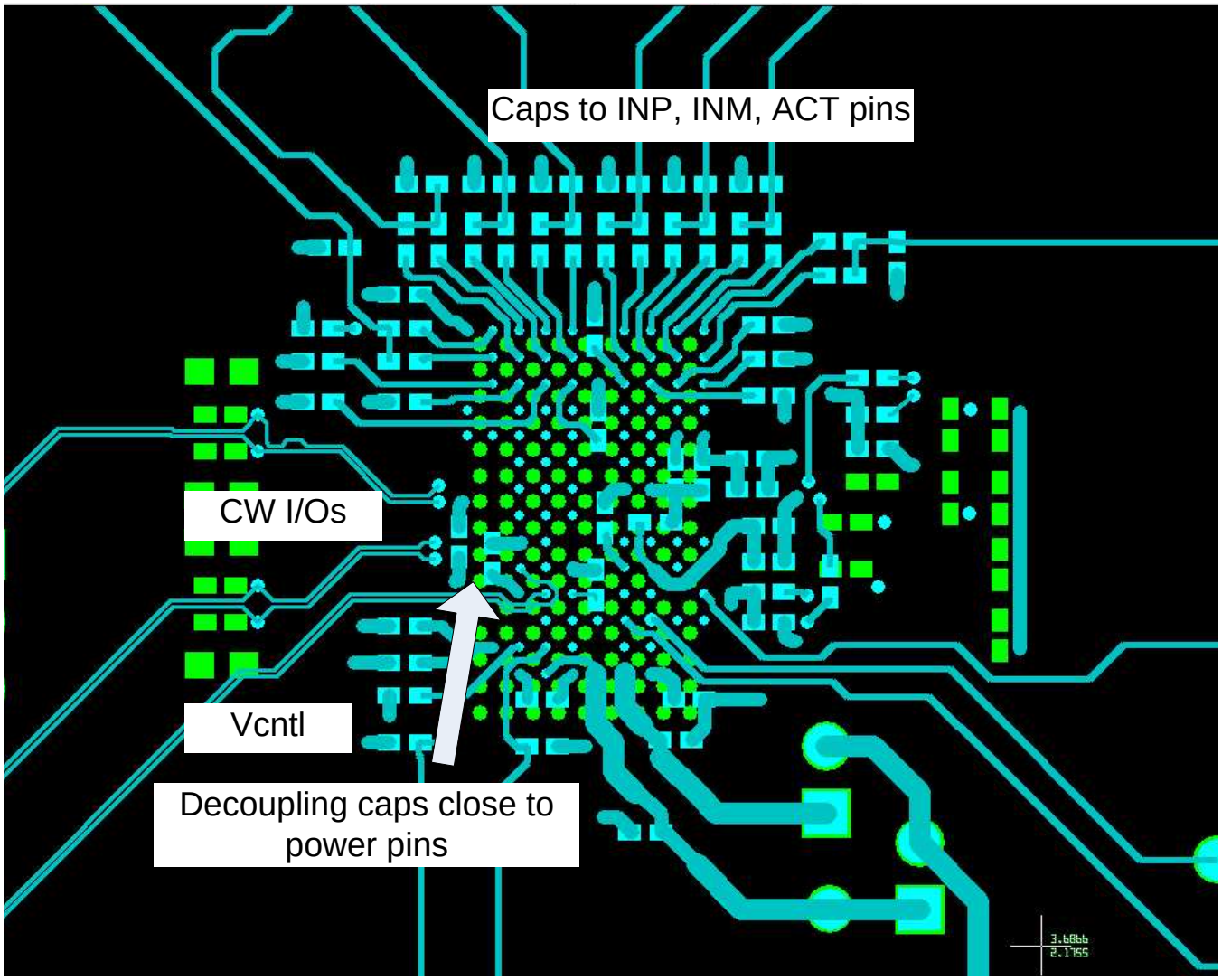


Figure 112. Layout Example

Layout Example (continued)

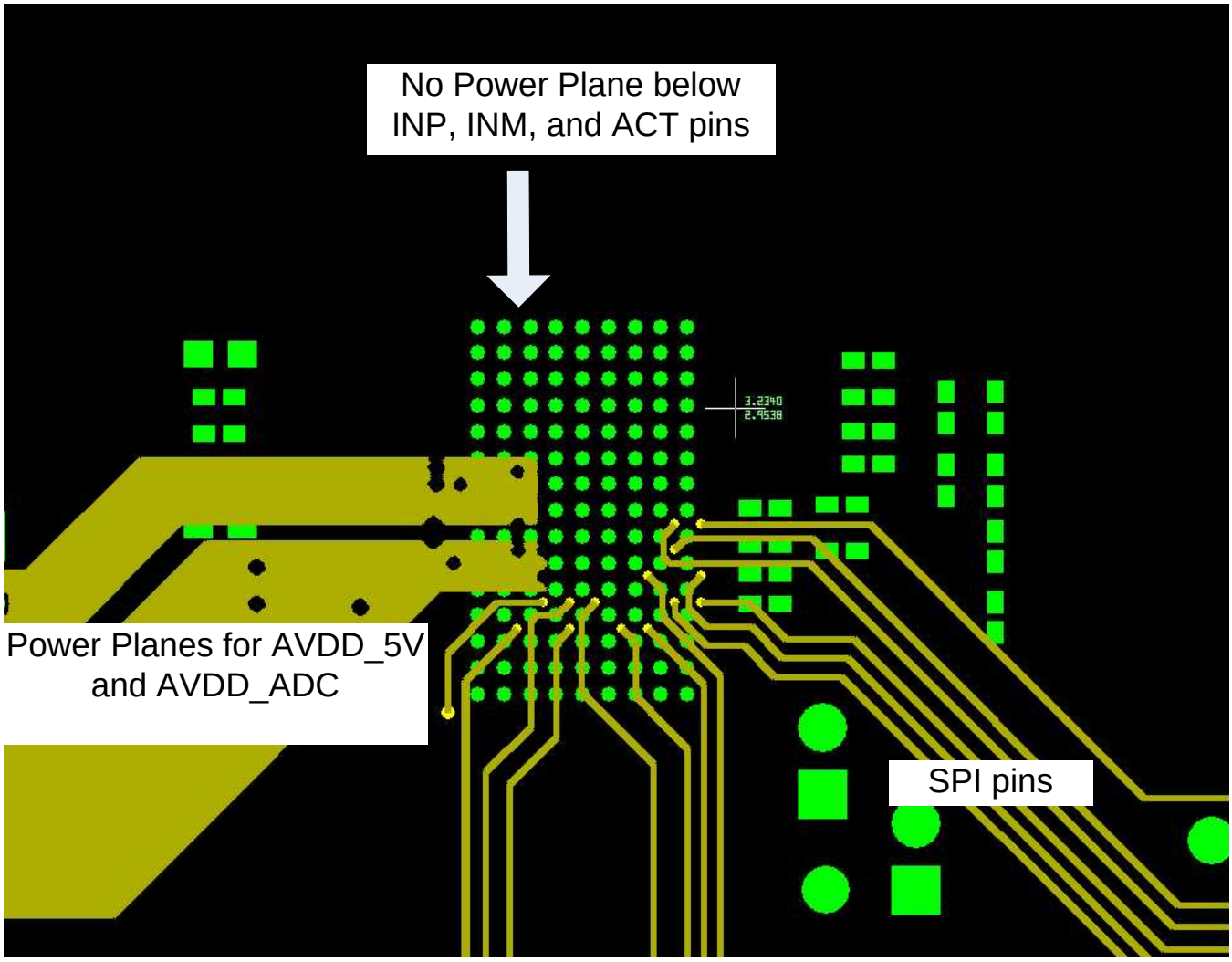


Figure 113. Layout Example

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Layout Example (continued)

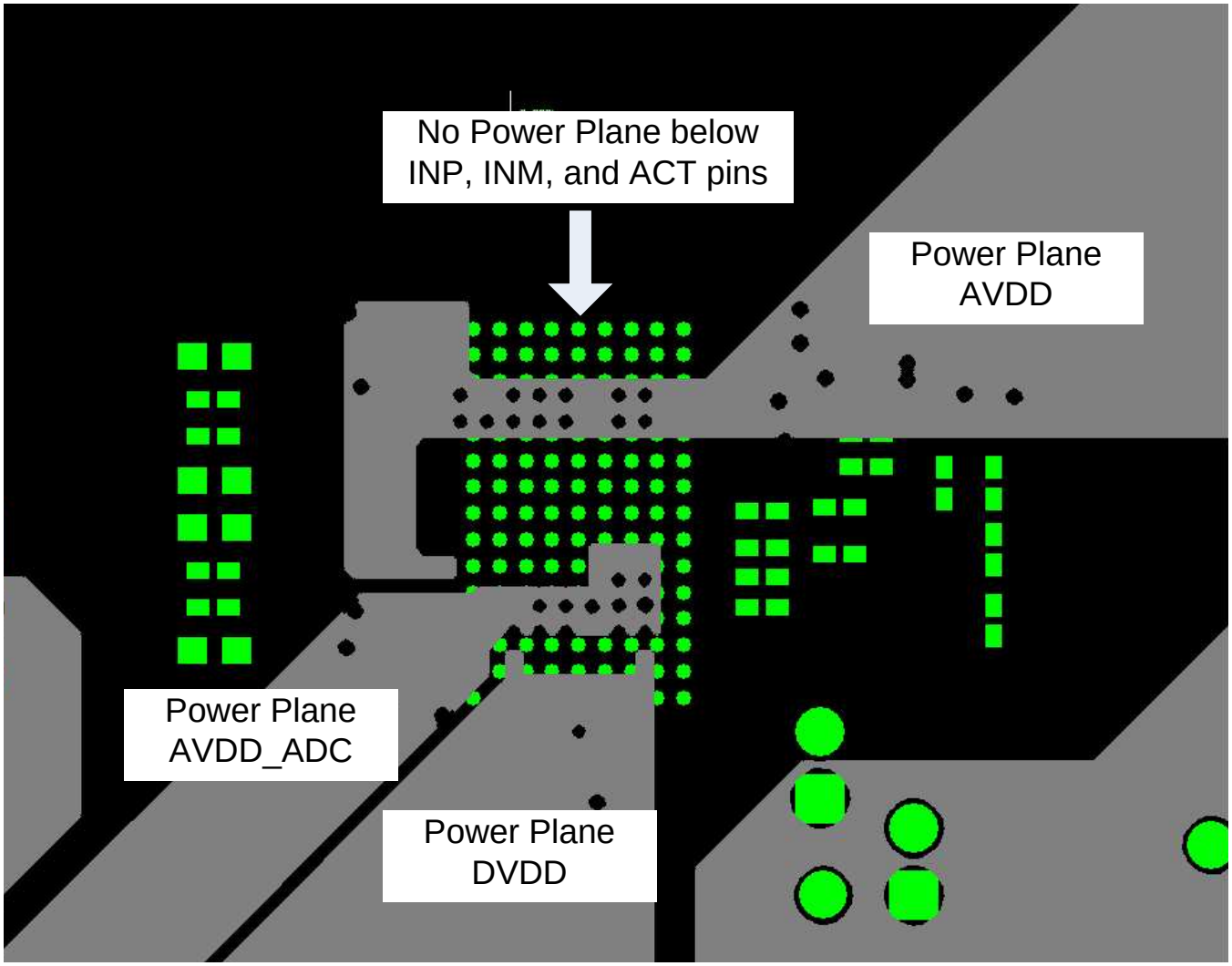


Figure 114. Layout Example

Layout Example (continued)

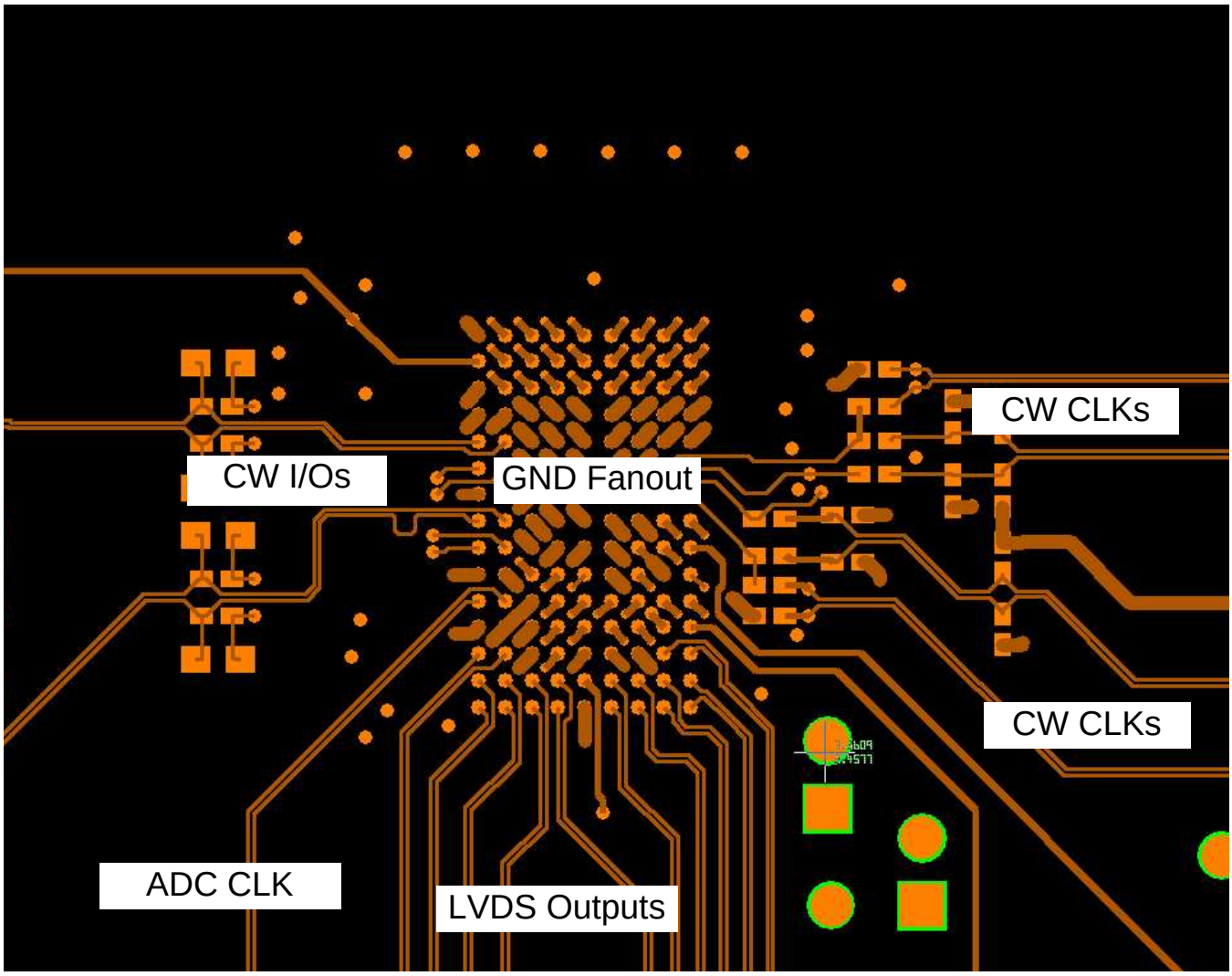


Figure 115. Layout Example

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14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

MicroStar BGA Packaging Reference Guide, SSYZ015

Clocking High-Speed Data Converters, SLYT075

Design for a Wideband Differential Transimpedance DAC Output, SBAA150

TI Active Filter Design Tool, WEBENCH® Filter Designer

AFE5818 Data Sheet, SBAS624

AFE5816 Data Sheet, SBAS688

CDCM7005 Data Sheet, SCAS793

CDCE72010 Data Sheet, SCAS858

TLV5626 Data Sheet, SLAS236

DAC7821 Data Sheet, SBAS365

THS413x Data Sheet, SLOS318

OPA1632 Data Sheet, SBOS286

LMK048x Data Sheet, SNAS489

OPA2211 Data Sheet, SBOS377

ADS8413 Data Sheet, SLAS490

ADS8472 Data Sheet, SLAS514

SN74AUP1T04 Data Sheet, SCES800

ISO7240 Data Sheet, SLLS868

14.2 Trademarks

All trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5812ZCF	ACTIVE	NFBGA	ZCF	135	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE5812	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

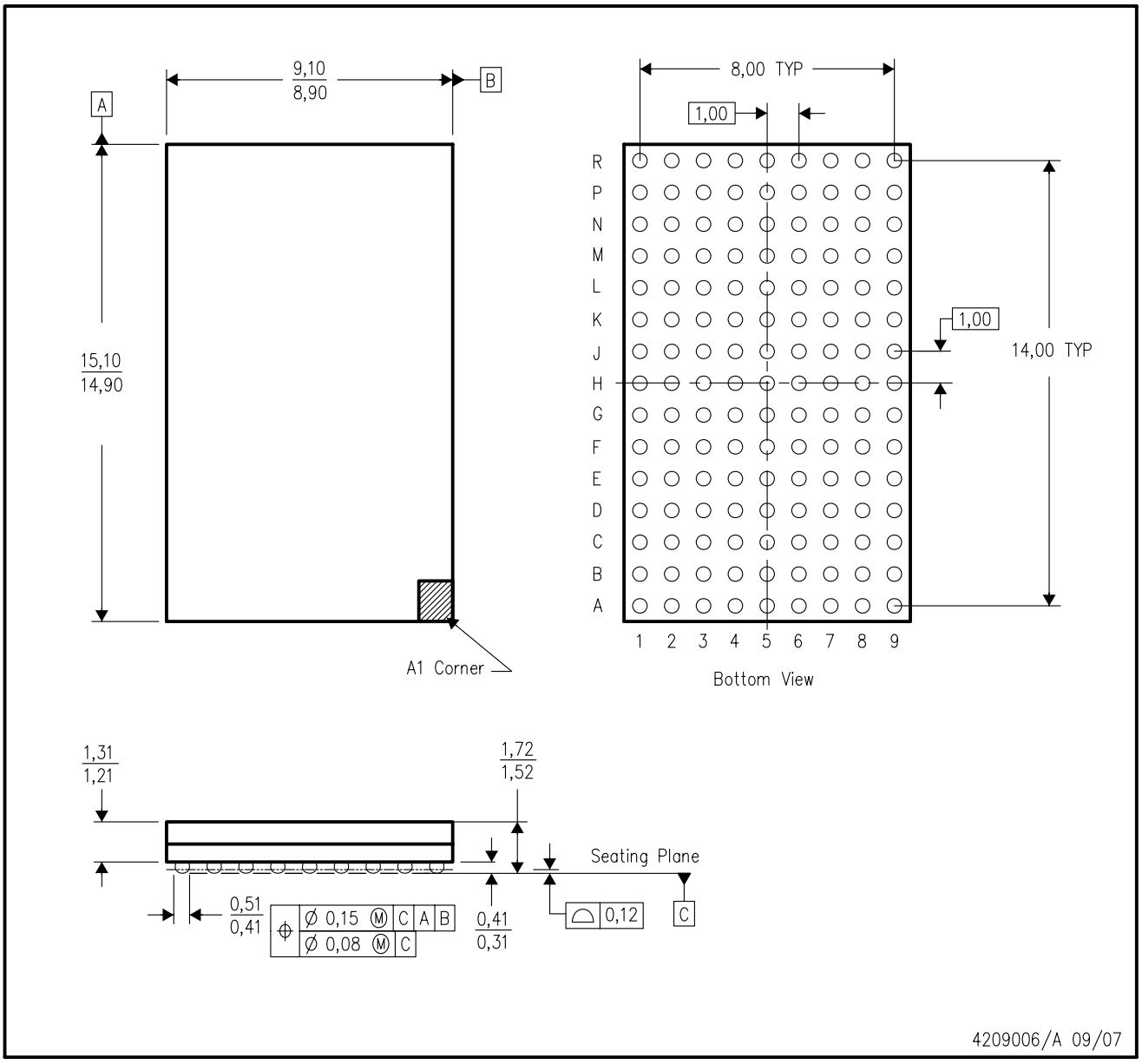
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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