AFBR-79EIPZ

QSFP+ iSR4 Pluggable, Parallel Fiber-Optics Module for 40 Gb Ethernet, 4 x 10 Gb Ethernet and InfiniBand Applications

Data Sheet



Description

The Avago Technologies AFBR-79EIPZ is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ Transceiver with an integrated push-pull tab for 40 Gigabit Ethernet (40GbE) applications with added capability of inter-operating with IEEE 10GBASE-SR compliant products. It also supports 4 x 10G InfiniBand (IB) quadruple data rate (40G-IB-QDR) application and is backward compatible to the 4 x 5G IB dual data rate (20G-IB-DDR) and 4 x 2.5G IB single data rate (10G-IB-SDR) applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with each lane operating at 10.3125 Gbps, giving an aggregated bandwidth of 40 Gbps. This transceiver can also be used for high density 10 Gigabit Ethernet application. It allows optical interoperability with any 10 Gigabit Ethernet (10GbE) transceivers, compliant to the IEEE 802.3ae 10GBASE-SR specifications, of form factors such as SFP+, XFP and X2, to provide an effective port count of over 100 within 1 RU rack. The push-pull tab facilitates the insertion and extraction of these transceivers in such high density environment. This transceiver is designated as a QSFP+ iSR4 solution, where the letter "i" represents interoperability between this QSFP+ transceiver with any 10GBASE-SR compliant modules.

This QSFP+ transceiver link length for either 40 Gigabit Ethernet or high density 10 Gigabit Ethernet application is up to 100 m using OM3 fiber or 150 m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses an 8 or 12 fiber MTP® (MPO) connector. This module incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Part Number Ordering Options

AFBR-79EIPZ	QSFP+ iSR4 module with full real-time digital diagnostic monitoring and push-pull tab
AFBR-79Q4EKZ*	Evaluation Board
AFBR-79Q2EKZ**	Evaluation Kit

* Includes GUI and User Guide

** Includes GUI, User Guide, i-Port and Power Supply

Features

- Compliant to the 40GBASE-SR4 and XLPPI Specifications per IEEE 802.3ba-2010
- Support optical interoperability with IEEE 802.3ae 10GBASE-SR modules of various form factors such as SFP+, XFP, and X2
- Support 40G-IB-QDR / 20G-IB-DDR / 10G-IB-SDR InfiniBand applications
- Compliant to the industry standard SFF-8436 QSFP+ Specification Revision 3.5
- Power Level 1: Max Power <1.5W
- High port density: 21mm horizontal port pitch
- Push-pull tab: ease of transceiver insertion and extraction; tab front clip color coded "Green" for iSR4 identification
- Operates at 10.3125 Gbps per channel with 64b/66b encoded data for 40GbE / 10GbE applications and at 10 Gbps with 8b/10b compatible encoded data for 40G-IB-QDR application
- Links up to 100m using OM3 fiber and 150m using OM4 fiber
- 0 to 70°C case temperature operating range
- Proven High Reliability 850 nm technology: Avago VCSEL array transmitter and Avago PIN array receiver
- Hot pluggable transceiver for servicing and ease of installation
- Two Wire Serial (TWS) interface with maskable interrupts for expanded functionality
- Utilizes a standard 12/8 lane optical fiber with MTP® (MPO) optical connector for high density and thin, light-weight cable management

Applications

- 40GbE, high density 4 x 10GbE, and 40G-IB-QDR / 20G-IB-DDR / 10G-IB-SDR interconnects
- Datacom/Telecom switch & router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

Patent - www.avagotech.com/patents

Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for EN 60825 and CDRH eye safety compliance; Class 1 out of the module. The Tx Input Buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors are located inside the QSFP+ module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals. Diagnostic monitors for VCSEL bias, module temperature, and module power supply voltage are implemented and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm/warning and fault information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning, LOS and/or Tx fault.

Receiver

The optical receiver portion of the transceiver (see Figure 1) incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4 channel output buffer, diagnostic monitors, and control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. AC coupling capacitors are located inside the QSFP+ module and are not required on the host board. Diagnostic monitors for optical input power are implemen-ted and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the flag clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm/warning information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning and/or LOS.

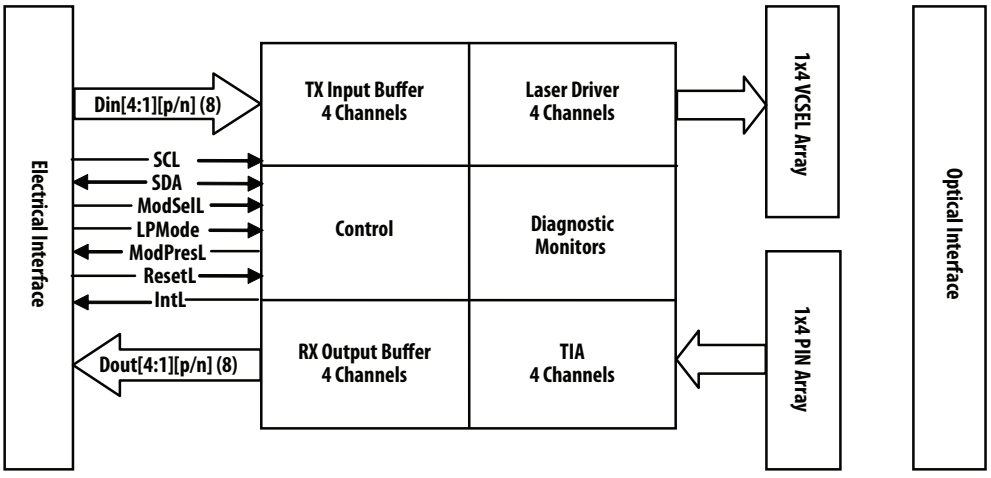


Figure 1. Transceiver Block Diagram

High Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP+ module. For simplicity, only one channel is shown. The high speed signal lines are AC-coupled 100 Ohm differential lines. The AC coupling is inside the QSFP+ module and not required on the host board. The 100 Ohm differential terminations are inside the QSFP+ module for the transmitter lines and at the host ASIC/SerDes for the Receiver lines. All transmitter and receiver electrical channels are compliant to module XLPPI specifications per IEEE 802.3ba.

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signals and timing characteristics are further defined in the Control Interface section. The registers of the serial interface memory are defined in the Memory Map section and corresponding Avago Technologies QSFP+ Memory Map document.

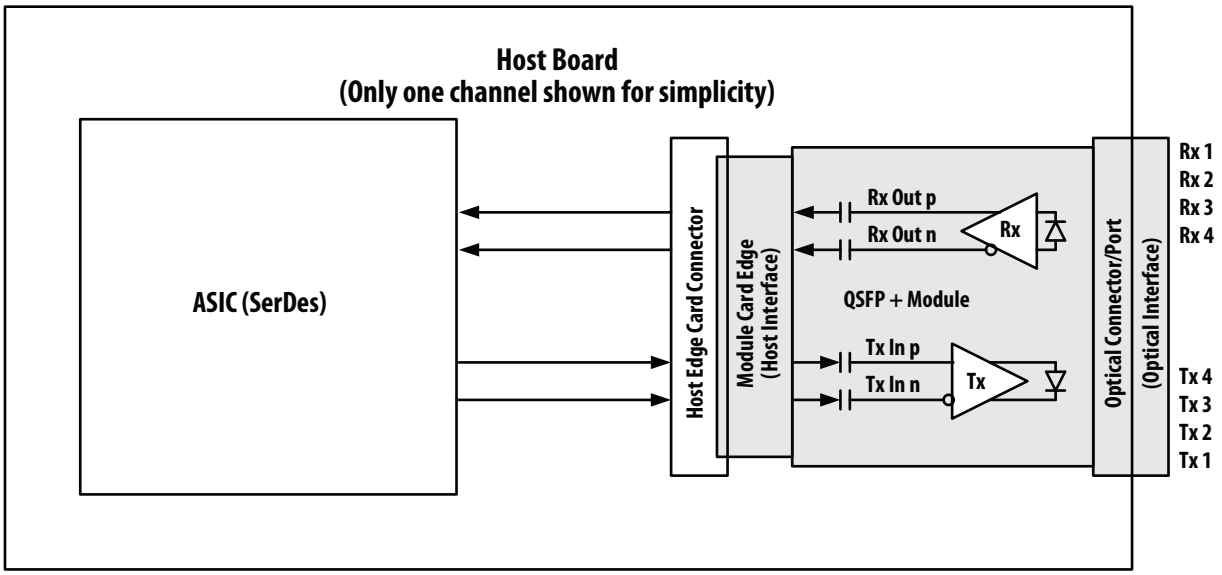


Figure 2. Application Reference Diagram

Digital Diagnostic Monitoring

Digital diagnostic monitoring is available for AFBR-79EIPZ. The information provides opportunity for predictive failure identification, compliance prediction, fault isolation and component monitoring.

Predictive Failure Identification – The diagnostic information allows the host system to identify potential link problems. Once identified, a "failover" technique can be used to isolate and replace suspect devices before system uptime is impacted.

Compliance Prediction – The real-time diagnostic parameters can be monitored to alert the system when operating limits are exceeded and compliance cannot be ensured. As an example, the real time average receiver optical power can be used to assess the compliance of the cable plant and remote transmitter.

Fault Isolation – The diagnostic information can allow the host to pinpoint the location of a link problem and accelerate system servicing and minimize downtime.

Component Monitoring – As part of host system qualification and verification, real time transceiver diagnostic information can be combined with system level monitoring to ensure performance and operating environment are meeting application requirements.

Digital diagnostic monitoring for the following attributes is implemented.

Transceiver module temperature – represents the module internal temperature (lower page 0 bytes 22-23)

Transceiver module power supply – reports the module +3.3V

Regulatory & Compliance

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details regarding these and component recognition. Please note the module transmitter is a Class 1 laser product. See Regulatory Compliance Table for details.

Package Outline

The module is designed to meet the package outline defined in the QSFP+ SFF-8436 Specification. See the package outline and host board footprint figures (Figures 13 – 16) for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no additional cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Reference
Storage Temperature	Ts	-40	85	°C	
3.3 V Power Supply Voltage	Vcc	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	Vcc+0.5	V	
Data Input Voltage – Differential	$\|V_{dip} - V_{din}\|$		1.0	V	1
Control Input Voltage	Vi	-0.5	Vcc+0.5, 3.6	V	
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Note:
1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0	40	70	°C	1
3.3 V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signal Rate per Channel			10.3125		GBd	2
Control* Input Voltage High	Vih	2		Vcc+.3	V	
Control* Input Voltage Low	Vil	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	
Power Supply Noise				50	mVpp	3
Receiver Differential Data Output Load			100		Ohms	
Fiber Length: 2000 MHz·km 50µm MMF (OM3)		0.5		100	m	4
Fiber Length: 4700 MHz·km 50µm MMF (OM4)		0.5		150	m	

* Control signals, LVTTL (3.3 V) compatible

Notes:
1. The position of case temperature measurement is shown in Figure 8.
2. 64b/66b coding is assumed
3. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 9 for recommended power supply filter.
4. Channel insertion loss of 1.9dB (OM3) / 1.5dB (OM4) included with 1.5dB (OM3) / 1dB (OM4) allocated for connection and splice loss.

Transceiver Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbols	Min	Typ	Max	Units	Reference
Transceiver Power Consumption				1.5	W	
Transceiver Power Supply Current				475	mA	
Transceiver Power On Initialization Time	$t_{pwr\ init}$			2000	ms	1

* For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL and SDA see Control Interface Section.

Note:
1. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.

Transmitter Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Notes
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	50			mVpp	
LOS Hysteresis		0.5		4	dB	1

Parameter (From Table 86A-2 of IEEE 802.3ba)	Test Point*	Min	Typ	Max	Units	Notes/Conditions
Single ended input voltage tolerance [2]	TP1a	-0.3		4	V	Referred to TP1 signal common
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1	See IEEE 802.3ba 86A.4.1.1			dB	10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in IEEE 802.3ba spec
J9 Jitter tolerance	TP1a	0.29			UI	Defined in IEEE 802.3ba spec
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	
Eye Mask Coordinates: X1, X2 Y1, Y2	TP1a	SPECIFICATION VALUES 0.11, 0.31 95, 350			 UI mV	Hit Ratio = $5x10^{-5}$

* See Figure 6 for Test Point definitions.

Note:
1. LOS Hysteresis is defined as 20*Log(LOS De-assert Level / LOS Assert Level).
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals

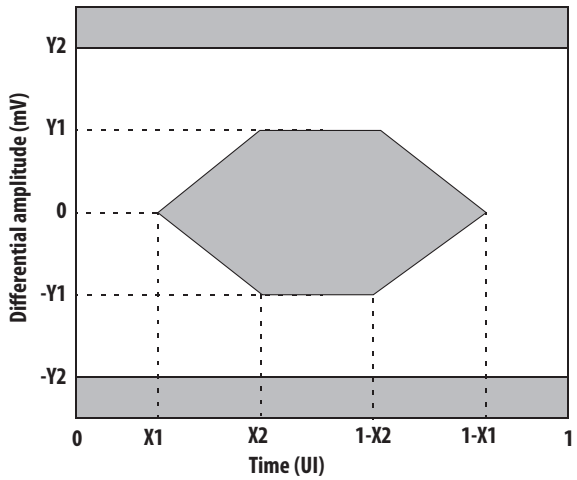


Figure 3. Electrical Eye Mask Coordinates at Hit ratio 5 x 10^{-5} hits per sample

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter (From Table 86A-3 of IEEE 802.3ba)	Test Point*	Min	Typ	Max	Units	Notes/Conditions
Single ended output voltage	TP4	-0.3		4	V	Referred to signal common
AC common mode voltage (RMS)	TP4			7.5	mV	RMS
Termination mismatch at 1MHz	TP4			5	%	
Differential output return loss	TP4	See IEEE 802.3ba 86A.4.2.1			dB	10 MHz to 11.1 GHz
Common-mode output return loss	TP4	See IEEE 802.3ba 86A.4.2.2			dB	10 MHz to 11.1 GHz
Output transition time 20% to 80%	TP4	28			ps	
J2 Jitter output	TP4			0.42	UI	
J9 Jitter output	TP4			0.65	UI	
Eye Mask coordinates: X1, X2 Y1, Y2	TP4	SPECIFICATION VALUES 0.29, 0.5 150, 425			 UI mV	Hit Ratio = $5x10^{-5}$

* See Figure 6 for Test Point definitions.

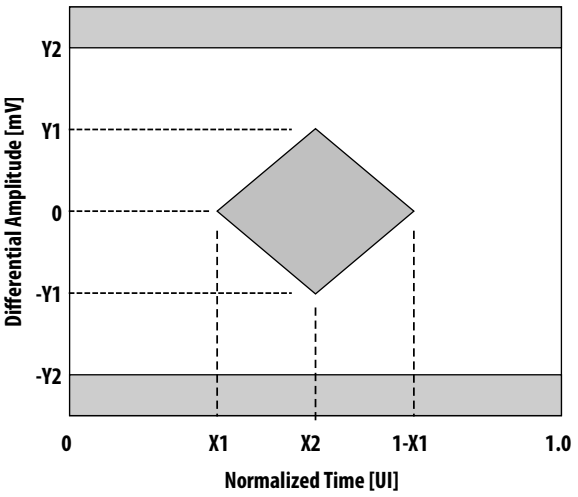


Figure 4. Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample

Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter (From Table 86-6 of IEEE 802.3ba)	Test Point*	Min	Typ	Max	Units	Notes/Conditions
Center wavelength	TP2	840	850	860	nm	
RMS spectral width	TP2			0.65	nm	RMS Spectral Width is the standard deviation of the spectrum
Average launch power, each lane	TP2	-7.6		-1	dBm	
Optical Modulation Amplitude (OMA) each lane	TP2	-5.6		3	dBm	Even if the TDP<0.9 dB, the OMA minimum must exceed -5.6 dBm
Difference in launch power between any two lanes (OMA)	TP2			4	dB	
Peak power, each lane	TP2			4	dBm	
Launch power in OMA minus TDP, each lane	TP2	-6.5			dBm	
Transmitter and dispersion penalty (TDP), each lane	TP2			3.5	dB	
Extinction ratio	TP2	3			dB	
Optical return loss tolerance	TP2			12	dB	
Encircled flux	TP2	≥ 86% at 19 µm, ≤ 30% at 4.5 µm				If measured into type A1a.2 50 µm fiber in accordance with EN 61280-1-4
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	TP2	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4			UI	Hit Ratio = $5x10^{-5}$
Average launch power of OFF transmitter, each lane	TP2			-30	dBm	

* See Figure 6 for Test Point definitions.

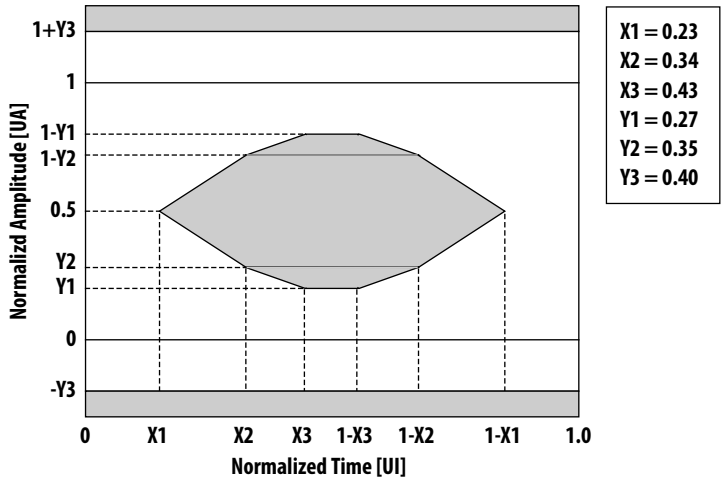


Figure 5. Transmitter eye mask definitions at Hit ratio 5 x 10^{-5} hits per sample

Receiver Optical Characteristics

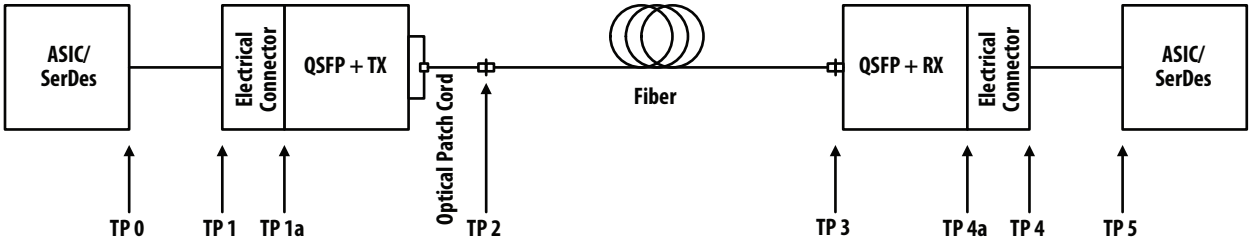
The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter (From Table 86-8 of IEEE 802.3ba)	Test Point*	Min	Typ	Max	Units	Notes/Conditions
Center wavelength, each lane	TP3	840	850	860	nm	
Damage Threshold[1]	TP3	3.4			dBm	
Maximum Average power at receiver input, each lane	TP3			2.4	dBm	
Receiver Reflectance	TP3			-12	dB	
Optical Modulation Amplitude (OMA), each lane	TP3			3	dBm	
Stressed receiver sensitivity in OMA, each lane	TP3			-5.4	dBm	Measured with conformance test signal at TP3 for BER = 10e-12
Conditions of stressed receiver sensitivity: [2]	TP3					
Vertical Eye Closure Penalty, each lane	TP3		1.9		dB	
Stressed eye J2 Jitter, each lane	TP3		0.30		UI	
Stressed eye J9 Jitter, each lane	TP3		0.47		UI	
OMA of each aggressor lane	TP3		-0.4		dBm	
Peak power, each lane	TP3			4	dBm	
LOS Assert	TP3	-30			dBm	
LOS De-Assert – OMA	TP3			-7.5	dBm	
LOS Hysteresis	TP3	0.5			dB	

* See Figure 6 for Test Point definitions.

Note:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power
2. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant



TP0 : Host ASIC transmitter output at ASIC package contact on the Host board
TP1 : Host ASIC transmitter output across the Host Board at the input side of the Host QSFP+ electrical connector
TP1a : Host ASIC transmitter output across the Host board at the output side of the Host QSFP+ electrical connector
TP2 : QSFP+ transmitter optical output at the end of a 2m to 5m patch cord
TP3 : QSFP+ receiver optical input at the end of the fiber
TP4a : QSFP+ receiver electrical output at the input side of the Host QSFP+ electrical connector
TP4 : QSFP+ receiver electrical output at the output side of the Host QSFP+ electrical connector
TP5 : Host ASIC receiver input at ASIC package contact on the Host board

Figure 6. Test point definitions

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transceiver module withstands 1kV on high speed pins and 2kV on low speed pins
	JEDEC Charge Device Model (CDM) (JESD22-C101D)	Transceiver module withstands 250V
Electrostatic Discharge (ESD) to Optical connector	GR1089	10 discharges of 8 kV on the electrical faceplate with device inserted into a panel
Electrostatic Discharge (ESD) to Optical Connector	Variation of EN 61000-4-2	Air discharge of 15kV(min) to connector w/o damage
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically passes with 10 dB margin. Actual performance dependent on enclosure design
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007 and EN 60950-1:2006+A11+A1+A12	EN AEL & US FDA CDRH Class 1
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A & 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm of lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

QSFP+ Transceiver Pad Layout

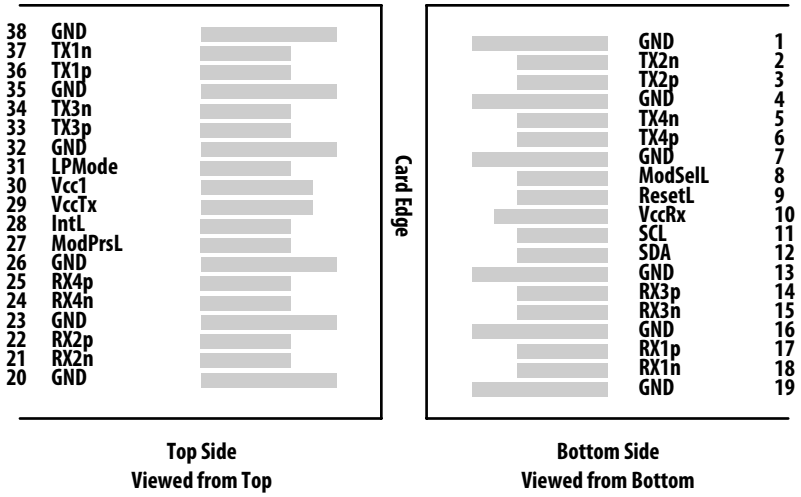


Figure 7. QSFP+ Transceiver Pad Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

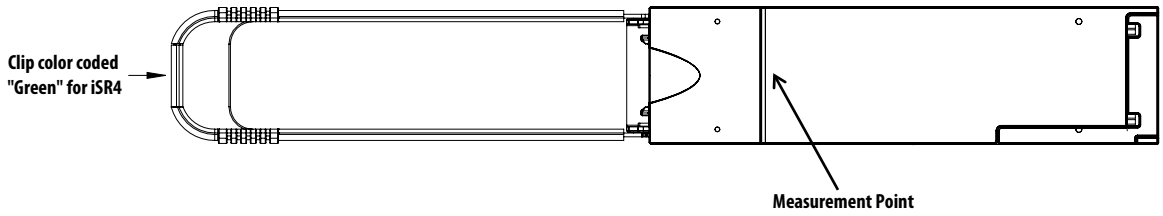


Figure 8. Case Temperature Measurement Point

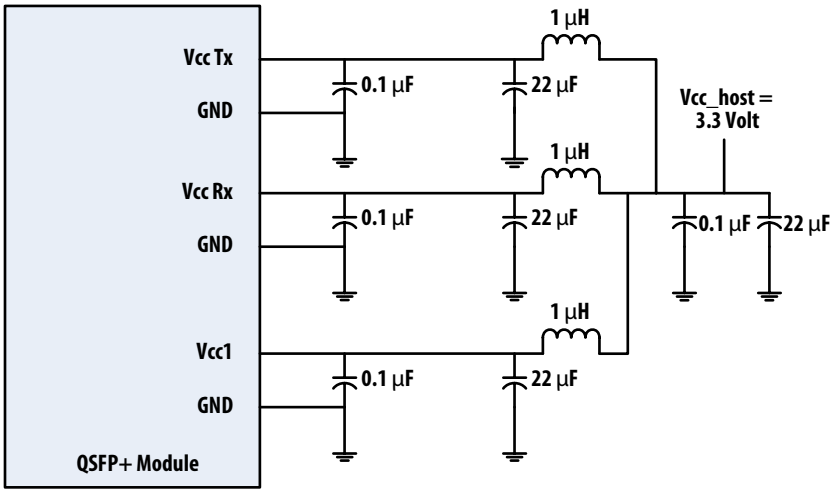


Figure 9. Recommended Power Supply Filter

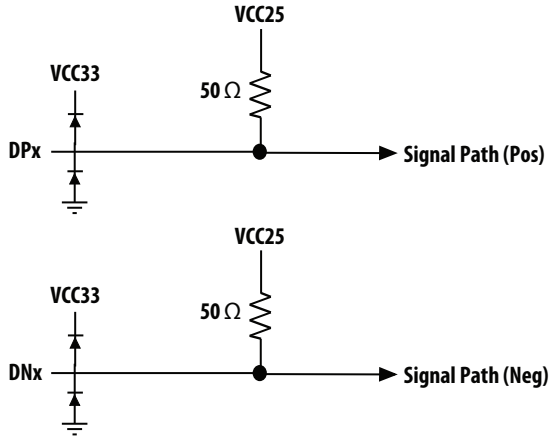


Figure 10. Transmitter Data Input Equivalent Circuit

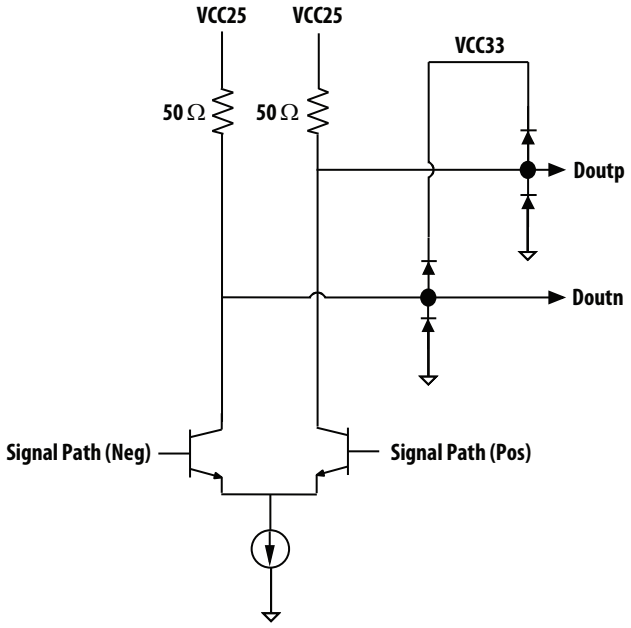


Figure 11. Receiver Data Output Equivalent Circuit

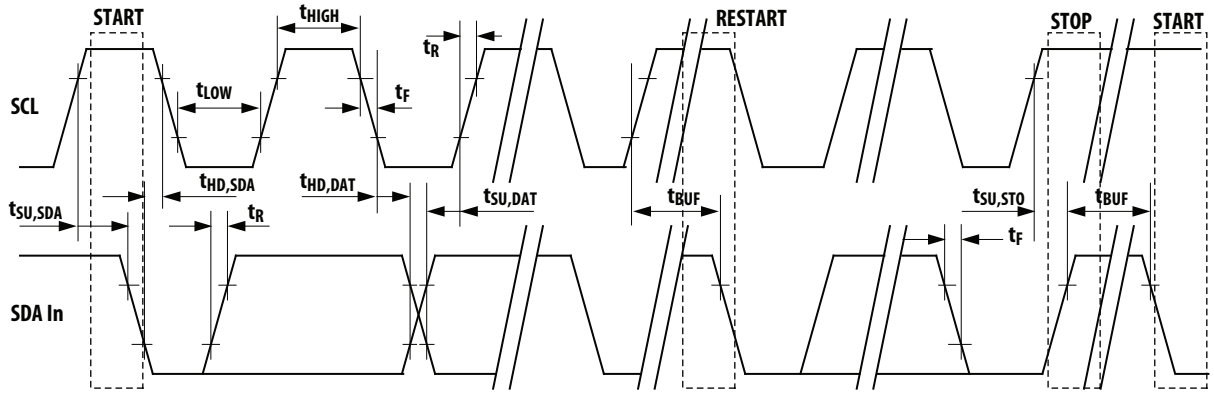
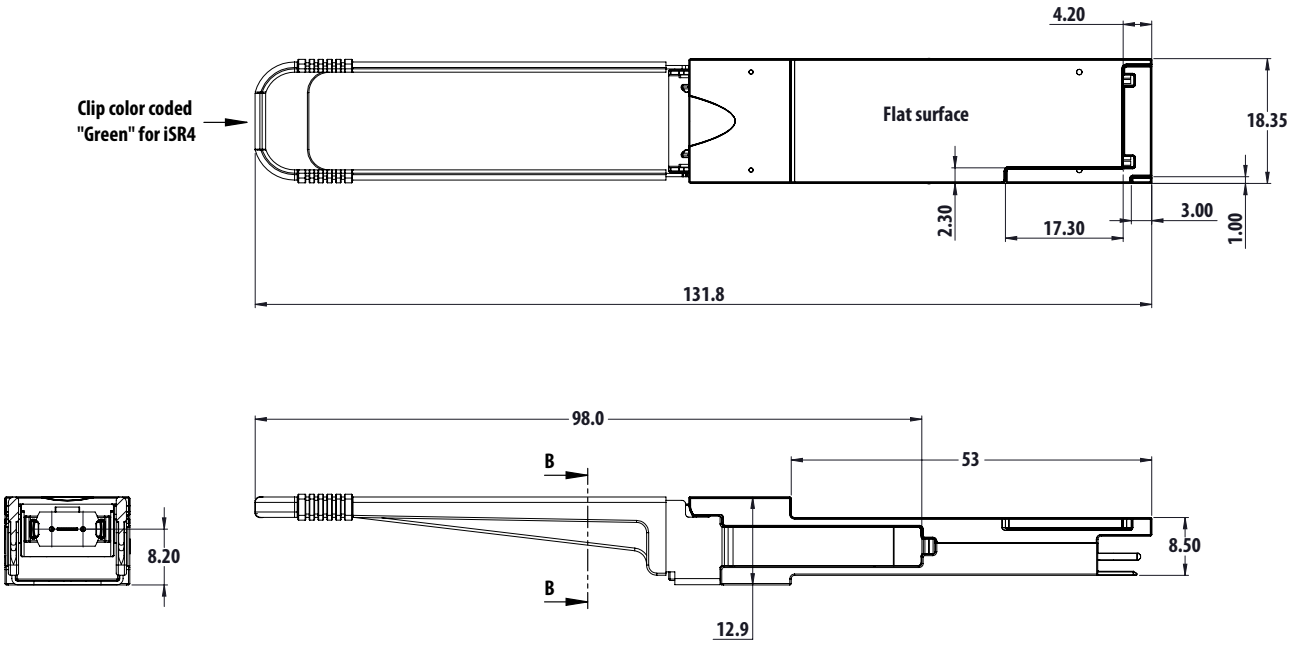


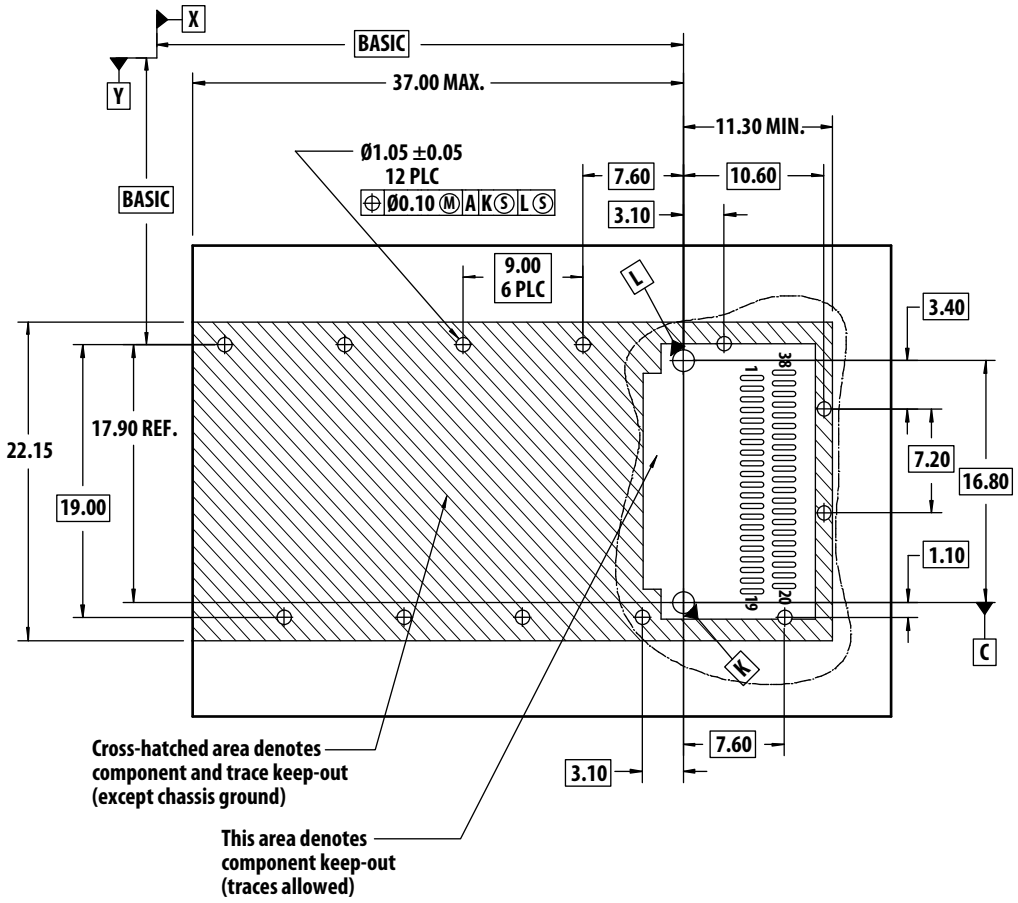
Figure 12. TWS Interface Bus Timing

Package Outline, Host PCB Footprint and Bezel Design



All dimensions in mm

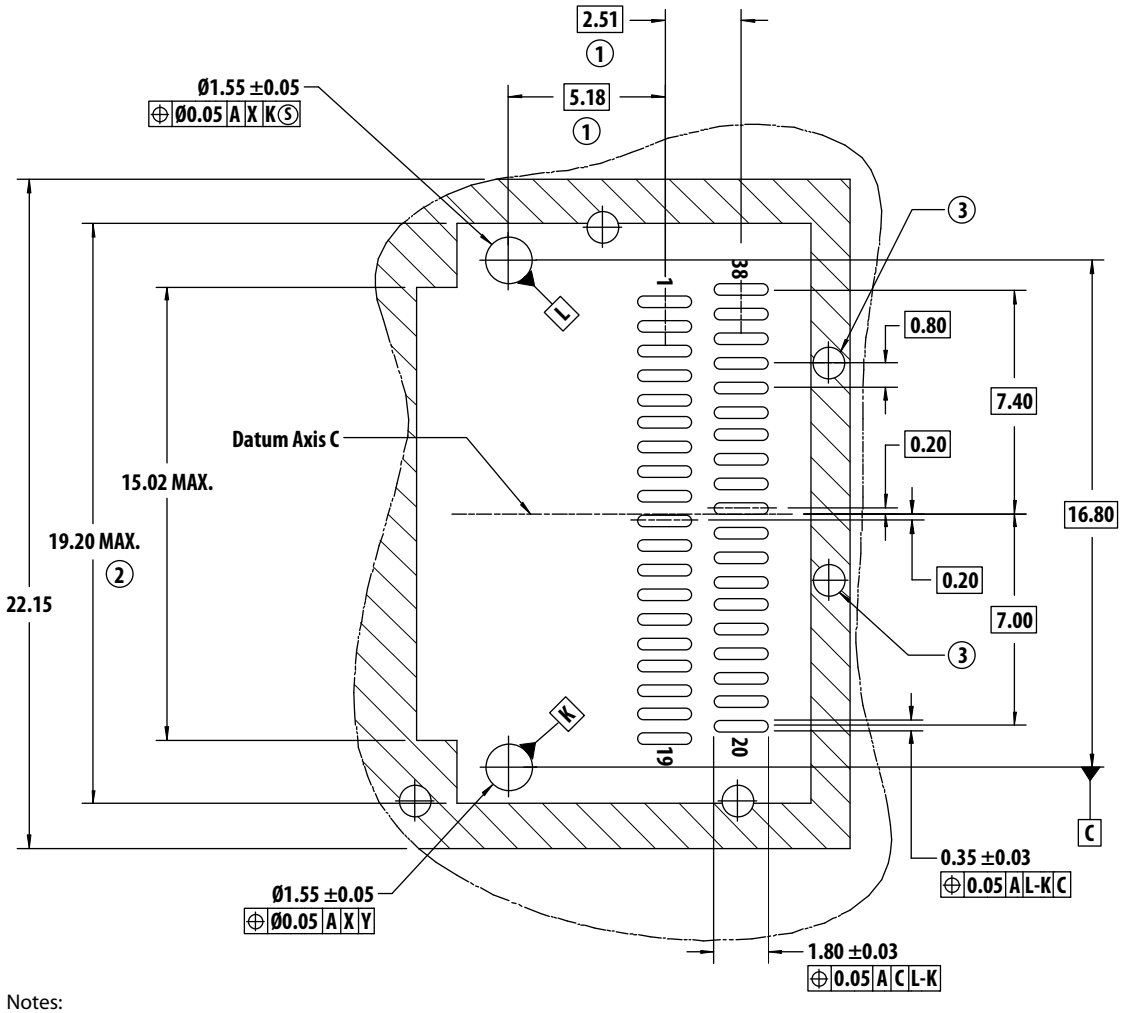
Figure 13. Mechanical Package Outline



Notes:
1. Datum X & Y are established by the customer's fiducial
2. Datum A is the top surface of the host board
3. Location of the edge of PCB is application specific
4. Finished hole size

All dimensions in mm

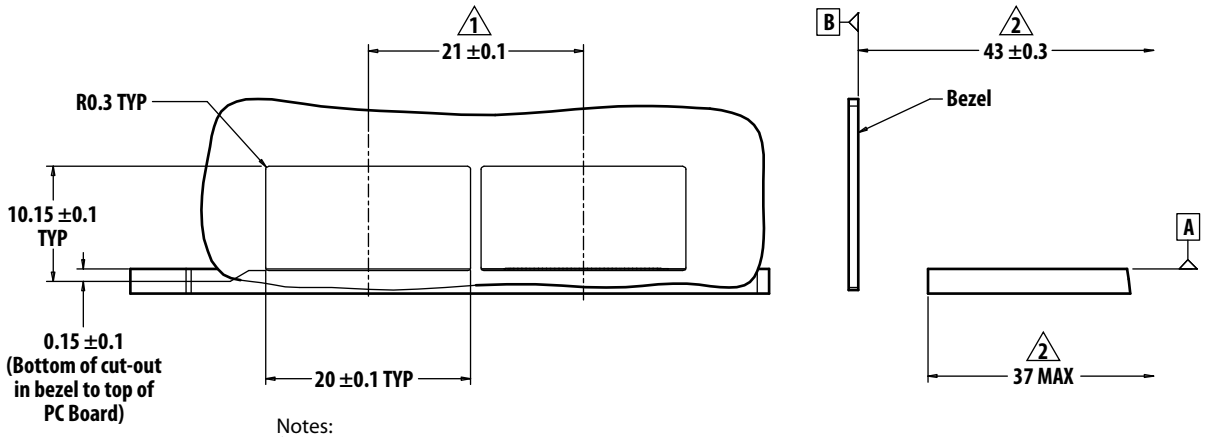
Figure 14. QSFP+ Host Board Mechanical Footprint



Notes:
1. Centerline of Pad
2. Surface traces permitted within this length
3. Indicated holes are optional

All dimensions in mm

Figure 15. QSFP+ Host Board Mechanical Footprint Detail



Notes:
1. Minimum pitch dimension for individual cages.
2. Dimension baseline is datum K or L.
3. Not recommended for PCI applications.

All dimensions in mm

Figure 16. Host Board Bezel Design

Control Interface

The control interface combines dedicated signal lines for ModSelL, LPMode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTL. Outputs are high-z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. For more details, see QSFP+ SFF-8436.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ module is deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled to Vcc in the QSFP+ module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode. When held high by host, the module is held at low power mode. When held low by host, the module operates in the normal mode. For class 1 power level modules (1.5W), low power mode has no effect.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when module is inserted into the host connector, and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL is an output signal. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board. A corresponding soft status IntL signal is also available in the transceiver memory page 0 address 2 bit 1.

Soft Status and Control

A number of soft status signals and controls are available in the AFBR-79EIPZ transceiver memory and accessible through the TWS interface. Some soft status signals include receiver LOS, optional transmitter LOS, transmitter fault and diagnostic monitor alarms and warnings. Some soft controls include transmitter disable (Tx_Dis), receiver output disable (Rx_Dis), transmitter squelch disable (Tx_SqDis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. All soft status signals and controls are per channel basis. All soft control entries are volatile.

Receiver LOS

The receiver LOS status signal is on page 0 address 3 bits 0-3 for channels 1-4 respectively. Receiver LOS is based on input optical modulation amplitude (OMA). This status register is latched and it is cleared on read.

Transmitter LOS

The transmitter LOS status signal is on page 0 address 3 bits 4-7 for channels 1-4 respectively. Transmitter LOS is based on input differential voltage. This status register is latched and it is cleared on read.

Transmitter Fault

The transmitter fault status signal is on page 0 address 4 bits 0-3 for channels 1-4 respectively. Conditions that lead to transmitter fault include laser fault, which occurs generally at transceiver end of life. In addition, unbalanced electrical input data can cause transmitter fault to be triggered. When fault is triggered, the corresponding transmitter channel output will be disabled. Module reset or toggling of soft transmitter disable can restore the transmitter channel function unless fault condition persists. This status register is latched and it is cleared on read.

Transmitter Disable

The transmitter disable control is on page 0 address 86 bits 0-3 for channels 1-4 respectively. When in transmitter fault, toggling the transmitter disable bit signals the transmitter channel to exit the fault state and restores the channel function, unless fault condition persists.

Receiver Disable

The receiver disable control is on page 3 address 241 bits 4-7 for channels 1-4 respectively.

Transmitter Squelch Disable

The transmitter squelch disable control is on page 3 address 240 bits 0-3 for channels 1-4 respectively. AFBR-79EIPZ transceivers have transmitter output squelch function enabled as default.

Receiver Squelch Disable

The receiver squelch disable control is on page 3 address 240 bits 4-7 for channels 1-4 respectively. AFBR-79EIPZ transceivers have receiver output squelch function enabled as default.

I/O Timing for Control and Status Functions

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Reference
Initialization Time	t_init			2000	ms	Time from power on, hot plug or rising edge of Reset until the module is fully functional. This time does not apply to non Power level 0 modules in the Low Power state
LPMode Assert Time	ton_LPMode			100	µs	Time from assertion of LPMode until the module power consumption enters power level 1
Interrupt Assert Time	ton_IntL			200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
Interrupt De-assert Time	Toff_IntL			500	µs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for RX LOS, TX Fault and other flag bits
Reset Init Assert Time	t_reset_init			2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Reset Assert Time	t_reset			2000	ms	Time from rising edge on the ResetL pin until the module is fully functional
Serial Bus Hardware Ready Time	t_serial			2000	ms	Time from power on until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data			2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
RX LOS Assert Time	ton_los			100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted
TX Fault Assert Time	ton_Txfault			200	ms	Time from TX Fault state to TX fault bit set and IntL asserted
Flag Assert Time	ton_Flag			200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask			100	ms	Time from mask bit set until associated IntL assertion is inhibited
Mask Deassert TIme	toff_Mask			100	ms	Time from mask bit cleared until associated IntL operation resumes
Power Set Assert Time	ton_Pdown			100	ms	Time from P_Down bit set until module power consumption enters power level 1
Power Set Deassert Time	toff_Pdown			300	ms	Time from P_Down bit cleared until the module is fully functional
RX Squelch Assert Time	ton_Rxsq			80	µs	Time from loss of RX input signal until the squelched output condition is reached
RX Squelch Deassert Time	toff_Rxsq			80	µs	Time from resumption of RX input signals until normal RX output condition is reached
TX Squelch Assert Time	ton_Txsq			400	ms	Time from loss of TX input signal until the squelched output condition is reached
TX Squelch Deassert Time	toff_Txsq			400	ms	Time from resumption of TX input signals until normal TX output condition is reached
TX Disable Assert Time	ton_txdis			100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal
TX Disable Deassert Time	toff_txdis			400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal
RX Output Disable Assert Time	ton_rxdis			100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal
RX Output Disable Deassert Time	toff_rxdis			100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled
Squelch Disable Deassert Time	toff_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality is enabled

Memory Map

The memory is structured as a single address, multiple page approach. The address is given as A0xh. The structure of the memory is shown in Figure 17. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages of 128 bytes each. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP+ memory map see the QSFP+ SFF-8436 Specification or the Avago Technologies QSFP+ Memory Map document.

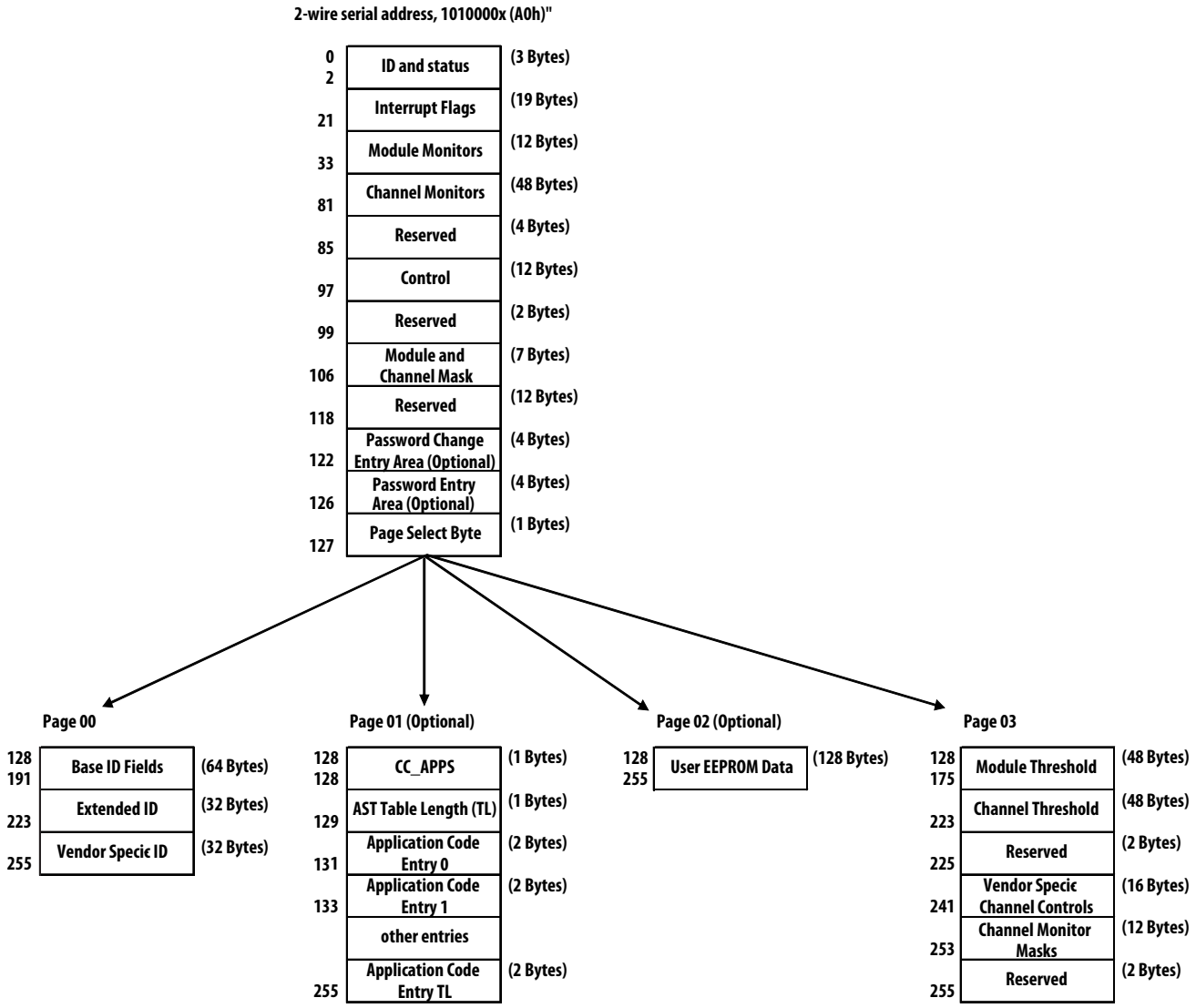


Figure 17. Two-Wire Serial Address A0xh Page Structure

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