Low Power HDMI/DVI Transmitter with Consumer Electronic Control (CEC)

ADV7520NK

FEATURES

General
- Low power HDMI/DVI transmitter ideal for portable applications
- CEC controller and buffer reduce system overhead
- Compatible with HDMI v.1.3, DVI v.1.0, and HDCP 1.3
- Supports xvYCC functionality
- Single 1.8 V power supply
- Video/audio inputs accept logic levels from 1.8 V to 3.3 V

Digital video
- 80 MHz operation supports all HDTV resolutions from 480i to 1080i
- Programmable 2-way color space converter
- Supports RGB, YCbCr, and DDR
- Supports ITU656-based embedded syncs
- Automatic input video format timing detection (CEA-861D)

Digital audio
- Supports standard S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 8-channel, uncompressed LPCM I²S audio up to 192 kHz

Special features for easy system design
- On-chip MPU with I²C master to perform HDCP operations and EDID reading operations
- 5 V tolerant I²C and HPD I/Os, no extra device needed
- No audio master clock needed for supporting S/PDIF and I²S
- On-chip MPU reports HDMI events through interrupts and registers

APPLICATIONS

Digital video cameras
Digital still cameras
Personal media players
Cellular handsets
DVD players and recorders
Digital set-top boxes
A/V receivers
HDMI repeater/splitter

GENERAL DESCRIPTION

The ADV7520NK is an 80 MHz, high definition multimedia interface (HDMI™) v.1.3 transmitter with consumer electronic control (CEC). It supports HDTV formats up to 720p and 1080i and computer graphic resolutions up to XGA (1024 × 768 @ 75 Hz). With the inclusion of HDCP, the ADV7520NK allows the secure transmission of protected content, as specified by the HDCP 1.3 protocol.

FUNCTIONAL BLOCK DIAGRAM

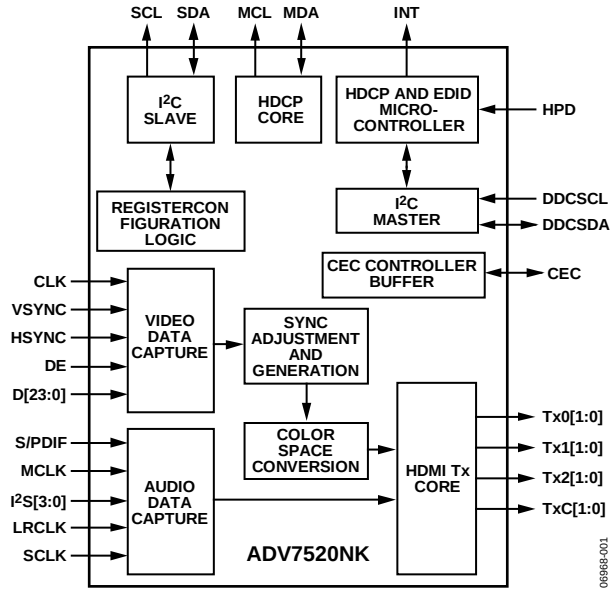

Figure 1.

The ADV7520NK supports both S/PDIF and 8-channel I²S audio. Its high fidelity, 8-channel I²S can transmit either stereo or 7.1 surround audio at 192 kHz. The S/PDIF can carry stereo linear pulse-code modulation (LPCM) audio or compressed audio, including Dolby® Digital and DTS®.

The ADV7520NK helps reduce system design complexity and cost by incorporating such features as an internal microprocessor for high-bandwidth digital content protection (HDCP) operations, an I²C® master for extended display identification data (EDID) reading, a single 1.8 V power supply, and 5 V tolerance on the I²C and hot plug detect pins. For additional information and resources, see the Applications Information section.

Fabricated in an advanced CMOS process, the ADV7520NK is available in a space saving, 76-ball CSP_BGA. The package is RoHS compliant and is specified for −25°C to +90°C operation.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

1/08—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Conditions	Temp	Test Level[1]	Min	Typ	Max	Unit
DIGITAL INPUTS							
Input Voltage, High (V_{IH})		Full	VI	1.4		3.5	V
Input Voltage, Low (V_{IL})		Full	VI	−0.3		+0.7	V
Input Capacitance		25°C	VIII			1.5	pF
THERMAL CHARACTERISTICS							
Thermal Resistance							
Junction-to-Case BGA (θ_{JC})			V		15.2		°C/W
Junction-to-Ambient (θ_{JA})			V		59		°C/W
Ambient Temperature		Full	V	−25	+25	+90	°C
DC SPECIFICATIONS							
Input Leakage Current (I_{IL})		Full	VI	−1		+1	µA
AC SPECIFICATIONS							
CLK Frequency		Full	IV	13.5		80	MHz
TMDS Output CLK Duty Cycle		Full	IV	48		52	%
Input Data Setup Time		Full	IV	1			ns
Input Data Hold Time		Full	IV	0.7			ns
TMDS Differential Swing			VI	900	1000	1100	mV
VSYNC and HSYNC Delay from DE Falling Edge			IV		1		UI[2]
VSYNC and HSYNC Delay to DE Rising Edge			IV		1		UI[2]
Differential Output Swing							
Low-to-High Transition Time		25°C	VII	75	175		ps
High-to-Low Transition Time		25°C	VII	75	175		ps
AUDIO AC TIMING							
Sample Rate	I^2S and S/PDIF	Full	IV	32		192	kHz
I^2S Setup Time		25°C	IV	2			ns
I^2S Hold Time		25°C	IV	2			ns

[1] See the Explanation of Test Levels section.
[2] UI = unit interval.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Digital Inputs	−0.3 V to +5 V
Digital Output Current	20 mA
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

VII. Limits defined by HDMI specification; guaranteed by design and characterization testing.

VIII. Guaranteed by design.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

APPLICATIONS INFORMATION

DESIGN RESOURCES

The following resources, as well as evaluation kits, reference design schematics, and other support documentation, are available after signing an NDA available from flatpanel_apps@analog.com. Users can access a programming guide, a hardware user guide, a software driver user guide, and software driver source code after signing an NDA.

Other references include the following:

EIA/CEA-861, a technical specifications document, describes audio and video InfoFrames, as well as the E-EDID structure for HDMI. It is available from the Consumer Electronics Association (CEA).

HDMI v.1.3, a defining document for HDMI v.1.3, and the *HDMI Compliance Test Specification* v.1.3 are available from HDMI Licensing, LLC.

HDCP Specification v.1.3, the defining technical specifications document for the HDCP v.1.3, is available from Digital Content Protection, LLC.

DOCUMENT CONVENTIONS

In this data sheet, data is represented using the conventions described in Table 3.

Table 3. Document Conventions

Data Type	Format
0xNN	Hexadecimal (Base 16) numbers are represented using the C language notation, preceded by 0x.
0bNN	Binary (Base 2) numbers are represented using the C language notation, preceded by 0b.
NN	Decimal (Base 10) numbers are represented using no additional prefixes or suffixes.
Bit	Bits are numbered in little endian format; that is, the least significant bit of a byte or word is referred to as Bit 0.

OUTLINE DIMENSIONS

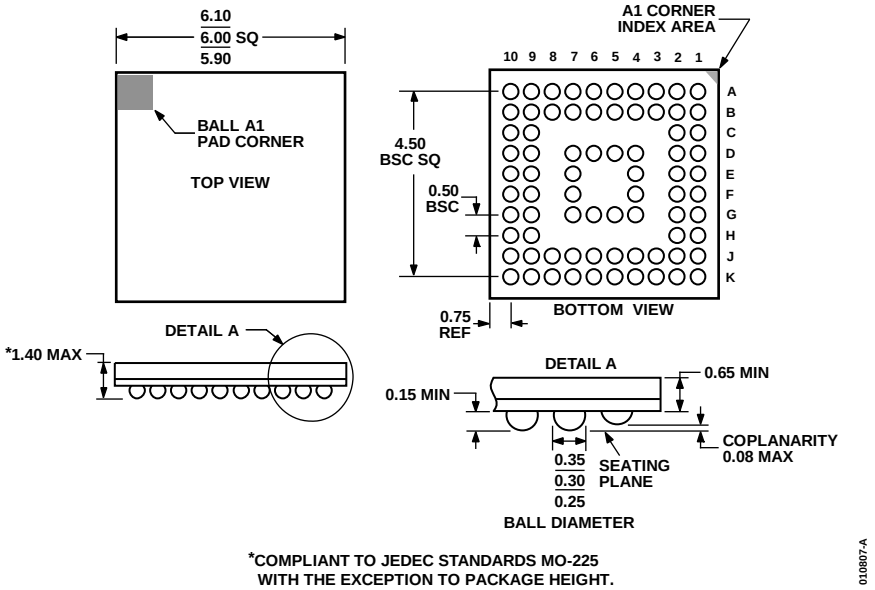

Figure 2. 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
6 mm × 6 mm × 1.4 mm
(BC-76-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7520NKBBCZ-80[1]	−25°C to +90°C	76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-76-1
ADV7520NKBBCZRL-80[1]	−25°C to +90°C	76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-76-1
ADV7520NK/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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