10-Bit, 4× Oversampling SDTV Video Decoder

Data Sheet

ADV7180

FEATURES

- Qualified for automotive applications
- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit ADC, 4× oversampling for CVBS, 2× oversampling for Y/C mode, and 2× oversampling for YPrPb (per channel)
- 3 video input channels with on-chip antialiasing filter
- CVBS (composite), Y/C (S-Video), and YPrPb (component) video input support
- 5-line adaptive comb filters and CTI/DNR video enhancement
- Mini-TBC functionality provided by adaptive digital line length tracking (ADLLT), signal processing, and enhanced FIFO management
- Integrated AGC with adaptive peak white mode
- Macrovision copy protection detection
- NTSC/PAL/SECAM autodetection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, and FIELD[1]
- 1.0 V analog input signal range
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode and ultralow sleep mode current
- 2-wire serial MPU interface (I²C compatible)
- Single 1.8 V supply possible
- 1.8 V analog, 1.8 V PLL, 1.8 V digital, 1.8 V to 3.3 V I/O supply
- −10°C to +70°C commercial temperature grade
- −40°C to +85°C industrial/automotive qualified temperature grade
- −40°C to +125°C temperature grade for automotive qualified
- 4 package types
  - 64-lead, 10 mm × 10 mm, RoHS compliant LQFP
  - 48-Lead, 7 mm × 7 mm, RoHS compliant LQFP
  - 40-lead, 6 mm × 6 mm, RoHS compliant LFCSP
  - 32-lead, 5 mm × 5 mm, RoHS compliant LFCSP

APPLICATIONS

- Digital camcorders and PDAs
- Low cost SDTV PIP decoders for digital TVs
- Multichannel DVRs for video security
- AV receivers and video transcoding
- PCI-/USB-based video capture and TV tuner cards
- Personal media players and recorders
- Smartphone/multimedia handsets
- In-car/automotive infotainment units
- Rearview camera/vehicle safety systems

FUNCTIONAL BLOCK DIAGRAM

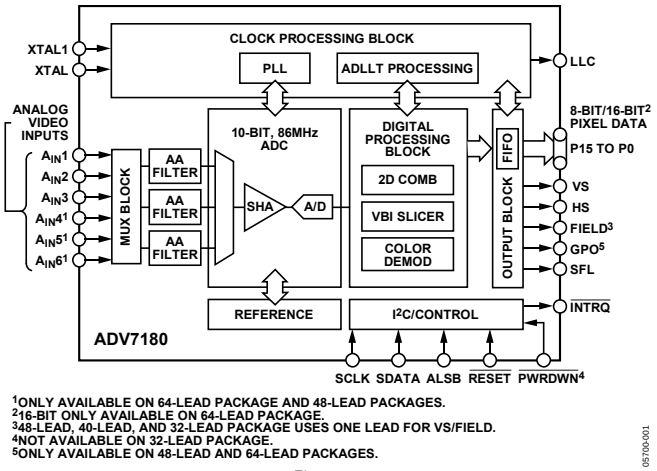

Figure 1.

GENERAL DESCRIPTION

The ADV7180 automatically detects and converts standard analog baseband television signals compatible with worldwide NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with the 8-bit ITU-R BT.656 interface standard.

The simple digital output interface connects gluelessly to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices, Inc., digital video encoders, such as the ADV7391. External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs, if required. Accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution. Three analog video input channels accept standard composite, S-Video, or component video signals, supporting a wide range of consumer video sources. AGC and clamp-restore circuitry allow an input video signal peak-to-peak range to 1.0 V. Alternatively, these can be bypassed for manual settings.

The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% line length variation. Output control signals allow glueless interface connections in many applications. The ADV7180 is programmed via a 2-wire, serial bidirectional port (I²C-compatible) and is fabricated in a 1.8 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. LFCSP package options make the decoder ideal for space-constrained portable applications. The 64-lead LQFP package is pin compatible with the ADV7181C.

[1] The 48-Lead LQFP, 40-lead LFCSP, and 32-lead LFCSP use one pin to output VS or FIELD.

Rev. J
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2/14—Rev. H to Rev. I

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3/12—Rev. F to Rev. G

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1/06—Revision 0: Initial Version

INTRODUCTION

The ADV7180 is a versatile one-chip multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format.

The simple digital output interface connects gluelessly to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices digital video encoders, such as the ADV7391. External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs that do not support the ITU-R BT.656 interface standard. The different package options available for the ADV7180 are shown in Table 2.

ANALOG FRONT END

The ADV7180 analog front end comprises a single high speed, 10-bit analog-to-digital converter (ADC) that digitizes the analog video signal before applying it to the standard definition processor. The analog front end employs differential channels to the ADC to ensure high performance in mixed-signal applications.

The front end also includes a 3-channel input mux that enables multiple composite video signals to be applied to the ADV7180. Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter. A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 29). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7180.

Table 1 shows the three ADC clocking rates that are determined by the video input format to be processed—that is, INSEL[3:0]. These clock rates ensure 4× oversampling per channel for CVBS mode and 2× oversampling per channel for Y/C and YPrPb modes.

Table 1. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)[2]	86	2×
YPrPb	86	2×

[1] Based on a 28.6363 MHz crystal between the XTAL and XTAL1 pins.
[2] See INSEL[3:0] in Table 107 for the mandatory write for Y/C (S-Video) mode.

STANDARD DEFINITION PROCESSOR

The ADV7180 is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported by the video processor include PAL B/D/I/G/H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7180 can automatically detect the video standard and process it accordingly.

The ADV7180 has a five-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7180.

The ADV7180 implements a patented ADLLT™ algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7180 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7180 contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The video processor can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar® 1×/2×, and extended data service (XDS). Teletext data slicing for world standard teletext (WST), along with program delivery control (PDC) and video programming service (VPS), are provided. Data is transmitted via the 8-bit video output port as ancillary data packets (ANC). The ADV7180 is fully Macrovision® certified; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

Table 2. ADV7180 Selection Guide

Part Number[1]	Package Type	Analog Inputs	Digital Outputs	Temperature Grade
ADV7180KCP32Z	32-lead LFCSP	3	8-bit	−10°C to +70°C
ADV7180WBCP32Z (Automotive)	32-lead LFCSP	3	8-bit	−40°C to +85°C
ADV7180BCPZ	40-lead LFCSP	3	8-bit	−40°C to +85°C
ADV7180WBCPZ (Automotive)	40-lead LFCSP	3	8-bit	−40°C to +125°C
ADV7180BSTZ	64-lead LQFP	6	8-bit/16-bit	−40°C to +85°C
ADV7180WBSTZ (Automotive)	64-lead LQFP	6	8-bit/16-bit	−40°C to +125°C
ADV7180WBST48Z (Automotive)	48-lead LQFP	6	8-bit	−40°C to +85°C

[1] W = Automotive qualification completed.

FUNCTIONAL BLOCK DIAGRAMS

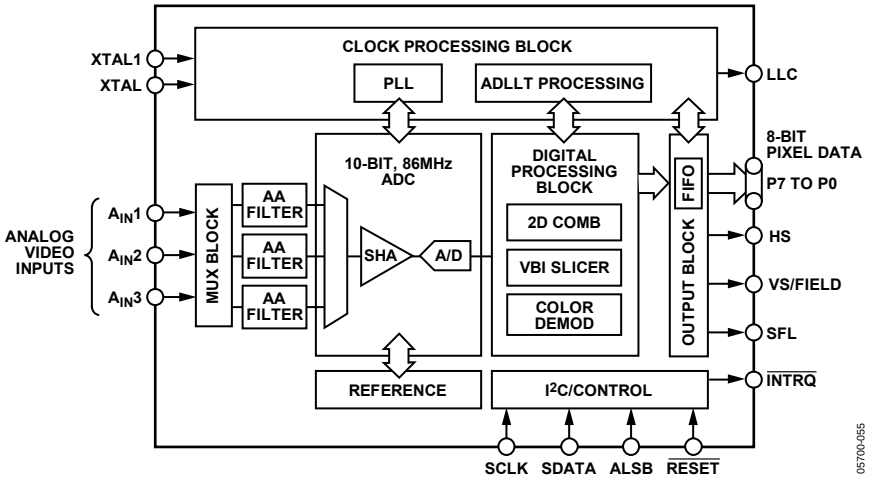


Figure 2. 32-Lead LFCSP Functional Diagram

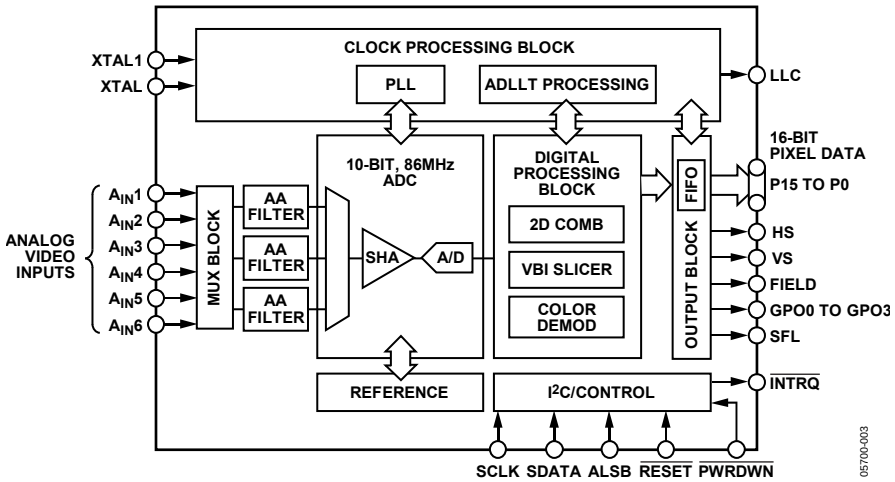


Figure 3. 64-Lead LQFP Functional Block Diagram

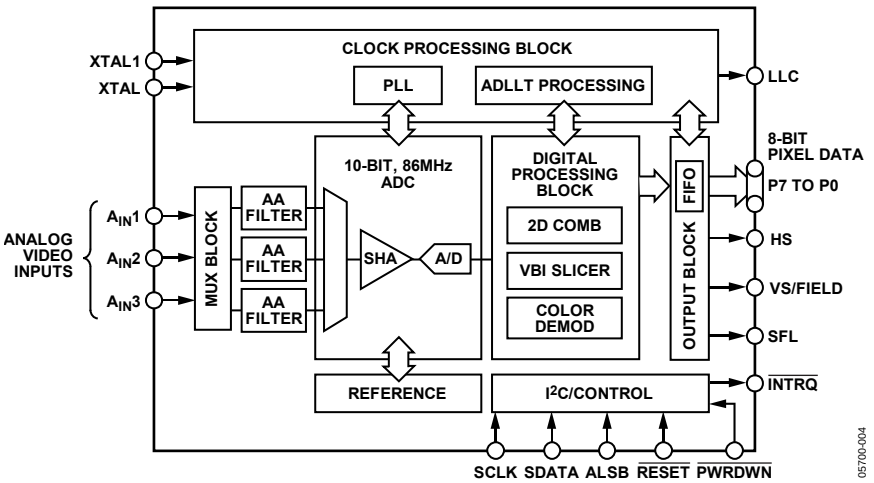


Figure 4. 40-Lead LFCSP Functional Block Diagram

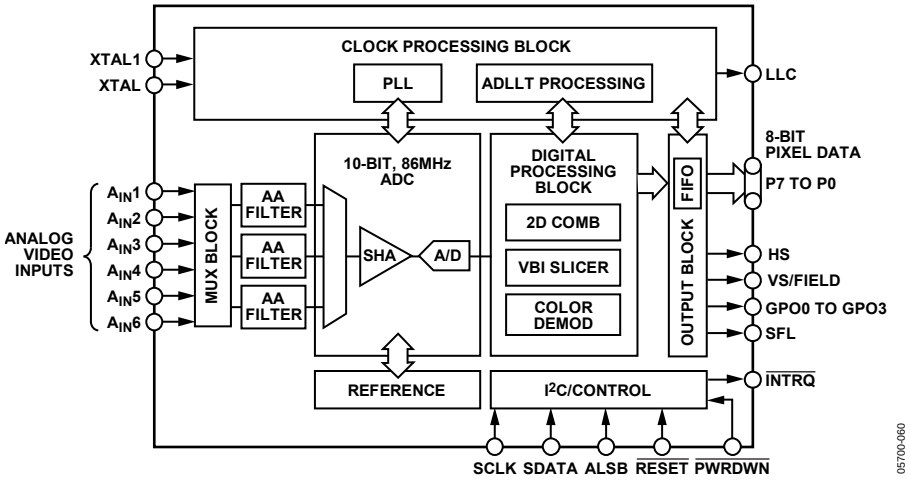


Figure 5. 48-Lead LQFP Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL in CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		−0.6/+0.6		LSB
DIGITAL INPUTS						
Input High Voltage (DVDDIO = 3.3 V)	V_{IH}		2			V
Input High Voltage (DVDDIO = 1.8 V)	V_{IH}		1.2			V
Input Low Voltage (DVDDIO = 3.3 V)	V_{IL}				0.8	V
Input Low Voltage (DVDDIO = 1.8 V)	V_{IL}				0.4	V
Crystal Inputs	V_{IH}		1.2			V
	V_{IL}				0.4	V
Input Current	I_{IN}		−10		+10	µA
Input Current (SDA, SCLK)[1]	I_{IN}		−10		+15	µA
Input Current ($\overline{\text{PWRDWN}}$)[2]	I_{IN}		−10		+48	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage (DVDDIO = 3.3 V)	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output High Voltage (DVDDIO = 1.8 V)	V_{OH}	I_{SOURCE} = 0.4 mA	1.4			V
Output Low Voltage (DVDDIO = 3.3 V)	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Output Low Voltage (DVDDIO = 1.8 V)	V_{OL}	I_{SINK} = 1.6 mA			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[3, 4, 5]						
Digital Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		1.62	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2.0	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Supply Current	I_{DVDD}			77	85	mA
Digital I/O Supply Current[6]	I_{DVDDIO}			3	5	mA
PLL Supply Current	I_{PVDD}			12	15	mA
Analog Supply Current	I_{AVDD}	CVBS input[7]		33	43	mA
		CVBS input[8]		43	53	mA
		Y/C input		59	75	mA
		YPrPb input		77	94	mA
Power-Down Current	I_{DVDD}			6	10	µA
	I_{DVDDIO}			0.1	1	µA
	I_{PVDD}			1	5	µA
	I_{AVDD}			1	5	µA
Total Power Dissipation in Power-Down Mode[9]				15	44	µW
Power-Up Time	t_{PWRUP}			20		ms

[1] ADV7180KCP32Z, ADV7180WBCP32Z, and ADV7180WBST48Z only.
[2] Applies to ADV7180WBST48Z, ADV7180WBST48Z-RL, ADV7180KST48Z, ADV7180KST48Z-RL, ADV7180BST48Z, ADV7180BST48Z-RL only.
[3] Guaranteed by characterization.
[4] Typical current consumption values are recorded with nominal voltage supply levels and a SMPTEBAR pattern.
[5] Maximum current consumption values are recorded with maximum rated voltage supply levels and a multiburst pattern.
[6] Typical (Typ) number is measured with DVDDIO = 3.3 V and maximum (Max) number is measured with DVDDIO = 3.6 V.
[7] CVBS input when CVBS_IBIAS[3:0] (User Map, Register 0x52, Bits[3:0]) equal 0b'1011.
[8] CVBS input when CVBS_IBIAS[3:0] (User Map, Register 0x52, Bits [3:0]) equal 0b'1101. Recommended setting.
[9] ADV7180 clocked.

VIDEO SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulate five-step [NTSC]		0.6		Degrees
Differential Gain	DG	CVBS input, modulate five-step [NTSC]		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step [NTSC]		2.0		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed				100		Lines
Chroma Luma Gain Delay	CVBS			2.9		ns
	Y/C			5.6		ns
	YPrPb			−3.0		ns
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

TIMING SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.6363		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Times	t_6				300	ns
SCLK and SDA Fall Times	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{SETUP} = t_{10} - t_{11}$)			3.6	ns
Data Output Transitional Time	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 - t_{12}$)			2.4	ns

Timing Diagrams

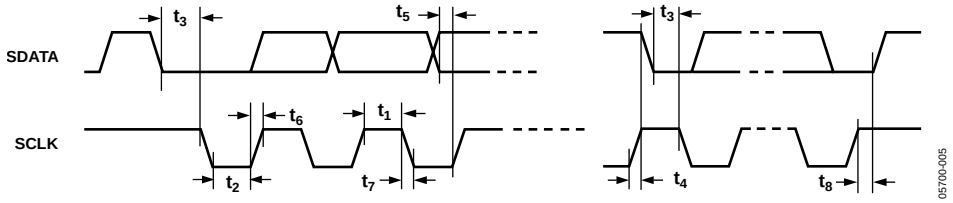


Figure 6. I²C Timing

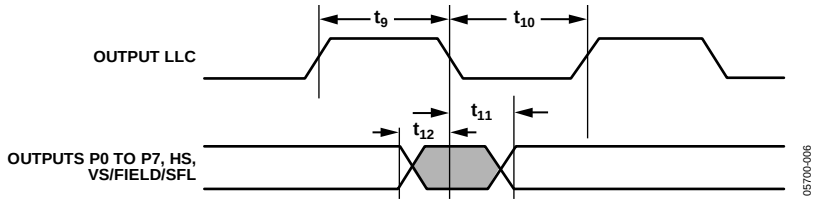


Figure 7. Pixel Port and Control Output Timing

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 1.71 V to 1.89 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 1.62 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, specified at operating temperature range, unless otherwise noted.

Table 6.

Parameter	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large-Clamp Source Current			0.4		mA
Large-Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		µA
Fine Clamp Sink Current			10		µA

THERMAL SPECIFICATIONS

Table 7.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 32-lead LFCSP		32.5		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 32-lead LFCSP		2.3		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 40-lead LFCSP		30		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 40-lead LFCSP		3		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 64-lead LQFP		47		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 64-lead LQFP		11.1		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane, 48-lead LQFP		50		°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane, 48-lead LQFP		20		°C/W

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
A_{VDD} to AGND	2.2 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to A_{VDD}	−0.3 V to +4 V
P_{VDD} to D_{VDD}	−0.3 V to +0.9 V
D_{VDDIO} to P_{VDD}	−0.3 V to +4 V
D_{VDDIO} to D_{VDD}	−0.3 V to +4 V
A_{VDD} to P_{VDD}	−0.3 V to +0.3 V
A_{VDD} to D_{VDD}	−0.3 V to +0.9 V
Digital Inputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to AGND	AGND − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

32-LEAD LFCSP

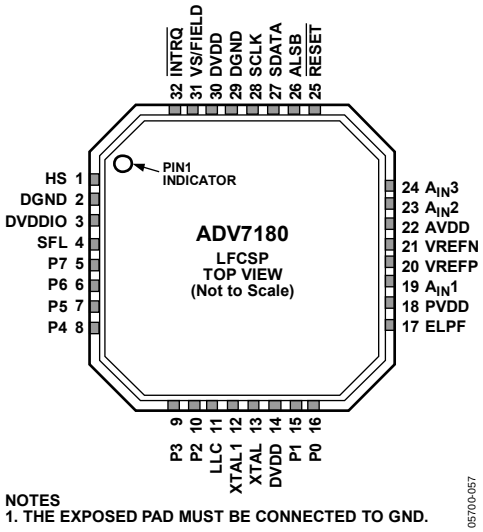


Figure 8. 32-Lead LFCSP Pin Configuration

Table 9. 32-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	HS	O	Horizontal Synchronization Output Signal.
2, 29	DGND	G	Ground for Digital Supply.
3	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
4	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
5 to 10, 15, 16	P7 to P2, P1, P0	O	Video Pixel Output Port.
11	LLC	O	Line-Locked Output Clock for the Output Pixel Data. Nominally 27 MHz but varies up or down according to video line length.
12	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
13	XTAL	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
14, 30	DVDD	P	Digital Supply Voltage (1.8 V).
17	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 60.
18	PVDD	P	PLL Supply Voltage (1.8 V).
19, 23, 24	$A_{IN}1$ to $A_{IN}3$	I	Analog Video Input Channels.
20	VREFP	O	Internal Voltage Reference Output. See Figure 60 for recommended output circuitry.
21	VREFN	O	Internal Voltage Reference Output. See Figure 60 for recommended output circuitry.
22	AVDD	P	Analog Supply Voltage (1.8 V).
25	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
26	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
27	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
28	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
31	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
32	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
	EPAD (EP)		The exposed pad must be connected to GND.

40-LEAD LFCSP

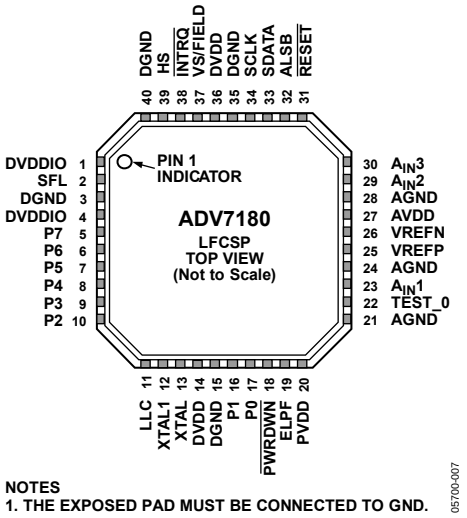


Figure 9. 40-Lead LFCSP Pin Configuration

Table 10. 40-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
2	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
3, 15, 35, 40	DGND	G	Ground for Digital Supply.
5 to 10, 16, 17	P7 to P2, P1, P0	O	Video Pixel Output Port.
11	LLC	O	Line-Locked Output Clock for the Output Pixel Data. Nominally 27 MHz but varies up or down according to video line length.
12	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
13	XTAL	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
14, 36	DVDD	P	Digital Supply Voltage (1.8 V).
18	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 into power-down mode.
19	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 57.
20	PVDD	P	PLL Supply Voltage (1.8 V).
21, 24, 28	AGND	G	Ground for Analog Supply.
22	TEST_0	I	This pin must be tied to DGND.
23, 29, 30	$A_{IN}1$ to $A_{IN}3$	I	Analog Video Input Channels.
25	VREFP	O	Internal Voltage Reference Output. See Figure 57 for recommended output circuitry.
26	VREFN	O	Internal Voltage Reference Output. See Figure 57 for recommended output circuitry.
27	AVDD	P	Analog Supply Voltage (1.8 V).
31	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
32	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
33	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
34	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
37	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
38	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
39	HS	O	Horizontal Synchronization Output Signal.
	EPAD (EP)		The exposed pad must be connected to GND.

64-LEAD LQFP

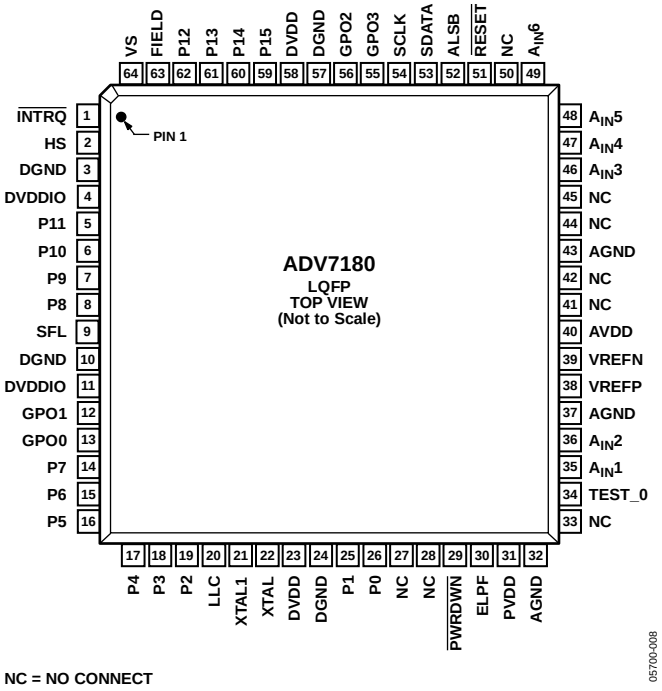


Figure 10. 64-Lead LQFP Pin Configuration

Table 11. 64-Lead LQFP Pin Function Description

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
2	HS	O	Horizontal Synchronization Output Signal.
3, 10, 24, 57	DGND	G	Digital Ground.
4, 11	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
5 to 8, 14 to 19, 25, 26, 59 to 62	P11 to P8, P7 to P2, P1, P0, P15 to P12	O	Video Pixel Output Port. See Table 100 for output configuration for 8-bit and 16-bit modes.
9	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
12, 13, 55, 56	GPO0 to GPO3	O	General-Purpose Outputs. These pins can be configured via I^2C to allow control of external devices.
20	LLC	O	This is a line-locked output clock for the pixel data output by the ADV7180. It is nominally 27 MHz but varies up or down according to video line length.
21	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
22	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or this pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
23, 58	DVDD	P	Digital Supply Voltage (1.8 V).
27, 28, 33, 41, 42, 44, 45, 50	NC		No Connect. These pins are not connected internally.
29	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 in power-down mode.
30	ELPF	I	The recommended external loop filter must be connected to the ELPF pin, as shown in Figure 58.
31	PVDD	P	PLL Supply Voltage (1.8 V).
32, 37, 43	AGND	G	Analog Ground.
34	TEST_0	I	This pin must be tied to DGND.
35, 36, 46 to 49	$A_{IN}1$ to $A_{IN}6$	I	Analog Video Input Channels.
38	VREFP	O	Internal Voltage Reference Output. See Figure 58 for recommended output circuitry.

Pin No.	Mnemonic	Type	Description
39	VREFN	O	Internal Voltage Reference Output. See Figure 58 for recommended output circuitry.
40	AVDD	P	Analog Supply Voltage (1.8 V).
51	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
52	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
53	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
54	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
63	FIELD	O	Field Synchronization Output Signal.
64	VS	O	Vertical Synchronization Output Signal.

48-LEAD LQFP

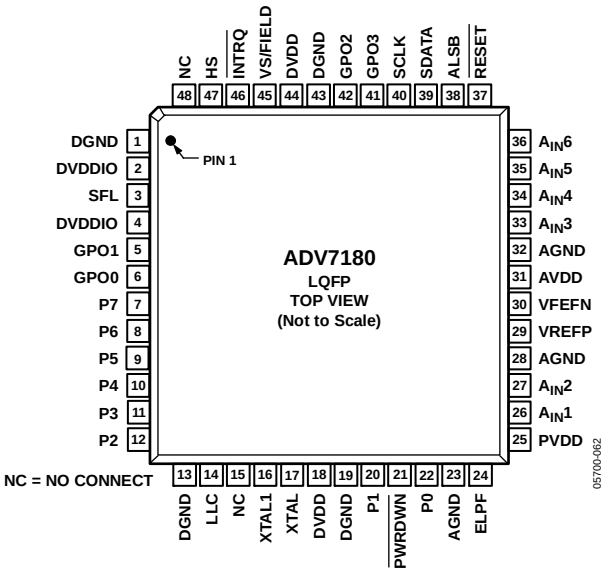


Figure 11. 48-Lead LQFP Pin Configuration

Table 12. 48-Lead LQFP Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 13, 19, 43	DGND	G	Digital Ground.
2, 4	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
3	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
5, 6, 41, 42	GPO0 to GPO3	O	General-Purpose Outputs. These pins can be configured via I^2C to allow control of external devices.
7 to 12, 20, 22	P7 to P2, P1, P0	O	Video Pixel Output Port. See Table 100 for output configuration for 8-bit and 16-bit modes.
14	LLC	O	This is a line-locked output clock for the pixel data output by the ADV7180. It is nominally 27 MHz but varies up or down according to video line length.
15, 48	NC		No Connect Pins. These pins are not connected internally.
16	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the ADV7180. In crystal mode, the crystal must be a fundamental crystal.
17	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or this pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
18, 44	DVDD	P	Digital Supply Voltage (1.8 V).
21	$\overline{\text{PWRDWN}}$	I	A logic low on this pin places the ADV7180 in power-down mode.
23, 28, 32	AGND	G	Analog Ground.
24	ELPF	I	The recommended external loop filter must be connected to the ELPF pin, as shown in Figure 59.
25	PVDD	P	PLL Supply Voltage (1.8 V).
26, 27, 33 to 36	$A_{IN}1$ to $A_{IN}6$	I	Analog Video Input Channels.
29	VREFP	O	Internal Voltage Reference Output. See Figure 59 for recommended output circuitry.
30	VREFN	O	Internal Voltage Reference Output. See Figure 59 for recommended output circuitry.
31	AVDD	P	Analog Supply Voltage (1.8 V).
37	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7180 circuitry.
38	ALSB	I	This pin selects the I^2C address for the ADV7180. For ALSB set to Logic 0, the address selected for a write is Address 0x40; for ALSB set to Logic 1, the address selected is Address 0x42.
39	SDATA	I/O	I^2C Port Serial Data Input/Output Pin.
40	SCLK	I	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
45	VS/FIELD	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal.
46	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video (see Table 108).
47	HS	O	Horizontal Synchronization Output Signal.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The power-up sequence for the ADV7180 is to power up all power supplies simultaneously. If this is not possible, the 3.3 V supply (D_{VDDIO}) must be established first. When the 3.3 V supply is stable, power up the 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}) as quickly as possible. Until the 1.8 V supplies are fully established, all digital pins are in an undefined state.

During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

Take care to ensure that a lower rated supply does not go above a higher rated supply. For example, the 3.3 V D_{VDDIO} supply must never drop below a 1.8 V supply such as the D_{VDD}, P_{VDD}, or A_{VDD}.

To power up the ADV7180, follow these steps.

1. Assert the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin (that is, pull the pins low.)
2. Power up the 3.3 V supply (D_{VDDIO}) and 1.8 V supplies (D_{VDD}, P_{VDD}, and A_{VDD}) simultaneously.[1, 2]
3. When all supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high. Note that this step can be ignored on the 32-lead LFCSP, as the $\overline{\text{PWRDWN}}$ pin is not available.
4. Wait 5 ms, then pull the $\overline{\text{RESET}}$ pin high.
5. When all power supplies, the $\overline{\text{PWRDWN}}$ pin, and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7180.

POWER-DOWN SEQUENCE

The ADV7180 supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY

The ADV7180 can operate with a D_{VDDIO} supply at a nominal value of 1.8 V. Therefore, it is possible to power up all the supplies for the ADV7180 (D_{VDD}, A_{VDD}, P_{VDD}, and D_{VDDIO}) to 1.8 V.

When D_{VDDIO} is at a nominal value of 1.8 V, power up the ADV7180 in the following manner:

1. Follow the power-up sequence described in the Power-Up Sequence section, but power up the D_{VDDIO} supply to 1.8 V instead of 3.3 V. In addition, power up the $\overline{\text{PWRDWN}}$ pin and the $\overline{\text{RESET}}$ pin to 1.8 V instead of 3.3 V.
2. Set the drive strengths of the digital outputs of the ADV7180 to their maximum setting. See the Global Pin Control section.
3. Connect any pull-up resistors connected to pins on the ADV7180, such as the SCLK pin and the SDATA pin, to 1.8 V, rather than 3.3 V.

[1] If it is not possible to power up the D_{VDDIO} and 1.8 V supplies simultaneously, the D_{VDDIO} supply must be powered up first. When the D_{VDDIO} is stable, power up the 1.8 V supplies as quickly as possible.
[2] During power-up, take care to ensure that the D_{VDDIO} supply never drops below any of the 1.8 V supplies.

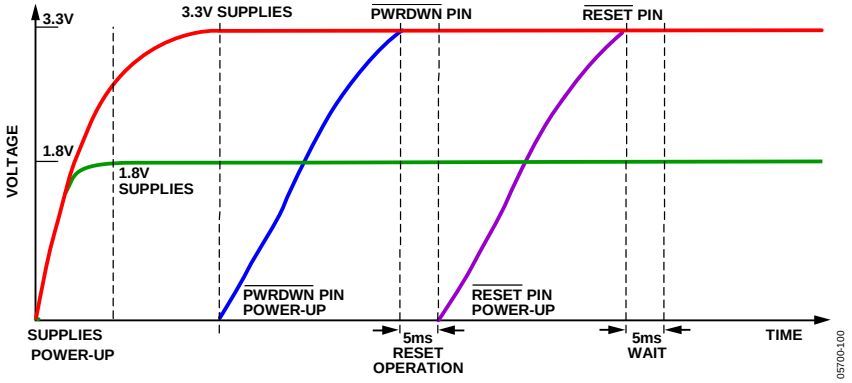


Figure 12. Power-Up Sequence of the 40-Lead LFCSP, 48-Lead LQFP, and 64-Lead LQFP

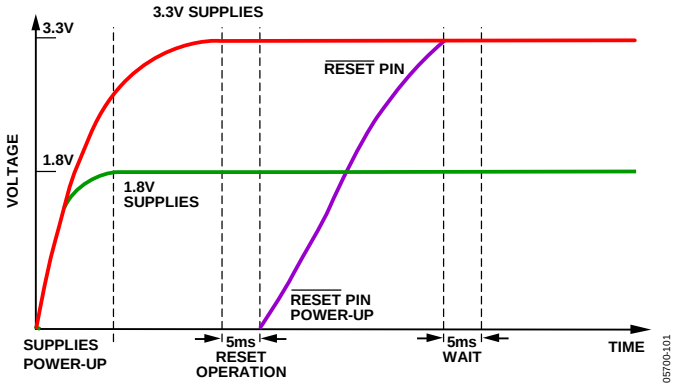


Figure 13. Power-Up Sequence of the 32-Lead LFCSP

ANALOG FRONT END

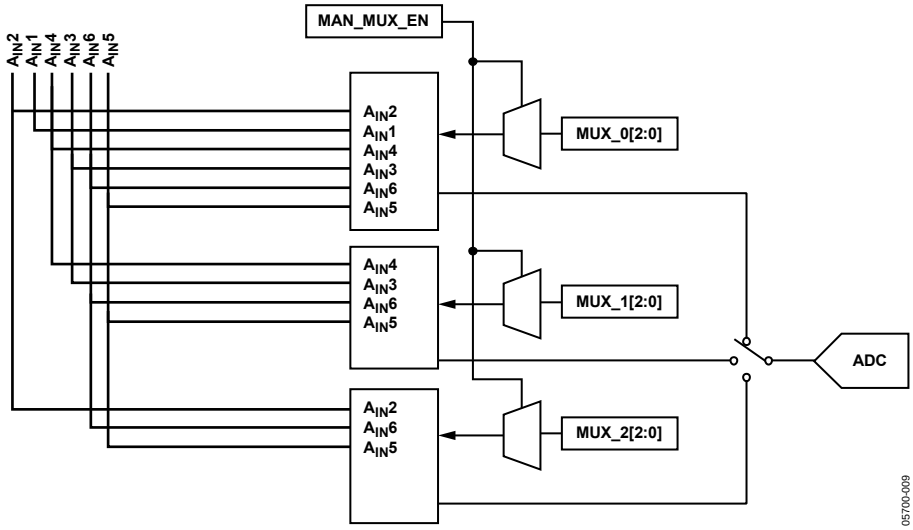


Figure 14. 64-Lead and 48-Lead LQFP Internal Pin Connections

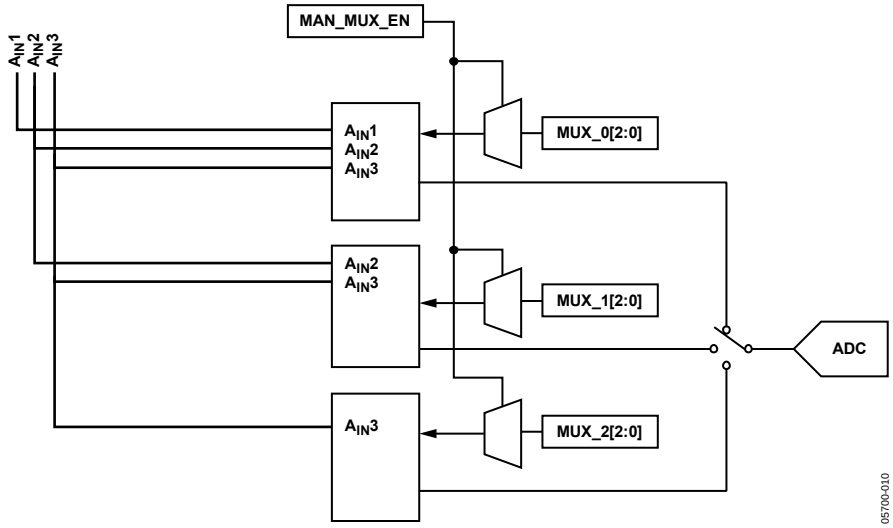


Figure 15. 40-Lead and 32-Lead LFCSP Internal Pin Connections

INPUT CONFIGURATION

The following are the two key steps for configuring the ADV7180 to correctly decode the input video:

1. Use INSEL[3:0] to configure the routing and format decoding (CVBS, Y/C, or YPrPb). For the 64-lead and 48-lead LQFP, see Table 13. For the 40-lead and 32-lead LFCSP, see Table 14.
2. If the input requirements are not met using the INSEL[3:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. The standard definition processor block, which decodes the digital data, must be configured to process the CVBS, Y/C, or YPrPb format. This is performed by INSEL[3:0] selection.

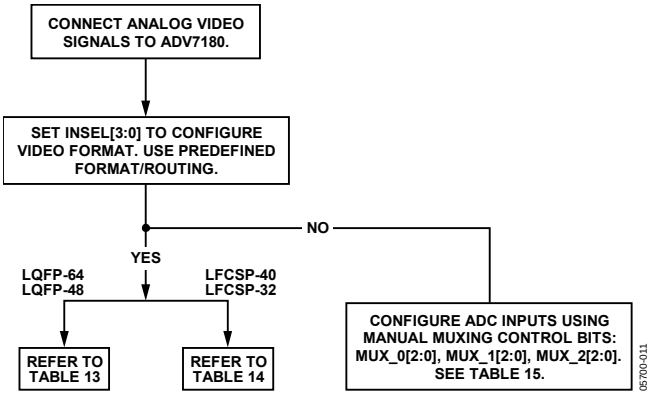


Figure 16. Signal Routing Options

INSEL[3:0], Input Selection, Address 0x00[3:0]

The INSEL bits allow the user to select the input format. They also configure the standard definition processor core to process composite (CVBS), S-Video (Y/C), or component (YPrPb) format.

INSEL[3:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 13 and Table 14). This allows the user to route the various video signal types to the decoder and select them using INSEL[3:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 13. 64-Lead and 48-Lead LQFP INSEL[3:0]

INSEL[3:0]	Video Format	Analog Input
0000	Composite	CVBS input on $A_{IN}1$
0001	Composite	CVBS input on $A_{IN}2$
0010	Composite	CVBS input on $A_{IN}3$
0011	Composite	CVBS input on $A_{IN}4$
0100	Composite	CVBS input on $A_{IN}5$
0101	Composite	CVBS input on $A_{IN}6$
0110	Y/C (S-Video)	Y input on $A_{IN}1$
		C input on $A_{IN}4$
0111	Y/C (S-Video)	Y input on $A_{IN}2$
		C input on $A_{IN}5$
1000	Y/C (S-Video)	Y input on $A_{IN}3$
		C input on $A_{IN}6$
1001	YPrPb	Y input on $A_{IN}1$
		Pb input on $A_{IN}4$
		Pr input on $A_{IN}5$
1010	YPrPb	Y input on $A_{IN}2$
		Pr input on $A_{IN}6$
		Pb input on $A_{IN}3$
1011 to 1111	Reserved	Reserved

Table 14. 40-Lead and 32-Lead LFCSP INSEL[3:0]

INSEL[3:0]	Video Format	Analog Input
0000	Composite	CVBS input on $A_{IN}1$
0001 to 0010	Reserved	Reserved
0011	Composite	CVBS input on $A_{IN}2$
0100	Composite	CVBS input on $A_{IN}3$
0101	Reserved	Reserved
0110	Y/C (S-Video)	Y input on $A_{IN}1$
		C input on $A_{IN}2$
0111 to 1000	Reserved	Reserved
1001	YPrPb	Y input on $A_{IN}1$
		Pr input on $A_{IN}3$
		Pb input on $A_{IN}2$
1010 to 1111	Reserved	Reserved

ANALOG INPUT MUXING

The ADV7180 has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 14 and Figure 15 outline the overall structure of the input muxing provided in the ADV7180.

A maximum of six CVBS inputs can be connected to and decoded by the 64-lead and 48-lead devices, and a maximum of three CVBS inputs can be connected to and decoded by the 40-lead and 32-lead LFCSP devices. As shown in the Pin Configurations and Function Descriptions section, these analog input pins lie in close proximity to one another, which requires careful design of the printed circuit board (PCB) layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended to connect any unused analog input pins to AGND to act as a shield.

MAN_MUX_EN, Manual Input Muxing Enable, Address 0xC4[7]

To configure the ADV7180 analog muxing section, the user must select the analog input ($A_{IN}1$ to $A_{IN}6$ for the 64-lead LQFP and 48-lead devices or $A_{IN}1$ to $A_{IN}3$ for the 40-lead and 32-lead LFCSP devices) that is to be processed by the ADC. MAN_MUX_EN must be set to 1 to enable the following muxing blocks:

- MUX0[2:0], ADC Mux Configuration, Address 0xC3[2:0]
- MUX1[2:0], ADC Mux Configuration, Address 0xC3[6:4]
- MUX2[2:0], ADC Mux Configuration, Address 0xC4[2:0]

The three mux sections are controlled by the signal buses MUX0/MUX1/MUX2[2:0]. Table 15 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX0. For example, in a Y/C input configuration, MUX0 should be connected to the Y channel and MUX1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers should be powered down (see the description of Register 0x3A in Table 107).

Table 15. Manual Mux Settings for the ADC (MAN_MUX_EN Must be Set to 1)

	ADC Connected To			ADC Connected To			ADC Connected To	
MUX0[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32	MUX1[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32	MUX2[2:0]	LQFP-64 or LQFP-48	LFCSP-40 or LFCSP-32
000	No connect	No connect	000	No connect	No connect	000	No connect	No connect
001	$A_{IN}1$	$A_{IN}1$	001	No connect	No connect	001	No connect	No connect
010	$A_{IN}2$	No connect	010	No connect	No connect	010	$A_{IN}2$	No connect
011	$A_{IN}3$	No connect	011	$A_{IN}3$	No connect	011	No connect	No connect
100	$A_{IN}4$	$A_{IN}2$	100	$A_{IN}4$	$A_{IN}2$	100	No connect	No connect
101	$A_{IN}5$	$A_{IN}3$	101	$A_{IN}5$	$A_{IN}3$	101	$A_{IN}5$	$A_{IN}3$
110	$A_{IN}6$	No connect	110	$A_{IN}6$	No connect	110	$A_{IN}6$	No connect
111	No connect	No connect	111	No connect	No connect	111	No connect	No connect

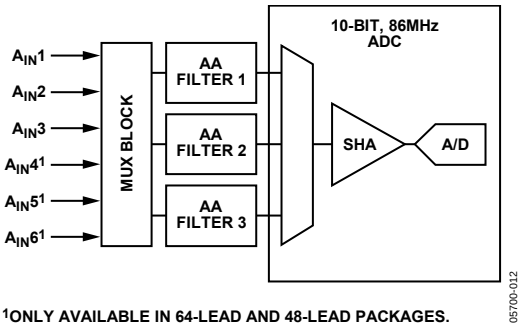
Note the following:

- CVBS can only be processed by MUX0.
- Y/C can only be processed by MUX0 and MUX1.
- YPrPb can only be processed by MUX0, MUX1, and MUX2.

ANTIALIASING FILTERS

The ADV7180 has optional on-chip antialiasing (AA) filters on each of the three channels that are multiplexed to the ADC (see Figure 17). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 18 and Figure 19 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[3:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.



1ONLY AVAILABLE IN 64-LEAD AND 48-LEAD PACKAGES.

Figure 17. Antialias Filter Configuration

AA_FILT_MAN_OVR, Antialiasing Filter Override, Address 0xF3[3]

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[3:0].

AA_FILT_EN, Antialiasing Filter Enable, Address 0xF3[2:0]

These bits allow the user to enable or disable the antialiasing filters on each of the three input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filter and is routed directly to the ADC.

AA_FILT_EN, Address 0xF3[0]

When AA_FILT_EN[0] is 0, AA Filter 1 is bypassed.

When AA_FILT_EN[0] is 1, AA Filter 1 is enabled.

AA_FILT_EN, Address 0xF3[1]

When AA_FILT_EN[1] is 0, AA Filter 2 is bypassed.

When AA_FILT_EN[1] is 1, AA Filter 2 is enabled.

AA_FILT_EN, Address 0xF3[2]

When AA_FILT_EN[2] is 0, AA Filter 3 is bypassed.

When AA_FILT_EN[2] is 1, AA Filter 3 is enabled.

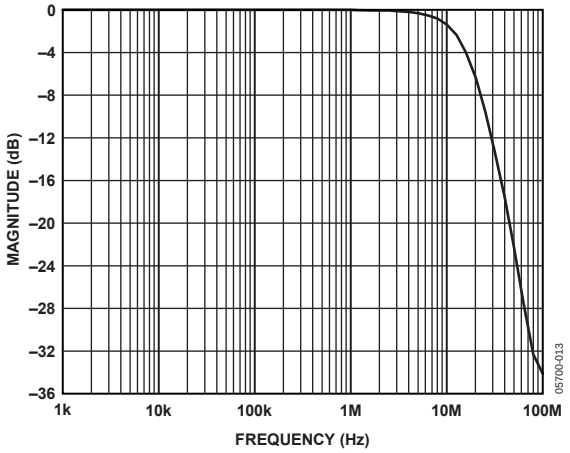


Figure 18. Antialiasing Filter Magnitude Response

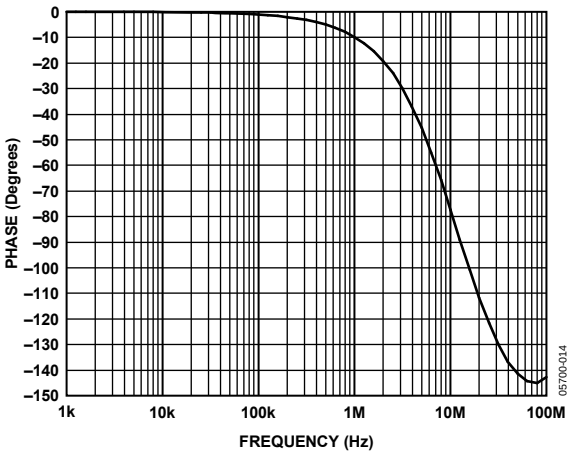


Figure 19. Antialiasing Filter Phase Response

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVING MODES

Power-Down

PDBP, Address 0x0F[2]

The digital supply of the ADV7180 can be shut down by using the $\overline{\text{PWRDWN}}$ pin or via I²C[1] (see the PWRDWN, Address 0x0F[5] section). PDBP controls whether the I²C control or the pin has the higher priority. The default is to give the pin ($\overline{\text{PWRDWN}}$) priority[2]. This allows the user to have the ADV7180 powered down by default at power-up without the need for an I²C write.

When PDBP is 0 (default), the digital supply power is controlled by the $\overline{\text{PWRDWN}}$ pin[2] (the PWRDWN bit, Address 0x0F[5], is disregarded).

When PDBP is 1, the PWRDWN bit has priority (the pin is disregarded).

PWRDWN, Address 0x0F[5]

When PDBP is set to 1, setting the PWRDWN bit switches the ADV7180 to a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No I²C bits are lost during power-down. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I²C interface is unaffected and remains operational in power-down mode.

The ADV7180 leaves the power-down state if the $\overline{\text{PWRDWN}}$ bit is set to 0 (via I²C) or if the ADV7180 is reset using the $\overline{\text{RESET}}$ pin.

PDBP must be set to 1 for the PWRDWN bit to power down the ADV7180.

When PWRDWN is 0 (default), the chip is operational. When PWRDWN is 1, the ADV7180 is in a chip-wide power-down mode.

RESET CONTROL

Reset, Chip Reset, Address 0x0F[7]

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7180, issues a full chip reset. All I²C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register tables (see Table 107 and Table 108). After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the part returns to the default for its primary mode of operation. All I²C bits are loaded with their default values, making this bit self-clearing.

Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I²C writes are performed.

The I²C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the MPU Port Description section).

When the reset bit is 0 (default), operation is normal.

When the reset bit is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Three-State Output Drivers

TOD, Address 0x03[6]

This bit allows the user to three-state the output drivers of the ADV7180.

Upon setting the TOD bit, the P15 to P0 (P7 to P0 for the 48-lead, 40-lead, and 32-lead devices), HS, VS, FIELD (VS/FIELD pin for the 48-lead, 40-lead, and 32-lead LFCSP), and SFL pins are three-stated.

The timing pins (HS, VS, FIELD) can be forced active via the TIM_OE bit. For more information on three-state control, see the Three-State LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TOD is 0 (default), the output drivers are enabled.

When TOD is 1, the output drivers are three-stated.

Three-State LLC Driver

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC pin of the ADV7180 to be three-stated. For more information on three-state control, refer to the Three-State Output Drivers and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_x bits.

When TRI_LLC is 0 (default), the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is 1, the LLC pin drivers are three-stated.

[1] For 32-lead, I²C is the only power-down option.
[2] For 64-lead, 48-lead, and 40-lead only.

Timing Signals Output Enable

TIM_OE, Address 0x04[3]

The TIM_OE bit is regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD into the active state (that is, driving state) even if the TOD bit is set. If TIM_OE is set to low, the HS, VS, and FIELD pins are three-stated depending on the TOD bit. This functionality is beneficial if the decoder is only used as a timing generator. This may be the case if only the timing signals are extracted from an incoming signal or if the part is in free-run mode, where a separate chip can output a company logo, for example.

For more information on three-state control, see the Three-State Output Drivers section and the Three-State LLC Driver section.

Individual drive strength controls are provided via the DR_STR_x bits.

When TIM_OE is 0 (default), HS, VS, and FIELD are three-stated according to the TOD bit.

When TIM_OE is 1, HS, VS, and FIELD are forced active all the time.

Drive Strength Selection (Data)

DR_STR[1:0], Address 0xF4[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[15:0] for the 64-lead device or P[7:0] for the 48-lead, 40-lead, and 32-lead devices output drivers.

Note that DR_STR[1:0] also affects the drive strength of the INTRQ interrupt pin on all ADV7180 models.

For more information on three-state control, see the Drive Strength Selection (Clock) and the Drive Strength Selection (Sync) sections.

Table 16. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Drive Strength Selection (Clock)

DR_STR_C[1:0], Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Sync) and the Drive Strength Selection (Data) sections.

Table 17. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Drive Strength Selection (Sync)

DR_STR_S[1:0], Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and FIELD are driven. For more information, see the Drive Strength Selection (Data) section.

Table 18. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] Not recommended for the optimal performance of the ADV7180.

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN, Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7180 core to an encoder in a decoder/encoder back-to-back arrangement.

When EN_SFL_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

Polarity LLC Pin

PCLK, Address 0x37[0]

The polarity of the clock that leaves the ADV7180 via the LLC pin can be inverted using the PCLK bit.

Changing the polarity of the LLC clock output may be necessary to meet the setup-and-hold time expectations of follow-on chips.

When PCLK is 0, the LLC output polarity is inverted.

When PCLK is 1 (default), the LLC output polarity is normal (see the Timing Specifications section).

GLOBAL STATUS REGISTER

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7180. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV7180.

IDENTIFICATION

IDENT[7:0], Address 0x11[7:0]

This is the register identification of the ADV7180 revision. Table 19 describes the various versions of the ADV7180.

Table 19. IDENT CODE

IDENT[7:0]	Description
0x1B[1]	Initial release silicon
0x1C[1]	Improved ESD and PDC fix
0x1E	48-lead and 32-lead devices only

[1] 64-lead and 40-lead models only.

STATUS 1

Status 1[7:0], Address 0x10[7:0]

This read-only register provides information about the internal status of the ADV7180.

See the CIL[2:0], Count Into Lock, Address 0x51[2:0] section and the COL[2:0], Count Out of Lock, Address 0x51[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the Status Register 0 and Status Register 1 are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable, Address 0x51[7] section.

AUTODETECTION RESULT

AD_RESULT[2:0], Address 0x10[6:4]

The AD_RESULT[2:0] bits report back on the findings from the ADV7180 autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure it.

Table 20. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/G/H/I/D
101	SECAM
110	PAL Combination N
111	SECAM 525

Table 21. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read of this register)
2	FSC_LOCK	f_{SC} locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2

Status 2[7:0], Address 0x12[7:0]

Table 22. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Macrovision color striping
1	MVCS T3	Macrovision color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV PS DET	Detected Macrovision pseudo-sync pulses
3	MV AGC DET	Detected Macrovision AGC pulses
4	LL NSTD	Line length is nonstandard
5	FSC NSTD	f_{SC} frequency is nonstandard
6	Reserved	
7	Reserved	

STATUS 3

Status 3[7:0], Address 0x13[7:0]

Table 23. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	GEMD	Gemstar detect
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved for future use
4	FREE_RUN_ACT	ADV7180 outputs a blue screen (see the DEF_VAL_EN, Default Value Enable, Address 0x0C[0] section)
5	STD FLD LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

VIDEO PROCESSOR

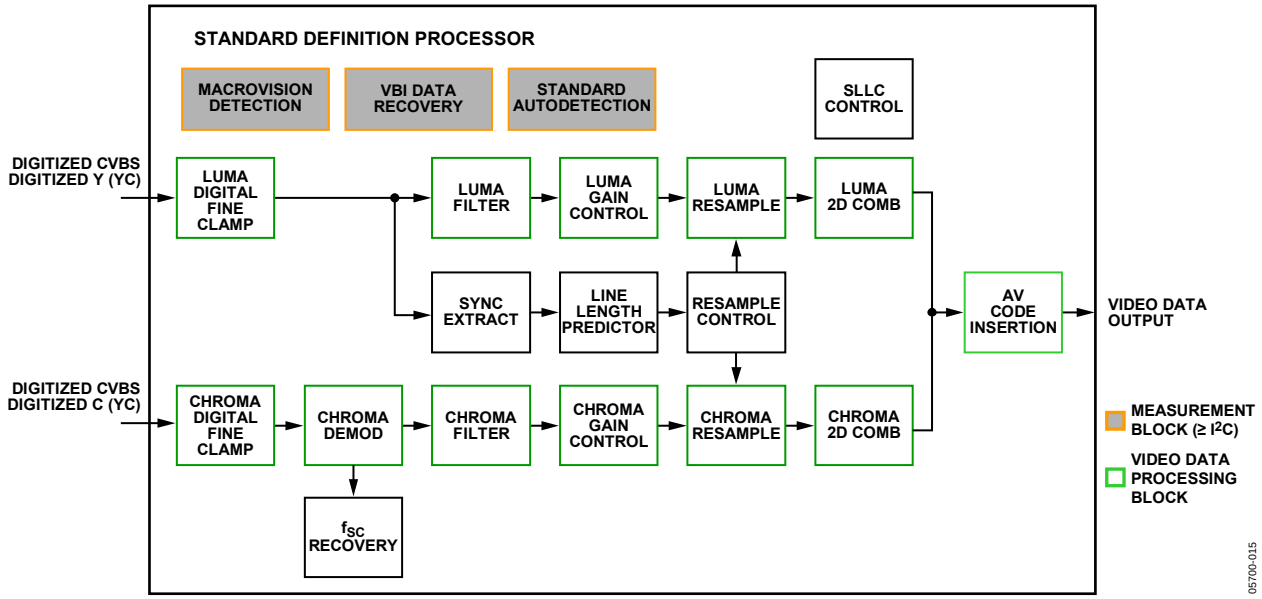


Figure 20. Block Diagram of the Video Processor

Figure 20 shows a block diagram of the ADV7180 video processor. The ADV7180 can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

SD LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma gain control. The automatic gain control (AGC) can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct for line length errors as well as dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted (as per ITU-R BT.656).

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, superadaptive comb filter provides high quality Y/C separation in case the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted (as per ITU-R BT.656).

SYNC PROCESSING

The ADV7180 extracts syncs embedded in the analog input video signal. There is currently no support for external HS/VS inputs. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure that the ADV7180 outputs 720 active pixels per line.

The sync processing on the ADV7180 also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSYNC processor. This block provides extra filtering of the detected VSYNCs to improve vertical lock.
- HSYNC processor. The HSYNC processor is designed to filter incoming HSYNCs that have been corrupted by noise, providing much improved performance for video signals with a stable time base but poor SNR.

VBI DATA RECOVERY

The ADV7180 can retrieve the following information from the input video:

- Wide screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed captioning (CCAP)
- Macrovision protection presence
- EDTV data
- Gemstar-compatible data slicing
- Teletext
- VITC/VPS

The ADV7180 is also capable of automatically detecting the incoming video standard with respect to

- Color subcarrier frequency
- Field rate
- Line rate

The ADV7180 can configure itself to support PAL B/D/I/G/H, PAL M, PAL N, PAL Combination N, NTSC M, NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x00[7:4]) allow the user to force the digital core into a specific video standard. Under normal circumstances, this is not necessary. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Autodetection of SD Modes

To guide the autodetect system of the ADV7180, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x00[7:4]

Table 24. VID_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect (PAL B/G/H/I/D), NTSC J (no pedestal), SECAM
0001	Autodetect (PAL B/G/H/I/D), NTSC M (pedestal), SECAM
0010	Autodetect (PAL N) (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect (PAL N) (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/G/H/I/D
1001	PAL N = PAL B/G/H/I/D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM (with pedestal)

AD_SEC525_EN, Enable Autodetection of SECAM 525 Line Video, Address 0x07[7]

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM-modulated color component.

AD_SECAM_EN, Enable Autodetection of SECAM, Address 0x07[6]

Setting AD_SECAM_EN to 0 (default) disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 enables the detection of SECAM.

AD_N443_EN, Enable Autodetection of NTSC 4.43, Address 0x07[5]

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, Enable Autodetection of PAL 60, Address 0x07[4]

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, Enable Autodetection of PAL N, Address 0x07[3]

Setting AD_PALN_EN to 0 (default) disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 enables the detection of the PAL N standard.

AD_PALM_EN, Enable Autodetection of PAL M, Address 0x07[2]

Setting AD_PALM_EN to 0 (default) disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 enables the detection of PAL M.

AD_NTSC_EN, Enable Autodetection of NTSC, Address 0x07[1]

Setting AD_NTSC_EN to 0 (default) disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 enables the detection of standard NTSC.

AD_PAL_EN, Enable Autodetection of PAL B/D/I/G/H, Address 0x07[0]

Setting AD_PAL_EN to 0 (default) disables the detection of standard PAL.

Setting AD_PAL_EN to 1 enables the detection of standard PAL.

SFL_INV, Subcarrier Frequency Lock Inversion

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems.

First, the PAL switch bit is only meaningful in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

Second, there was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (genlock telegram) bit directly, whereas the newer ones invert the bit prior to using it. The reason for this is that the inversion compensated for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the ADV717x and ADV73xx encoders, the PAL switch bit in the SFL (genlock telegram) must be 0 for NTSC to work. For the ADV7194 video encoder, the PAL switch bit in the SFL must be 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

SFL_INV, Subcarrier Frequency Lock Inversion, Address 0x41[6]

Setting SFL_INV to 0 (default) makes the part SFL compatible with the ADV717x and ADV73xx video encoders.

Setting SFL_INV to 1 makes the part SFL compatible with the ADV7194 video encoder.

Lock Related Controls

Lock information is presented to the user through Bits[1:0] of the Status 1 register (see the Status 1[7:0], Address 0x10[7:0] section). Figure 21 outlines the signal flow and the controls available to influence the way the lock status information is generated.

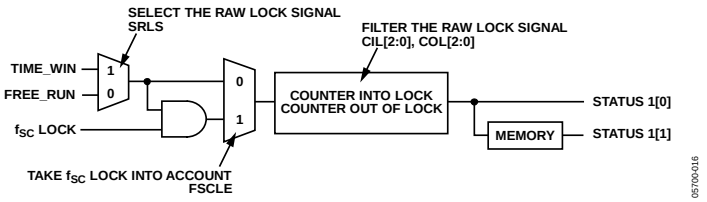


Figure 21. Lock Related Signal Path

SRLS, Select Raw Lock Signal, Address 0x51[6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register). See Figure 21.

- The TIME_WIN signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE_RUN signal.

Setting SRLS to 1 selects the TIME_WIN signal.

FSCLE, f_{SC} Lock Enable, Address 0x51[7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7180 in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is set to 0 (default), only the overall lock status is dependent on horizontal sync lock.

When FSCLE is set to 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

CIL[2:0], Count Into Lock, Address 0x51[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Status 1[1:0]. The bit counts the value in lines of video.

Table 25. CIL Function

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COL[2:0], Count Out of Lock, Address 0x51[5:3]

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into the unlocked state and reports this via Status 1[1:0]. It counts the value in lines of video.

Table 26. COL Function

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROLS

These registers allow the user to control picture appearance, including control of the active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Contrast Adjust, Address 0x08[7:0]

This register allows the user to control contrast adjustment of the picture.

Table 27. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0], SD Saturation Cb Channel, Address 0xE3[7:0]

This register allows the user to control the gain of the Cb channel only, which in turn adjusts the saturation of the picture.

Table 28. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0], SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only, which in turn adjusts the saturation of the picture.

Table 29. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cr channel = −42 dB
0xFF	Gain on Cr channel = +6 dB

SD_OFF_Cb[7:0], SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 30. SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 mV offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0], SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 31. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 mV offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0], Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 32. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = −30 IRE

HUE[7:0], Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM-modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 33. HUE Function

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0], Default Value Y, Address 0x0C[7:2]

When the ADV7180 loses lock on the incoming video signal or when there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF_VAL_AUTO_EN bit is set to high and the ADV7180 has lost lock to the input video signal. This is the intended mode of operation (automatic mode).
- The DEF_VAL_EN bit is set, regardless of the lock status of the video decoder. This is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = {DEF_Y[5:0], 0, 0}.

For DEF_Y[5:0], 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

DEF_C[7:0], Default Value C, Address 0x0D[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7180 cannot lock to the input video (automatic mode).
- DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7180 for the chroma side is Cr[3:0] = {DEF_C[7:4], 0, 0, 0, 0}, and Cb[3:0] = {DEF_C[3:0], 0, 0, 0, 0}.

For DEF_C[7:0], 0x7C (blue) is the default value for Cr and Cb.

DEF_VAL_EN, Default Value Enable, Address 0x0C[0]

This bit forces the use of the default values for Y, Cr, and Cb. See the descriptions in the DEF_Y[5:0], Default Value Y, Address 0x0C[7:2] and DEF_C[7:0], Default Value C, Address 0x0D[7:0] sections for additional information. In this mode, the decoder also outputs a stable 27 MHz clock, HS, and VS.

Setting DEF_VAL_EN to 0 (default) outputs a colored screen determined by user-programmable Y, Cr, and Cb values when the decoder free-runs. Free-run mode is turned on and off by the DEF_VAL_AUTO_EN bit.

Setting DEF_VAL_EN to 1 forces a colored screen output determined by user-programmable Y, Cr, and Cb values. This overrides picture data even if the decoder is locked.

DEF_VAL_AUTO_EN, Default Value Automatic Enable, Address 0x0C[1]

This bit enables the automatic use of the default values for Y, Cr, and Cb when the ADV7180 cannot lock to the video signal.

Setting DEF_VAL_AUTO_EN to 0 disables free-run mode. If the decoder is unlocked, it outputs noise.

Setting DEF_VAL_EN to 1 (default) enables free-run mode, and a colored screen set by user-programmable Y, Cr, and Cb values is displayed when the decoder loses lock.

CLAMP OPERATION

The input video is ac-coupled into the ADV7180. Therefore, its dc value needs to be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7180 and shows the different ways in which a user can configure its behavior.

The ADV7180 uses a combination of current sources and a digital processing block for clamping, as shown in Figure 22. The analog processing channel shown is replicated three times inside the IC. While only one single channel is needed for a CVBS signal, two independent channels are needed for Y/C (SVHS) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections:

- Clamping before the ADC (analog domain): current sources.
- Clamping after the ADC (digital domain): digital processing block.

The ADC can digitize an input signal only if it resides within the ADC 1.0 V input voltage range. An input signal with a dc level that is too large or too small is clipped at the top or bottom of the ADC range.

The primary task of the analog clamping circuits is to ensure that the video signal stays within the valid ADC input window so that the analog-to-digital conversion can take place. It is not necessary to clamp the input signal with a very high accuracy in the analog domain as long as the video signal fits within the ADC range.

After digitization, the digital fine clamp block corrects for any remaining variations in dc level. Because the dc level of an input video signal refers directly to the brightness of the picture transmitted, it is important to perform a fine clamp with high accuracy; otherwise, brightness variations may occur. Furthermore, dynamic changes in the dc level almost certainly lead to visually objectionable artifacts and must, therefore, be prohibited.

The clamping scheme has to complete two tasks. It must acquire a newly connected video signal with a completely unknown dc level, and it must maintain the dc level during normal operation.

To acquire an unknown video signal quickly, the large current clamps must be activated. It is assumed that the amplitude of the video signal at this point is of a nominal value. Control of the coarse and fine current clamp parameters is performed automatically by the decoder.

Standard definition video signals may have excessive noise on them. In particular, CVBS signals transmitted by terrestrial broadcast and demodulated using a tuner usually show very large levels of noise (>100 mV). A voltage clamp is unsuitable for this type of video signal. Instead, the ADV7180 employs a set of four current sources that can cause coarse (>0.5 mA) and fine (<0.1 mA) currents to flow into and away from the high impedance node that carries the video signal (see Figure 22).

The following sections describe the I²C signals that can be used to influence the behavior of the clamping block.

CCLEN, Current Clamp Enable, Address 0x14[4]

The current clamp enable bit allows the user to switch off the current sources in the analog front end altogether. This may be useful if the incoming analog video signal is clamped externally.

When CCLEN is 0, the current sources are switched off.

When CCLEN is 1 (default), the current sources are enabled.

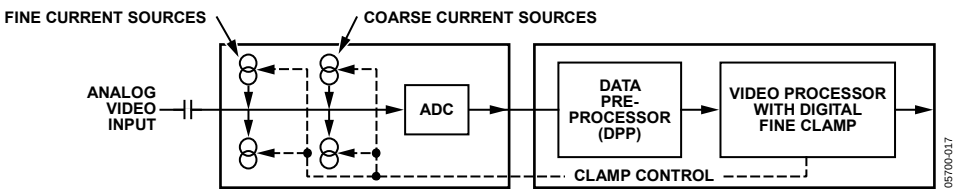


Figure 22. Clamping Overview

DCT[1:0], Digital Clamp Timing, Address 0x15[6:5]

The clamp timing register determines the time constant of the digital fine clamp circuitry. It is important to note that the digital fine clamp reacts quickly because it immediately corrects any residual dc level error for the active line. The time constant from the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 34. DCT Function

DCT[1:0]	Description
00 (default)	Slow (TC = 1 sec)
01	Medium (TC = 0.5 sec)
10	Fast (TC = 0.1 sec)
11	Determined by ADV7180, depending on the input video parameters

DCFE, Digital Clamp Freeze Enable, Address 0x15[4]

This register bit allows the user to freeze the digital clamp loop at any time. It is intended for users who want to do their own clamping. To do this, disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is 0 (default), the digital clamp is operational.

When DCFE is 1, the digital clamp loop is frozen.

LUMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. Note that the data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

- Luma antialias filter (YAA). The ADV7180 receives video at a rate of 28.6363 MHz. (In the case of 4× oversampled video, the ADC samples at 57.27 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the ADV7180 is always 28.6363 MHz.) The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality linear phase, low-pass filter that preserves the luma signal while at the same time attenuating out-of-band components. The luma antialias filter (YAA) has a fixed response.
- Luma shaping filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can be used to selectively reduce the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. A follow-on video compression stage may work more efficiently if the video is low-pass filtered.
  The ADV7180 has two responses for the shaping filter: one that is used for good quality composite, component, and SVHS type sources, and a second for nonstandard CVBS signals.
  The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 24 through Figure 27 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. Y/C separation must aim for best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV7180. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (fSC). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship may be disturbed, and the comb filters may not be able to remove all crosstalk artifacts in the best fashion without the assistance of the shaping filter block.

An automatic mode is provided that allows the ADV7180 to evaluate the quality of the incoming video signal and select the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has three control registers.

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (depending on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality composite (CVBS), component (YPrPb), and SVHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources (because they can be successfully combed) as well as for luma components of YPrPb and Y/C sources (because they need not be combed). For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 23.

YSFM[4:0], Y Shaping Filter Mode, Address 0x17[4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter selection is based on other register selections, such as detected video standard, as well as properties extracted from the incoming video itself, such as quality and time base stability. The automatic selection always selects the widest possible bandwidth for the video input encountered.

The Y-shaping filter mode operates as follows:

- If the YSFM settings specify a filter (that is, YSFM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wideband filters are used.

WYSFMOVR, Wideband Y Shaping Filter Override, Address 0x18[7]

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information on luma shaping filters, see the Y Shaping Filter section and the flowchart shown in Figure 23.

When WYSFMOVR is 0, the shaping filter for good quality video signals is selected automatically.

Setting WYSFMOVR to 1 (default) enables manual override via WYSFM[4:0].

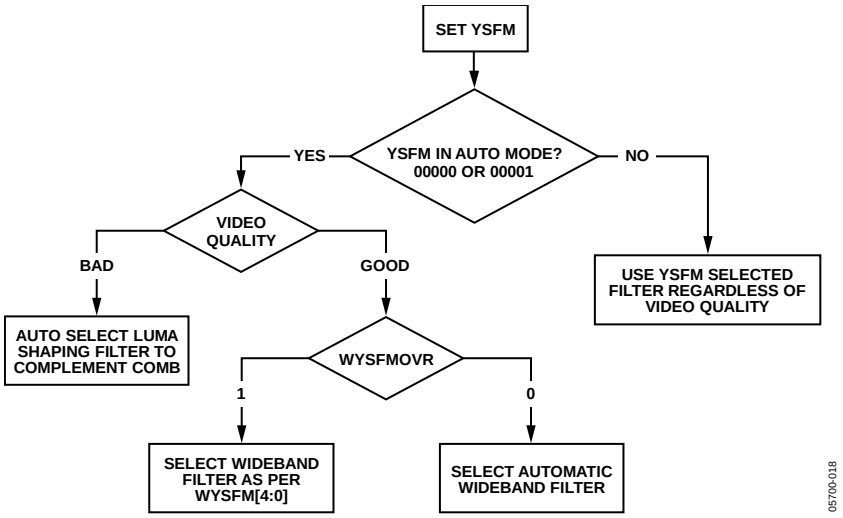


Figure 23. YSFM and WYSFM Control Flowchart

Table 35. YSFM Function

YSFM[4:0]	Description
00000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
00001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011	SVHS 18 (CCIR 601)
10100	PAL NN1
10101	PAL NN2
10110	PAL NN3
10111	PAL WN1
11000	PAL WN2
11001	NTSC NN1
11010	NTSC NN2
11011	NTSC NN3
11100	NTSC WN1
11101	NTSC WN2
11110	NTSC WN3
11111	Reserved

WYSFM[4:0], Wideband Y Shaping Filter Mode, Address 0x18[4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, for example, CVBS with stable time base, luma component of YPrPb, and luma component of Y/C. The WYSFM bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 36. WYSFM Function

WYSFM[4:0]	Description
00000	Do not use
00001	Do not use
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011 (default)	SVHS 18 (CCIR 601)
10100 to 11111	Do not use

The filter plots in Figure 24 show the SVHS 1 (narrowest) to SVHS 18 (widest) shaping filter settings. Figure 26 shows the PAL notch filter responses. The NTSC-compatible notches are shown in Figure 27.

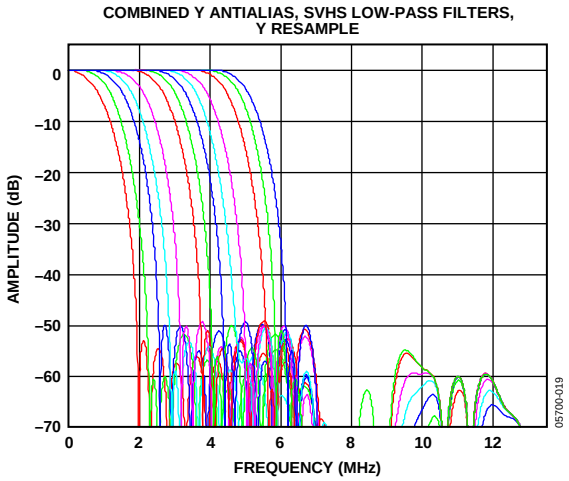


Figure 24. Y SVHS Combined Responses

CHROMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. Note that the data format at this point is CVBS for CVBS inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

- Chroma antialias filter (CAA). The ADV7180 oversamples the CVBS by a factor of 4 and the chroma/YPrPb by a factor of 2. A decimating filter (CAA) is used to preserve the active video band and to remove any out-of-band components. The CAA filter has a fixed response.
- Chroma shaping filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

Figure 28 shows the overall response of all filters together.

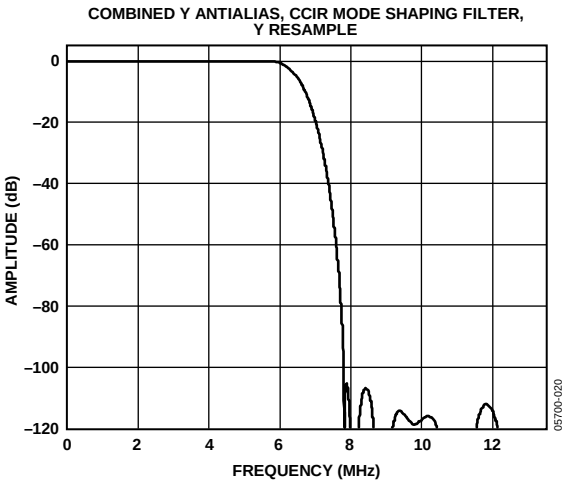


Figure 25. Combined Y Antialias, CCIR Mode Shaping Filter

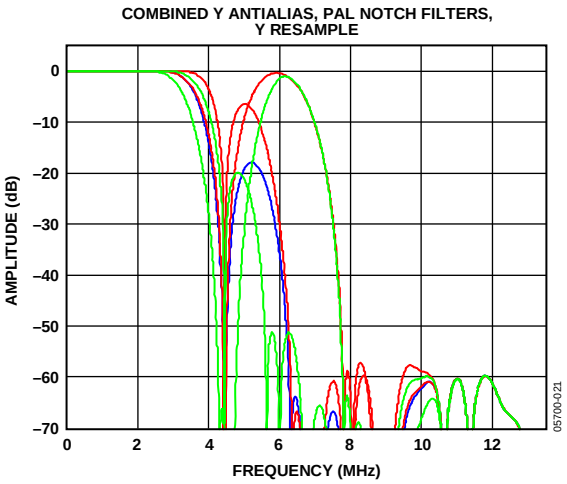


Figure 26. Combined Y Antialias, PAL Notch Filters

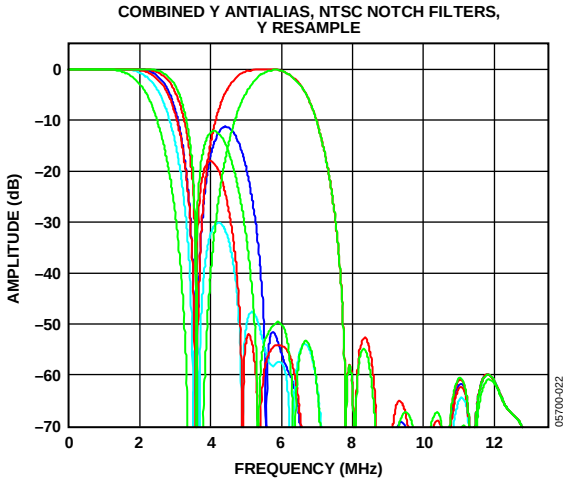


Figure 27. Combined Y Antialias Filter, NTSC Notch Filters

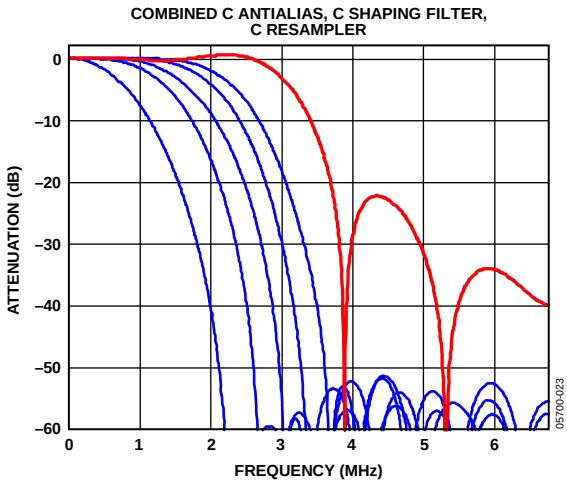


Figure 28. Chroma Shaping Filter Responses

CSFM[2:0], C Shaping Filter Mode, Address 0x17[7:5]

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see Setting 000 and Setting 001 in Table 37).

Table 37. CSFM Function

CSFM[2:0]	Description
000 (default)	Autoselection 1.5 MHz bandwidth
001	Autoselection 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

Figure 28 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode (shown in red).

GAIN OPERATION

The gain control within the ADV7180 is done on a purely digital basis. The input ADC supports a 10-bit range mapped into a 1.0 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

Advantages of this architecture over the commonly used programmable gain amplifier (PGA) before the ADC include the fact that the gain is now completely independent of supply, temperature, and process variations.

As shown in Figure 30, the ADV7180 can decode a video signal as long as it fits into the ADC window. The components for this are the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

Figure 29 shows a typical voltage divider network that is required to keep the input video signal within the allowed range of the ADC, 0 V to 1 V. Place this circuit before all analog inputs to the ADV7180.

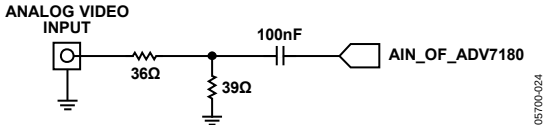


Figure 29. Input Voltage Divider Network

The minimum supported amplitude of the input video is determined by the ability of the ADV7180 to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are separate gain control units for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are shown in Table 38.

Table 38. AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color-burst amplitude taken from luma path
	Peak white	Dependent on color-burst amplitude taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color-burst amplitude taken from luma path
	Peak white	Dependent on color-burst amplitude
YPrPb	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops. This causes the loops to stop updating and the AGC determined gain at the time of the freeze to stay active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual-function manual gain registers, LG[11:0] luma gain and CG[11:0] chroma gain, in the Luma Gain and Chroma Gain sections.

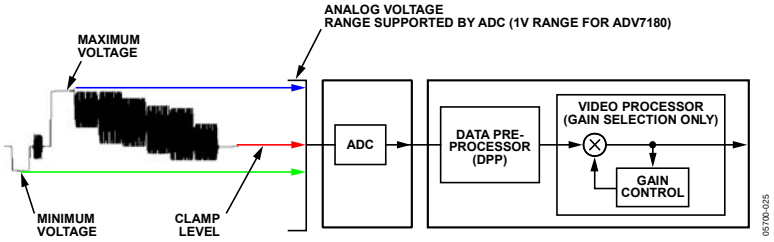


Figure 30. Gain Control Overview

Luma Gain

LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4]

The luma automatic gain control mode bits select the operating mode for the gain control in the luma path.

Table 39. LAGC Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip), peak white algorithm off
010 (default)	AGC (blank level to sync tip), peak white algorithm on
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0], Luma Automatic Gain Timing, Address 0x2F[7:6]

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. This register only has an effect if the LAGC[2:0] register is set to 001 or 010 (automatic gain control modes).

If peak white AGC is enabled and active (see the Status 1[7:0], Address 0x10[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white AGC, LAGT becomes relevant again.

Table 40. LAGT Function

LAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11 (default)	Adaptive

LG[11:0], Luma Gain, Address 0x2F[3:0], Address 0x30[7:0]

LMG[11:0], Luma Manual Gain, Address 0x2F[3:0], Address 0x30[7:0]

Luma gain[11:0] is a dual-function register. If all of these registers are written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the LAGC[2:0] bits, the value is one of the following:

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to any of the automatic modes)

Table 41. LG/LMG Function

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = x	Write	Manual gain for luma path
LG[11:0] = x	Read	Actual used gain

$$Luma\ Gain = \frac{LMG[11:0]}{LumaCalibrationFactor} \quad (1)$$

where *LMG[11:0]* is a decimal value between 1024 and 4095.

Calculation of the Luma Calibration Factor

1. Using a video source, set content to a grey field and apply as a standard CVBS signal to the CVBS input of the board.
2. Using an oscilloscope, measure the signal at CVBS input to ensure that its sync depth, color burst, and luma are at the standard levels.
3. Connect the output parallel pixel bus of the ADV7180 to a backend system that has unity gain and monitor output voltage.
4. Measure the luma level correctly from the black level. Turn off the Luma AGC and manually change the value of the luma gain control register, LMG[11:0], until the output luma level matches the input measured in Step 2.

This value, in decimal, is the luma calibration factor.

BETACAM, Enable Betacam Levels, Address 0x01[5]

If YPrPb data is routed through the ADV7180, the automatic gain control modes can target different video input levels, as outlined in Table 44. The BETACAM bit is valid only if the input mode is YPrPb (component). The BETACAM bit sets the target value for AGC operation.

A review of the following sections is useful:

- The MAN_MUX_EN, Manual Input Muxing Enable, Address 0xC4[7] section for how component video (YPrPb) can be routed through the ADV7180.
- The Video Standard Selection section to select the various standards, for example, with and without pedestal.

The AGC algorithms adjust the levels based on the setting of the BETACAM bit (see Table 42).

PW_UPD, Peak White Update, Address 0x2B[0]

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, see the LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4] section.

Setting PW_UPD to 0 updates the gain once per video line.

Setting PW_UPD to 1 (default) updates the gain once per field.

Chroma Gain

CAGC[1:0], Chroma Automatic Gain Control, Address 0x2C[1:0]

The two bits of color automatic gain control mode select the basic mode of operation for automatic gain control in the chroma path.

Table 42. BETACAM Function

BETACAM	Description
0 (default)	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects MII. Selecting PAL without pedestal selects SMPTE. Selecting NTSC with pedestal selects MII. Selecting NTSC without pedestal selects SMPTE.
1	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects BETACAM. Selecting PAL without pedestal selects BETACAM variant. Selecting NTSC with pedestal selects BETACAM. Selecting NTSC without pedestal selects BETACAM variant.

Table 43. CAGC Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Luma gain used for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

Table 44. BETACAM Levels

Name	BETACAM (mV)	BETACAM Variant (mV)	SMPTE (mV)	MII (mV)
Y	0 to +714 (including 7.5% pedestal)	0 to +714	0 to +700	0 to +700 (including 7.5% pedestal)
Pb and Pr	−467 to +467	−505 to +505	−350 to +350	−324 to +324
Sync Depth	+286	+286	+300	+300

CAGT[1:0], Chroma Automatic Gain Timing, Address 0x2D[7:6]

The chroma automatic gain timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register has an effect only if the CAGC[1:0] register is set to 10 (automatic gain).

Table 45. CAGT Function

CAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Reserved
11 (default)	Adaptive

CG[11:0], Chroma Gain, Address 0x2D[3:0], Address 0x2E[7:0]; CMG[11:0], Chroma Manual Gain, Address 0x2D[3:0], Address 0x2E[7:0]

Chroma gain[11:0] is a dual-function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] function is switched to manual fixed gain. See Equation 2 for calculating a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this is either:

- The chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
- The chroma automatic gain value (CAGC[1:0] set to any of the automatic modes).

Table 46. CG/CMG Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma_Gain \cong \frac{CMG[11:0]_{decimal}}{ChromaCalibrationFactor} \quad (2)$$

where *ChromaCalibrationFactor* is a decimal value between 0 and 4095.

Calculation of the Chroma Calibration Factor

1. Apply a CVBS signal with the color bars/SMPTE bars test pattern content directly to the measurement equipment.
2. Ensure correct termination of 75 Ω on the measurement equipment. Measure chroma output levels.
3. Reconnect the source to the CVBS input of the ADV7180 system that has a backend gain of 1. Repeat the measurement of chroma levels.
4. Turn off the Chroma AGC and manually change the Chroma Gain Control Register CMG[11:0] until the chroma level matches that measured directly from the source.

This value, in decimal, is the chroma calibration factor.

CKE, Color Kill Enable, Address 0x2B[6]

The color kill enable bit allows the optional color kill function to be switched on or off.

For QAM-based video standards (PAL and NTSC) as well as FM-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled and the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Setting CKE to 0 disables color kill.

Setting CKE to 1 (default) enables color kill.

CKILLTHR[2:0], Color Kill Threshold, Address 0x3D[6:4]

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM-based (NTSC and PAL) or FM-modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For Setting 000, Setting 001, Setting 010, and Setting 011, chroma demodulation inside the ADV7180 may not work satisfactorily for poor input video signals.

Table 47. CKILLTHR Function

	Description	
CKILLTHR[2:0]	SECAM	NTSC, PAL
000	No color kill	Kill at <0.5%
001	Kill at <5%	Kill at <1.5%
010	Kill at <7%	Kill at <2.5%
011 (default)	Kill at <8%	Kill at <4%
100	Kill at <9.5%	Kill at <8.5%
101	Kill at <15%	Kill at <16%
110	Kill at <32%	Kill at <32%
111	Reserved for Analog Devices internal use only; do not select	

CHROMA TRANSIENT IMPROVEMENT (CTI)

The signal bandwidth allocated for chroma is typically much smaller than that for luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, may lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 31). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than that of the chroma component. The color edge is not sharp and can be blurred, in the worst case, over several pixels.

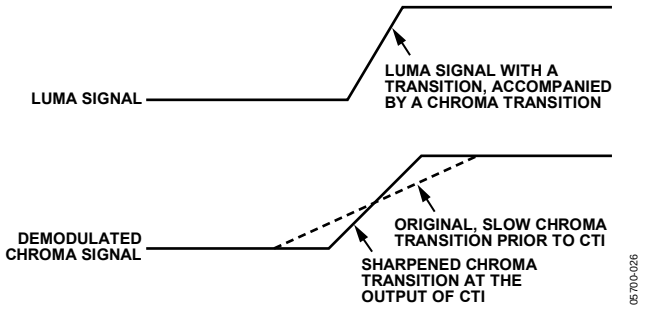


Figure 31. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to create steeper chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure that noise is not emphasized. Care has also been taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that have severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN, Chroma Transient Improvement Enable, Address 0x4D[0]

Setting CTI_EN to 0 disables the CTI block.

Setting CTI_EN to 1 (default) enables the CTI block.

CTI_AB_EN, Chroma Transient Improvement Alpha Blend Enable, Address 0x4D[1]

The CTI_AB_EN bit enables an alpha blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI_EN bit.

Setting CTI_AB_EN to 0 disables the CTI alpha blender.

Setting CTI_AB_EN to 1 (default) enables the CTI alpha-blend mixing function.

CTI_AB[1:0], Chroma Transient Improvement Alpha Blend, Address 0x4D[3:2]

The CTI_AB[1:0] controls the behavior of alpha blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become active, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture but may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 48. CTI_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 (default)	Smoothest alpha blend function

CTI_C_TH[7:0], CTI Chroma Threshold, Address 0x4E[7:0]

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition must be to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI_C_TH[7:0] is 0x08, indicating the threshold for the chroma edges prior to CTI.

DIGITAL NOISE REDUCTION (DNR) AND LUMA PEAKING FILTER

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise and that, therefore, their removal improves picture quality. The following are the two DNR blocks in the ADV7180: the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 32.

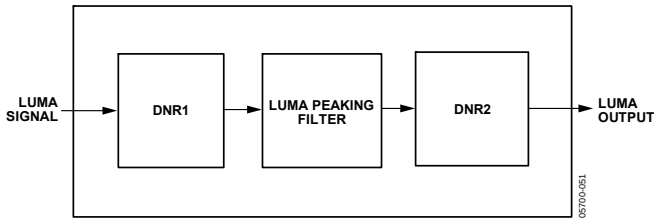


Figure 32. DNR and Peaking Block Diagram

DNR_EN, Digital Noise Reduction Enable, Address 0x4D[5]

The DNR_EN bit enables the DNR block or bypasses it.

Table 49. DNR_EN Function

Setting	Description
0	Bypasses DNR (disable)
1 (default)	Enables digital noise reduction on the luma data

DNR_TH[7:0], DNR Noise Threshold, Address 0x50[7:0]

The DNR1 block is positioned before the luma peaking block. The DNR_TH[7:0] value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 50. DNR_TH[7:0] Function

Setting	Description
0x08 (default)	Threshold for maximum luma edges to be interpreted as noise

PEAKING_GAIN[7:0], Luma Peaking Gain, Address 0xFB[7:0]

This filter can be manually enabled. The user can select to boost or to attenuate the mid region of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the luma data unaltered. A lower value attenuates the signal, and a higher value gains the luma signal. A plot of the responses of the filter is shown in Figure 33.

Table 51. PEAKING_GAIN[7:0] Function

Setting	Description
0x40 (Default)	0 dB response

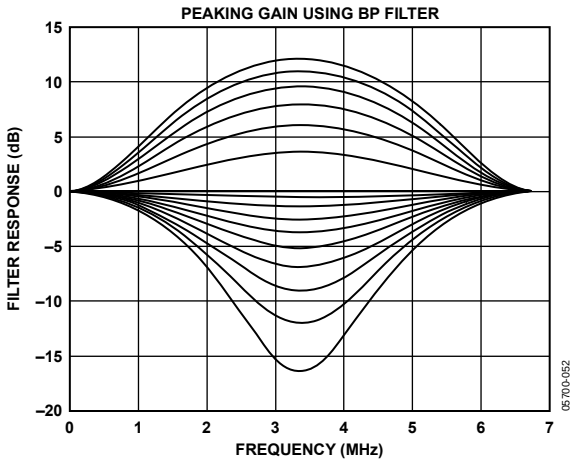


Figure 33. Peaking Filter Responses

DNR_TH2[7:0], DNR Noise Threshold 2, Address 0xFC[7:0]

The DNR2 block is positioned after the luma peaking block and, therefore, affects the gained luma signal. It operates in the same way as the DNR1 block, but there is an independent threshold control, DNR_TH2[7:0], for this block. This value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH2[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 52. DNR_TH2[7:0] Function

Setting	Description
0x04 (default)	Threshold for maximum luma edges to be interpreted as noise

COMB FILTERS

The comb filters of the ADV7180 have been greatly improved to automatically handle video of all types, standards, and levels of quality. The NTSC and PAL configuration registers allow the user to customize the comb filter operation depending on which video standard is detected (by autodetection) or selected (by manual programming).

NTSC Comb Filter Settings

These settings are used for NTSC M/J CVBS inputs.

NSFSEL[1:0], Split Filter Selection NTSC, Address 0x19[3:2]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection results in better performance on diagonal lines but more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Table 53. NSFSEL Function

NSFSEL[1:0]	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

CTAPSN[1:0], Chroma Comb Taps, NTSC, Address 0x38[7:6]

Table 54. CTAPSN Function

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts three lines (three taps) to two lines (two taps)
10 (default)	NTSC chroma comb adapts five lines (five taps) to three lines (three taps)
11	NTSC chroma comb adapts five lines (five taps) to four lines (four taps)

CCMN[2:0], Chroma Comb Mode, NTSC, Address 0x38[5:3]

Table 55. CCMN Function

CCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMN[2:0], Luma Comb Mode NTSC, Address 0x38[2:0]

Table 56. YCMN Function

YCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed two-line (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed three-line (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed two-line (two taps) luma comb

PAL Comb Filter Settings

These settings are used for PAL B/G/H/I/D, PAL M, PAL Combinational N, PAL 60, and NTSC 4.43 CVBS inputs.

PSFSEL[1:0], Split Filter Selection, PAL, Address 0x19[1:0]

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 57. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

CTAPSP[1:0], Chroma Comb Taps PAL, Address 0x39[7:6]

Table 58. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use.
01	PAL chroma comb adapts five lines (three taps) to three lines (two taps); cancels cross luma only
10	PAL chroma comb adapts five lines (five taps) to three lines (three taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts five lines (five taps) to four lines (four taps); cancels cross luma and hue error well

CCMP[2:0], Chroma Comb Mode PAL, Address 0x39[5:3]

Table 59. CCMP Function

CCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMP[2:0], Luma Comb Mode PAL, Address 0x39[2:0]

Table 60. YCMP Function

YCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive five lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed three lines (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed five lines (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed three lines (two taps) luma comb

IF FILTER COMPENSATION

IFFILTSEL[2:0], IF Filter Select, Address 0xF8[2:0]

The IFFILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input, as would be observed on tuner outputs. Figure 34 and Figure 35 show IF filter compensation for NTSC and PAL, respectively.

The options for this feature are as follows:

- Bypass mode
- NTSC, consists of three filter characteristics
- PAL, consists of three filter characteristics

See Table 107 for programming details.

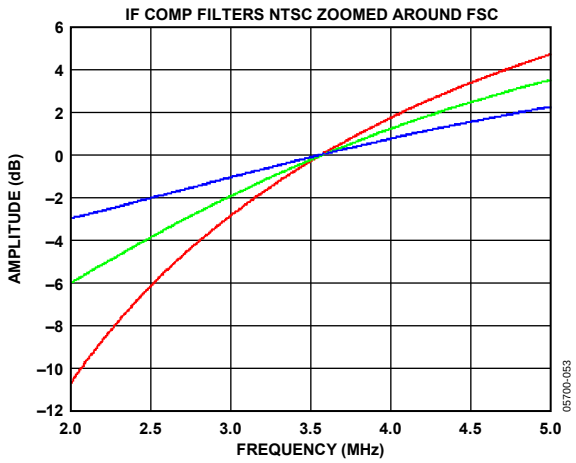


Figure 34. NTSC IF Filter Compensation

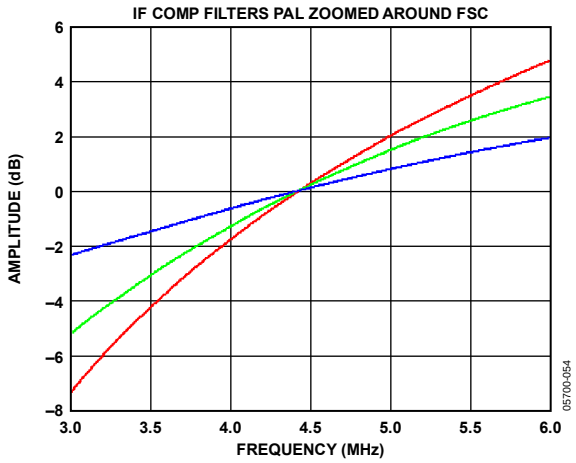


Figure 35. PAL IF Filter Compensation

AV CODE INSERTION AND CONTROLS

This section describes the I²C-based controls that affect the following:

- Insertion of AV codes into the data stream
- Data blanking during the vertical blank interval (VBI)
- The range of data values permitted in the output data stream
- The relative delay of luma vs. chroma signals

Some of the decoded VBI data is inserted during the horizontal blanking interval. See the Gemstar Data Recovery section for more information.

BT.656-4, ITU-R BT.656-4 Enable, Address 0x04[7]

Between Revision 3 and Revision 4 of the ITU-R BT.656 standards, the ITU has changed the toggling position for the V bit within the SAV EAV codes for NTSC. The ITU-R BT.656-4 standard bit allows the user to select an output mode that is compliant with either the previous or new standard. For further information, visit the International Telecommunication Union website.

Note that the standard change only affects NTSC and has no bearing on PAL.

When ITU-R BT.656-4 is 0 (default), the ITU-R BT.656-3 specification is used. The V bit goes low at EAV of Line 10 and Line 273.

When ITU-R BT.656-4 is 1, the ITU-R BT.656-4 specification is used. The V bit goes low at EAV of Line 20 and Line 283.

SD_DUP_AV, Duplicate AV Codes, Address 0x03[0]

Depending on the output interface width, it may be necessary to duplicate the AV codes from the luma path into the chroma path.

In an 8-bit wide output interface (Cb/Y/Cr/Y interleaved data), the AV codes are defined as FF/00/00/AV, with AV being the transmitted word that contains information about H/V/F.

In this output interface mode, the following assignment takes place: Cb = FF, Y = 00, Cr = 00, and Y = AV.

In a 16-bit output interface (64-lead LQFP only), where Y and Cr/Cb are delivered via separate data buses, the AV code is spread over the whole 16 bits. The SD_DUP_AV bit allows the user to replicate the AV codes on both buses; therefore, the full AV sequence can be found on the Y bus as well as on the Cr/Cb bus (see Figure 36).

When SD_DUP_AV is 0 (default), the AV codes are in single fashion (to suit 8-bit interleaved data output).

When SD_DUP_AV is 1, the AV codes are duplicated (for 16-bit interfaces).

VBI_EN, Vertical Blanking Interval Data Enable, Address 0x03[7]

The VBI enable bit allows data such as intercast and closed caption data to be passed through the luma channel of the decoder with a minimal amount of filtering. All data for Line 1 to Line 21 is passed through and available at the output port. The ADV7180 does not blank the luma data and automatically switches all filters along the luma data path into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

See the BL_C_VBI, Blank Chroma During VBI, Address 0x04[2] section for information on the chroma path.

When VBI_EN is 0 (default), all video lines are filtered/scaled.

When VBI_EN is 1, only the active video region is filtered/scaled.

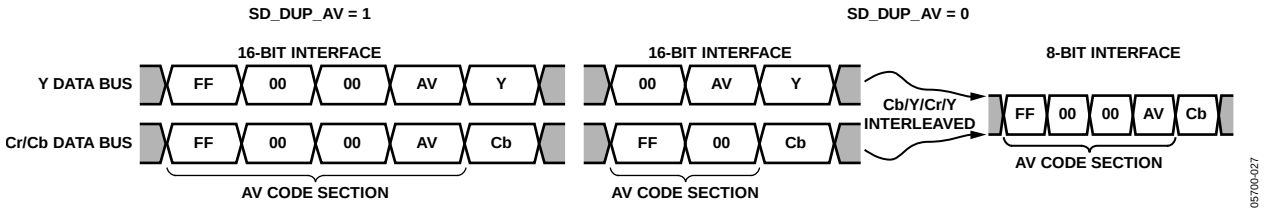


Figure 36. AV Code Duplication Control (64-Lead LQFP Only)

BL_C_VBI, Blank Chroma During VBI, Address 0x04[2]

Setting BL_C_VBI high blanks the Cr and Cb values of all VBI lines. This is done so any data that may arrive during VBI is not decoded as color and is output through Cr and Cb. As a result, it is possible to send VBI lines into the decoder and then output them through an encoder again, undistorted. Without this blanking, any color that is incorrectly decoded is encoded by the video encoder, thus distorting the VBI lines.

Setting BL_C_VBI to 0 decodes and outputs color during VBI.

Setting BL_C_VBI to 1 (default) blanks Cr and Cb values during VBI.

Range, Range Selection, Address 0x04[0]

AV codes (as per ITU-R BT.656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and, therefore, are not to be used for active video. Additionally, the ITU specifies that the nominal range for video should be restricted to values between 16 and 235 for luma and 16 and 240 for chroma.

The range bit allows the user to limit the range of values output by the ADV7180 to the recommended value range. The ADV7180 does not scale the data to fit within the smaller range. Any value outside of the range is ignored. In any case, it ensures that the reserved values of 255d (0xFF) and 00d (0x00) are not presented on the output pins unless they are part of an AV code header.

Table 61. RANGE Function

Range	Description
0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240
1 (default)	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254

AUTO_PDC_EN, Automatic Programmed Delay Control, Address 0x27[6]

Enabling AUTO_PDC_EN activates a function within the ADV7180 that automatically programs the LTA[1:0] and CTA[2:0] registers to have the chroma and luma data match delays for all modes of operation. If AUTO_PDC__EN is set, the LTA[1:0] and CTA[2:0] manual registers are not used. If the automatic mode is disabled (by setting the AUTO_PDC_EN bit to 0), the values programmed into the LTA[1:0] and CTA[2:0] registers become active.

When AUTO_PDC_EN is 0, the ADV7180 uses the LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. See the LTA[1:0], Luma Timing Adjust, Address 0x27[1:0] section and the CTA[2:0], Chroma Timing Adjust, Address 0x27[5:3] section.

When AUTO_PDC_EN is 1 (default), the ADV7180 automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

LTA[1:0], Luma Timing Adjust, Address 0x27[1:0]

The luma timing adjust register allows the user to specify a timing difference between chroma and luma samples.

There is a functionality overlap with the CTA[2:0] register. For manual programming, use the following defaults:

- CVBS input LTA[1:0] = 00
- Y/C input LTA[1:0] = 01
- YPrPb input LTA[1:0] = 01

Table 62. LTA Function

LTA[1:0]	Description
00 (default)	No delay
01	Luma 1 clock (37 ns) late
10	Luma 2 clock (74 ns) early
11	Luma 1 clock (37 ns) early

CTA[2:0], Chroma Timing Adjust, Address 0x27[5:3]

The chroma timing adjust register allows the user to specify a timing difference between chroma and luma samples. This can be used to compensate for external filter group delay differences in the luma vs. chroma path and to allow a different number of pipeline delays while processing the video downstream. Review this functionality together with the LTA[1:0] register.

The chroma can be delayed or advanced only in chroma pixel steps. One chroma pixel step is equal to two luma pixels. The programmable delay occurs after demodulation, where delay cannot be made by luma pixel steps.

For manual programming, use the following defaults:

- CVBS input CTA[2:0] = 011
- Y/C input CTA[2:0] = 101
- YPrPb input CTA[2:0] = 110

Table 63. CTA Function

CTA[2:0]	Description
000	Not a valid setting
001	Chroma + two pixels (early)
010	Chroma + one pixel (early)
011 (default)	No delay
100	Chroma – one pixel (late)
101	Chroma – two pixels (late)
110	Chroma – three pixels (late)
111	Not a valid setting

SYNCHRONIZATION OUTPUT SIGNALS

HS Configuration

The following controls allow the user to configure the behavior of the HS output pin only:

- Beginning of HS signal via HSB[10:0]
- End of HS signal via HSE[10:0]
- Polarity of HS using PHS

The HS begin (HSB) and HS end (HSE) registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and length of the HS output signal.

HSB[10:0], HS Begin, Address 0x34[6:4], Address 0x35[7:0]

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 37). HSB is set to 00000000010b, which is two LLC clock cycles from count [0].

The default value of HSB[10:0] is 0x02, indicating that the HS pulse starts two pixels after the falling edge of HS.

HSE[10:0], HS End, Address 0x34[2:0], Address 0x36[7:0]

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 37). HSE is set to 00000000000b, which is 0 LLC clock cycles from count [0].

The default value of HSE[10:0] is 00, indicating that the HS pulse ends 0 pixels after the falling edge of HS.

For example,

- To shift the HS toward active video by 20 LLCs, add 20 LLCs to both HSB and HSE, that is, HSB[10:0] = [00000010110], HSE[10:0] = [00000010100].
- To shift the HS away from active video by 20 LLCs, add 1696 LLCs to both HSB and HSE (for NTSC), that is, HSB[10:0] = [11010100010], HSE[10:0] = [11010100000]. Therefore, 1696 is derived from the NTSC total number of pixels, 1716.
- To move 20 LLCs away from active video, subtract 20 from 1716 and add the result in binary to both HSB[10:0] and HSE[10:0].

PHS, Polarity HS, Address 0x37[7]

The polarity of the HS pin can be inverted using the PHS bit.

When PHS is 0 (default), HS is active low.

When PHS is 1, HS is active high.

Table 64. HS Timing Parameters (See Figure 37)

	Characteristic				
Standard	HS Begin Adjust HSB[10:0] (Default)	HS End Adjust HSE[10:0] (Default)	HS to Active Video LLC Clock Cycles, C in Figure 37 (Default)	Active Video Samples/ Line, D in Figure 37	Total LLC Clock Cycles, E in Figure 37
NTSC	00000000010b	00000000000b	272	720Y + 720C = 1440	1716
PAL	00000000010b	00000000000b	284	720Y + 720C = 1440	1728

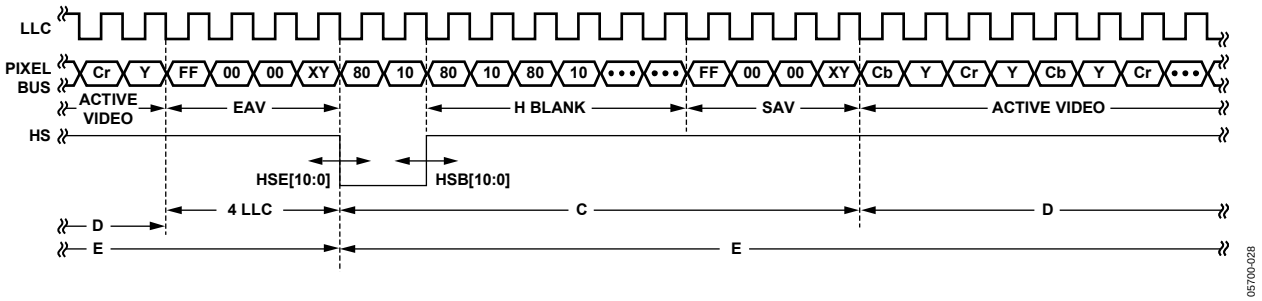


Figure 37. HS Timing

VS and FIELD Configuration

The following controls allow the user to configure the behavior of the VS and FIELD output pins, as well as the generation of embedded AV codes.

The 64-lead LQFP has separate VS and FIELD pins. The 48-lead LQFP, 40-lead LFCSP, and 32-lead LFCSP do not have separate VS and FIELD pins but can output either VS or FIELD on Pin 45 (48-lead LQFP), Pin 37 (40-lead LFCSP), or Pin 31 (32-lead LFCSP), which is the VS/FIELD pin.

SQPE, Square Pixel Mode, Address 0x01[2]

The SQPE bit allows the user to select the square pixel mode. This mode is not suitable for poor time-based video sources. This mode is recommended for professional applications only and should not be used with VCR or tuner sources.

Setting SQPE to 1 enables square pixel mode. The LLC for NTSC is 24.5454 MHz and 29.5 MHz for PAL. The crystal frequency does not change.

VS/FIELD, Address 0x58[0]

This feature is used for the 48-lead LQFP, 40-lead LFCSP, and 32-lead LFCSP only. The polarity of this bit determines what signal appears on the VS/FIELD pin.

When this bit is set to 0 (default), the FIELD signal is output.

When this bit is set to 1, the VSYNC signal is output.

The 64-lead LQFP has dedicated FIELD and VSYNC pins.

ADV encoder-compatible signals via the NEWAVMODE register follow:

- PVS, PF
- HVSTIM
- VSBHO, VSBHE
- VSEHO, VSEHE

For NTSC control,

- NVBEGDELO, NVBEGDELE, NVBEGSIGN, NVBEG[4:0]
- NVENDDELO, NVENDDELE, NVENDSIGN, NVEND[4:0]
- NFTOGDELO, NFTOGDELE, NFTOGSIGN, NFTOG[4:0]

For PAL control,

- PVBEGDELO, PVBEGDELE, PVBEGSIGN, PVBEG[4:0]
- PVENDDELO, PVENDDELE, PVENDSIGN, PVEND[4:0]
- PFTOGDELO, PFTOGDELE, PFTOGSIGN, PFTOG[4:0]

NEWAVMODE, New AV Mode, Address 0x31[4]

When NEWAVMODE is 0, EAV/SAV codes are generated to suit Analog Devices encoders. No adjustments are possible.

Setting NEWAVMODE to 1 (default) enables the manual position of the VSYNC, FIELD, and AV codes using Register 0x32 to Register 0x33 and Register 0xE5 to Register 0xEA. Default register settings are CCIR656 compliant; see Figure 38 for NTSC and Figure 43 for PAL. For recommended manual user settings, see Table 65 and Figure 39 for NTSC and Table 66 and Figure 44 for PAL.

HVSTIM, Horizontal VS Timing, Address 0x31[3]

The HVSTIM bit allows the user to select where the VS signal is asserted within a line of video. Some interface circuitry may require VS to go low while HS is low.

When HVSTIM is 0 (default), the start of the line is relative to HSE.

When HVSTIM is 1, the start of the line is relative to HSB.

VSBHO, VS Begin Horizontal Position Odd, Address 0x32[7]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high or low.

When VSBHO is 0 (default), the VS pin goes high in the middle of a line of video (odd field).

When VSBHO is 1, the VS pin changes state at the start of a line (odd field).

VSBHE, VS Begin Horizontal Position Even, Address 0x32[6]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to only change state when HS is high or low.

When VSBHE is 0 (default), the VS pin goes high in the middle of a line of video (even field).

When VSBHE is 1, the VS pin changes state at the start of a line (even field).

VSEHO, VS End Horizontal Position Odd, Address 0x33[7]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high or low.

When VSEHO is 0 (default), the VS pin goes low (inactive) in the middle of a line of video (odd field).

When VSEHO is 1, the VS pin changes state at the start of a line (odd field).

VSEHE, VS End Horizontal Position Even, Address 0x33[6]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high or low.

When VSEHE is 0 (default), the VS pin goes low (inactive) in the middle of a line of video (even field).

When VSEHE is 1, the VS pin changes state at the start of a line (even field).

PVS, Polarity VS, Address 0x37[5]

The polarity of the VS pin can be inverted using the PVS bit.

When PVS is 0 (default), VS is active high.

When PVS is 1, VS is active low.

PF, Polarity FIELD, Address 0x37[3]

The polarity of the FIELD pin for the 64-lead LQFP part can be inverted using the PF bit.

The FIELD pin can be inverted using the PF bit.

When PF is 0 (default), FIELD is active high.

When PF is 1, FIELD is active low.

Table 65. User Settings for NTSC (See Figure 39)

Register	Register Name	Write
0x31	VS/FIELD Control 1	0x1A
0x32	VS/FIELD Control 2	0x81
0x33	VS/FIELD Control 3	0x84
0x34	HS Position Control 1	0x00
0x35	HS Position Control 2	0x00
0x36	HS Position Control 3	0x7D
0x37	Polarity	0xA1
0xE5	NTSV V bit begin	0x41
0xE6	NTSC V bit end	0x84
0xE7	NTSC F bit toggle	0x06

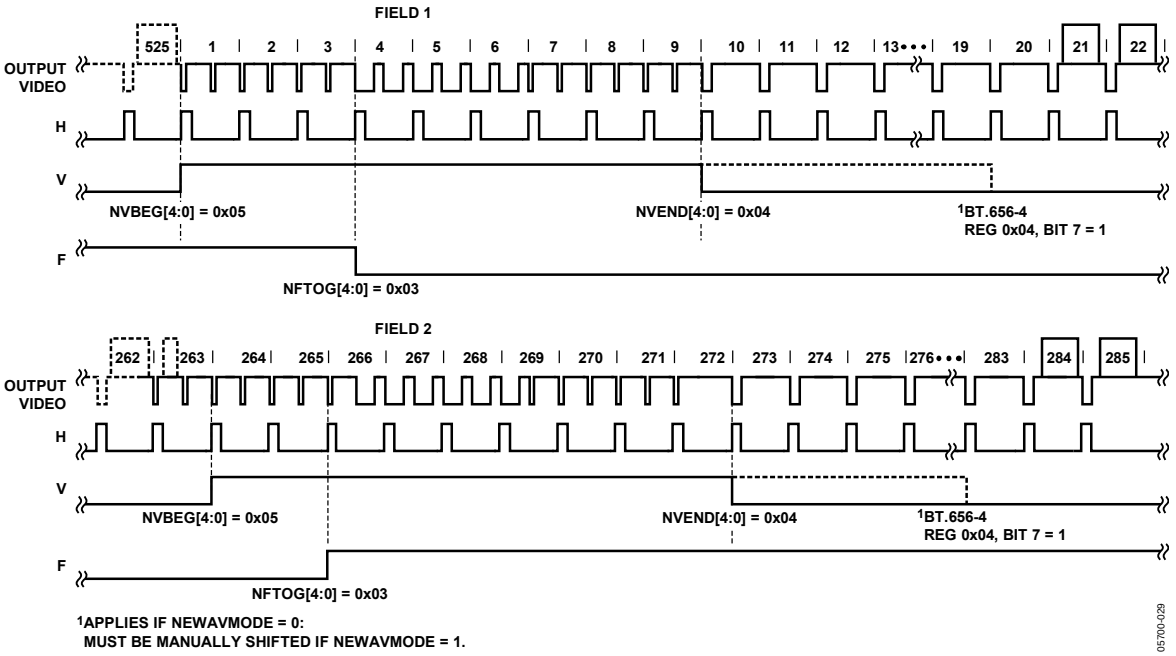


Figure 38. NTSC Default, ITU-R BT.656 (the Polarity of H, V, and F is Embedded in the Data)

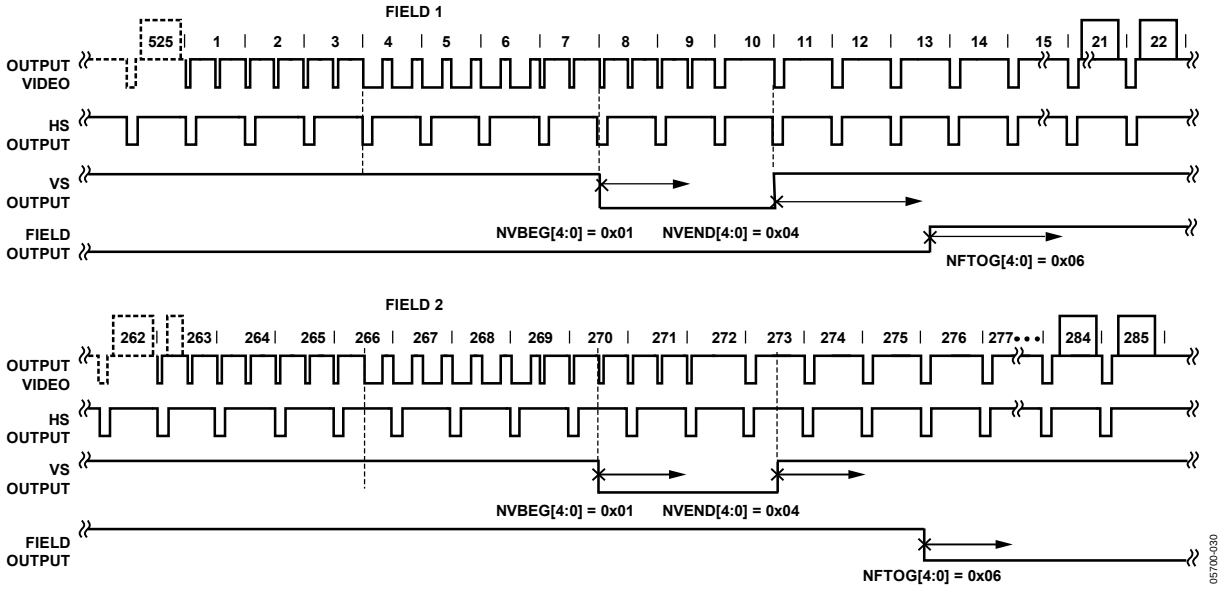


Figure 39. NTSC Typical VSYNC/FIELD Positions Using the Register Writes in Table 65

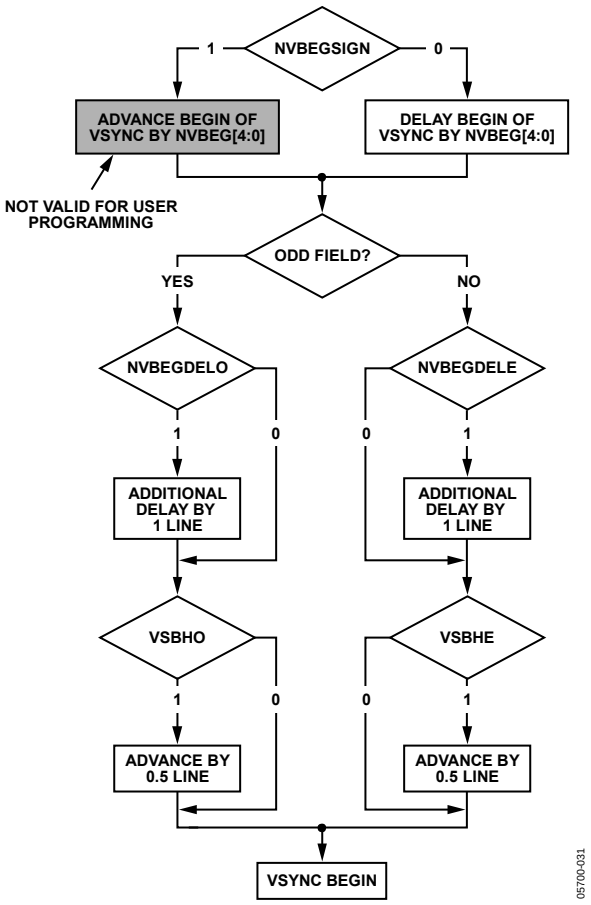


Figure 40. NTSC VSYNC Begin

NVBEGDELO, NTSC VSYNC Begin Delay on Odd Field, Address 0xE5[7]

When NVBEGDELO is 0 (default), there is no delay.

Setting NVBEGDELO to 1 delays VSYNC going high on an odd field by a line relative to NVBEG.

NVBEGDELE, NTSC VSYNC Begin Delay on Even Field, Address 0xE5[6]

When NVBEGDELE is 0 (default), there is no delay.

Setting NVBEGDELE to 1 delays VSYNC going high on an even field by a line relative to NVBEG.

NVBEGSIGN, NTSC VSYNC Begin Sign, Address 0xE5[5]

Setting NVBEGSIGN to 0 delays the start of VSYNC. Set for user manual programming.

Setting NVBEGSIGN to 1 (default) advances the start of VSYNC (not recommended for user programming).

NVBEG[4:0], NTSC VSYNC Begin, Address 0xE5[4:0]

The default value of NVBEG is 00101, indicating the NTSC VSYNC begin position.

For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal on the VS pin are modified.

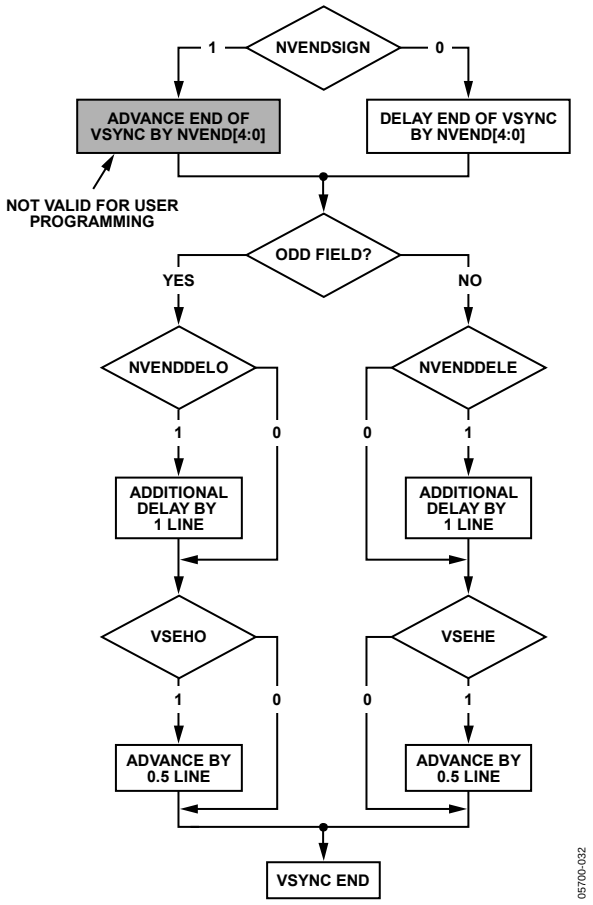


Figure 41. NTSC VSYNC End

NVENDDELO, NTSC VSYNC End Delay on Odd Field, Address 0xE6[7]

When NVENDDELO is 0 (default), there is no delay.

Setting NVENDDELO to 1 delays VSYNC from going low on an odd field by a line relative to NVEND.

NVENDDELE, NTSC VSYNC End Delay on Even Field, Address 0xE6[6]

When NVENDDELE is set to 0 (default), there is no delay.

Setting NVENDDELE to 1 delays VSYNC from going low on an even field by a line relative to NVEND.

NVENDSIGN, NTSC VSYNC End Sign, Address 0xE6[5]

Setting NVENDSIGN to 0 (default) delays the end of VSYNC. Set for user manual programming.

Setting NVENDSIGN to 1 advances the end of VSYNC (not recommended for user programming).

NVEND[4:0], NTSC VSYNC End, Address 0xE6[4:0]

The default value of NVEND is 00100, indicating the NTSC VSYNC end position.

For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal on the VS pin are modified.

NFTOGDELO, NTSC FIELD Toggle Delay on Odd Field, Address 0xE7[7]

When NFTOGDELO is 0 (default), there is no delay.

Setting NFTOGDELO to 1 delays the field toggle/transition on an odd field by a line relative to NFTOG.

NFTOGDELE, NTSC Field Toggle Delay on Even Field, Address 0xE7[6]

When NFTOGDELE is 0, there is no delay.

Setting NFTOGDELE to 1 (default) delays the field toggle/transition on an even field by a line relative to NFTOG.

NFTOGSIGN, NTSC Field Toggle Sign, Address 0xE7[5]

Setting NFTOGSIGN to 0 delays the field transition. Set for user manual programming.

Setting NFTOGSIGN to 1 (default) advances the field transition (not recommended for user programming).

NFTOG[4:0], NTSC Field Toggle, Address 0xE7[4:0]

The default value of NFTOG is 00011, indicating the NTSC field toggle position.

For all NTSC/PAL field timing controls, both the F bit in the AV code and the field signal on the FIELD pin are modified.

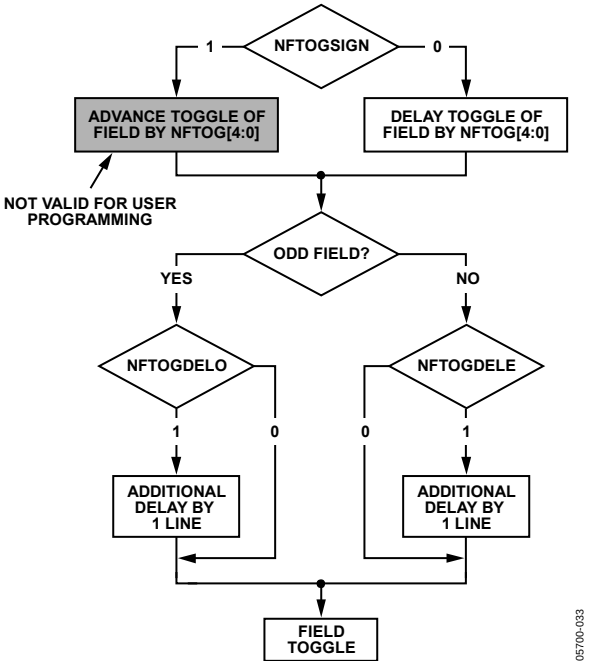


Figure 42. NTSC FIELD Toggle

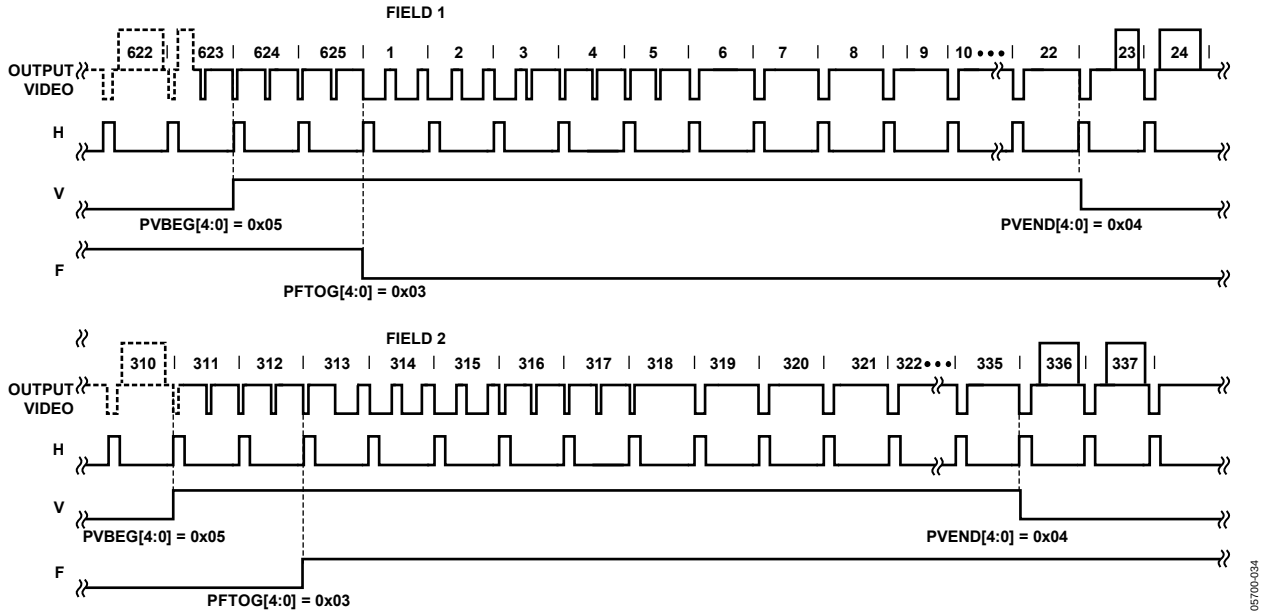


Figure 43. PAL Default, ITU-R BT.656 (the Polarity of H, V, and F Is Embedded in the Data)

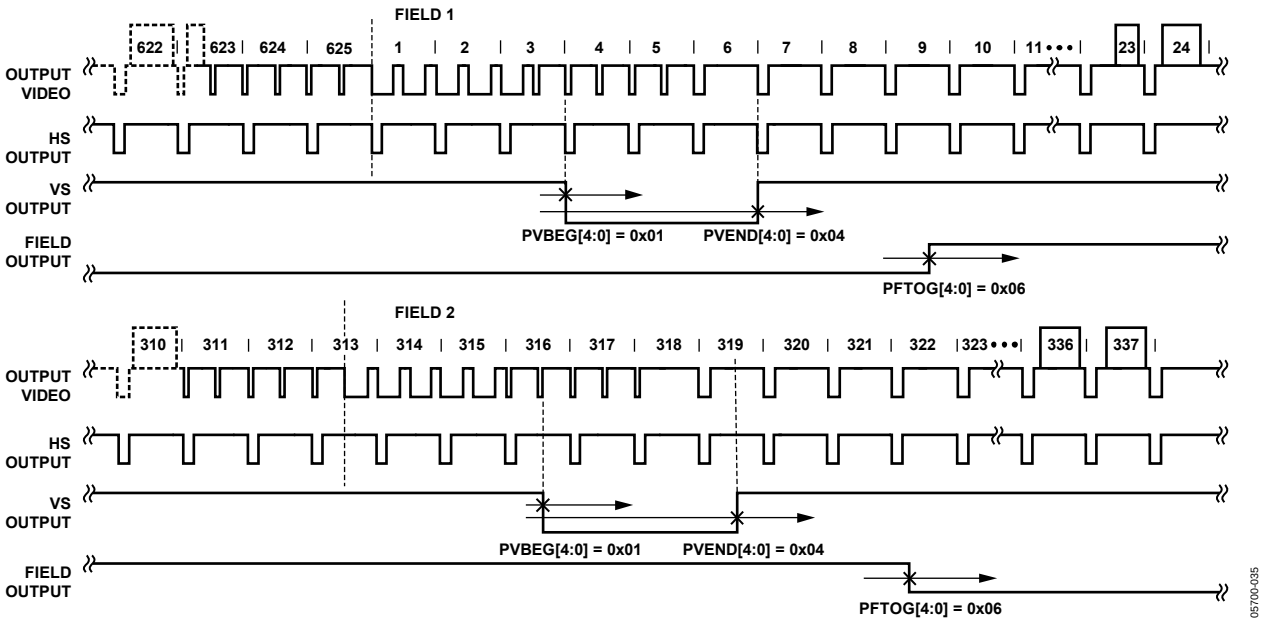


Figure 44. PAL Typical VS/FIELD Positions Using the Register Writes Shown in Table 66

Table 66. User Settings for PAL (See Figure 44)

Register	Register Name	Write
0x31	VS/FIELD Control 1	0x1A
0x32	VS/FIELD Control 2	0x81
0x33	VS/FIELD Control 3	0x84
0x34	HS Position Control 1	0x00
0x35	HS Position Control 2	0x00
0x36	HS Position Control 3	0x7D
0x37	Polarity	0xA1
0xE8	PAL V bit begin	0x41
0xE9	PAL V bit end	0x84
0xEA	PAL F bit toggle	0x06

PVBEGDELO, PAL VSYNC Begin Delay on Odd Field, Address 0xE8[7]

When PVBEGDELO is 0 (default), there is no delay.

Setting PVBEGDELO to 1 delays VSYNC going high on an odd field by a line relative to PVBEG.

PVBEGDELE, PAL VSYNC Begin Delay on Even Field, Address 0xE8[6]

When PVBEGDELE is 0, there is no delay.

Setting PVBEGDELE to 1 (default) delays VSYNC going high on an even field by a line relative to PVBEG.

PVBEGSIGN, PAL VSYNC Begin Sign, Address 0xE8[5]

Setting PVBEGSIGN to 0 delays the beginning of VSYNC. Set for user manual programming.

Setting PVBEGSIGN to 1 (default) advances the beginning of VSYNC (not recommended for user programming).

PVBEG[4:0], PAL VSYNC Begin, Address 0xE8[4:0]

The default value of PVBEG is 00101, indicating the PAL VSYNC begin position. For all NTSC/PAL VSYNC timing controls, the V bit in the AV code and the VSYNC signal on the VS pin are modified.

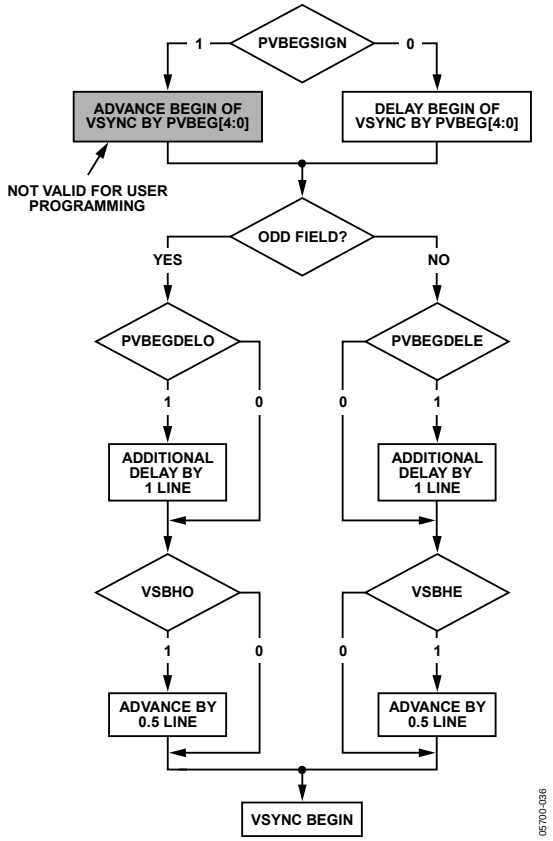


Figure 45. PAL VSYNC Begin

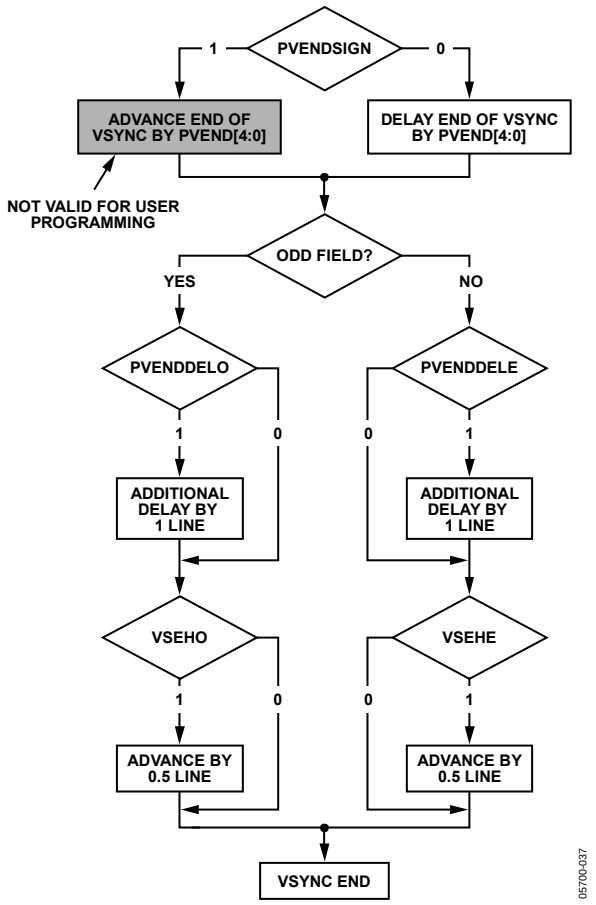


Figure 46. PAL VSYNC End

PVENDDELO, PAL VSYNC End Delay on Odd Field, Address 0xE9[7]

When PVENDDELO is 0 (default), there is no delay.

Setting PVENDDELO to 1 delays VSYNC going low on an odd field by a line relative to PVEND.

PVENDDELE, PAL VSYNC End Delay on Even Field, Address 0xE9[6]

When PVENDDELE is 0 (default), there is no delay.

Setting PVENDDELE to 1 delays VSYNC going low on an even field by a line relative to PVEND.

PVENDSIGN, PAL VSYNC End Sign, Address 0xE9[5]

Setting PVENDSIGN to 0 (default) delays the end of VSYNC (set for user manual programming).

Setting PVENDSIGN to 1 advances the end of VSYNC (not recommended for user programming).

PVEND[4:0], PAL VSYNC End, Address 0xE9[4:0]

The default value of PVEND is 10100, indicating the PAL VSYNC end position.

For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal on the VS pin are modified.

PFTOGDELO, PAL Field Toggle Delay on Odd Field, Address 0xEA[7]

When PFTOGDELO is 0 (default), there is no delay.

Setting PFTOGDELO to 1 delays the F toggle/transition on an odd field by a line relative to PFTOG.

PFTOGDELE, PAL Field Toggle Delay on Even Field, Address 0xEA[6]

When PFTOGDELE is 0, there is no delay.

Setting PFTOGDELE to 1 (default) delays the F toggle/transition on an even field by a line relative to PFTOG.

PFTOGSIGN, PAL Field Toggle Sign, Address 0xEA[5]

Setting PFTOGSIGN to 0 delays the field transition. Set for user manual programming.

Setting PFTOGSIGN to 1 (default) advances the field transition (not recommended for user programming).

PFTOG, PAL Field Toggle, Address 0xEA[4:0]

The default value of PFTOG is 00011, indicating the PAL field toggle position.

For all NTSC/PAL field timing controls, the F bit in the AV code and the field signal on the FIELD pin are modified.

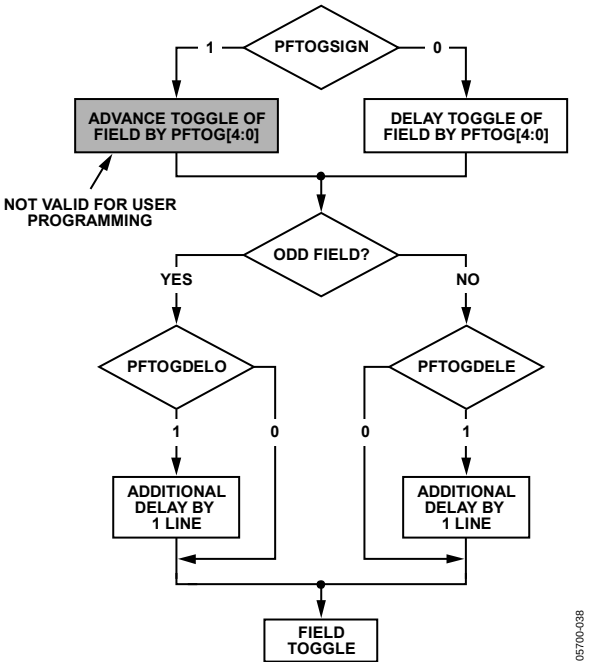


Figure 47. PAL F Toggle

SYNC PROCESSING

The ADV7180 has two additional sync processing blocks that postprocess the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the following two I²C bits: ENHSPLL and ENVSPROC.

ENHSPLL, Enable HSYNC Processor, Address 0x01[6]

The HSYNC processor is designed to filter incoming HSYNCs that have been corrupted by noise, providing improved performance for video signals with stable time bases but poor SNR.

Setting ENHSPLL to 0 disables the HSYNC processor.

Setting ENHSPLL to 1 (default) enables the HSYNC processor.

ENVSPROC, Enable VSYNC Processor, Address 0x01[3]

This block provides extra filtering of the detected VSYNCs to improve vertical lock.

Setting ENVSPROC to 0 disables the VSYNC processor.

Setting ENVSPROC to 1 (default) enables the VSYNC processor.

VBI DATA DECODE

The following are the two VBI data slicers on the ADV7180: the VBI data processor (VDP) and the VBI System 2.

The VDP can slice both low bandwidth standards and high bandwidth standards such as teletext. VBI System 2 can slice low data rate VBI standards only.

The VDP is capable of slicing multiple VBI data standards on SD video. It decodes the VBI data on the incoming CVBS and Y/C or YUV data. The decoded results are available as ancillary data in output 656 data stream. For low data rate VBI standards like CC/WSS/CGMS, users can read the decoded data bytes from the I²C registers.

The VBI data standards that can be decoded by the VDP are listed in Table 67 and Table 68.

Table 67. PAL

Feature	Standard
Teletext System A, C, or D	ITU-R BT.653
Teletext System B/WST	ITU-R BT.653
Video Programming System (VPS)	ETSI EN 300 231 V 1.3.1
Vertical Interval Time Codes (VITC)	Not applicable
Wide Screen Signaling (WSS)	ITU-R BT.1119-1/ ETSI EN.300294
Closed Captioning (CCAP)	Not applicable

Table 68. NTSC

Feature	Standard
Teletext System B and D	ITU-R BT.653
Teletext System C/NABTS	ITU-R BT.653/EIA-516
Vertical Interval Time Codes (VITC)	Not applicable
Copy Generation Management System (CGMS)	EIA-J CPR-1204/IEC 61880
Gemstar	Not applicable
Closed Captioning (CCAP)	EIA-608

The VBI data standard that the VDP decodes on a particular line of incoming video has been set by default as described in Table 69. This can be overridden manually and any VBI data can be decoded on any line. The details of manual programming are described in Table 70.

VDP Default Configuration

The VDP can decode different VBI data standards on a line-to-line basis. The various standards supported by default on different lines of VBI are explained in Table 69.

VDP Manual Configuration

MAN_LINE_PGM, Enable Manual Line Programming of VBI Standards, Address 0x64[7], User Sub Map

The user can configure the VDP to decode different standards on a line-to-line basis through manual line programming. For this, the user must set the MAN_LINE_PGM bit. The user must write into all the line programming registers, VBI_DATA_Px_Ny and VBI_DATA_Px (see Register 0x64 to Register 0x77 in Table 108).

When MAN_LINE_PGM to 0 (default) is set, the VDP decodes default standards on lines, as shown in Table 69.

When MAN_LINE_PGM to 1 is set, the VBI standards to be decoded are manually programmed.

VBI_DATA_Px_Ny[3:0], VBI_DATA_Px[3:0], VBI Standard to be Decoded on Line X for PAL, Line Y for NTSC, Address 0x64 to Address 0x77, User Sub Map

These are related 4-bit clusters in Register 0x64 to Register 0x77 of the user sub map. These 4-bit, line programming registers, VBI_DATA_Px_Ny and VBI_DATA_Px, identify the VBI data standard that are decoded on Line X in PAL mode or on Line Y in NTSC mode. The different types of VBI standards decoded by VBI_DATA_Px_Ny and VBI_DATA_Px are shown in Table 70. Note that the X or Y value depends on whether the ADV7180 is in PAL or NTSC mode.

Table 69. Default Standards on Lines for PAL and NTSC

PAL—625/50				NTSC—525/60			
Line No.	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**	**Line No.**	**Default VBI Data Decoded**
6	WST	318	VPS	23	Gemstar_1×	286	Gemstar_1×
7	WST	319	WST	24	Gemstar_1×	287	Gemstar_1×
8	WST	320	WST	25	Gemstar_1×	288	Gemstar_1×
9	WST	321	WST	10	NABTS	272	NABTS
10	WST	322	WST	11	NABTS	273	NABTS
11	WST	323	WST	12	NABTS	274	NABTS
12	WST	324	WST	13	NABTS	275	NABTS
13	WST	325	WST	14	VITC	276	NABTS
14	WST	326	WST	15	NABTS	277	VITC
15	WST	327	WST	16	VITC	278	NABTS
16	VPS	328	WST	17	NABTS	279	VITC
17	N/A	329	VPS	18	NABTS	280	NABTS
18	N/A	332	VITC	19	NABTS	281	NABTS
19	VITC	333	WST	20	CGMS	282	NABTS
20	WST	334	WST	21	CCAP	283	CGMS
21	WST	335	CCAP	22 + full odd field	NABTS	284	CCAP
22	CCAP	336	WST			285 + full even field	NABTS
23	WSS	337 + full even field	WST				
24 + full odd field	WST						

Table 70. VBI Data Standards for Manual Configuration

VBI_DATA_Px_Ny	625/50—PAL	525/60—NTSC
0000	Disable VDP	Disable VDP
0001	Teletext system identified by VDP_TTXT_TYPE	Teletext system identified by VDP_TTXT_TYPE
0010	VPS-ETSI EN 300 231 V 1.3.1	Reserved
0011	VITC	VITC
0100	WSS ITU-R BT.1119-1/ETSI.EN.300294	CGMS EIA-J CPR-1204/IEC 61880
0101	Reserved	Gemstar_1×
0110	Reserved	Gemstar_2×
0111	CCAP	CCAP EIA-608
1000 to 1111	Reserved	Reserved

Table 71.VBI Data Standards to be Decoded on Line Px (PAL) or Line Ny (NTSC)

Signal Name	Register Location	Dec Address	Hex Address
VBI_DATA_P6_N23	VDP_LINE_00F[7:4]	101	0x65
VBI_DATA_P7_N24	VDP_LINE_010[7:4]	102	0x66
VBI_DATA_P8_N25	VDP_LINE_011[7:4]	103	0x67
VBI_DATA_P9	VDP_LINE_012[7:4]	104	0x68
VBI_DATA_P10	VDP_LINE_013[7:4]	105	0x69
VBI_DATA_P11	VDP_LINE_014[7:4]	106	0x6A
VBI_DATA_P12_N10	VDP_LINE_015[7:4]	107	0x6B
VBI_DATA_P13_N11	VDP_LINE_016[7:4]	108	0x6C
VBI_DATA_P14_N12	VDP_LINE_017[7:4]	109	0x6D
VBI_DATA_P15_N13	VDP_LINE_018[7:4]	110	0x6E
VBI_DATA_P16_N14	VDP_LINE_019[7:4]	111	0x6F
VBI_DATA_P17_N15	VDP_LINE_01A[7:4]	112	0x70
VBI_DATA_P18_N16	VDP_LINE_01B[7:4]	113	0x71
VBI_DATA_P19_N17	VDP_LINE_01C[7:4]	114	0x72
VBI_DATA_P20_N18	VDP_LINE_01D[7:4]	115	0x73
VBI_DATA_P21_N19	VDP_LINE_01E[7:4]	116	0x74
VBI_DATA_P22_N20	VDP_LINE_01F[7:4]	117	0x75
VBI_DATA_P23_N21	VDP_LINE_020[7:4]	118	0x76
VBI_DATA_P24_N22	VDP_LINE_021[7:4]	119	0x77
VBI_DATA_P318	VDP_LINE_00E[3:0]	100	0x64
VBI_DATA_P319_N286	VDP_LINE_00F[3:0]	101	0x65
VBI_DATA_P320_N287	VDP_LINE_010[3:0]	102	0x66
VBI_DATA_P321_N288	VDP_LINE_011[3:0]	103	0x67
VBI_DATA_P322	VDP_LINE_012[3:0]	104	0x68
VBI_DATA_P323	VDP_LINE_013[3:0]	105	0x69
VBI_DATA_P324_N272	VDP_LINE_014[3:0]	106	0x6A
VBI_DATA_P325_N273	VDP_LINE_015[3:0]	107	0x6B
VBI_DATA_P326_N274	VDP_LINE_016[3:0]	108	0x6C
VBI_DATA_P327_N275	VDP_LINE_017[3:0]	109	0x6D
VBI_DATA_P328_N276	VDP_LINE_018[3:0]	110	0x6E
VBI_DATA_P329_N277	VDP_LINE_019[3:0]	111	0x6F
VBI_DATA_P330_N278	VDP_LINE_01A[3:0]	112	0x70
VBI_DATA_P331_N279	VDP_LINE_01B[3:0]	113	0x71
VBI_DATA_P332_N280	VDP_LINE_01C[3:0]	114	0x72
VBI_DATA_P333_N281	VDP_LINE_01D[3:0]	115	0x73
VBI_DATA_P334_N282	VDP_LINE_01E[3:0]	116	0x74
VBI_DATA_P335_N283	VDP_LINE_01F[3:0]	117	0x75
VBI_DATA_P336_N284	VDP_LINE_020[3:0]	118	0x76
VBI_DATA_P337_N285	VDP_LINE_021[3:0]	119	0x77

Note that full field detection (lines other than VBI lines) of any standard can also be enabled by writing into the VBI_DATA_P24_N22[3:0] and VBI_DATA_P337_N285[3:0] registers. So, if VBI_DATA_P24_N22[3:0] is programmed with any teletext standard, then teletext is decoded off for the entire odd field. The corresponding register for the even field is VBI_DATA_P337_N285[3:0].

For teletext system identification, VDP assumes that if teletext is present in a video channel, all the teletext lines comply with a single standard system. Therefore, the line programming using the VBI_DATA_Px_Ny and VBI_DATA_Px registers identifies whether the data in line is teletext; the actual standard is identified by the VDP_TTXT_TYPE_MAN bit.

To program the VDP_TTXT_TYPE_MAN bit, the VDP_TTXT_TYPE_MAN_ENABLE bit must be set to 1.

VDP_TTXT_TYPE_MAN_ENABLE, Enable Manual Selection of Teletext Type, Address 0x60[2], User Sub Map

Setting VDP_TTXT_TYPE_MAN_ENABLE to 0 (default), the manual programming of the teletext type is disabled.

Setting VDP_TTXT_TYPE_MAN_ENABLE to 1, the manual programming of the teletext type is enabled.

VDP_TTXT_TYPE_MAN[1:0], Specify the Teletext Type, Address 0x60[1:0], User Sub Map

These bits specify the teletext type to be decoded. These bits are functional only if VDP_TTXT_TYPE_MAN_ENABLE is set to 1.

Table 72. VDP_TTXT_TYPE_MAN Function

VDP_TTXT_TYPE_MAN[1:0]	625/50 (PAL)	525/60 (NTSC)
00 (default)	Teletext-ITU-BT.653-625/50-A	Reserved
01	Teletext-ITU-BT.653-625/50-B (WST)	Teletext-ITU-BT.653-525/60-B
10	Teletext-ITU-BT.653-625/50-C	Teletext-ITU-BT.653-525/60-C or EIA516 (NABTS)
11	Teletext-ITU-BT.653-625/50-D	Teletext-ITU-BT.653-525/60-D

VDP Ancillary Data Output

Reading the data back via I²C may not be feasible for VBI data standards with high data rates (for example, teletext). An alternative is to place the sliced data in a packet in the line blanking of the digital output CCIR656 stream. This is available for all standards sliced by the VDP module.

When data is sliced on a given line, the corresponding ancillary data packet is placed immediately after the next EAV code that occurs at the output (that is, data sliced from multiple lines are not buffered up and then emitted in a burst). Note that, due to the vertical delay through the comb filters, the line number on which the packet is placed differs from the line number on which the data was sliced.

The user can enable or disable the insertion of VDP results that have been decoded into the 656 ancillary streams by using the ADF_ENABLE bit.

ADF_ENABLE, Enable Ancillary Data Output Through 656 Stream, Address 0x62[7], User Sub Map

Setting ADF_ENABLE to 0 (default) disables the insertion of VBI decoded data into the ancillary 656 stream.

Setting ADF_ENABLE to 1 enables the insertion of VBI decoded data into the ancillary 656 stream.

The user may select the data identification word (DID) and the secondary data identification word (SDID) through programming the ADF_DID[4:0] and ADF_SDID[5:0] bits, respectively.

ADF_DID[4:0], User-Specified Data ID Word in Ancillary Data, Address 0x62[4:0], User Sub Map

This bit selects the data ID word to be inserted into the ancillary data stream with the data decoded by the VDP.

The default value of ADF_DID[4:0] is 10101.

ADF_SDID[5:0], User-Specified Secondary Data ID Word in Ancillary Data, Address 0x63[5:0], User Sub Map

These bits select the secondary data ID word to be inserted in the ancillary data stream with the data decoded by the VDP.

The default value of ADF_SDID[5:0] is 101010.

DUPLICATE_ADF, Enable Duplication/Spreading of Ancillary Data over Y and C Buses, Address 0x63[7], User Sub Map

This bit determines whether the ancillary data is duplicated over both Y and C buses or if the data packets are spread between the two channels.

When DUPLICATE_ADF to 0 (default) is set, the ancillary data packet is spread across the Y and C data streams.

When DUPLICATE_ADF to 1 is set, the ancillary data packet is duplicated on the Y and C data streams.

ADF_MODE[1:0], Determine the Ancillary Data Output Mode, Address 0x62[6:5], User Sub Map

These bits determine whether the ancillary data output mode is in byte mode or nibble mode.

Table 73. ADF_MODE

ADF_MODE[1:0]	Description
00 (default)	Nibble mode
01	Byte mode, no code restrictions
10	Byte mode, but 0x00 and 0xFF prevented (0x00 replaced by 0x01, 0xFF replaced by 0xFE)
11	Reserved

The ancillary data packet sequence is explained in Table 74 and Table 75. The nibble output mode is the default mode of output from the ancillary stream when ancillary stream output is enabled. This format is in compliance with ITU-R BT.1364.

The following abbreviations are used in Table 74 and Table 75:

- EP—Even parity for Bit B8 to Bit B2. The EP of the parity bit is set so that an even number of 1s are in Bit B8 to Bit B2, including the parity bit, D8.
- CS—Checksum word. The CS word is used to increase confidence of the integrity of the ancillary data packet from the DID, SDID, and DC through user data-words (UDWs). It consists of 10 bits that include the following: a 9-bit calculated value and B9 as the inverse of B8. The checksum value B8 to B0 is equal to the nine LSBs of the sum of the nine LSBs of the DID, SDID, and DC and all UDWs in the packet. Prior to the start of the checksum count cycle, all checksum and carry bits are preset to 0. Any carry resulting from the checksum count cycle is ignored.
- $\overline{EP}$—The MSB, B9, is the inverse of EP. This ensures that restricted Code 0x00 and Code 0xFF do not occur.
- LINE_NUMBER[9:0]—The line number of the line that immediately precedes the ancillary data packet. The line number is from the numbering system in ITU-R BT.470. The line number runs from 1 to 625 in a 625-line system and from 1 to 263 in a 525-line system. Note that, due to the vertical delay through the comb filters, the line number on which the packet is output differs from the line number on which the VBI data was sliced.
- Data count—The data count specifies the number of UDWs in the ancillary stream for the standard. The total number of user data-words is four times the data count. Padding words can be introduced to make the total number of UDWs divisible by 4.

Table 74. Ancillary Data in Nibble Output Format

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{EP}$	EP	0	I²C_DID6_2[4:0]					0	0	DID (data identification word)
4	$\overline{EP}$	EP	I²C_SDID7_2[5:0]						0	0	SDID (secondary data identification word)
5	$\overline{EP}$	EP	0	DC[4:0]					0	0	Data count
6	$\overline{EP}$	EP	Padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 (User Data-Word 1)
7	$\overline{EP}$	EP	0	LINE_NUMBER[9:5]					0	0	ID1 (User Data-Word 2)
8	$\overline{EP}$	EP	EVEN_FIELD	LINE_NUMBER[4:0]					0	0	ID2 (User Data-Word 3)
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 (User Data-Word 4)
10	$\overline{EP}$	EP	0	0	VBI_WORD_1[7:4]				0	0	ID4 (User Data-Word 5)
11	$\overline{EP}$	EP	0	0	VBI_WORD_1[3:0]				0	0	ID5 (User Data-Word 6)
12	$\overline{EP}$	EP	0	0	VBI_WORD_2[7:4]				0	0	ID6 (User Data-Word 7)
13	$\overline{EP}$	EP	0	0	VBI_WORD_2[3:0]				0	0	ID7 (User Data-Word 8)
14	$\overline{EP}$	EP	0	0	VBI_WORD_3[7:4]				0	0	ID8 (User Data-Word 9)
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word
n – 3	1	0	0	0	0	0	0	0	0	0	
n – 2	1	0	0	0	0	0	0	0	0	0	
n – 1	$\overline{B8}$	Checksum (CS)							0	0	CS (checksum word)

Table 75. Ancillary Data in Byte Output Format[1]

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble
1	1	1	1	1	1	1	1	1	1	1	
2	1	1	1	1	1	1	1	1	1	1	
3	$\overline{EP}$	EP	0	I^2C_DID6_2[4:0]					0	0	DID
4	$\overline{EP}$	EP	I^2C_SDID7_2[5:0]						0	0	SDID
5	$\overline{EP}$	EP	0	DC[4:0]					0	0	Data count
6	$\overline{EP}$	EP	Padding[1:0]		VBI_DATA_STD[3:0]				0	0	ID0 (User Data-Word 1)
7	$\overline{EP}$	EP	0	LINE_NUMBER[9:5]					0	0	ID1 (User Data-Word 2)
8	$\overline{EP}$	EP	EVEN_FIELD	LINE_NUMBER[4:0]					0	0	ID2 (User Data-Word 3)
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0	ID3 (User Data-Word 4)
10	VBI_WORD_1[7:0]								0	0	ID4 (User Data-Word 5)
11	VBI_WORD_2[7:0]								0	0	ID5 (User Data-Word 6)
12	VBI_WORD_3[7:0]								0	0	ID6 (User Data-Word 7)
13	VBI_WORD_4[7:0]								0	0	ID7 (User Data-Word 8)
14	VBI_WORD_5[7:0]								0	0	ID8 (User Data-Word 9)
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word
n – 3	1	0	0	0	0	0	0	0	0	0	
n – 2	1	0	0	0	0	0	0	0	0	0	
n – 1	$\overline{B8}$	Checksum							0	0	CS (checksum word)

[1] This mode does not fully comply with ITU-R BT.1364.

Structure of VBI Words in the Ancillary Data Stream

Each VBI data standard has been split into a clock-run-in (CRI), a framing code (FC), and a number of data bytes (n). The data packet in the ancillary stream includes only the FC and data bytes. Table 76 shows the format of VBI_WORD_x in the ancillary data stream.

Table 76. Structure of VBI Data-Words in the Ancillary Stream

Ancillary Data Byte No.	Byte Type	Description
VBI_WORD_1	FC0	Framing Code[23:16]
VBI_WORD_2	FC1	Framing Code[15:8]
VBI_WORD_3	FC2	Framing Code[7:0]
VBI_WORD_4	DB1	First data byte
…	…	…
VBI_WORD_N + 3	DBn	Last (n^{th}) data byte

VDP Framing Code

The length of the actual framing code depends on the VBI data standard. For uniformity, the length of the framing code reported in the ancillary data stream is always 24 bits. For standards with a smaller framing code length, the extra LSB bits are set to 0. The valid length of the framing code can be decoded from the VBI_DATA_STD bits available in ID0 (UDW 1). The framing code is always reported in the inverse-transmission order.

Table 77 shows the framing code and its valid length for VBI data standards supported by VDP.

Example

For teletext (B-WST), the framing code byte is 11100100 (0xE4), with bits shown in the order of transmission. VBI_WORD_1 = 0x27, VBI_WORD_2 = 0x00, and VBI_WORD_3 = 0x00 translated into UDWs in the ancillary data stream for nibble mode are as follows:

UDW5[5:2] = 0010

UDW6[5:2] = 0111

UDW7[5:2] = 0000 (undefined bits set to 0)

UDW8[5:2] = 0000 (undefined bits set to 0)

UDW9[5:2] = 0000 (undefined bits set to 0)

UDW10[5:2] = 0000 (undefined bits set to 0)

For byte mode,

UDW5[9:2] = 0010_0111

UDW6[9:2] = 0000_0000 (undefined bits set to 0)

UDW7[9:2] = 0000_0000 (undefined bits set to 0)

Data Bytes

VBI_WORD_4 to VBI_WORD_N + 3 contain the data-words that were decoded by the VDP in the transmission order. The position of bits in bytes is in the inverse transmission order.

For example, closed captioning has two user data bytes, as shown in Table 82.

The data bytes in the ancillary data stream are as follows:

VBI_WORD_4 = Byte 1[7:0]

VBI_WORD_5 = Byte 2[7:0]

The number of VBI_WORDS for each VBI data standard and the total number of UDWs in the ancillary data stream is shown in Table 78.

Table 77. Framing Code Sequence for Different VBI Standards

VBI Standard	Length in Bits	Error-Free Framing Code Bits (in Order of Transmission)	Error-Free Framing Code Reported by VDP (in Reverse Order of Transmission)
TTXT_SYSTEM_A (PAL)	8	11100111	11100111
TTXT_SYSTEM_B (PAL)	8	11100100	00100111
TTXT_SYSTEM_B (NTSC)	8	11100100	00100111
TTXT_SYSTEM_C (PAL and NTSC)	8	11100111	11100111
TTXT_SYSTEM_D (PAL and NTSC)	8	11100101	10100111
VPS (PAL)	16	10001010100011001	1001100101010001
VITC (NTSC and PAL)	1	0	0
WSS (PAL)	24	000111100011110000011111	111110000011110001111000
GEMSTAR_1× (NTSC)	3	001	100
GEMSTAR_2× (NTSC)	11	1001_1011_101	101_1101_1001
CCAP (NTSC and PAL)	3	001	100
CGMS (NTSC)	1	0	0

Table 78. Total User Data-Words for Different VBI Standards[1]

VBI Standard	ADF Mode	Framing Code UDWs	VBI Data-Words	No. of Padding Words	Total UDWs
TTXT_SYSTEM_A (PAL)	00 (nibble mode)	6	74	0	84
	01, 10 (byte mode)	3	37	0	44
TTXT_SYSTEM_B (PAL)	00 (nibble mode)	6	84	2	96
	01, 10 (byte mode)	3	42	3	52
TTXT_SYSTEM_B (NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
TTXT_SYSTEM_C (PAL and NTSC)	00 (nibble mode)	6	66	0	76
	01, 10 (byte mode)	3	33	2	42
TTXT_SYSTEM_D (PAL and NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
VPS (PAL)	00 (nibble mode)	6	26	0	36
	01, 10 (byte mode)	3	13	0	20
VITC (NTSC and PAL)	00 (nibble mode)	6	18	0	28
	01, 10 (byte mode)	3	9	0	16
WSS (PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
GEMSTAR_1× (NTSC)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
GEMSTAR_2× (NTSC)	00 (nibble mode)	6	8	2	20
	01, 10 (byte mode)	3	4	1	12
CCAP (NTSC and PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
CGMS (NTSC)	00 (nibble mode)	6	6	0	16
	01, 10 (byte mode)	3	3 + 3	2	12

[1] The first four UDWs are always the ID.

I²C Interface

Dedicated I²C readback registers are available for CCAP, CGMS, WSS, Gemstar, VPS, PDC/UTC, and VITC. Because teletext is a high data rate standard, data extraction is supported only through the ancillary data packet.

User Interface for I²C Readback Registers

The VDP decodes all enabled VBI data standards in real time. Because the I²C access speed is much lower than the decoded rate, when the registers are accessed, they may be updated with data from the next line. To avoid this, VDP has a self-clearing clear bit and an available (AVL) status bit accompanying all I²C readback registers.

The user must clear the I²C readback register by writing a high to the clear bit. This resets the state of the available bit to low and indicates that the data in the associated readback registers is not valid. After the VDP decodes the next line of the corresponding VBI data, the decoded data is placed into the I²C readback register and the available bit is set to high to indicate that valid data is now available.

Though the VDP decodes this VBI data in subsequent lines if present, the decoded data is not updated to the readback registers until the clear bit is set high again. However, this data is available through the 656 ancillary data packets.

The clear and available bits are in the VDP_STATUS_CLEAR (Address 0x78, user sub map, write only) and VDP_STATUS (Address 0x78, user sub map, read only) registers, respectively.

Example I²C Readback Procedure

The following tasks must be performed to read one packet (line) of PDC data from the decoder:

1. Write 10 to I²C_GS_VPS_PDC_UTC[1:0] (Address 0x9C, user sub map) to specify that PDC data must be updated to I²C registers.
2. Write high to the GS_PDC_VPS_UTC_CLEAR bit (Address 0x78, user sub map) to enable I²C register updating.
3. Poll the GS_PDC_VPS_UTC_AVL bit (Address 0x78, user sub map) going high to check the availability of the PDC packets.
4. Read the data bytes from the PDC I²C registers. Repeat Step 1 to Step 3 to read another line or packet of data.

To read a packet of CCAP, CGMS, or WSS data, Step 1 to Step 3 are required only because they have dedicated registers.

VDP—Content-Based Data Update

For certain standards, such as WSS, CGMS, Gemstar, PDC, UTC, and VPS, the information content in the signal transmitted remains the same over numerous lines, and the user may want to be notified only when there is a change in the information content or loss of the information content. The user must enable content-based updating for the required standard through the GS_VPS_PDC_UTC_CB_CHANGE and WSS_CGMS_CB_CHANGE bits. Therefore, the available bit shows the availability of that standard only when its content has changed.

Content-based updating also applies to lines with lost data. Therefore, for standards like VPS, Gemstar, CGMS, and WSS, if no data arrives in the next four lines programmed, the corresponding available bit in the VDP_STATUS register is set high and the content in the I²C registers for that standard is set to 0. The user must write high to the corresponding clear bit so that when a valid line is decoded after some time, the decoded results are available in the I²C registers, with the available status bit set high.

If content-based updating is enabled, the available bit is set high (assuming the clear bit was written) in the following cases:

- The data contents have changed.
- Data was being decoded and four lines with no data have been detected.
- No data was being decoded and new data is now being decoded.

GS_VPS_PDC_UTC_CB_CHANGE, Enable Content-Based Updating for Gemstar/VPS/PDC/UTC, Address 0x9C[5], User Sub Map

Setting GS_VPS_PDC_UTC_CB_CHANGE to 0 disables content-based updating.

Setting GS_VPS_PDC_UTC_CB_CHANGE to 1 (default) enables content-based updating.

WSS_CGMS_CB_CHANGE, Enable Content-Based Updating for WSS/CGMS, Address 0x9C[4], User Sub Map

Setting WSS_CGMS_CB_CHANGE to 0 disables content-based updating.

Setting WSS_CGMS_CB_CHANGE to 1 (default) enables content-based updating.

VDP—Interrupt-Based Reading of VDP I²C Registers

Some VDP status bits are also linked to the interrupt request controller so that the user does not have to poll the available status bit. The user can configure the video decoder to trigger an interrupt request on the $\overline{\text{INTRQ}}$ pin in response to the valid data available in the I²C registers. This function is available for the following data types:

- CGMS or WSS. The user can select either triggering an interrupt request each time sliced data is available or triggering an interrupt request only when the sliced data has changed. Selection is made via the WSS_CGMS_CB_CHANGE bit.
- Gemstar, PDC, VPS, or UTC. The user can select to trigger an interrupt request each time sliced data is available or to trigger an interrupt request only when the sliced data has changed. Selection is made via the GS_VPS_PDC_UTC_CB_CHANGE bit.

The sequence for the interrupt-based reading of the VDP I²C data registers is as follows for the CCAP standard:

1. The user unmasks the CCAP interrupt mask bit (Register 0x50, Bit 0, user sub map = 1). CCAP data occurs on the incoming video. VDP slices CCAP data and places it into the VDP readback registers.
2. The VDP CCAP available bit CC_CAP goes high, and the VDP module signals to the interrupt controller to stimulate an interrupt request (for CCAP in this case).
3. The user reads the interrupt status bits (user sub map) and sees that new CCAP data is available (Register 0x4E, Bit 0, user sub map = 1).
4. The user writes 1 to the CCAP interrupt clear bit (Register 0x4F, Bit 0, user sub map = 1) in the interrupt I²C space (this is a self-clearing bit). This clears the interrupt on the INTRQ pin but does not have an effect in the VDP I²C area.
5. The user reads the CCAP data from the VDP I²C area.
6. The user writes to Bit CC_CLEAR in the VDP_STATUS_CLEAR register, (Register 0x78, Bit 0, user sub map = 1) to signify the CCAP data has been read (therefore the VDP CCAP can be updated at the next occurrence of CCAP).
7. The user goes back to Step 2.

Interrupt Mask Register Details

The following bits set the interrupt mask on the signal from the VDP VBI data slicer.

VDP_CCAPD_MSK, Address 0x50[0], User Sub Map

Setting VDP_CCAPD_MSK to 0 (default) disables the interrupt on the VDP_CCAPD_Q signal.

Setting VDP_CCAPD_MSK to 1 enables the interrupt on the VDP_CCAPD_Q signal.

VDP_CGMS_WSS_CHNGD_MSK, Address 0x50[2], User Sub Map

Setting VDP_CGMS_WSS_CHNGD_MSK to 0 (default) disables the interrupt on the VDP_CGMS_WSS_ CHNGD_Q signal.

Setting VDP_CGMS_WSS_CHNGD_MSK to 1 enables the interrupt on the VDP_CGMS_WSS_CHNGD_Q signal.

VDP_GS_VPS_PDC_UTC_CHNG_MSK, Address 0x50[4], User Sub Map

Setting VDP_GS_VPS_PDC_UTC_CHNG_MSK to 0 (default) disables the interrupt on the VDP_GS_VPS_PDC_UTC_CHNG_Q signal.

Setting VDP_GS_VPS_PDC_UTC_CHNG_MSK to 1 enables the interrupt on the VDP_GS_VPS_PDC_UTC_CHNG_Q signal.

VDP_VITC_MSK, Address 0x50[6], User Sub Map

Setting VDP_VITC_MSK to 0 (default) disables the interrupt on the VDP_VITC_Q signal.

Setting VDP_VITC_MSK to 1 enables the interrupt on the VDP_VITC_Q signal.

Interrupt Status Register Details

The following read-only bits contain data detection information from the VDP module since the status bit is last cleared or unmasked.

VDP_CCAPD_Q, Address 0x4E[0], User Sub Map

When VDP_CCAPD_Q is 0 (default), CCAP data is not detected.

When VDP_CCAPD_Q is 1, CCAP data is detected.

VDP_CGMS_WSS_CHNGD_Q, Address 0x4E[2], User Sub Map

When VDP_CGMS_WSS_CHNGD_Q is 0 (default), CGMS or WSS data is not detected.

When VDP_CGMS_WSS_CHNGD_Q is 1, CGM or WSS data is detected.

VDP_GS_VPS_PDC_UTC_CHNG_Q, Address 0x4E[4], User Sub Map

When VDP_GS_VPS_PDC_UTC_CHNG_Q is 0 (default), Gemstar, PDC, UTC, or VPS data is not detected.

When VDP_GS_VPS_PDC_UTC_CHNG_Q is 1, Gemstar, PDC, UTC, or VPS data is detected.

VDP_VITC_Q, Address 0x4E[6], User Sub Map, Read Only

When VDP_VITC_Q is 0 (default), VITC data is not detected.

When VDP_VITC_Q is 1, VITC data is detected.

Interrupt Status Clear Register Details

It is not necessary to write 0 to these write-only bits because they automatically reset after they are set to 1 (self-clearing).

VDP_CCAPD_CLR, Address 0x4F[0], User Sub Map

Setting VDP_CCAPD_CLR to 1 clears the VDP_CCAP_Q bit.

VDP_CGMS_WSS_CHNGD_CLR, Address 0x4F[2], User Sub Map

Setting VDP_CGMS_WSS_CHNGD_CLR to 1 clears the VDP_CGMS_WSS_CHNGD_Q bit.

VDP_GS_VPS_PDC_UTC_CHNG_CLR, Address 0x4F[4], User Sub Map

Setting VDP_GS_VPS_PDC_UTC_CHNG_CLR to 1 clears the VDP_GS_VPS_PDC_UTC_CHNG_Q bit.

VDP_VITC_CLR, Address 0x4F[6], User Sub Map

Setting VDP_VITC_CLR to 1 clears the VDP_VITC_Q bit.

I²C READBACK REGISTERS

Teletext

Because teletext is a high data rate standard, the decoded bytes are available only as ancillary data. However, a TTXT_AVL bit is provided in I²C so that the user can check whether the VDP detects teletext. Note that the TTXT_AVL bit is a plain status bit and does not use the protocol identified in the I²C Interface section.

TTXT_AVL, Teletext Detected Status, Address 0x78[7], User Sub Map, Read Only

When TTXT_AVL is 0, teletext is not detected.

When TTXT_AVL is 1, teletext is detected.

WST Packet Decoding

For WST only, the VDP decodes the magazine and row address of teletext packets and further decodes 8 × 4 hamming coded words of the packet. This feature can be disabled using the WST_PKT_DECODE_DISABLE bit (Bit 3, Register 0x60, user sub map). This feature is valid for WST only.

WST_PKT_DECODE_DISABLE, Disable Hamming Decoding of Bytes in WST, Address 0x60[3], User Sub Map

Setting WST_PKT_DECODE_DISABLE to 0 enables hamming decoding of WST packets.

Setting WST_PKT_DECODE_DISABLE to 1 (default) disables hamming decoding of WST packets.

For hamming-coded bytes, the dehammed nibbles are output along with some error information from the hamming decoder as follows:

- Input hamming coded byte: {D3, P3, D2, P2, D1, P1, D0, P0} (bits in decoded order)
- Output dehammed byte: {E1, E0, 0, 0, D3', D2', D1', D0'} (Di' – corrected bits, Ei error information).

Table 79. Error Bits in the Dehammed Output Byte

E[1:0]	Error Information	Output Data Bits in Nibble
00	No errors detected	Okay
01	Error in P4	Okay
10	Double error	Bad
11	Single error found and corrected	Okay

Table 80 describes the WST packets that are decoded.

Table 80. WST Packet Description

Packet	Byte	Description
Header Packet (X/00)	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Page number—Dehammed Byte 6
	4th	Page number—Dehammed Byte 7
	5th to 10th	Control bytes—Dehammed Byte 8 to Byte 13
	11th to 42nd	Raw data bytes
Text Packets (X/01 to X/25)	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd to 42nd	Raw data bytes
8/30 (Format 1) Packet	1st	Magazine number—Dehammed Byte 4
Design Code = 0000 or 0001	2nd	Row number—Dehammed Byte 5
UTC	3rd	Design code—Dehammed Byte 6
	4th to 10th	Dehammed initial teletext page, Byte 7 to Byte 12
	11th to 23rd	UTC bytes—Dehammed Byte 13 to Byte 25
	24th to 42nd	Raw status bytes
8/30 (Format 2) Packet	1st	Magazine number—Dehammed Byte 4
Design Code = 0010 or 0011	2nd	Row number—Dehammed Byte 5
PDC	3rd	Design code—Dehammed Byte 6
	4th to 10th	Dehammed initial teletext page, Byte 7 to Byte 12
	11th to 23rd	PDC bytes—Dehammed Byte 13 to Byte 25
	24th to 42nd	Raw status bytes
X/26, X/27, X/28, X/29, X/30, X/31[1]	1st	Magazine number—Dehammed Byte 4
	2nd	Row number—Dehammed Byte 5
	3rd	Design code—Dehammed Byte 6
	4th to 42nd	Raw data bytes

[1] For X/26, X/28, and X/29, further decoding needs 24 × 18 hamming decoding. Not supported at present.

CGMS and WSS

The CGMS and WSS data packets convey the same type of information for different video standards. WSS is for PAL and CGMS is for NTSC; therefore, the CGMS and WSS readback registers are shared. WSS is biphase coded; the VDP performs a biphase decoding to produce the 14 raw WSS bits in the CGMS/WSS readback I²C registers and to set the CGMS_WSS_AVL bit.

CGMS_WSS_CLEAR, CGMS/WSS Clear, Address 0x78[2], User Sub Map, Write Only, Self-Clearing

Setting CGMS_WSS_CLEAR to 1 reinitializes the CGMS/WSS readback registers.

CGMS_WSS_AVL, CGMS/WSS Available, Address 0x78[2], User Sub Map, Read Only

When CGMS_WSS_AVL is 0, CGMS/WSS is not detected.

When CGMS_WSS_AVL is 1, CGMS/WSS is detected.

VDP_CGMS_WSS_DATA_0[3:0], Address 0x7D[3:0];

VDP_CGMS_WSS_DATA_1[7:0], Address 0x7E[7:0];

VDP_CGMS_WSS_DATA_2[7:0], Address 0x7F[7:0]; User Sub Map, Read Only

These bits hold the decoded CGMS or WSS data.

Refer to Figure 48 and Figure 49 for the I²C-to-WSS and I²C-to-CGMS bit mapping.

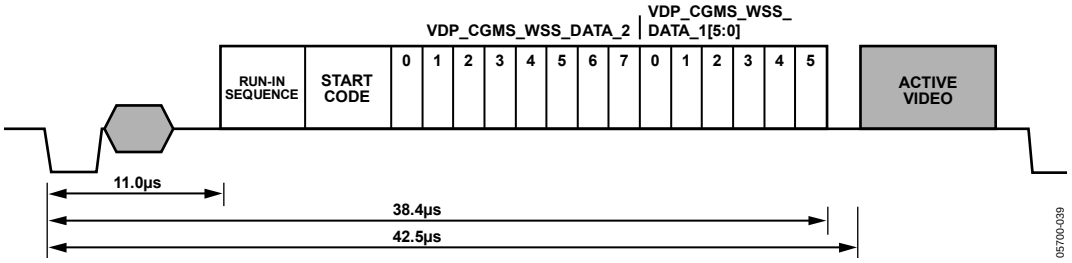


Figure 48. WSS Waveform

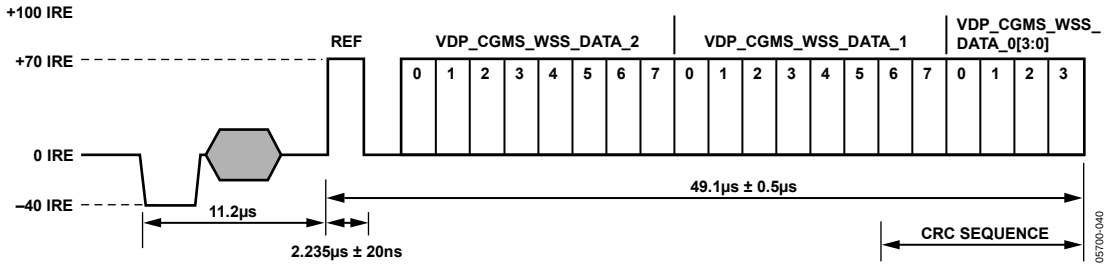


Figure 49. CGMS Waveform

Table 81. CGMS Readback Registers[1]

Signal Name	Register Location	Address (User Sub Map)	
CGMS_WSS_DATA_0[3:0]	VDP_CGMS_WSS_DATA_0[3:0]	125	0x7D
CGMS_WSS_DATA_1[7:0]	VDP_CGMS_WSS_DATA_1[7:0]	126	0x7E
CGMS_WSS_DATA_2[7:0]	VDP_CGMS_WSS_DATA_2[7:0]	127	0x7F

[1] These registers are readback registers; default value does not apply.

CCAP

Two bytes of decoded closed caption data are available in the I²C registers. The field information of the decoded CCAP data can be obtained from the CC_EVEN_FIELD bit (Register 0x78).

CC_CLEAR, Closed Caption Clear, Address 0x78[0], User Sub Map, Write Only, Self-Clearing

Setting CC_CLEAR to 1 reinitializes the CCAP readback registers.

CC_AVL, Closed Caption Available, Address 0x78[0], User Sub Map, Read Only

When CC_AVL is 0, closed captioning is not detected.

When CC_AVL is 1, closed captioning is detected.

CC_EVEN_FIELD, Address 0x78[1], User Sub Map, Read Only

Identifies the field from which the CCAP data is decoded.

When CC_EVEN_FIELD is 0, closed captioning is detected from an odd field.

When CC_EVEN_FIELD is 1, closed captioning is detected from an even field.

VDP_CCAP_DATA_0, Address 0x79[7:0], User Sub Map, Read Only

Decoded Byte 1 of CCAP data.

VDP_CCAP_DATA_1, Address 0x7A[7:0], User Sub Map, Read Only

Decoded Byte 2 of CCAP data.

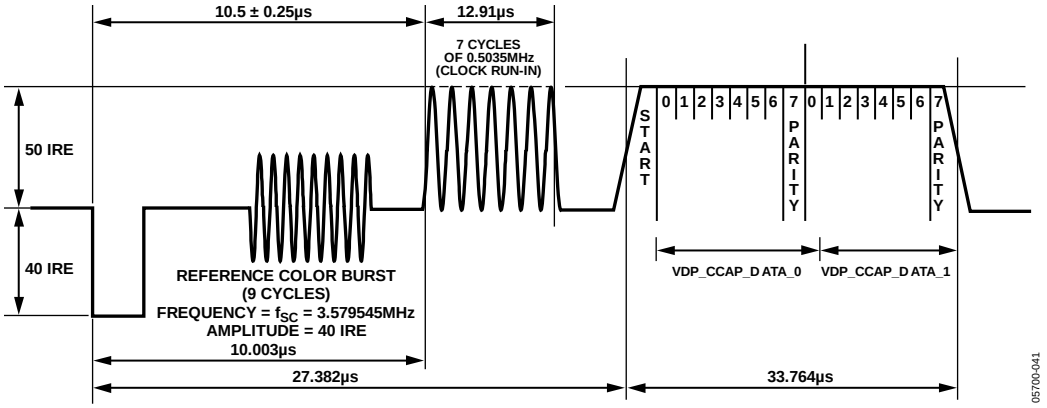


Figure 50. CCAP Waveform and Decoded Data Correlation

Table 82. CCAP Readback Registers[1]

Signal Name	Register Location	Address (User Sub Map)	
CCAP_BYTE_1[7:0]	VDP_CCAP_DATA_0[7:0]	121	0x79
CCAP_BYTE_2[7:0]	VDP_CCAP_DATA_1[7:0]	122	0x7A

[1] These registers are readback registers; default value does not apply.

VITC

VITC has a sequence of 10 syncs between each data byte. The VDP strips these syncs from the data stream to output only the data bytes. The VITC results are available in Register VDP_VITC_DATA_0 to Register VDP_VITC_DATA_8 (Register 0x92 to Register 0x9A, user sub map).

The VITC has a CRC byte at the end; the syncs in between each data byte are also used in this CRC calculation. Because the syncs in between each data byte are not output, the CRC is calculated internally. The calculated CRC is available for the user in the VDP_VITC_CALC_CRC register (Resister 0x9B, user sub map). When the VDP completes decoding the VITC line, the VITC_DATA_x and VITC_CRC registers are updated and the VITC_AVL bit is set.

VITC_CLEAR, VITC Clear, Address 0x78[6], User Sub Map, Write Only, Self-Clearing

Setting VITC_CLEAR to 1 reinitializes the VITC readback registers.

VITC_AVL, VITC Available, Address 0x78[6], User Sub Map, Read Only

When VITC_AVL is 0, VITC data is not detected.

When VITC_AVL is 1, VITC data is detected.

VITC Readback Registers

See Figure 51 for the I²C-to-VITC bit mapping.

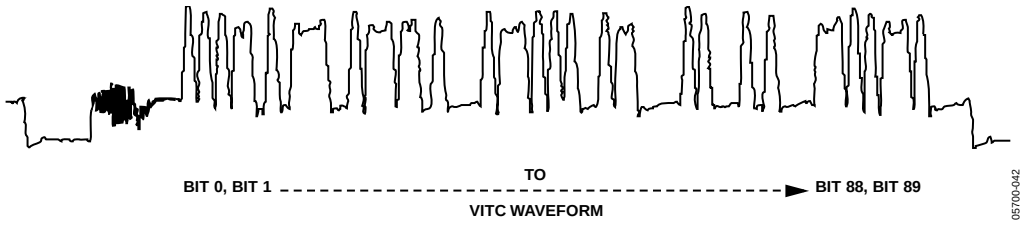


Figure 51. VITC Waveform and Decoded Data Correlation

Table 83. VITC Readback Registers[1]

Signal Name	Register Location	Address (User Sub Map)	
VITC_DATA_0[7:0]	VDP_VITC_DATA_0[7:0] (VITC Bits[9:2])	146	0x92
VITC_DATA_1[7:0]	VDP_VITC_DATA_1[7:0] (VITC Bits[19:12])	147	0x93
VITC_DATA_2[7:0]	VDP_VITC_DATA_2[7:0] (VITC Bits[29:22])	148	0x94
VITC_DATA_3[7:0]	VDP_VITC_DATA_3[7:0] (VITC Bits[39:32])	149	0x95
VITC_DATA_4[7:0]	VDP_VITC_DATA_4[7:0] (VITC Bits[49:42])	150	0x96
VITC_DATA_5[7:0]	VDP_VITC_DATA_5[7:0] (VITC Bits[59:52])	151	0x97
VITC_DATA_6[7:0]	VDP_VITC_DATA_6[7:0] (VITC Bits[69:62])	152	0x98
VITC_DATA_7[7:0]	VDP_VITC_DATA_7[7:0] (VITC Bits[79:72])	153	0x99
VITC_DATA_8[7:0]	VDP_VITC_DATA_8[7:0] (VITC Bits[89:82])	154	0x9A
VITC_CRC[7:0]	VDP_VITC_CALC_CRC[7:0]	155	0x9B

[1] These registers are readback registers; default value does not apply.

VPS/PDC/UTC/GEMSTAR

The readback registers for VPS, PDC, and UTC are shared. Gemstar is a high data rate standard and is available only through the ancillary stream. However, for evaluation purposes, any one line of Gemstar is available through the I²C registers sharing the same register space as PDC, UTC, and VPS. Therefore, only VPS, PDC, UTC, or Gemstar can be read through the I²C at one time.

To identify the data that should be made available in the I²C registers, the user must program I²C_GS_VPS_PDC_UTC[1:0] (Register Address 0x9C, user sub map).

I²C_GS_VPS_PDC_UTC[1:0] (VDP), Address 0x9C[7:6], User Sub Map

Specifies which standard result is available for I²C readback.

GS_PDC_VPS_UTC_CLEAR, GS/PDC/VPS/UTC Clear, Address 0x78[4], User Sub Map, Write Only, Self-Clearing

Setting GS_PDC_VPS_UTC_CLEAR to 1 reinitializes the GS/PDC/VPS/UTC data readback registers.

GS_PDC_VPS_UTC_AVL, GS/PDC/VPS/UTC Available, Address 0x78[4], User Sub Map, Read Only

When GS_PDC_VPS_UTC_AVL is 0, no GS, PDC, VPS, or UTC data is detected.

When GS_PDC_VPS_UTC_AVL is 1, one GS, PDC, VPS, or UTC data is detected.

VDP_GS_VPS_PDC_UTC, Readback Registers, Address 0x84 to Address 0x90

See Table 85 for information on the readback registers.

VPS

The VPS data bits are biphase decoded by the VDP. The decoded data is available in both the ancillary stream and in the I²C readback registers. VPS decoded data is available in the VDP_GS_VPS_PDC_UTC_0 to VDP_VPS_PDC_UTC_12 registers (Address 0x84 to Address 0x90, user sub map). The GS_PDC_VPS_UTC_AVL bit is set if the user programmed I²C_GS_VPS_PDC_UTC to 01, as explained in Table 84.

Gemstar

The Gemstar-decoded data is made available in the ancillary stream, and any one line of Gemstar is also available in the I²C registers for evaluation purposes. To read Gemstar results through the I²C registers, the user must program I²C_GS_VPS_PDC_UTC to 00, as explained in Table 84.

Table 84. I²C_GS_VPS_PDC_UTC[1:0] Function

I²C_GS_VPS_PDC_UTC[1:0]	Description
00 (default)	Gemstar 1×/2×
01	VPS
10	PDC
11	UTC

VDP supports autodetection of the Gemstar standard, either Gemstar 1× or Gemstar 2×, and decodes accordingly. For the autodetection mode to work, the user must set the AUTO_DETECT_GS_TYPE bit (Register 0x61, user sub map) and program the decoder to decode Gemstar 2× on the required lines through line programming. The type of Gemstar decoded can be determined by observing the GS_DATA_TYPE bit (Register 0x78, user sub map).

AUTO_DETECT_GS_TYPE, Address 0x61[4], User Sub Map

Setting AUTO_DETECT_GS_TYPE to 0 (default) disables the autodetection of the Gemstar type.

Setting AUTO_DETECT_GS_TYPE to 1 enables the autodetection of the Gemstar type.

GS_DATA_TYPE, Address 0x78[5], User Sub Map, Read Only

Identifies the decoded Gemstar data type.

When GS_DATA_TYPE is 0, Gemstar 1× mode is detected. Read two data bytes from Register 0x84.

When GS_DATA_TYPE is 1, Gemstar 2× mode is detected. Read four data bytes from Register 0x84.

The Gemstar data that is available in the I²C register can be from any line of the input video on which Gemstar was decoded. To read the Gemstar data on a particular video line, the user should use the manual configuration described in Table 70 and Table 71 and enable Gemstar decoding only on the required line.

PDC/UTC

PDC and UTC are data transmitted through Teletext Packet 8/30 Format 2 (Magazine 8, Row 30, Design Code 2 or Design Code 3) and Packet 8/30 Format 1 (Magazine 8, Row 30, Design Code 0 or Design Code 1). Therefore, if PDC or UTC data is to be read through I²C, the corresponding teletext standard (WST or PAL System B) should be decoded by VDP. The whole teletext decoded packet is output on the ancillary data stream. The user can look for the magazine number, row number, and design code and qualify the data as PDC, UTC, or neither of these.

If PDC/UTC packets are identified, Byte 0 to Byte 12 are updated to the VDP_GS_VPS_PDC_UTC_0 to VDP_VPS_PDC_UTC_12 registers, and the GS_PDC_VPS_UTC_AVL bit is set. The full packet data is also available in the ancillary data format.

Note that the data available in the I²C register depends on the status of the WST_PKT_DECODE_DISABLE bit (Bit 3, Subaddress 0x60, user sub map).

Table 85. GS/VPS/PDC/UTC Readback Registers[1]

Signal Name	Register Location	Dec Address (User Sub Map)	Hex Address (User Sub Map)
GS_VPS_PDC_UTC_BYTE_0[7:0]	VDP_GS_VPS_PDC_UTC_0[7:0]	132	0x84
GS_VPS_PDC_UTC_BYTE_1[7:0]	VDP_GS_VPS_PDC_UTC_1[7:0]	133	0x85
GS_VPS_PDC_UTC_BYTE_2[7:0]	VDP_GS_VPS_PDC_UTC_2[7:0]	134	0x86
GS_VPS_PDC_UTC_BYTE_3[7:0]	VDP_GS_VPS_PDC_UTC_3[7:0]	135	0x87
VPS_PDC_UTC_BYTE_4[7:0]	VDP_VPS_PDC_UTC_4[7:0]	136	0x88
VPS_PDC_UTC_BYTE_5[7:0]	VDP_VPS_PDC_UTC_5[7:0]	137	0x89
VPS_PDC_UTC_BYTE_6[7:0]	VDP_VPS_PDC_UTC_6[7:0]	138	0x8A
VPS_PDC_UTC_BYTE_7[7:0]	VDP_VPS_PDC_UTC_7[7:0]	139	0x8B
VPS_PDC_UTC_BYTE_8[7:0]	VDP_VPS_PDC_UTC_8[7:0]	140	0x8C
VPS_PDC_UTC_BYTE_9[7:0]	VDP_VPS_PDC_UTC_9[7:0]	141	0x8D
VPS_PDC_UTC_BYTE_10[7:0]	VDP_VPS_PDC_UTC_10[7:0]	142	0x8E
VPS_PDC_UTC_BYTE_11[7:0]	VDP_VPS_PDC_UTC_11[7:0]	143	0x8F
VPS_PDC_UTC_BYTE_12[7:0]	VDP_VPS_PDC_UTC_12[7:0]	144	0x90

[1] The default value does not apply to readback registers.

VBI System 2

The user has an option of using a different VBI data slicer called VBI System 2. This data slicer is used to decode Gemstar and closed caption VBI signals only.

Using this system, the Gemstar data is available only in the ancillary data stream. A special mode enables one line of data to be read back through I²C.

Gemstar Data Recovery

The Gemstar-compatible data recovery block (GSCD) supports 1× and 2× data transmissions. In addition, it can serve as a closed caption decoder. Gemstar-compatible data transmissions can occur only in NTSC. Closed caption data can be decoded in both PAL and NTSC.

The block can be configured via I²C as follows:

- GDECEL[15:0] allows data recovery on selected video lines on even fields to be enabled or disabled.
- GDECOL[15:0] enables the data recovery on selected lines for odd fields.
- GDECAD[0] configures the way in which data is embedded in the video data stream.

The recovered data is not available through I²C but is inserted into the horizontal blanking period of an ITU-R BT.656-compatible data stream. The data format is intended to comply with the recommendation by the International Telecommunications Union, ITU-R BT.1364. For more information, visit the International Telecommunication Union website. See Figure 52.

GDE_SEL_OLD_ADF, Address 0x4C[3], User Sub Map

The ADV7180 has a new ancillary data output block that can be used by the VDP data slicer and the VBI System 2 data slicer. The new ancillary data formatter is used by setting GDE_SEL_OLD_ADF to 0 (default). See Table 74 and Table 75 for information about how the data is packaged in the ancillary data stream when this bit is set low.

To use the old ancillary data formatter (to be backward compatible with the ADV7183B), set GDE_SEL_OLD_ADF to 1. The ancillary data format in this section refers to the ADV7183B-compatible ancillary data formatter.

Setting GDE_SEL_OLD_ADF to 0 (default) enables a new ancillary data system for use with the VDP and VBI System 2.

Setting GDE_SEL_OLD_ADF to 1 enables the old ancillary data system for use with the VBI System 2 only (ADV7183B compatible).

The format of the data packet depends on the following criteria:

- Transmission is 1× or 2×.
- Data is output in 8-bit or 4-bit format (see the description of the bit).
- Data is closed caption (CCAP) or Gemstar compatible.

Data packets are output if the corresponding enable bit is set (see the GDECEL[15:0], Gemstar Decoding Even Lines, Address 0x48[7:0], Address 0x49[7:0] and the GDECOL[15:0], Gemstar Decoding Odd Lines, Address 0x4A[7:0], Address 0x4B[7:0] sections), and the decoder detects the presence of data. For video lines where no data is decoded, no data packet is output, even if the corresponding line enable bit is set.

Each data packet starts immediately after the EAV code of the preceding line. Figure 52 and Table 86 show the overall structure of the data packet.

Entries within the packet are as follows:

- Fixed preamble sequence of 0x00, 0xFF, and 0xFF.
- DID. The value for the DID marking a Gemstar or CCAP data packet is 0x140 (10-bit value).
- SDID, which contains information about the video line from which data was retrieved, whether the Gemstar transmission was in 1× or 2× format, and whether it was retrieved from an even or odd field.
- Data count byte, giving the number of user data-words that follow.
- User data section.
- Optional padding to ensure that the length of the user data-word section of a packet is a multiple of four bytes (requirement as set in ITU-R BT.1364).
- Checksum byte.

Table 86 lists the values within a generic data packet that is output by the ADV7180 in 8-bit format.

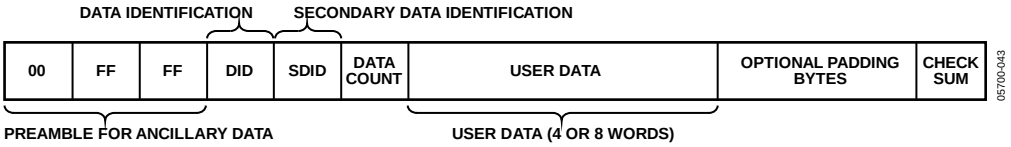


Figure 52. Gemstar- and CCAP-Embedded Data Packet (Generic)

Table 86. Generic Data Output Packet

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	2X	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	DC[1]	DC[0]	0	0	Data count (DC)
6	$\overline{EP}$	EP	0	0	Word1[7:4]				0	0	User data-words
7	$\overline{EP}$	EP	0	0	Word1[3:0]				0	0	User data-words
8	$\overline{EP}$	EP	0	0	Word2[7:4]				0	0	User data-words
9	$\overline{EP}$	EP	0	0	Word2[3:0]				0	0	User data-words
10	$\overline{EP}$	EP	0	0	Word3[7:4]				0	0	User data-words
11	$\overline{EP}$	EP	0	0	Word3[3:0]				0	0	User data-words
12	$\overline{EP}$	EP	0	0	Word4[7:4]				0	0	User data-words
13	$\overline{EP}$	EP	0	0	Word4[3:0]				0	0	User data-words
14	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	0	0	Checksum

Table 87. Data Byte Allocation

2×	Raw Information Bytes Retrieved from the Video Line	GDECAD	User Data-Words (Including Padding)	Padding Bytes	DC[1:0]
1	4	0	8	0	10
1	4	1	4	0	01
0	2	0	4	0	01
0	2	1	4	2	01

Gemstar Bit Names

The following are the Gemstar bit names:

- DID—The data identification value is 0x140 (10-bit value). Care is taken so that in 8-bit systems, the two LSBs do not carry vital information.
- EP and $\overline{EP}$—The EP bit is set to ensure even parity on the D[8:0] data-word. Even parity means there is always an even number of 1s within the D[8:0] bit arrangement. This includes the EP bit. $\overline{EP}$ describes the logic inverse of EP and is output on D[9]. The $\overline{EP}$ is output to ensure that the reserved codes of 00 and FF do not occur.
- EF—Even field identifier. EF = 1 indicates that the data was recovered from a video line on an even field.
- 2×—This bit indicates whether the data sliced was in Gemstar 1× or 2× format. A high indicates 2× format. The 2× bit determines whether the raw information retrieved from the video line was two bytes or four bytes. The state of the GDECAD bit affects whether the bytes are transmitted straight (that is, two bytes transmitted as two bytes) or whether they are split into nibbles (that is, two bytes transmitted as four half bytes). Padding bytes are then added where necessary.
- Line[3:0]—This entry provides a code that is unique for each of the possible 16 source lines of video from which Gemstar data may have been retrieved. Refer to Table 96 and Table 97.
- DC[1:0]—Data count value. The number of UDWs in the packet divided by 4. The number of UDWs in any packet must be an integral number of 4. Padding may be required at the end, as set in ITU-R BT.1364. See Table 87.
- CS[8:2]—The checksum is provided to determine the integrity of the ancillary data packet. It is calculated by summing up D[8:2] of DID, SDID, the data count byte, and all UDWs and ignoring any overflow during the summation. Because all data bytes that are used to calculate the checksum have their two LSBs set to 0, the CS[1:0] bits are also always 0.

$\overline{CS}$[8]—describes the logic inversion of CS[8]. The value $\overline{CS}$[8] is included in the checksum entry of the data packet to ensure that the reserved values of 0x00 and 0xFF do not occur. Table 88 to Table 91 outline the possible data packages.

Gemstar_2× Format, Half-Byte Output Mode

Half-byte output mode is selected by setting GDECAD to 0; full-byte output mode is selected by setting GDECAD to 1. See the GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

Gemstar_1× Format

Half-byte output mode is selected by setting CDECAD to 0, full-byte output mode is selected by setting CDECAD to 1. See the GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

Table 88. Gemstar_2× Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	1	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	1	0	0	0	Data count
6	$\overline{EP}$	EP	0	0	Gemstar Word1[7:4]				0	0	User data-words
7	$\overline{EP}$	EP	0	0	Gemstar Word1[3:0]				0	0	User data-words
8	$\overline{EP}$	EP	0	0	Gemstar Word2[7:4]				0	0	User data-words
9	$\overline{EP}$	EP	0	0	Gemstar Word2[3:0]				0	0	User data-words
10	$\overline{EP}$	EP	0	0	Gemstar Word3[7:4]				0	0	User data-words
11	$\overline{EP}$	EP	0	0	Gemstar Word3[3:0]				0	0	User data-words
12	$\overline{EP}$	EP	0	0	Gemstar Word4[7:4]				0	0	User data-words
13	$\overline{EP}$	EP	0	0	Gemstar Word4[3:0]				0	0	User data-words
14	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 89. Gemstar_2× Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	1	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	Gemstar Word1[7:0]								0	0	User data-words
7	Gemstar Word2[7:0]								0	0	User data-words
8	Gemstar Word3[7:0]								0	0	User data-words
9	Gemstar Word4[7:0]								0	0	User data-words
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 90. Gemstar_1× Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	$\overline{EP}$	EP	0	0	Gemstar Word1[7:4]				0	0	User data-words
7	$\overline{EP}$	EP	0	0	Gemstar Word1[3:0]				0	0	User data-words
8	$\overline{EP}$	EP	0	0	Gemstar Word2[7:4]				0	0	User data-words
9	$\overline{EP}$	EP	0	0	Gemstar Word2[3:0]				0	0	User data-words
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 91. Gemstar_1× Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	Line[3:0]				0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	Gemstar Word1[7:0]								0	0	User data-words
7	Gemstar Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 92. NTSC CCAP Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	1	0	1	1	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	$\overline{EP}$	EP	0	0	CCAP Word1[7:4]				0	0	User data-words
7	$\overline{EP}$	EP	0	0	CCAP Word1[3:0]				0	0	User data-words
8	$\overline{EP}$	EP	0	0	CCAP Word2[7:4]				0	0	User data-words
9	$\overline{EP}$	EP	0	0	CCAP Word2[3:0]				0	0	User data-words
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 93. NTSC CCAP Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	1	0	1	1	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	CCAP Word1[7:0]								0	0	User data-words
7	CCAP Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 94. PAL CCAP Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	1	0	1	0	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	$\overline{EP}$	EP	0	0	CCAP Word1[7:4]				0	0	User data-words
7	$\overline{EP}$	EP	0	0	CCAP Word1[3:0]				0	0	User data-words
8	$\overline{EP}$	EP	0	0	CCAP Word2[7:4]				0	0	User data-words
9	$\overline{EP}$	EP	0	0	CCAP Word2[3:0]				0	0	User data-words
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 95. PAL CCAP Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	$\overline{EP}$	EP	EF	0	1	0	1	0	0	0	SDID
5	$\overline{EP}$	EP	0	0	0	0	0	1	0	0	Data count
6	CCAP Word1[7:0]								0	0	User data-words
7	CCAP Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	$\overline{CS}$[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

NTSC CCAP Data

Half-byte output mode is selected by setting GDECAD to 0, and the full-byte mode is enabled by setting GDECAD to 1. See the GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0] section. The data packet formats are shown in Table 92 and Table 93. Only closed caption data can be embedded in the output data stream.

NTSC closed caption data is sliced on Line 21 of even and odd fields. The corresponding enable bit must be set high. See the GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0] section and the GDECOL[15:0], Gemstar Decoding Odd Lines, Address 0x4A[7:0], Address 0x4B[7:0] section.

PAL CCAP Data

Half-byte output mode is selected by setting GDECAD to 0, and full-byte output mode is selected by setting GDECAD to 1. See the GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0] section. Table 94 and Table 95 list the bytes of the data packet.

Only closed caption data can be embedded in the output data stream. PAL closed caption data is sliced from Line 22 and Line 335. The corresponding enable bits must be set.

See the GDECEL[15:0], Gemstar Decoding Even Lines, Address 0x48[7:0], Address 0x49[7:0] section and the GDECOL[15:0], Gemstar Decoding Odd Lines, Address 0x4A[7:0], Address 0x4B[7:0] section.

GDECEL[15:0], Gemstar Decoding Even Lines, Address 0x48[7:0], Address 0x49[7:0]

The 16 bits of GDECEL[15:0] are interpreted as a collection of 16 individual line decode enable signals. Each bit refers to a line of video in an even field. Setting the bit enables the decoder block trying to find Gemstar or closed caption-compatible data on that particular line. Setting the bit to 0 prevents the decoder from trying to retrieve data. See Table 96 and Table 97.

To retrieve closed caption data services on NTSC (Line 284), GDECEL[11] must be set.

To retrieve closed caption data services on PAL (Line 335), GDECEL[14] must be set.

The default value of GDECEL[15:0] is 0x0000. This setting instructs the decoder not to attempt to decode Gemstar or CCAP data from any line in the even field. Enable Gemstar slicing only on lines where VBI data is expected.

Table 96. NTSC Line Enable Bits and Corresponding Line Numbering

Line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
0	10	GDECOL[0]	Gemstar
1	11	GDECOL[1]	Gemstar
2	12	GDECOL[2]	Gemstar
3	13	GDECOL[3]	Gemstar
4	14	GDECOL[4]	Gemstar
5	15	GDECOL[5]	Gemstar
6	16	GDECOL[6]	Gemstar
7	17	GDECOL[7]	Gemstar
8	18	GDECOL[8]	Gemstar
9	19	GDECOL[9]	Gemstar
10	20	GDECOL[10]	Gemstar
11	21	GDECOL[11]	Gemstar or closed caption
12	22	GDECOL[12]	Gemstar
13	23	GDECOL[13]	Gemstar
14	24	GDECOL[14]	Gemstar
15	25	GDECOL[15]	Gemstar
0	273 (10)	GDECEL[0]	Gemstar
1	274 (11)	GDECEL[1]	Gemstar
2	275 (12)	GDECEL[2]	Gemstar
3	276 (13)	GDECEL[3]	Gemstar
4	277 (14)	GDECEL[4]	Gemstar
5	278 (15)	GDECEL[5]	Gemstar
6	279 (16)	GDECEL[6]	Gemstar
7	280 (17)	GDECEL[7]	Gemstar
8	281 (18)	GDECEL[8]	Gemstar
9	282 (19)	GDECEL[9]	Gemstar
10	283 (20)	GDECEL[10]	Gemstar
11	284 (21)	GDECEL[11]	Gemstar or closed caption
12	285 (22)	GDECEL[12]	Gemstar
13	286 (23)	GDECEL[13]	Gemstar
14	287 (24)	GDECEL[14]	Gemstar
15	288 (25)	GDECEL[15]	Gemstar

GDECOL[15:0], Gemstar Decoding Odd Lines, Address 0x4A[7:0], Address 0x4B[7:0]

The 16 bits of GDECOL[15:0] form a collection of 16 individual line decode enable signals. See Table 96 and Table 97.

To retrieve closed caption data services on NTSC (Line 21), GDECOL[11] must be set.

To retrieve closed caption data services on PAL (Line 22), GDECOL[14] must be set.

The default value of GDECOL[15:0] is 0x0000. This setting instructs the decoder not to attempt to decode Gemstar or CCAP data from any line in the odd field. Enable Gemstar slicing only on lines where VBI data is expected.

GDECAD, Gemstar Decode Ancillary Data Format, Address 0x4C[0]

The decoded data from Gemstar-compatible transmissions or closed caption-compatible transmissions is inserted into the horizontal blanking period of the respective line of video. A potential problem can arise if the retrieved data bytes have a value of 0x00 or 0xFF. In an ITU-R BT.656-compatible data stream, these values are reserved and used only to form a fixed preamble. The GDECAD bit allows the data to be inserted into the horizontal blanking period in two ways:

- Insert all data straight into the data stream, even the reserved values of 0x00 and 0xFF, if they occur. This may violate output data format specification ITU-R BT.1364.
- Split all data into nibbles and insert the half-bytes over double the number of cycles in a 4-bit format.

When GDECAD is 0 (default), the data is split into half-bytes and inserted.

When GDECAD is 1, the data is output straight into the data stream in 8-bit format.

Table 97. PAL Line Enable Bits and Line Numbering

Line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
12	8	GDECOL[0]	Not valid
13	9	GDECOL[1]	Not valid
14	10	GDECOL[2]	Not valid
15	11	GDECOL[3]	Not valid
0	12	GDECOL[4]	Not valid
1	13	GDECOL[5]	Not valid
2	14	GDECOL[6]	Not valid
3	15	GDECOL[7]	Not valid
4	16	GDECOL[8]	Not valid
5	17	GDECOL[9]	Not valid
6	18	GDECOL[10]	Not valid
7	19	GDECOL[11]	Not valid
8	20	GDECOL[12]	Not valid
9	21	GDECOL[13]	Not valid
10	22	GDECOL[14]	Closed caption
11	23	GDECOL[15]	Not valid
12	321 (8)	GDECEL[0]	Not valid
13	322 (9)	GDECEL[1]	Not valid
14	323 (10)	GDECEL[2]	Not valid
15	324 (11)	GDECEL[3]	Not valid
0	325 (12)	GDECEL[4]	Not valid
1	326 (13)	GDECEL[5]	Not valid
2	327 (14)	GDECEL[6]	Not valid
3	328 (15)	GDECEL[7]	Not valid
4	329 (16)	GDECEL[8]	Not valid
5	330 (17)	GDECEL[9]	Not valid
6	331 (18)	GDECEL[10]	Not valid
7	332 (19)	GDECEL[11]	Not valid
8	333 (20)	GDECEL[12]	Not valid
9	334 (21)	GDECEL[13]	Not valid
10	335 (22)	GDECEL[14]	Closed caption
11	336 (23)	GDECEL[15]	Not valid

Letterbox Detection

Incoming video signals may conform to different aspect ratios (16:9 wide screen or 4:3 standard). For certain transmissions in the wide-screen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from the digitally decoded bits that WSS contains.

In the absence of a WSS sequence, letterbox detection can be used to find wide-screen signals. The detection algorithm examines the active video content of lines at the start and end of a field. If black lines are detected, this may indicate that the currently shown picture is in wide-screen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold, and a decision is made as to whether or not a particular line is black. The threshold value needed may depend on the type of input signal; some control is provided via LB_TH[4:0].

Detection at the Start of a Field

The ADV7180 expects a section of at least six consecutive black lines of video at the top of a field. After those lines are detected, LB_LCT[7:0] reports the number of black lines that were actually found. By default, the ADV7180 starts looking for those black lines in sync with the beginning of active video, for example, immediately after the last VBI video line. LB_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line-by-line basis. The detection window closes in the middle of the field.

Detection at the End of a Field

The ADV7180 expects at least six continuous lines of black video at the bottom of a field before reporting the number of lines actually found via the LB_LCB[7:0] value. The activity window for letterbox detection (end of field) starts in the middle of an active field. Its end is programmable via LB_EL[3:0].

Detection at the Midrange

Some transmissions of wide-screen video include subtitles within the lower black box. If the ADV7180 finds at least two black lines followed by some more nonblack video, for example, the subtitle followed by the remainder of the bottom black block, it reports a midcount via LB_LCM[7:0]. If no subtitles are found, LB_LCM[7:0] reports the same number as LB_LCB[7:0].

There is a two-field delay in reporting any line count parameter.

There is no letterbox detected bit. Read the LB_LCT[7:0] and LB_LCB[7:0] register values to determine whether the letterbox-type video is present in the software.

LB_LCT[7:0], Letterbox Line Count Top, Address 0x9B[7:0]; LB_LCM[7:0], Letterbox Line Count Mid, Address 0x9C[7:0]; LB_LCB[7:0], Letterbox Line Count Bottom, Address 0x9D[7:0]

Table 98. LB_LCx Access Information

Signal Name	Address
LB_LCT[7:0]	0x9B
LB_LCM[7:0]	0x9C
LB_LCB[7:0]	0x9D

LB_TH[4:0], Letterbox Threshold Control, Address 0xDC[4:0]

Table 99. LB_TH Function

LB_TH[4:0]	Description
01100 (default)	Default threshold for detection of black lines
01101 to 10000	Increase threshold (need larger active video content before identifying nonblack lines)
00000 to 01011	Decrease threshold (even small noise levels can cause the detection of nonblack lines)

LB_SL[3:0], Letterbox Start Line, Address 0xDD[7:4]

The LB_SL[3:0] bits are set at 0100 by default. For an NTSC signal, this window is from Line 23 to Line 286.

By changing the bits to 0101, the detection window starts on Line 24 and ends on Line 287.

LB_EL[3:0], Letterbox End Line, Address 0xDD[3:0]

The LB_EL[3:0] bits are set at 1101 by default. This means that the letterbox detection window ends with the last active video line. For an NTSC signal, this window is from Line 262 to Line 525.

By changing the bits to 1100, the detection window starts on Line 261 and ends on Line 254.

PIXEL PORT CONFIGURATION

The ADV7180 has a very flexible pixel port that can be configured in a variety of formats to accommodate downstream ICs.

Table 100, Table 101, and Table 102 summarize the various functions that the ADV7180 pins can have in different modes of operation.

The ordering of components, for example, Cr vs. Cb for Channel A, Channel B, and Channel C can be changed. See the SWPC, Swap Pixel Cr/Cb, Address 0x27[7] section. Table 100 indicates the default positions for the Cr/Cb components.

OF_SEL[3:0], Output Format Selection, Address 0x03[5:2]

The modes in which the ADV7180 pixel port can be configured are under the control of OF_SEL[3:0]. See Table 102 for details.

The default LLC frequency output on the LLC pin is approximately 27 MHz. For modes that operate with a nominal data rate of 13.5 MHz (0001, 0010), the clock frequency on the LLC pin stays at the higher rate of 27 MHz. For information on outputting the nominal 13.5 MHz clock on the LLC pin, see the LLC_PAD_SEL[2:0] LLC Output Selection, Address 0x8F[6:4] section.

SWPC, Swap Pixel Cr/Cb, Address 0x27[7]

This bit allows Cr and Cb samples to be swapped.

When SWPC is 0 (default), no swapping is allowed.

When SWPC is 1, the Cr and Cb values can be swapped.

LLC_PAD_SEL[2:0] LLC Output Selection, Address 0x8F[6:4]

The following I^2C write allows the user to select between LLC (nominally at 27 MHz) and LLC (nominally at 13.5 MHz).

The LLC signal is useful for LLC-compatible wide bus (16-bit) output modes. See the OF_SEL[3:0], Output Format Selection, Address 0x03[5:2] section for additional information. The LLC signal and data on the data bus are synchronized. By default, the rising edge of LLC/LLC is aligned with the Y data; the falling edge occurs when the data bus holds C data. The polarity of the clock, and therefore the Y/C assignments to the clock edges, can be altered by using the polarity LLC pin.

When LLC_PAD_SEL is 000, the output is nominally 27 MHz LLC on the LLC pin (default).

When LLC_PAD_SEL is 101, the output is nominally 13.5 MHz LLC on the LLC pin.

Table 100. 64-Lead LQFP P15 to P0 Output/Input Pin Mapping

	Data Port Pins P[15:0]															
Format and Mode	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Video Out, 8-Bit, 4:2:2	YCrCb[7:0]OUT															
Video Out, 16-Bit, 4:2:2	Y[7:0]OUT								CrCb[7:0]OUT							

Table 101. 48-Lead, 40-Lead, and 32-Lead Devices P7 to P0 Output/Input Pin Mapping

	Data Port Pins P[7:0]							
Format and Mode	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Video Out, 8-Bit, 4:2:2	YCrCb[7:0]OUT							

Table 102. ADV7180 Standard Definition Pixel Port Modes

		64-Lead LQFP P[15:0]		48-Lead LQFP, 40-Lead LFCSP, or 32-Lead LFCSP
OF_SEL[3:0]	**Format**	**P[15:8]**	**P[7:0]**	**P[7:0]**
0000 to 0001	Reserved	Reserved, do not use		
0010	16-bit at LLC 4:2:2	Y[7:0]	CrCb[7:0]	Not valid
0011 (default)	8-bit at LLC 4:2:2 (default)	YCrCb[7:0]	Three-state	YCrCb[7:0]
0100 to 1111	Reserved	Reserved, do not use		

GPO CONTROL

The 64-lead and 48-lead LQFP has four general-purpose outputs (GPO). These outputs allow the user to control other devices in a system via the I²C port of the device.

The 40-lead and 32-lead LFCSP do not have GPO pins.

GPO_ENABLE, General-Purpose Output Enable, Address 0x59[4]

When GPO_ENABLE is set to 0, all GPO pins are three-stated.

When GPO_ENABLE is set to 1, all GPO pins are in a driven state. The polarity output from each GPO is controlled by GPO[3:0] for the 64-lead and 48-lead LQFP.

GPO[3:0], General-Purpose Outputs, Address 0x59[3:0]

Individual control of the four GPO ports is achieved using GPO[3:0].

GPO_ENABLE must be set to 1 for the GPO pins to become active.

GPO[0]

When GPO[0] is set to 0, Logic 0 is output from the GPO0 pin.

When GPO[0] is set to 1, Logic 1 is output from the GPO0 pin.

GPO[1]

When GPO[1] is set to 0, Logic 0 is output from the GPO1 pin.

When GPO[1] is set to 1, Logic 1 is output from the GPO1 pin.

GPO[2]

When GPO[2] is set to 0, Logic is output from the GPO2 pin.

When GPO[2] is set to 1, Logic 1 is output from the GPO2 pin.

GPO[3]

When GPO[3] is set to 0, Logic 0 is output from the GPO3 pin.

When GPO[3] is set to 1, Logic 1 is output from the GPO3 pin.

Table 103. General-Purpose Output Truth Table

GPO_ENABLE	GPO[3:0]	GPO3	GPO2	GPO1	GPO0
0	XXXX[1]	Z	Z	Z	Z
1	0000	0	0	0	0
1	0001	0	0	0	1
1	0010	0	0	1	0
1	0011	0	0	1	1
1	0100	0	1	0	0
1	0101	0	1	0	1
1	0110	0	1	1	0
1	0111	0	1	1	1
1	1000	1	0	0	0
1	1001	1	0	0	1
1	1010	1	0	1	0
1	1011	1	0	1	1
1	1100	1	1	0	0
1	1101	1	1	0	1
1	1110	1	1	1	0
1	1111	1	1	1	1

[1] X indicates any value.

MPU PORT DESCRIPTION

The ADV7180 supports a 2-wire (I^2C-compatible) serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7180 and the system I^2C master controller. Each slave device is recognized by a unique address. The ADV7180 I^2C port allows the user to set up and configure the decoder and to read back the captured VBI data. The ADV7180 has four possible slave addresses for both read and write operations, depending on the logic level of the ALSB pin. The four unique addresses are shown in Table 104. The ADV7180 ALSB pin controls Bit 1 of the slave address. By altering the ALSB, it is possible to control two ADV7180 devices in an application without the conflict of using the same slave address. The LSB (Bit 0) sets either a read or write operation. Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

Table 104. I^2C Address for ADV7180

ALSB	R/$\overline{W}$	Slave Address
0	0	0x40
0	1	0x41
1	0	0x42
1	1	0x43

To control the device on the bus, a specific protocol must be followed. First, the master initiates a data transfer by establishing a start condition, which is defined by a high-to-low transition on SDATA while SCLK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7180 acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has 249 subaddresses to enable access to the internal registers. Therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7180 does not issue an acknowledge and returns to the idle condition.

In auto-increment mode, if the user exceeds the highest subaddress, the following action is taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the ADV7180, and the part returns to the idle condition.

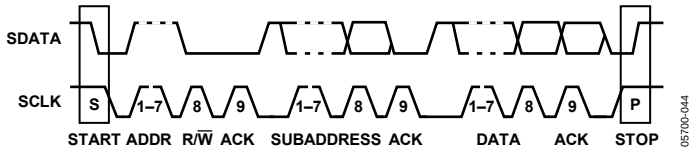


Figure 53. Bus Data Transfer

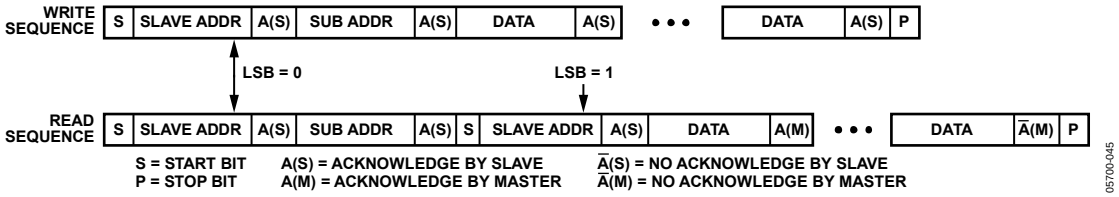


Figure 54. Read and Write Sequence

REGISTER ACCESS

The MPU can write to or read from all of the ADV7180 registers except the subaddress register, which is write only. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is then performed from or to the target address, which increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following sections describe the configuration for each register. The communication register is an 8-bit, write-only register. After the part is accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place. Table 105 lists the various operations under the control of the subaddress register for the control port.

SUB_USR_EN, Address 0x0E[5]

This bit splits the register map at Register 0x40.

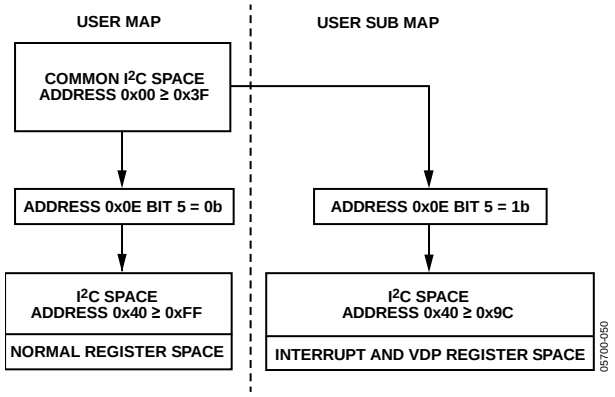


Figure 55. Register Access—User Map and User Sub Map

I²C SEQUENCER

An I²C sequencer is used when a parameter exceeds eight bits and is therefore distributed over two or more I²C registers, for example, HSB[10:0].

When such a parameter is changed using two or more I²C write operations, the parameter may hold an invalid value for the time between the first I²C being completed and the last I²C being completed. In other words, the top bits of the parameter may hold the new value while the remaining bits of the parameter still hold the previous value.

To avoid this problem, the I²C sequencer holds the updated bits of the parameter in local memory, and all bits of the parameter are updated together once the last register write operation has completed.

The correct operation of the I²C sequencer relies on the following:

- All I²C registers for the parameter in question must be written to in order of ascending addresses. For example, for HSB[10:0], write to Address 0x34 first, followed by Address 0x35, and so on.
- No other I²C can take place between the two (or more) I²C writes for the sequence. For example, for HSB[10:0], write to Address 0x34 first, immediately followed by Address 0x35, and so on.

I²C REGISTER MAPS

Table 105. Main Register Map Details (User Map)

Address													Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0		Value	(Hex)
0	00	Input control	RW	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]		00000000	00
1	01	Video selection	RW		ENHSPLL	BETACAM		ENVSPROC	SQPE				11001000	C8
3	03	Output control	RW	VBI_EN	TOD	OF_SEL[3]	OF_SEL[2]	OF_SEL[1]	OF_SEL[0]		SD_DUP_AV		00001100	0C
4	04	Extended output control	RW	BT.656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	Range		01xx0101	45
5	05	Reserved												
6	06	Reserved												
7	07	Autodetect enable	RW	AD_SECS25_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN		01111111	7F
8	08	Contrast	RW	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]		10000000	80
9	09	Reserved												
10	0A	Brightness	RW	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]		00000000	00
11	0B	Hue	RW	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]		00000000	00
12	0C	Default Value Y	RW	DEF_Y[5]	DEF_Y[4]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_VAL_ AUTO_EN	DEF_VAL_EN		00110110	36
13	0D	Default Value C	RW	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]		01111100	7C
14	0E	ADI Control 1	RW			SUB_USR_EN							00000000	00
15	0F	Power management	RW	Reset		PWRDWN			PDBP				00000000	00
16	10	Status 1	R	COL_KILL	AD_RESULT[2]	AD_RESULT[1]	AD_RESULT[0]	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK			
17	11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]		00011100	1C
18	12	Status 2	R			FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET			
19	13	Status 3	R	PAL_SW_LOCK	Interlaced	STD FLD LEN	FREE_RUN_ACT	Reserved	SD_OP_50Hz	GEMD	INST_HLOCK			
20	14	Analog clamp control	RW			VCLEN	CCLEN						00010010	12
21	15	Digital Clamp Control 1	RW		DCT[1]	DCT[0]	DCFE						0000xxxx	00
22	16	Reserved												
23	17	Shaping Filter Control 1	RW	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]		00000001	01
24	18	Shaping Filter Control 2	RW	WYSFMOVR			WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]		10010011	93
25	19	Comb filter control	RW					NSFSEL[1]	NSFSEL[0]	PSFSEL[1]	PSFSEL[0]		11110001	F1
29	1D	ADI Control 2	RW	TRI_LLC	EN28XTAL								01000xxx	40
39	27	Pixel delay control	RW	SWPC	AUTO_PDC_EN	CTA[2]	CTA[1]	CTA[0]		LTA[1]	LTA[0]		01011000	58
43	2B	Misc gain control	RW		CKE						PW_UPD		11100001	E1
44	2C	AGC mode control	RW		LAGC[2]	LAGC[1]	LAGC[0]			CAGC[1]	CAGC[0]		10101110	AE
45	2D	Chroma Gain Control 1	W	CAGT[1]	CAGT[0]			CMG[11]	CMG[10]	CMG[9]	CMG[8]		11110100	F4
45	2D	Chroma Gain 1	R					CG[11]	CG[10]	CG[9]	CG[8]			
46	2E	Chroma Gain Control 2	W	CMG[7]	CMG[6]	CMG[5]	CMG[4]	CMG[3]	CMG[2]	CMG[1]	CMG[0]		00000000	00
46	2E	Chroma Gain 2	R	CG[7]	CG[6]	CG[5]	CG[4]	CG[3]	CG[2]	CG[1]	CG[0]			
47	2F	Luma Gain Control 1	W	LAGT[1]	LAGT[0]			LMG[11]	LMG[10]	LMG[9]	LMG[8]		1111xxxx	F0
47	2F	Luma Gain 1	R					LG[11]	LG[10]	LG[9]	LG[8]			
48	30	Luma Gain Control 2	W	LMG[7]	LMG[6]	LMG[5]	LMG[4]	LMG[3]	LMG[2]	LMG[1]	LMG[0]		xxxxxxxx	00
48	30	Luma Gain 2	R	LG[7]	LG[6]	LG[5]	LG[4]	LG[3]	LG[2]	LG[1]	LG[0]			
49	31	VS/FIELD Control 1	RW				NEWAVMODE	HVSTIM					00010010	12
50	32	VS/FIELD Control 2	RW	VSBHO	VSBHE								01000001	41
51	33	VS/FIELD Control 3	RW	VSEHO	VSEHE								10000100	84
52	34	HS Position Control 1	RW		HSB[10]	HSB[9]	HSB[8]		HSE[10]	HSE[9]	HSE[8]		00000000	00
53	35	HS Position Control 2	RW	HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]		00000010	02
54	36	HS Position Control 3	RW	HSE[7]	HSE[6]	HSE[5]	HSE[4]	HSE[3]	HSE[2]	HSE[1]	HSE[0]		00000000	00
55	37	Polarity	RW	PHS		PVS		PF			PCLK		00000001	01
56	38	NTSC comb control	RW	CTAPSN[1]	CTAPSN[0]	CCMN[2]	CCMN[1]	CCMN[0]	YCMN[2]	YCMN[1]	YCMN[0]		10000000	80
57	39	PAL comb control	RW	CTAPSP[1]	CTAPSP[0]	CCMP[2]	CCMP[1]	CCMP[0]	YCMP[2]	YCMP[1]	YCMP[0]		11000000	C0
58	3A	ADC control	RW					PWRDWN_MUX_0	PWRDWN_MUX_1	PWRDWN_MUX_2	MUX PDN override		00010000	10
61	3D	Manual window control	RW		CKILLTHR[2]	CKILLTHR[1]	CKILLTHR[0]						01110010	B2
65	41	Resample control	RW		SFL_INV								00000001	01
72	48	Gemstar Control 1	RW	GDECEL[15]	GDECEL[14]	GDECEL[13]	GDECEL[12]	GDECEL[11]	GDECEL[10]	GDECEL[9]	GDECEL[8]		00000000	00
73	49	Gemstar Control 2	RW	GDECEL[7]	GDECEL[6]	GDECEL[5]	GDECEL[4]	GDECEL[3]	GDECEL[2]	GDECEL[1]	GDECEL[0]		00000000	00
74	4A	Gemstar Control 3	RW	GDECOL[15]	GDECOL[14]	GDECOL[13]	GDECOL[12]	GDECOL[11]	GDECOL[10]	GDECOL[9]	GDECOL[8]		00000000	00
75	4B	Gemstar Control 4	RW	GDECOL[7]	GDECOL[6]	GDECOL[5]	GDECOL[4]	GDECOL[3]	GDECOL[2]	GDECOL[1]	GDECOL[0]		00000000	00
76	4C	Gemstar Control 5	RW					GDE_SEL_OLD_ADF			GDECAD		xxxx0000	00
77	4D	CTI DNR Control 1	RW			DNR_EN		CTI_AB[1]	CTI_AB[0]	CTI_AB_EN	CTI_EN		11101111	EF
78	4E	CTI DNR Control 2	RW	CTI_C_TH[7]	CTI_C_TH[6]	CTI_C_TH[5]	CTI_C_TH[4]	CTI_C_TH[3]	CTI_C_TH[2]	CTI_C_TH[1]	CTI_C_TH[0]		00001000	08
80	50	CTI DNR Control 4	RW	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]		00001000	08
81	51	Lock count	RW	FSCLE	SRLS	COL[2]	COL[1]	COL[0]	CIL[2]	CIL[1]	CIL[0]		00100100	24
82	52	CVBS_TRIM	RW					CVBS_IBIAS[3]	CVBS_IBIAS[2]	CVBS_IBIAS[1]	CVBS_IBIAS[0]		00001011	0B
88	58	VS/FIELD pin control[1]	RW						ADC sampling control		VS/FIELD		00000000	00
89	59	General-purpose outputs[2]	RW				GPO_ENABLE	GPO[3]	GPO[2]	GPO[1]	GPO[0]		00000000	00
143	8F	Free-Run Line Length 1	W		LLC_PAD_SEL[2]	LLC_PAD_ SEL[1]	LLC_PAD_ SEL[0]						00000000	00
153	99	CCAP 1	R	CCAP1[7]	CCAP1[6]	CCAP1[5]	CCAP1[4]	CCAP1[3]	CCAP1[2]	CCAP1[1]	CCAP1[0]			

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	(Hex)
154	9A	CCAP 2	R	CCAP2[7]	CCAP2[6]	CCAP2[5]	CCAP2[4]	CCAP2[3]	CCAP2[2]	CCAP2[1]	CCAP2[0]		
155	9B	Letterbox 1	R	LB_LCT[7]	LB_LCT[6]	LB_LCT[5]	LB_LCT[4]	LB_LCT[3]	LB_LCT[2]	LB_LCT[1]	LB_LCT[0]		
156	9C	Letterbox 2	R	LB_LCM[7]	LB_LCM[6]	LB_LCM[5]	LB_LCM[4]	LB_LCM[3]	LB_LCM[2]	LB_LCM[1]	LB_LCM[0]		
157	9D	Letterbox 3	R	LB_LCB[7]	LB_LCB[6]	LB_LCB[5]	LB_LCB[4]	LB_LCB[3]	LB_LCB[2]	LB_LCB[1]	LB_LCB[0]		
178	B2	CRC enable	W						CRC_ENABLE			00011100	1C
195	C3	ADC Switch 1	RW	Reserved	MUX1[2]	MUX1[1]	MUX1[0]	Reserved	MUX0[2]	MUX0[1]	MUX0[0]	xxxxxxxx	00
196	C4	ADC Switch 2	RW	MAN_MUX_EN				Reserved	MUX2[2]	MUX2[1]	MUX2[0]	0xxxxxxx	00
220	DC	Letterbox Control 1	RW				LB_TH[4]	LB_TH[3]	LB_TH[2]	LB_TH[1]	LB_TH[0]	10101100	AC
221	DD	Letterbox Control 2	RW	LB_SL[3]	LB_SL[2]	LB_SL[1]	LB_SL[0]	LB_EL[3]	LB_EL[2]	LB_EL[1]	LB_EL[0]	01001100	4C
222	DE	ST Noise Readback 1	R					ST_NOISE_VLD	ST_NOISE[10]	ST_NOISE[9]	ST_NOISE[8]		
223	DF	ST Noise Readback 2	R	ST_NOISE[7]	ST_NOISE[6]	ST_NOISE[5]	ST_NOISE[4]	ST_NOISE[3]	ST_NOISE[2]	ST_NOISE[1]	ST_NOISE[0]		
224	E0	Reserved											
225	E1	SD Offset Cb	RW	SD_OFF_Cb[7]	SD_OFF_Cb[6]	SD_OFF_Cb[5]	SD_OFF_Cb[4]	SD_OFF_Cb[3]	SD_OFF_Cb[2]	SD_OFF_Cb[1]	SD_OFF_Cb[0]	10000000	80
226	E2	SD Offset Cr	RW	SD_OFF_Cr[7]	SD_OFF_Cr[6]	SD_OFF_Cr[5]	SD_OFF_Cr[4]	SD_OFF_Cr[3]	SD_OFF_Cr[2]	SD_OFF_Cr[1]	SD_OFF_Cr[0]	10000000	80
227	E3	SD Saturation Cb	RW	SD_SAT_Cb[7]	SD_SAT_Cb[6]	SD_SAT_Cb[5]	SD_SAT_Cb[4]	SD_SAT_Cb[3]	SD_SAT_Cb[2]	SD_SAT_Cb[1]	SD_SAT_Cb[0]	10000000	80
228	E4	SD Saturation Cr	RW	SD_SAT_Cr[7]	SD_SAT_Cr[6]	SD_SAT_Cr[5]	SD_SAT_Cr[4]	SD_SAT_Cr[3]	SD_SAT_Cr[2]	SD_SAT_Cr[1]	SD_SAT_Cr[0]	10000000	80
229	E5	NTSC V bit begin	RW	NVBEGDELO	NVBEGDELE	NVBEGSIGN	NVBEG[4]	NVBEG[3]	NVBEG[2]	NVBEG[1]	NVBEG[0]	00100101	25
230	E6	NTSC V bit end	RW	NVENDDELO	NVENDDELE	NVENDSIGN	NVEND[4]	NVEND[3]	NVEND[2]	NVEND[1]	NVEND[0]	00000100	04
231	E7	NTSC F bit toggle	RW	NFTOGDELO	NFTOGDELE	NFTOGSIGN	NFTOG[4]	NFTOG[3]	NFTOG[2]	NFTOG[1]	NFTOG[0]	01100011	63
232	E8	PAL V bit begin	RW	PVBEGDELO	PVBEGDELE	PVBEGSIGN	PVBEG[4]	PVBEG[3]	PVBEG[2]	PVBEG[1]	PVBEG[0]	01100101	65
233	E9	PAL V bit end	RW	PVENDDELO	PVENDDELE	PVENDSIGN	PVEND[4]	PVEND[3]	PVEND[2]	PVEND[1]	PVEND[0]	00010100	14
234	EA	PAL F bit toggle	RW	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG[4]	PFTOG[3]	PFTOG[2]	PFTOG[1]	PFTOG[0]	01100011	63
235	EB	Vblank Control 1	RW	NVBIOLCM[1]	NVBIOLCM[0]	NVBIELCM[1]	NVBIELCM[0]	PVBIOLCM[1]	PVBIOLCM[0]	PVBIELCM[1]	PVBIELCM[0]	01010101	55
236	EC	Vblank Control 2	RW	NVBIOCCM[1]	NVBIOCCM[0]	NVBIECCM[1]	NVBIECCM[0]	PVBIOCCM[1]	PVBIOCCM[0]	PVBIECCM[1]	PVBIECCM[0]	01010101	55
243	F3	AFE_CONTROL 1	RW					AA_FILT_ MAN_OVR	AA_FILT_EN[2]	AA_FILT_EN[1]	AA_FILT_EN[0]	00000000	00
244	F4	Drive strength	RW			DR_STR[1]	DR_STR[0]	DR_STR_C[1]	DR_STR_C[0]	DR_STR_S[1]	DR_STR_S[0]	xx010101	15
248	F8	IF comp control	RW						IFFILTSEL[2]	IFFILTSEL[1]	IFFILTSEL[0]	00000000	00
249	F9	VS mode control	RW					VS_COAST_ MODE[1]	VS_COAST_ MODE[0]	EXTEND_VS_ MIN_FREQ	EXTEND_VS_ MAX_FREQ	00000011	03
251	FB	Peaking control	RW	PEAKING_ GAIN[7]	PEAKING_ GAIN[6]	PEAKING_ GAIN[5]	PEAKING_ GAIN[4]	PEAKING_ GAIN[3]	PEAKING_ GAIN[2]	PEAKING_ GAIN[1]	PEAKING_ GAIN[0]	01000000	40
252	FC	Coring threshold	RW	DNR_TH2[7]	DNR_TH2[6]	DNR_TH2[5]	DNR_TH2[4]	DNR_TH2[3]	DNR_TH2[2]	DNR_TH2[1]	DNR_TH2[0]	00000100	04

[1] This feature applies to the 48-lead, 40-lead, and 32-lead LFCSP only because VS or FIELD is shared on a single pin.
[2] This feature applies to the 64-lead and 48-lead LQFP only.

Table 106. Interrupt and VDP System Register Map Details (User Sub Map)[1, 2]

Address														
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
64	40	Interrupt Configuration 1	RW	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	MV_INTRQ_SEL[1]	MV_INTRQ_SEL[0]		MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]	0001x000	10
66	42	Interrupt Status 1	R		MV_PS_CS_Q	SD_FR_CHNG_Q				SD_UNLOCK_Q	SD_LOCK_Q		
67	43	Interrupt Clear 1	W		MV_PS_CS_CLR	SD_FR_CHNG_CLR				SD_UNLOCK_CLR	SD_LOCK_CLR	x0000000	00
68	44	Interrupt Mask 1	RW		MV_PS_CS_MSKB	SD_FR_CHNG_MSKB				SD_UNLOCK_MSKB	SD_LOCK_MSKB	x0000000	00
69	45	Raw Status 1	R	MPU_STIM_INTRQ			EVEN_FIELD				CCAPD		
70	46	Interrupt Status 2	R	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q			GEMD_Q	CCAPD_Q		
71	47	Interrupt Clear 2	W	MPU_STIM_INTRQ_CLR			SD_FIELD_CHNGD_CLR			GEMD_CLR	CCAPD_CLR	0xx00000	00
72	48	Interrupt Mask 2	RW	MPU_STIM_INTRQ_MSKB			SD_FIELD_CHNGD_MSKB			GEMD_MSKB	CCAPD_MSKB	0xx00000	00
73	49	Raw Status 2	R				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz		
74	4A	Interrupt Status 3	R			PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q		
75	4B	Interrupt Clear 3	W			PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	xx000000	00
76	4C	Interrupt Mask 3	RW			PAL_SW_LK_CHNG_MSKB	SCM_LOCK_CHNG_MSKB	SD_AD_CHNG_MSKB	SD_H_LOCK_CHNG_MSKB	SD_V_LOCK_CHNG_MSKB	SD_OP_CHNG_MSKB	xx000000	00
78	4E	Interrupt Status 4	R		VDP_VITC_Q		VDP_GS_VPS_PDC_UTC_CHNG_Q		VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q		
79	4F	Interrupt Clear 4	W		VDP_VITC_CLR		VDP_GS_VPS_PDC_UTC_CHNG_CLR		VDP_CGMS_WSS_CHNGD_CLR		VDP_CCAPD_CLR	00x0x0x0	00
80	50	Interrupt Mask 4	RW		VDP_VITC_MSKB		VDP_GS_VPS_PDC_UTC_CHNG_MSKB		VDP_CGMS_WSS_CHNGD_MSKB		VDP_CCAPD_MSKB	00x0x0x0	00
96	60	VDP_Config_1	RW					WST_PKT_DECODE_DISABLE	VDP_TTXT_TYPE_MAN_ENABLE	VDP_TTXT_TYPE_MAN[1]	VDP_TTXT_TYPE_MAN[0]	10001000	88
97	61	VDP_Config_2	RW				AUTO_DETECT_GS_TYPE					0001xx00	10
98	62	VDP_ADF_Config_1	RW	ADF_ENABLE	ADF_MODE[1]	ADF_MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]	00010101	15
99	63	VDP_ADF_Config_2	RW	DUPLICATE_ADF		ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]	0x101010	2A
100	64	VDP_LINE_00E	RW	MAN_LINE_PGM				VBI_DATA_P318[3]	VBI_DATA_P318[2]	VBI_DATA_P318[1]	VBI_DATA_P318[0]	0xxx0000	00
101	65	VDP_LINE_00F	RW	VBI_DATA_P6_N23[3]	VBI_DATA_P6_N23[2]	VBI_DATA_P6_N23[1]	VBI_DATA_P6_N23[0]	VBI_DATA_P319_N286[3]	VBI_DATA_P319_N286[2]	VBI_DATA_P319_N286[1]	VBI_DATA_P319_N286[0]	00000000	00
102	66	VDP_LINE_010	RW	VBI_DATA_P7_N24[3]	VBI_DATA_P7_N24[2]	VBI_DATA_P7_N24[1]	VBI_DATA_P7_N24[0]	VBI_DATA_P320_N287[3]	VBI_DATA_P320_N287[2]	VBI_DATA_P320_N287[1]	VBI_DATA_P320_N287[0]	00000000	00
103	67	VDP_LINE_011	RW	VBI_DATA_P8_N25[3]	VBI_DATA_P8_N25[2]	VBI_DATA_P8_N25[1]	VBI_DATA_P8_N25[0]	VBI_DATA_P321_N288[3]	VBI_DATA_P321_N288[2]	VBI_DATA_P321_N288[1]	VBI_DATA_P321_N288[0]	00000000	00
104	68	VDP_LINE_012	RW	VBI_DATA_P9[3]	VBI_DATA_P9[2]	VBI_DATA_P9[1]	VBI_DATA_P9[0]	VBI_DATA_P322[3]	VBI_DATA_P322[2]	VBI_DATA_P322[1]	VBI_DATA_P322[0]	00000000	00
105	69	VDP_LINE_013	RW	VBI_DATA_P10[3]	VBI_DATA_P10[2]	VBI_DATA_P10[1]	VBI_DATA_P10[0]	VBI_DATA_P323[3]	VBI_DATA_P323[2]	VBI_DATA_P323[1]	VBI_DATA_P323[0]	00000000	00
106	6A	VDP_LINE_014	RW	VBI_DATA_P11[3]	VBI_DATA_P11[2]	VBI_DATA_P11[1]	VBI_DATA_P11[0]	VBI_DATA_P324_N272[3]	VBI_DATA_P324_N272[2]	VBI_DATA_P324_N272[1]	VBI_DATA_P324_N272[0]	00000000	00
107	6B	VDP_LINE_015	RW	VBI_DATA_P12_N10[3]	VBI_DATA_P12_N10[2]	VBI_DATA_P12_N10[1]	VBI_DATA_P12_N10[0]	VBI_DATA_P325_N273[3]	VBI_DATA_P325_N273[2]	VBI_DATA_P325_N273[1]	VBI_DATA_P325_N273[0]	00000000	00
108	6C	VDP_LINE_016	RW	VBI_DATA_P13_N11[3]	VBI_DATA_P13_N11[2]	VBI_DATA_P13_N11[1]	VBI_DATA_P13_N11[0]	VBI_DATA_P326_N274[3]	VBI_DATA_P326_N274[2]	VBI_DATA_P326_N274[1]	VBI_DATA_P326_N274[0]	00000000	00
109	6D	VDP_LINE_017	RW	VBI_DATA_P14_N12[3]	VBI_DATA_P14_N12[2]	VBI_DATA_P14_N12[1]	VBI_DATA_P14_N12[0]	VBI_DATA_P327_N275[3]	VBI_DATA_P327_N275[2]	VBI_DATA_P327_N275[1]	VBI_DATA_P327_N275[0]	00000000	00
110	6E	VDP_LINE_018	RW	VBI_DATA_P15_N13[3]	VBI_DATA_P15_N13[2]	VBI_DATA_P15_N13[1]	VBI_DATA_P15_N13[0]	VBI_DATA_P328_N276[3]	VBI_DATA_P328_N276[2]	VBI_DATA_P328_N276[1]	VBI_DATA_P328_N276[0]	00000000	00
111	6F	VDP_LINE_019	RW	VBI_DATA_P16_N14[3]	VBI_DATA_P16_N14[2]	VBI_DATA_P16_N14[1]	VBI_DATA_P16_N14[0]	VBI_DATA_P329_N277[3]	VBI_DATA_P329_N277[2]	VBI_DATA_P329_N277[1]	VBI_DATA_P329_N277[0]	00000000	00
112	70	VDP_LINE_01A	RW	VBI_DATA_P17_N15[3]	VBI_DATA_P17_N15[2]	VBI_DATA_P17_N15[1]	VBI_DATA_P17_N15[0]	VBI_DATA_P330_N278[3]	VBI_DATA_P330_N278[2]	VBI_DATA_P330_N278[1]	VBI_DATA_P330_N278[0]	00000000	00
113	71	VDP_LINE_01B	RW	VBI_DATA_P18_N16[3]	VBI_DATA_P18_N16[2]	VBI_DATA_P18_N16[1]	VBI_DATA_P18_N16[0]	VBI_DATA_P331_N279[3]	VBI_DATA_P331_N279[2]	VBI_DATA_P331_N279[1]	VBI_DATA_P331_N279[0]	00000000	00
114	72	VDP_LINE_01C	RW	VBI_DATA_P19_N17[3]	VBI_DATA_P19_N17[2]	VBI_DATA_P19_N17[1]	VBI_DATA_P19_N17[0]	VBI_DATA_P332_N280[3]	VBI_DATA_P332_N280[2]	VBI_DATA_P332_N280[1]	VBI_DATA_P332_N280[0]	00000000	00
115	73	VDP_LINE_01D	RW	VBI_DATA_P20_N18[3]	VBI_DATA_P20_N18[2]	VBI_DATA_P20_N18[1]	VBI_DATA_P20_N18[0]	VBI_DATA_P333_N281[3]	VBI_DATA_P333_N281[2]	VBI_DATA_P333_N281[1]	VBI_DATA_P333_N281[0]	00000000	00
116	74	VDP_LINE_01E	RW	VBI_DATA_P21_N19[3]	VBI_DATA_P21_N19[2]	VBI_DATA_P21_N19[1]	VBI_DATA_P21_N19[0]	VBI_DATA_P334_N282[3]	VBI_DATA_P334_N282[2]	VBI_DATA_P334_N282[1]	VBI_DATA_P334_N282[0]	00000000	00
117	75	VDP_LINE_01F	RW	VBI_DATA_P22_N20[3]	VBI_DATA_P22_N20[2]	VBI_DATA_P22_N20[1]	VBI_DATA_P22_N20[0]	VBI_DATA_P335_N283[3]	VBI_DATA_P335_N283[2]	VBI_DATA_P335_N283[1]	VBI_DATA_P335_N283[0]	00000000	00

Address													
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
118	76	VDP_LINE_020	RW	VBI_DATA_P23_N21[3]	VBI_DATA_P23_N21[2]	VBI_DATA_P23_N21[1]	VBI_DATA_P23_N21[0]	VBI_DATA_P336_N284[3]	VBI_DATA_P336_N284[2]	VBI_DATA_P336_N284[1]	VBI_DATA_P336_N284[0]	00000000	00
119	77	VDP_LINE_021	RW	VBI_DATA_P24_N22[3]	VBI_DATA_P24_N22[2]	VBI_DATA_P24_N22[1]	VBI_DATA_P24_N22[0]	VBI_DATA_P337_N285[3]	VBI_DATA_P337_N285[2]	VBI_DATA_P337_N285[1]	VBI_DATA_P337_N285[0]	00000000	00
120	78	VDP_STATUS	R	TTXT_AVL	VITC_AVL	GS_DATA_TYPE	GS_PDC_VPS_UTC_AVL		CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL		
120	78	VDP_STATUS_CLEAR	W		VITC_CLEAR		GS_PDC_VPS_UTC_CLEAR		CGMS_WSS_CLEAR		CC_CLEAR	00000000	00
121	79	VDP_CCAP_DATA_0	R	CCAP_BYTE_1[7]	CCAP_BYTE_1[6]	CCAP_BYTE_1[5]	CCAP_BYTE_1[4]	CCAP_BYTE_1[3]	CCAP_BYTE_1[2]	CCAP_BYTE_1[1]	CCAP_BYTE_1[0]		
122	7A	VDP_CCAP_DATA_1	R	CCAP_BYTE_2[7]	CCAP_BYTE_2[6]	CCAP_BYTE_2[5]	CCAP_BYTE_2[4]	CCAP_BYTE_2[3]	CCAP_BYTE_2[2]	CCAP_BYTE_2[1]	CCAP_BYTE_2[0]		
125	7D	VDP_CGMS_WSS_DATA_0	R					CGMS_CRC[5]	CGMS_CRC[4]	CGMS_CRC[3]	CGMS_CRC[2]		
126	7E	VDP_CGMS_WSS_DATA_1	R	CGMS_CRC[1]	CGMS_CRC[0]	CGMS_WSS[13]	CGMS_WSS[12]	CGMS_WSS[11]	CGMS_WSS[10]	CGMS_WSS[9]	CGMS_WSS[8]		
127	7F	VDP_CGMS_WSS_DATA_2	R	CGMS_WSS[7]	CGMS_WSS[6]	CGMS_WSS[5]	CGMS_WSS[4]	CGMS_WSS[3]	CGMS_WSS[2]	CGMS_WSS[1]	CGMS_WSS[0]		
132	84	VDP_GS_VPS_PDC_UTC_0	R	GS_VPS_PDC_UTC_BYTE_0[7]	GS_VPS_PDC_UTC_BYTE_0[6]	GS_VPS_PDC_UTC_BYTE_0[5]	GS_VPS_PDC_UTC_BYTE_0[4]	GS_VPS_PDC_UTC_BYTE_0[3]	GS_VPS_PDC_UTC_BYTE_0[2]	GS_VPS_PDC_UTC_BYTE_0[1]	GS_VPS_PDC_UTC_BYTE_0[0]		
133	85	VDP_GS_VPS_PDC_UTC_1	R	GS_VPS_PDC_UTC_BYTE_1[7]	GS_VPS_PDC_UTC_BYTE_1[6]	GS_VPS_PDC_UTC_BYTE_1[5]	GS_VPS_PDC_UTC_BYTE_1[4]	GS_VPS_PDC_UTC_BYTE_1[3]	GS_VPS_PDC_UTC_BYTE_1[2]	GS_VPS_PDC_UTC_BYTE_1[1]	GS_VPS_PDC_UTC_BYTE_1[0]		
134	86	VDP_GS_VPS_PDC_UTC_2	R	GS_VPS_PDC_UTC_BYTE_2[7]	GS_VPS_PDC_UTC_BYTE_2[6]	GS_VPS_PDC_UTC_BYTE_2[5]	GS_VPS_PDC_UTC_BYTE_2[4]	GS_VPS_PDC_UTC_BYTE_2[3]	GS_VPS_PDC_UTC_BYTE_2[2]	GS_VPS_PDC_UTC_BYTE_2[1]	GS_VPS_PDC_UTC_BYTE_2[0]		
135	87	VDP_GS_VPS_PDC_UTC_3	R	GS_VPS_PDC_UTC_BYTE_3[7]	GS_VPS_PDC_UTC_BYTE_3[6]	GS_VPS_PDC_UTC_BYTE_3[5]	GS_VPS_PDC_UTC_BYTE_3[4]	GS_VPS_PDC_UTC_BYTE_3[3]	GS_VPS_PDC_UTC_BYTE_3[2]	GS_VPS_PDC_UTC_BYTE_3[1]	GS_VPS_PDC_UTC_BYTE_3[0]		
136	88	VDP_VPS_PDC_UTC_4	R	VPS_PDC_UTC_BYTE_4[7]	VPS_PDC_UTC_BYTE_4[6]	VPS_PDC_UTC_BYTE_4[5]	VPS_PDC_UTC_BYTE_4[4]	VPS_PDC_UTC_BYTE_4[3]	VPS_PDC_UTC_BYTE_4[2]	VPS_PDC_UTC_BYTE_4[1]	VPS_PDC_UTC_BYTE_4[0]		
137	89	VDP_VPS_PDC_UTC_5	R	VPS_PDC_UTC_BYTE_5[7]	VPS_PDC_UTC_BYTE_5[6]	VPS_PDC_UTC_BYTE_5[5]	VPS_PDC_UTC_BYTE_5[4]	VPS_PDC_UTC_BYTE_5[3]	VPS_PDC_UTC_BYTE_5[2]	VPS_PDC_UTC_BYTE_5[1]	VPS_PDC_UTC_BYTE_5[0]		
138	8A	VDP_VPS_PDC_UTC_6	R	VPS_PDC_UTC_BYTE_6[7]	VPS_PDC_UTC_BYTE_6[6]	VPS_PDC_UTC_BYTE_6[5]	VPS_PDC_UTC_BYTE_6[4]	VPS_PDC_UTC_BYTE_6[3]	VPS_PDC_UTC_BYTE_6[2]	VPS_PDC_UTC_BYTE_6[1]	VPS_PDC_UTC_BYTE_6[0]		
139	8B	VDP_VPS_PDC_UTC_7	R	VPS_PDC_UTC_BYTE_7[7]	VPS_PDC_UTC_BYTE_7[6]	VPS_PDC_UTC_BYTE_7[5]	VPS_PDC_UTC_BYTE_7[4]	VPS_PDC_UTC_BYTE_7[3]	VPS_PDC_UTC_BYTE_7[2]	VPS_PDC_UTC_BYTE_7[1]	VPS_PDC_UTC_BYTE_7[0]		
140	8C	VDP_VPS_PDC_UTC_8	R	VPS_PDC_UTC_BYTE_8[7]	VPS_PDC_UTC_BYTE_8[6]	VPS_PDC_UTC_BYTE_8[5]	VPS_PDC_UTC_BYTE_8[4]	VPS_PDC_UTC_BYTE_8[3]	VPS_PDC_UTC_BYTE_8[2]	VPS_PDC_UTC_BYTE_8[1]	VPS_PDC_UTC_BYTE_8[0]		
141	8D	VDP_VPS_PDC_UTC_9	R	VPS_PDC_UTC_BYTE_9[7]	VPS_PDC_UTC_BYTE_9[6]	VPS_PDC_UTC_BYTE_9[5]	VPS_PDC_UTC_BYTE_9[4]	VPS_PDC_UTC_BYTE_9[3]	VPS_PDC_UTC_BYTE_9[2]	VPS_PDC_UTC_BYTE_9[1]	VPS_PDC_UTC_BYTE_9[0]		
142	8E	VDP_VPS_PDC_UTC_10	R	VPS_PDC_UTC_BYTE_10[7]	VPS_PDC_UTC_BYTE_10[6]	VPS_PDC_UTC_BYTE_10[5]	VPS_PDC_UTC_BYTE_10[4]	VPS_PDC_UTC_BYTE_10[3]	VPS_PDC_UTC_BYTE_10[2]	VPS_PDC_UTC_BYTE_10[1]	VPS_PDC_UTC_BYTE_10[0]		
143	8F	VDP_VPS_PDC_UTC_11	R	VPS_PDC_UTC_BYTE_11[7]	VPS_PDC_UTC_BYTE_11[6]	VPS_PDC_UTC_BYTE_11[5]	VPS_PDC_UTC_BYTE_11[4]	VPS_PDC_UTC_BYTE_11[3]	VPS_PDC_UTC_BYTE_11[2]	VPS_PDC_UTC_BYTE_11[1]	VPS_PDC_UTC_BYTE_11[0]		
144	90	VDP_VPS_PDC_UTC_12	R	VPS_PDC_UTC_BYTE_12[7]	VPS_PDC_UTC_BYTE_12[6]	VPS_PDC_UTC_BYTE_12[5]	VPS_PDC_UTC_BYTE_12[4]	VPS_PDC_UTC_BYTE_12[3]	VPS_PDC_UTC_BYTE_12[2]	VPS_PDC_UTC_BYTE_12[1]	VPS_PDC_UTC_BYTE_12[0]		
146	92	VDP_VITC_DATA_0	R	VITC_DATA_0[7]	VITC_DATA_0[6]	VITC_DATA_0[5]	VITC_DATA_0[4]	VITC_DATA_0[3]	VITC_DATA_0[2]	VITC_DATA_0[1]	VITC_DATA_0[0]		
147	93	VDP_VITC_DATA_1	R	VITC_DATA_1[7]	VITC_DATA_1[6]	VITC_DATA_1[5]	VITC_DATA_1[4]	VITC_DATA_1[3]	VITC_DATA_1[2]	VITC_DATA_1[1]	VITC_DATA_1[0]		
148	94	VDP_VITC_DATA_2	R	VITC_DATA_2[7]	VITC_DATA_2[6]	VITC_DATA_2[5]	VITC_DATA_2[4]	VITC_DATA_2[3]	VITC_DATA_2[2]	VITC_DATA_2[1]	VITC_DATA_2[0]		
149	95	VDP_VITC_DATA_3	R	VITC_DATA_3[7]	VITC_DATA_3[6]	VITC_DATA_3[5]	VITC_DATA_3[4]	VITC_DATA_3[3]	VITC_DATA_3[2]	VITC_DATA_3[1]	VITC_DATA_3[0]		
150	96	VDP_VITC_DATA_4	R	VITC_DATA_4[7]	VITC_DATA_4[6]	VITC_DATA_4[5]	VITC_DATA_4[4]	VITC_DATA_4[3]	VITC_DATA_4[2]	VITC_DATA_4[1]	VITC_DATA_4[0]		
151	97	VDP_VITC_DATA_5	R	VITC_DATA_5[7]	VITC_DATA_5[6]	VITC_DATA_5[5]	VITC_DATA_5[4]	VITC_DATA_5[3]	VITC_DATA_5[2]	VITC_DATA_5[1]	VITC_DATA_5[0]		
152	98	VDP_VITC_DATA_6	R	VITC_DATA_6[7]	VITC_DATA_6[6]	VITC_DATA_6[5]	VITC_DATA_6[4]	VITC_DATA_6[3]	VITC_DATA_6[2]	VITC_DATA_6[1]	VITC_DATA_6[0]		
153	99	VDP_VITC_DATA_7	R	VITC_DATA_7[7]	VITC_DATA_7[6]	VITC_DATA_7[5]	VITC_DATA_7[4]	VITC_DATA_7[3]	VITC_DATA_7[2]	VITC_DATA_7[1]	VITC_DATA_7[0]		
154	9A	VDP_VITC_DATA_8	R	VITC_DATA_8[7]	VITC_DATA_8[6]	VITC_DATA_8[5]	VITC_DATA_8[4]	VITC_DATA_8[3]	VITC_DATA_8[2]	VITC_DATA_8[1]	VITC_DATA_8[0]		
155	9B	VDP_VITC_CALC_CRC	R	VITC_CRC[7]	VITC_CRC[6]	VITC_CRC[5]	VITC_CRC[4]	VITC_CRC[3]	VITC_CRC[2]	VITC_CRC[1]	VITC_CRC[0]		
156	9C	VDP_OUTPUT_SEL	RW	I²C_GS_VPS_PDC_UTC[1]	I²C_GS_VPS_PDC_UTC[0]	GS_VPS_PDC_UTC_CB_CHANGE	WSS_CGMS_CB_CHANGE					00110000	30

[1] To access the registers listed in Table 106, SUB_USR_EN in Register Address 0x0E must be programmed to 1.
[2] x in a reset value indicates do not care.

Table 107. Main Register Map Descriptions (User Map)[1, 2]

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x00	Input control	INSEL[3:0]; the INSEL bits allow the user to select an input channel and the input format; refer to Table 13 and Table 14 for full routing details					0	0	0	0	Composite (LQFP and LFCSP)	Mandatory write required for Y/C (S-Video mode) Reg 0x58 = 0x04; see Reg 0x58 for bit description
							0	0	0	1	Composite (LQFP)/reserved (LFCSP)	
							0	0	1	0	Composite (LQFP)/reserved (LFCSP)	
							0	0	1	1	Composite (LQFP and LFCSP)	
							0	1	0	0	Composite (LQFP and LFCSP)	
							0	1	0	1	Composite (LQFP)/reserved (LFCSP)	
							0	1	1	0	S-Video (LQFP and LFCSP)	
							0	1	1	1	S-Video (LQFP)/reserved (LFCSP)	
							1	0	0	0	S-Video (LQFP)/reserved (LFCSP)	
							1	0	0	1	YPrPb (LQFP and LFCSP)	
							1	0	1	0	YPrPb (LQFP)/reserved (LFCSP)	
							1	0	1	1	Reserved (LQFP and LFCSP)	
							1	1	0	0	Reserved (LQFP and LFCSP)	
							1	1	0	1	Reserved (LQFP and LFCSP)	
							1	1	1	0	Reserved (LQFP and LFCSP)	
							1	1	1	1	Reserved (LQFP and LFCSP)	
		VID_SEL[3:0]; the VID_SEL bits allow the user to select the input video standard	0	0	0	0					Autodetect PAL B/G/H/I/D,NTSC J (no pedestal), SECAM	
			0	0	0	1					Autodetect PAL B/G/H/I/D, NTSC M (pedestal), SECAM	
			0	0	1	0					Autodetect (PAL N) (pedestal), NTSC J (no pedestal), SECAM	
			0	0	1	1					Autodetect (PAL N) (pedestal), NTSC M (pedestal), SECAM	
			0	1	0	0					NTSC J	
			0	1	0	1					NTSC M	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL B/G/H/I/D	
			1	0	0	1					PAL N = PAL B/G/H/I/D (with pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL Combination N	
			1	1	0	1					PAL Combination N (with pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM (with pedestal)	
0x01	Video selection	Reserved							0	0	Set to default	
		SQPE						0			Disable square pixel mode	
								1			Enable square pixel mode	
		ENVSPROC					0				Disable VSYNC processor	
							1				Enable VSYNC processor	
		Reserved				0					Set to default	
		BETACAM			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disable HSYNC processor	
				1							Enable HSYNC processor	
		Reserved	1								Set to default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x03	Output control	SD_DUP_AV; duplicates the AV codes from the luma into the chroma path								0	AV codes to suit 8-bit interleaved data output	
										1	AV codes duplicated (for 16-bit interfaces)	
		Reserved							0		Set as default	
		OF_SEL[3:0]; allows the user to choose from a set of output formats			0	0	0	0			Reserved	
					0	0	0	1			Reserved	
					0	0	1	0			16-bit at LLC 4:2:2	Options apply to 64-lead LQFP only
					0	0	1	1			8-bit at LLC 4:2:2 ITU-R BT.656	
					0	1	0	0			Reserved	
					0	1	0	1			Reserved	
					0	1	1	0			Reserved	
					0	1	1	1			Reserved	
					1	0	0	0			Reserved	
					1	0	0	1			Reserved	
					1	0	1	0			Reserved	
					1	0	1	1			Reserved	
					1	1	0	0			Reserved	
					1	1	0	1			Reserved	
					1	1	1	0			Reserved	
					1	1	1	1			Reserved	
		TOD; three-state output drivers; this bit allows the user to three-state the output drivers; pixel outputs, HS, VS, FIELD, and SFL		0							Output pins enabled	See also TIM_OE and TRI_LLC
				1							Drivers three-stated	
		VBI_EN; allows VBI data (Line 1 to Line 21) to be passed through with only a minimum amount of filtering performed	0								All lines filtered and scaled	
			1								Only active video region filtered	
0x04	Extended output control	Range; allows the user to select the range of output values; can be ITU-R BT.656 compliant or can fill the whole accessible number range								0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240	ITU-R BT.656
										1	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254	Extended range
		EN_SFL_PIN							0		SFL output is disabled	SFL output enables encoder and decoder to be connected directly
									1		SFL information output on the SFL pin	
		BL_C_VBI; blank chroma during VBI; if set, it enables data in the VBI region to be passed through the decoder undistorted						0			Decode and output color	During VBI
								1			Blank Cr and Cb	
		TIM_OE; timing signals output enable					0				HS, VS, FIELD three-stated	Controlled by TOD
							1				HS, VS, FIELD forced active	
		Reserved			x	x						
		Reserved		1								
		BT.656-4; allows the user to select an output mode compatible with ITU-R BT.656-3/-4	0								ITU-R BT.656-3 compatible	
			1								ITU-R BT.656-4 compatible	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x07	Autodetect enable	AD_PAL_EN; PAL B/D/I/G/H autodetect enable								0	Disable	
										1	Enable	
		AD_NTSC_EN; NTSC autodetect enable							0		Disable	
									1		Enable	
		AD_PALM_EN; PAL M autodetect enable						0			Disable	
								1			Enable	
		AD_PALN_EN; PAL N autodetect enable					0				Disable	
							1				Enable	
		AD_P60_EN; PAL 60 autodetect enable				0					Disable	
						1					Enable	
		AD_N443_EN; NTSC 4.43 autodetect enable			0						Disable	
					1						Enable	
		AD_SECAM_EN; SECAM autodetect enable		0							Disable	
				1							Enable	
		AD_SEC525_EN; SECAM 525 autodetect enable	0								Disable	
			1								Enable	
0x08	Contrast	CON[7:0]; contrast adjust; this is the user control for contrast adjustment	1	0	0	0	0	0	0	0	Luma gain = 1	0x00 gain = 0, 0x80 gain = 1, 0xFF gain = 2
0x0A	Brightness	BRI[7:0]; this register controls the brightness of the video signal	0	0	0	0	0	0	0	0		0x00 = 0 IRE, 0x7F = +30 IRE, 0x80 = −30 IRE
0x0B	Hue	HUE[7:0]; this register contains the value for the color hue adjustment	0	0	0	0	0	0	0	0		Hue range = −90° to +90°
0x0C	Default Value Y	DEF_VAL_EN; default value enable								0	Free-run mode dependent on DEF_VAL_AUTO_EN	
										1	Force free-run mode on and output blue screen	
		DEF_VAL_AUTO_EN; default value automatic enable							0		Disable free-run mode	When lock is lost, free-run mode can be enabled to output stable timing, clock, and a set color
									1		Enable automatic free-run mode (blue screen)	
		DEF_Y[5:0]; default value is Y; this register holds the Y default value	0	0	1	1	0	1			Y[7:0] = {DEF_Y[5:0], 0, 0}	Default Y value output in free-run mode
0x0D	Default Value C	DEF_C[7:0]; default value is C; the Cr and Cb default values are defined in this register	0	1	1	1	1	1	0	0	Cr[3:0] = {DEF_C[7:4], 0, 0, 0, 0} Cb[3:0] = {DEF_C[3:0], 0, 0, 0, 0}	Default Cb/Cr value output in free-run mode; default values give blue screen output
0x0E	ADI Control 1	Reserved				0	0	0	0	0	Set as default	
		SUB_USR_EN; enables user to access the interrupt/ VDP register map			0						Access main register space	See Figure 55
					1						Access interrupt/VDP register space	
		Reserved	0	0							Set as default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x0F	Power management	Reserved							0	0	Set to default	
		PDBP; power-down bit priority selects between PWRDWN bit or pin control						0			Chip power-down controlled by pin	Not applicable for 32-lead LFCSP
								1			Bit has priority (pin disregarded)	
		Reserved				0	0				Set to default	
		PWRDWN; power-down places the decoder into a full power-down mode			0						System functional	
					1						Powered down	See PDBP, 0x0F Bit 2
		Reserved		0							Set to default	
		Reset; chip reset, loads all I^2C bits with default values	0								Normal operation	
			1								Start reset sequence	Executing reset takes approximately 2 ms; this bit is self-clearing
0x10	Status 1 (read only)	IN_LOCK								x	1 = in lock (now)	Provides info about the internal status of the decoder
		LOST_LOCK							x		1 = lost lock (since last read)	
		FSC_LOCK						x			1 = f_{SC} lock (now)	
		FOLLOW_PW					x				1 = peak white AGC mode active	
		AD_RESULT[2:0]; auto-detection result reports the standard of the input video		0	0	0					NTSC M/J	Detected standard
				0	0	1					NTSC 4.43	
				0	1	0					PAL M	
				0	1	1					PAL 60	
				1	0	0					PAL B/G/H/I/D	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL	x								1 = color kill is active	Color kill
0x11	IDENT (read only)	IDENT[7:0]; provides identification on the revision of the part	0	0	0	1	1	1	0	0		Power-up value = 0x1C
0x12	Status 2 (read only)	MVCS DET								x	MV color striping detected	1 = detected
		MVCS T3							x		MV color striping type	0 = Type 2, 1 = Type 3
		MV PS DET						x			MV pseudosync detected	1 = detected
		MV AGC DET					x				MV AGC pulses detected	1 = detected
		LL NSTD				x					Nonstandard line length	1 = detected
		FSC NSTD			x						f_{SC} frequency nonstandard	1 = detected
		Reserved	x	x								
0x13	Status 3 (read only)	INST_HLOCK								x	1 = horizontal lock achieved	Unfiltered
		GEMD							x		1 = Gemstar data detected	
		SD_OP_50Hz						0			SD 60 Hz detected	SD field rate detect
								1			SD 50 Hz detected	
		Reserved					x					
		FREE_RUN_ACT				x					1 = free-run mode active	Blue screen output
		STD FLD LEN			x						1 = field length standard	Correct field length found
		Interlaced		x							1 = interlaced video detected	Field sequence found
		PAL_SW_LOCK	x								1 = swinging burst detected	Reliable swinging burst sequence
0x14	Analog clamp control	Reserved					0	0	1	0	Set to default	
		CCLEN; current clamp enable allows the user to switch off the current sources in the analog front				0					Current sources switched off	
						1					Current sources enabled	
		VCLEN; allows the user to reset the clamp circuitry			0						Normal Operation	
					1						Reset Clamp Circuitry	
		Reserved	0	0							Set to default	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x15	Digital Clamp Control 1	Reserved					x	x	x	x	Set to default	
		DCFE; digital clamp freeze enable				0					Digital clamp on	
						1					Digital clamp off	
		DCT[1:0]; digital clamp timing determines the time constant of the digital fine clamp circuitry		0	0						Slow (TC = 1 sec)	
				0	1						Medium (TC = 0.5 sec)	
				1	0						Fast (TC = 0.1 sec)	
				1	1						TC dependent on video	
		Reserved	0								Set to default	
0x17	Shaping Filter Control 1	YSFM[4:0]; selects Y shaping filter mode in CVBS-only mode; allows the user to select a wide range of low-pass and notch filters; if either auto mode is selected, the decoder selects the optimum Y filter depending on the CVBS video source quality (good vs. poor)				0	0	0	0	0	Autowide notch for poor quality sources or wideband filter with comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality
						0	0	0	0	1	Autonarrow notch for poor quality sources or wideband filter with comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected, the decoder does not change filter modes; depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	PAL NN1	
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN1	
						1	1	0	0	0	PAL WN2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	
		CSFM[2:0]; C shaping filter mode allows selection from a range of low-pass chrominance filters; if either auto mode is selected, the decoder selects the optimum C filter depending on the CVBS video source quality (good vs. bad); nonauto settings force a C filter for all standards and quality of CVBS video	0	0	0						Autoselection 1.5 MHz	Automatically selects a C filter based on video standard and quality
			0	0	1						Autoselection 2.17 MHz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wideband mode	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x18	Shaping Filter Control 2	WYSFM[4:0]; wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPrPb, B/W input signals; it is also used when a good quality input CVBS signal is detected; for all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0]				0	0	0	0	0	Reserved, do not use	
						0	0	0	0	1	Reserved, do not use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved, do not use	
						~	~	~	~	~	Reserved, do not use	
						1	1	1	1	1	Reserved, do not use	
		Reserved		0	0						Set to default	
		WYSFMOVR; enables use of the automatic WYSFM filter	0								Autoselection of best filter	
			1								Manual select filter using WYSFM[4:0]	
0x19	Comb filter control	PSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1					Set as default	
0x1D	ADI Control 2	Reserved			0	0	0	x	x	x	Set to default	
		EN28XTAL		0							Reserved, do not use	
				1							Use 28 MHz crystal	
		TRI_LLC	0								LLC pin active	
			1								LLC pin three-stated	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x27	Pixel delay control	LTA[1:0]; luma timing adjust allows the user to specify a timing difference between chroma and luma samples							0	0	No delay	CVBS mode LTA[1:0] = 00b, S-Video mode LTA[1:0] = 01b, YPrPb mode LTA[1:0] = 01b
									0	1	Luma one clock (37 ns) late	
									1	0	Luma two clocks (74 ns) early	
									1	1	Luma one clock (37 ns) early	
		Reserved						0			Set to 0	
		CTA[2:0]; chroma timing adjust allows a specified timing difference between the luma and chroma samples			0	0	0				Not a valid setting	CVBS mode CTA[2:0] = 011b, S-Video mode CTA[2:0] = 101b, YPrPb mode CTA[2:0] = 110b
					0	0	1				Chroma + two pixels (early)	
					0	1	0				Chroma + one pixel (early)	
					0	1	1				No delay	
					1	0	0				Chroma − one pixel (late)	
					1	0	1				Chroma − two pixels (late)	
					1	1	0				Chroma − three pixels (late)	
					1	1	1				Not a valid setting	
		AUTO_PDC_EN; automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma	
				1							LTA and CTA values determined automatically	
		SWPC; allows the Cr and Cb samples to be swapped	0								No swapping	
			1								Swap the Cr and Cb output samples	
0x2B	Misc gain control	PW_UPD; peak white update determines the rate of gain								0	Update once per video line	Peak white must be enabled; see LAGC[2:0]
										1	Update once per field	
		Reserved			1	0	0	0	0		Set to default	
		CKE; color kill enable allows the color kill function to be switched on and off		0							Color kill disabled	For SECAM color kill, the threshold is set at 8%; see CKILLTHR[2:0]
				1							Color kill enabled	
		Reserved	1								Set to default	
0x2C	AGC mode control	CAGC[1:0]; chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path							0	0	Manual fixed gain	Use CMG[11:0]
									0	1	Use luma gain for chroma	
									1	0	Automatic gain	Based on color burst
									1	1	Freeze chroma gain	
		Reserved					1	1			Set to 1	
		LAGC[2:0]; luma automatic gain control selects the mode of operation for the gain control in the luma path		0	0	0					Manual fixed gain	Use LMG[11:0]
				0	0	1					Peak white algorithm off	Blank level to sync tip
				0	1	0					Peak white algorithm on	Blank level to sync tip
				0	1	1					Reserved	
				1	0	0					Reserved	
				1	0	1					Reserved	
				1	1	0					Reserved	
				1	1	1					Freeze gain	
		Reserved	1								Set to 1	
0x2D	Chroma Gain Control 1, Chroma Gain1 (CG)	CMG[11:8]/CG[11:8]; in manual mode, the chroma gain control can be used to program a desired manual chroma gain; in auto mode, it can be used to read back the current gain value					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates
		Reserved			1	1					Set to 1	
		CAGT[1:0]; chroma auto matic gain timing allows adjustment of the chroma AGC tracking speed	0	0							Slow (TC = 2 sec)	Has an effect only if CAGC[1:0] is set to autogain (10)
			0	1							Medium (TC = 1 sec)	
			1	0							Reserved	
			1	1							Adaptive	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x2E	Chroma Gain Control 2, Chroma Gain2 (CG)	CMG[7:0]/CG[7:0]; chroma manual gain lower eight bits; see CMG[11:8]/ CG[11:8] for description	0	0	0	0	0	0	0	0	CMG[11:0] = see the CMG section CMG[11:0] = see the CMG section	Min value = 0d, Max value = 4095d
0x2F	Luma Gain Control 1, Luma Gain1 (LG)	LMG[11:8]/LG[11:8]; in manual mode, luma gain control can be used to program a desired manual luma gain; in auto mode, it can be used to read back the actual gain value used					x	x	x	x	LAGC[1:0] settings decide in which mode LMG[11:0] operates	
		Reserved			1	1					Set to 1	
		LAGT[1:0]; luma auto matic gain timing allows adjustment of the luma AGC tracking speed	0	0							Slow (TC = 2 sec)	Only has an effect if LAGC[1:0] is set to autogain (001, 010, 011, or 100)
			0	1							Medium (TC = 1 sec)	
			1	0							Fast (TC = 0.2 sec)	
			1	1							Adaptive	
0x30	Luma Gain Control 2, Luma Gain2 (LG)	LMG[7:0]/LG[7:0]; luma manual gain lower eight bits; see LMG[11:8]/ LG[11:8] for description	x	x	x	x	x	x	x	x	LMG[11:0] - see the LMG section LMG[11:0] =- see the LMG section	Min value = 1024d, Max value = 4095d
0x31	VS/FIELD Control 1	Reserved						0	1	0	Set to default	
		HVSTIM; selects where within a line of video the VS signal is asserted					0				Start of line relative to HSE	HSE = HSYNC end
							1				Start of line relative to HSB	HSB = HSYNC begin
		NEWAVMODE; sets the EAV/SAV mode				0					EAV/SAV codes generated to suit Analog Devices encoders	
						1					Manual VS/FIELD position controlled by Register 0x32, Register 0x33, and Register 0xE5 to Register 0xEA	
		Reserved	0	0	0						Set to default	
0x32	VS/FIELD Control 2	Reserved			0	0	0	0	0	1	Set to default	NEWAVMODE bit must be set high
		VSBHE		0							VS goes high in the middle of the line (even field)	
				1							VS changes state at the start of the line (even field)	
		VSBHO	0								VS goes high in the middle of the line (odd field)	
			1								VS changes state at the start of the line (odd field)	
0x33	VS/FIELD Control 3	Reserved			0	0	0	1	0	0	Set to default	
		VSEHE		0							VS goes low in the middle of the line (even field)	NEWAVMODE bit must be set high
				1							VS changes state at the start of the line (even field)	
		VSEHO	0								VS goes low in the middle of the line (odd field)	
			1								VS changes state at the start of the line odd field	
0x34	HS Position Control 1	HSE[10:8]; HS end allows positioning of the HS output within the video line						0	0	0	HS output ends HSE[10:0] pixels after the falling edge of HSYNC	Using HSB and HSE the user can program the position and length of the output HSYNC
		Reserved					0				Set to 0	
		HSB[10:8]; HS begin allows positioning of the HS output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSYNC	
		Reserved	0								Set to 0	
0x35	HS Position Control 2	HSB[7:0]; see Address 0x34, using HSB[10:0] and HSE[10:0], users can program the position and length of the HS output signal	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	HSE[7:0]; see Address 0x35 description	0	0	0	0	0	0	0	0		

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x37	Polarity	PCLK; sets polarity of LLC								0	Invert polarity	
										1	Normal polarity as per the timing diagrams	
		Reserved						0	0		Set to 0	
		PF; sets the FIELD polarity					0				Active high	
							1				Active low	
		Reserved				0					Set to 0	
		PVS; sets the VS polarity			0						Active high	
					1						Active low	
		Reserved		0							Set to 0	
		PHS; sets HS polarity	0								Active low	
			1								Active high	
0x38	NTSC comb control	YCMN[2:0]; luma comb mode, NTSC						0	0	0	Adaptive three-line, three-tap luma	
								1	0	0	Use low-pass notch	
								1	0	1	Fixed luma comb (two-line)	Top lines of memory
								1	1	0	Fixed luma comb (three-line)	All lines of memory
								1	1	1	Fixed luma comb (two-line)	Bottom lines of memory
		CCMN[2:0]; chroma comb mode, NTSC			0	0	0				Three-line adaptive for CTAPSN = 01, Four-line adaptive for CTAPSN = 10, Five-line adaptive for CTAPSN = 11	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, Fixed three-line for CTAPSN = 10, Fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, Fixed four-line for CTAPSN = 10, Fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, Fixed three-line for CTAPSN = 10, Fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSN[1:0]; chroma comb taps, NTSC	0	0							Not used	
			0	1							Adapts three lines to two lines	
			1	0							Adapts five lines to three lines	
			1	1							Adapts five lines to four lines	
0x39	PAL comb control	YCMP[2:0]; luma comb mode, PAL						0	0	0	Adaptive five-line, three-tap luma comb	
								1	0	0	Use low-pass notch	
								1	0	1	Fixed luma comb (three-line)	Top lines of memory
								1	1	0	Fixed luma comb (five-line)	All lines of memory
								1	1	1	Fixed luma comb (three-line)	Bottom lines of memory
		CCMP[2:0]; chroma comb mode, PAL			0	0	0				Three-line adaptive for CTAPSN = 01, Four-line adaptive for CTAPSN = 10, Five-line adaptive for CTAPSN = 11	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01	Top lines of memory
											Fixed three-line for CTAPSN = 10	
											Fixed four-line for CTAPSN = 11	
					1	1	0				Fixed three-line for CTAPSN = 01	All lines of memory
											Fixed four-line for CTAPSN = 10	
											Fixed five-line for CTAPSN = 11	
					1	1	1				Fixed two-line for CTAPSN = 01	Bottom lines of memory
											Fixed three-line for CTAPSN = 10	
											Fixed four-line for CTAPSN = 11	
		CTAPSP[1:0]; chroma comb taps, PAL	0	0							Not used	
			0	1							Adapts five lines to three lines (two taps)	
			1	0							Adapts five lines to three lines (three taps)	
			1	1							Adapts five lines to four lines (four taps)	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x3A	ADC control	MUX PDN override; mux power-down override								0		No control over power-down for muxes and associated channel circuit
										1		Allows power-down of MUX0/MUX1/MUX2 and associated channel circuit. When INSEL[3:0] is used, unused channels are automatically powered down.
		PWRDWN_MUX_2; enables power-down of MUX2 and associated channel clamp and buffer							0		MUX2 and associated channel in normal operation	
									1		Power down MUX2 and associated channel operation	MUX PDN Override = 1
		PWRDWN_MUX_1; enables power-down of MUX1 and associated channel clamp and buffer						0			MUX1 and associated channel in normal operation	
								1			Power down MUX1 and associated channel operation	MUX PDN Override = 1
		PWRDWN_MUX_0; enables power-down of MUX0 and associated channel clamp and buffer					0				MUX0 and associated channel in normal operation	
							1				Power down MUX0 and associated channel operation	MUX PDN Override = 1
		Reserved	0	0	0	1					Set as default	
0x3D	Manual window control	Reserved					0	0	1	0	Set to default	
		CKILLTHR[2:0]		0	0	0					NTSC, PAL color kill at <0.5%, SECAM no color kill	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					NTSC, PAL color kill at <1.5%, SECAM color kill at <5%	
				0	1	0					NTSC, PAL color kill at <2.5%, SECAM color kill at <7%	
				0	1	1					NTSC, PAL color kill at <4%, SECAM color kill at <8%	
				1	0	0					NTSC, PAL color kill at <8.5%, SECAM color kill at <9.5%	
				1	0	1					NTSC, PAL color kill at <16%, SECAM color kill at <15%	
				1	1	0					NTSC, PAL color kill at <32%, SECAM color kill at <32%	
				1	1	1					Reserved	
		Reserved	1								Set to default	
0x41	Resample control	Reserved			0	0	0	0	0	1	Set to default	
		SFL_INV; controls the behavior of the PAL switch bit		0							SFL-compatible with the ADV717x and ADV73xx video encoders	
				1							SFL-compatible with the ADV7194 video encoder	
		Reserved	0								Set to default	
0x48	Gemstar Control 1	GDECEL[15:8]; see the Comments column	0	0	0	0	0	0	0	0	GDECEL[15:0]: 16 individual enable bits that select the lines of video (even field Line 10 to Line 25) that the decoder checks for Gemstar-compatible data	LSB = Line 10, MSB = Line 25, Default = do not check for Gemstar-compatible data on any lines [10 to 25] in even fields
0x49	Gemstar Control 2	GDECEL[7:0]	0	0	0	0	0	0	0	0		

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x4A	Gemstar Control 3	GDECOL[15:8]; see the Comments column	0	0	0	0	0	0	0	0	GDECOL[15:0]: 16 individual enable bits that select the lines of video (odd field Line 10 to Line 25) that the decoder checks for Gemstar-compatible data	LSB = Line 10, MSB = Line 25, Default = do not check for Gemstar-compatible data on any lines [10 to 25] in odd fields
0x4B	Gemstar Control 4	GDECOL[7:0]	0	0	0	0	0	0	0	0		
0x4C	Gemstar Control 5	GDECAD; controls the manner decoded Gemstar data is inserted into the horizontal blanking period								0	Split data into half-byte	To avoid 00/FF code
										1	Output in straight 8-bit format	
		GDE_SEL_OLD_ADF					0				Enables a new ancillary data system	
		Reserved	x	x	x	x		x	x		Undefined	
0x4D	CTI DNR Control 1	CTI_EN; CTI enable								0	Disable CTI	
										1	Enable CTI	
		CTI_AB_EN; enables the mixing of the transient improved chroma with the original signal							0		Disable CTI alpha blender	
									1		Enable CTI alpha blender	
		CTI_AB[1:0]; controls the behavior of the alpha-blend circuitry					0	0			Sharpest mixing	
							0	1			Sharp mixing	
							1	0			Smooth mixing	
							1	1			Smoothest mixing	
		Reserved				0					Set to default	
		DNR_EN; enable or bypass the DNR block			0						Bypass the DNR block	
					1						Enable the DNR block	
		Reserved	1	1							Set to default	
0x4E	CTI DNR Control 2	CTI_C_TH[7:0]; specifies how big the amplitude step must be to be steep-ened by the CTI block	0	0	0	0	1	0	0	0	Set to 0x04 for AV input; set to 0x0A for tuner input	
0x50	CTI DNR Control 4	DNR_TH[7:0]; specifies the maximum edge that is interpreted as noise and is therefore blanked	0	0	0	0	1	0	0	0		
0x51	Lock count	CIL[2:0]; count into lock determines the number of lines the system must remain in lock before showing a locked status						0	0	0	One line of video	
								0	0	1	Two lines of video	
								0	1	0	Five lines of video	
								0	1	1	10 lines of video	
								1	0	0	100 lines of video	
								1	0	1	500 lines of video	
								1	1	0	1000 lines of video	
								1	1	1	100,000 lines of video	
		COL[2:0]; count out of lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status			0	0	0				1 line of video	
					0	0	1				2 lines of video	
					0	1	0				5 lines of video	
					0	1	1				10 lines of video	
					1	0	0				100 lines of video	
					1	0	1				500 lines of video	
					1	1	0				1000 lines of video	
					1	1	1				100,000 lines of video	
		SRLS; select raw lock signal; selects the determination of the lock status		0							Over field with vertical info	
				1							Line-to-line evaluation	
		FSCLE; f_{SC} lock enable	0								Lock status set only by horizontal lock	
			1								Lock status set by horizontal lock and subcarrier lock	
0x52	CVBS_TRIM	CVBS_IBIAS[3:0], sets the bias current for the analog front end for CVBS inputs.					1	0	1	1	Default AFE bias current setting	
							1	1	0	1	Recommended AFE bias current for CVBS inputs	
		Reserved	0	0	0	0						

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x58	VS/FIELD pin control	VS/FIELD; VSYNC or FIELD output; 40-lead and 32-lead LFCSP only								0	FIELD	Pin 37 on 40-lead LFCSP, Pin 31 on 32-lead LFCSP
										1	VSYNC	
		Reserved							0		Set to default	
		ADC sampling control						0			ADC sampling control	
								1			Y/C mode only	Mandatory write
		Reserved	0	0	0	0	0				Set to default	
0x59	General-purpose outputs	GPO[3:0]; LQFP only								0	Outputs 0 to GPO0	GPO_ENABLE must be set to 1 for these bits to take effect
										1	Outputs 1 to GPO0	
									0		Outputs 0 to GPO1	
									1		Outputs 1 to GPO1	
								0			Outputs 0 to GPO2	
								1			Outputs 1 to GPO2	
							0				Outputs 0 to GPO3	
							1				Outputs 1 to GPO3	
		GPO_ENABLE				0					GPO[3:0] three-stated	
						1					GPO[3:0] enabled	
		Reserved	0	0	0							
0x8F	Free-Run Line Length 1	Reserved					0	0	0	0	Set to default	
		LLC_PAD_SEL[2:0]; enables manual selection of the clock for the LLC pin		0	0	0					LLC (nominal 27 MHz) selected out on LLC pin	
				1	0	1					LLC (nominal 13.5 MHz) selected out on LLC pin	For 16-bit 4:2:2 out, OF_SEL[3:0] = 0010
		Reserved	0								Set to default	
0x99	CCAP1 (read only)	CCAP1[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP1[7] contains parity bit for Byte 0	
0x9A	CCAP2 (read only)	CCAP2[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP2[7] contains parity bit for Byte 0	
0x9B	Letterbox 1 (read only)	LB_LCT[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the top of active video	This feature examines the active video at the start and end of each field; it enables format detection even if the video is not accompanied by a CGMS or WSS sequence
0x9C	Letterbox 2 (read only)	LB_LCM[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected in the bottom half of active video if subtitles are detected	
0x9D	Letterbox 3 (read only)	LB_LCB[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the bottom of active video	
0xB2	CRC enable (write only)	Reserved							0	0	Set as default	
		CRC_ENABLE; enable CRC checksum decoded from FMS packet to validate CGMSD						0			Turn off CRC check	
								1			CGMSD goes high with valid checksum	
		Reserved	0	0	0	1	1				Set as default	

Main Map			Bits (Shading Indicates Default State)										
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments		Notes
0xC3	ADC Switch 1	MUX0[2:0]; manual muxing control for MUX0; this setting controls which input is routed to the ADC for processing									**LQFP**	**LFCSP**	MAN_MUX_EN = 1
								0	0	0	No connect	No connect	
								0	0	1	$A_{IN}1$	$A_{IN}1$	
								0	1	0	$A_{IN}2$	No connect	
								0	1	1	$A_{IN}3$	No connect	
								1	0	0	$A_{IN}4$	$A_{IN}2$	
								1	0	1	$A_{IN}5$	$A_{IN}3$	
								1	1	0	$A_{IN}6$	No connect	
								1	1	1	No connect	No connect	
		Reserved					0						
		MUX1[2:0]; manual muxing control for MUX1; this setting controls which input is routed to the ADC for processing									**LQFP**	**LFCSP**	MAN_MUX_EN = 1
				0	0	0					No connect	No connect	
				0	0	1					No connect	No connect	
				0	1	0					No connect	No connect	
				0	1	1					$A_{IN}3$	No connect	
				1	0	0					$A_{IN}4$	$A_{IN}2$	
				1	0	1					$A_{IN}5$	$A_{IN}3$	
				1	1	0					$A_{IN}6$	No connect	
				1	1	1					No connect	No connect	
		Reserved	0										
0xC4	ADC Switch 2	MUX2[2:0]; manual muxing control for MUX2; this setting controls which input is routed to the ADC for processing									**LQFP**	**LFCSP**	MAN_MUX_EN = 1
								0	0	0	No connect	No connect	
								0	0	1	No connect	No connect	
								0	1	0	$A_{IN}2$	No connect	
								0	1	1	No connect	No connect	
								1	0	0	No connect	No connect	
								1	0	1	$A_{IN}5$	$A_{IN}3$	
								1	1	0	$A_{IN}6$	No connect	
								1	1	1	No connect	No connect	
		Reserved		0	0	0	0						
		MAN_MUX_EN; enable manual setting of the input signal muxing	0								Disable		This bit must be set to 1 for manual muxing
			1								Enable		
0xDC	Letterbox Control 1	LB_TH[4:0]; sets the threshold value that determines if a line is black				0	1	1	0	0	Default threshold for the detection of black lines 01101 to 10000—increase threshold, 00000 to 01011—decrease threshold		
		Reserved	1	0	1						Set as default		
0xDD	Letterbox Control 2	LB_EL[3:0]; programs the end line of the activity window for LB detection (end of field)					1	1	0	0	LB detection ends with the last line of active video on a field, 1100b: 262/525		
		LB_SL[3:0]; programs the start line of the activity window for LB detection (start of field)	0	1	0	0					Letterbox detection aligned with the start of active video, 0100b: 23/286 NTSC		
0xDE	ST Noise Readback 1 (read only)	ST_NOISE[10:8]						x	x	x			
		ST_NOISE_VLD					x				When = 1, ST_NOISE[10:0] is valid		
0xDF	ST Noise Readback 2 (read only)	ST_NOISE[7:0]	x	x	x	x	x	x	x	x			
0xE1	SD Offset Cb	SD_OFF_Cb[7:0]; adjusts the hue by selecting the offset for the Cb channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cb channel		
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cb channel		
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cb channel		
0xE2	SD Offset Cr	SD_OFF_Cr[7:0]; adjusts the hue by selecting the offset for the Cr channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cr channel		
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cr channel		
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cr channel		
0xE3	SD Saturation Cb	SD_SAT_Cb[7:0]; adjusts the saturation by affecting gain on the Cb channel	0	0	0	0	0	0	0	0	Gain on Cb channel = −42 dB		
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB		
			1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB		

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xE4	SD Saturation Cr	SD_SAT_Cr[7:0]; adjusts the saturation by affecting gain on the Cr channel	0	0	0	0	0	0	0	0	Gain on Cr channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB	
0xE5	NTSC V bit begin	NVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	NTSC default (ITU-R BT.656)	
		NVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE; delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		NVBEGDELO; delay V bit going high by one line relative to NVBEG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE6	NTSC V bit end	NVEND[4:0]; number of lines after I_{COUNT} rollover to set V low				0	0	1	0	0	NTSC default (ITU-R BT.656)	
		NVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE; delay V bit going low by one line relative to NVEND (even field)		0							No delay	
				1							Additional delay by one line	
		NVENDDELO; delay V bit going low by one line relative to NVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xE7	NTSC F bit toggle	NFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	NTSC default	
		NFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE; delay F transition by one line relative to NFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		NFTOGDELO; delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE8	PAL V bit begin	PVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	PAL default (ITU-R BT.656)	
		PVBEGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE; delay V bit going high by one line relative to PVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		PVBEGDELO; delay V bit going high by one line relative to PVBEG (odd field)	0								No delay	
			1								Additional delay by one line	

Main Map			Bits (Shading Indicates Default State)									
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xE9	PAL V bit end	PVEND[4:0]; number of lines after I_{COUNT} rollover to set V low.				1	0	1	0	0	PAL default (ITU-R BT.656)	
		PVENDSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE; delay V bit going low by one line relative to PVEND (even field)		0							No delay	
				1							Additional delay by one line	
		PVENDDELO; delay V bit going low by one line relative to PVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xEA	PAL F bit toggle	PFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	PAL default (ITU-R BT.656)	
		PFTOGSIGN			0						Set to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE; delay F transition by one line relative to PFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		PFTOGDELO; delay F transition by one line relative to PFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xEB	Vblank Control 1	PVBIELCM[1:0]; PAL VBI even field line control							0	0	VBI ends one line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant (Line 336)	
									1	0	VBI ends one line later (Line 337)	
									1	1	VBI ends two lines later (Line 338)	
		PVBIOLCM[1:0]; PAL VBI odd field line control					0	0			VBI ends one line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on odd field in PAL
							0	1			ITU-R BT.470 compliant (Line 23)	
							1	0			VBI ends one line later (Line 24)	
							1	1			VBI ends two lines later (Line 25)	
		NVBIELCM[1:0]; NTSC VBI even field line control			0	0					VBI ends one line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on even field in NTSC
					0	1					ITU-R BT.470 compliant (Line 283)	
					1	0					VBI ends one line later (Line 284)	
					1	1					VBI ends two lines later (Line 285)	
		NVBIOLCM[1:0]; NTSC VBI odd field line control	0	0							VBI ends one line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant (Line 21)	
			1	0							VBI ends one line later (Line 22)	
			1	1							VBI ends two lines later (Line 23)	
0xEC	Vblank Control 2	PVBIECCM[1:0]; PAL VBI even field color control							0	0	Color output beginning Line 335	Controls the position of first line that outputs color after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant color output beginning Line 336	
									1	0	Color output beginning Line 337	
									1	1	Color output beginning Line 338	
		PVBIOCCM[1:0]; PAL VBI odd field color control					0	0			Color output beginning Line 22	Controls the position of first line that outputs color after VBI on odd field in PAL
							0	1			ITU-R BT.470-compliant color output beginning Line 23	
							1	0			Color output beginning Line 24	
							1	1			Color output beginning Line 25	
		NVBIECCM[1:0]; NTSC VBI even field color control			0	0					Color output beginning Line 282	Controls the position of first line that outputs color after VBI on even field in NTSC
					0	1					ITU-R BT.470-compliant color output beginning Line 283	
					1	0					VBI ends one line later (Line 284)	
					1	1					Color output beginning Line 285	
		NVBIOCCM[1:0]; NTSC VBI odd field color control	0	0							Color output beginning Line 20	Controls the position of first line that outputs color after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant color output beginning Line 21	
			1	0							Color output beginning Line 22	
			1	1							Color output beginning Line 23	

Main Map			Bits (Shading Indicates Default State)										Notes
Subaddress	Register	Bit Description	7	6	5	4	3	2	1	0	Comments		
0xF3	AFE_CONTROL 1	AA_FILT_EN[2:0]; antialiasing filter enable								0	Antialiasing Filter 1 disabled		AA_FILT_MAN_OVR must be enabled to change settings defined by INSEL[3:0]
										1	Antialiasing Filter 1 enabled		
									0		Antialiasing Filter 2 disabled		
									1		Antialiasing Filter 2 enabled		
								0			Antialiasing Filter 3 disabled		
								1			Antialiasing Filter 3 enabled		
		AA_FILT_MAN_OVR; antialiasing filter override					0				Override disabled		
							1				Override enabled		
		Reserved	0	0	0	0							
0xF4	Drive strength	DR_STR_S[1:0]; selects the drive strength for the sync output signals							0	0	Low drive strength (1×)		The low drive strength (1×) setting for DR_STR_S, DR_STR_C, and DR_STR is not recommended for the optimal performance of the ADV7180
									0	1	Medium low drive strength (2×)		
									1	0	Medium high drive strength (3×)		
									1	1	High drive strength (4×)		
		DR_STR_C[1:0]; selects the drive strength for the clock output signal					0	0			Low drive strength (1×)		
							0	1			Medium low drive strength (2×)		
							1	0			Medium high drive strength (3×)		
							1	1			High drive strength (4×)		
		DR_STR[1:0]; selects the drive strength for the data output signals; can be increased or decreased for EMC or crosstalk reasons			0	0					Low drive strength (1×)		
					0	1					Medium low drive strength (2×)		
					1	0					Medium high drive strength (3×)		
					1	1					High drive strength (4×)		
		Reserved	x	x									
0xF8	IF comp control	IFFILTSEL[2:0]; IF filter selection for PAL and NTSC						0	0	0	Bypass mode		0 dB
											2 MHz	**5 MHz**	NTSC filters
								0	0	1	−3 dB	−2 dB	
								0	1	0	−6 dB	+3.5 dB	
								0	1	1	−10 dB	+5 dB	
								1	0	0	Reserved		
											3 MHz	**6 MHz**	PAL filters
								1	0	1	−2 dB	+2 dB	
								1	1	0	−5 dB	+3 dB	
								1	1	1	−7 dB	+5 dB	
		Reserved	0	0	0	0	0						
0xF9	VS mode control	EXTEND_VS_MAX_FREQ								0	Limits maximum VSYNC frequency to 66.25 Hz (475 lines/frame)		
										1	Limits maximum VSYNC frequency to 70.09 Hz (449 lines/frame)		
		EXTEND_VS_MIN_FREQ							0		Limits minimum VSYNC frequency to 42.75 Hz (731 lines/frame)		
									1		Limits minimum VSYNC frequency to 39.51 Hz (791 lines/frame)		
		VS_COAST_MODE[1:0]					0	0			Autocoast mode		This value sets up the output coast frequency
							0	1			50 Hz coast mode		
							1	0			60 Hz coast mode		
							1	1			Reserved		
		Reserved	0	0	0	0							
0xFB	Peaking control	PEAKING_GAIN[7:0]	0	1	0	0	0	0	0	0	Increases/decreases the gain for high frequency portions of the video signal		
0xFC	Coring threshold	DNR_TH2[7:0]	0	0	0	0	0	1	0	0	Specifies the maximum edge that is interpreted as noise and therefore blanked		

[1] Shading indicates default values.
[2] x indicates a bit that keeps the last written value.

To read to and write from the registers in Table 108, the SUB_USR_EN bit (Address 0x0E[5]) must be set to Logic 1.

Table 108. Register Map Descriptions (User Sub Map)[1, 2]

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x40	Interrupt Configuration 1	INTRQ_OP_SEL[1:0]; interrupt drive level select							0	0	Open drain	
									0	1	Drive low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INTRQ; manual interrupt set mode						0			Manual interrupt mode disabled	
								1			Manual interrupt mode enabled	
		Reserved					x				Not used	
		MV_INTRQ_SEL[1:0]; Macrovision interrupt select			0	0					Reserved	
					0	1					Pseudo sync only	
					1	0					Color stripe only	
					1	1					Pseudo sync or color stripe	
		INTRQ_DUR_SEL[1:0]; interrupt duration select	0	0							Three XTAL periods	
			0	1							15 XTAL periods	
			1	0							63 XTAL periods	
			1	1							Active until cleared	
0x42	Interrupt Status 1 (read only)	SD_LOCK_Q								0	No change	These bits can be cleared or masked in Register 0x43 and Register 0x44, respectively
										1	SD input has caused the decoder to go from an unlocked state to a locked state	
		SD_UNLOCK_Q							0		No change	
									1		SD input has caused the decoder to go from a locked state to an unlocked state	
		Reserved				x	x	x				
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the free-run status	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync/color striping detected; see Register 0x40 MV_INTRQ_SEL[1:0] for selection	
		Reserved	x									
0x43	Interrupt Clear 1 (write only)	SD_LOCK_CLR								0	Do not clear	
										1	Clears SD_LOCK_Q bit	
		SD_UNLOCK_CLR							0		Do not clear	
									1		Clears SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		SD_FR_CHNG_CLR			0						Do not clear	
					1						Clears SD_FR_CHNG_Q bit	
		MV_PS_CS_CLR		0							Do not clear	
				1							Clears MV_PS_CS_Q bit	
		Reserved	x								Not used	
0x44	Interrupt Mask 1 (read/write)	$\overline{\text{SD_LOCK_MSK}}$								0	Masks SD_LOCK_Q bit	
										1	Unmasks SD_LOCK_Q bit	
		$\overline{\text{SD_UNLOCK_MSK}}$							0		Masks SD_UNLOCK_Q bit	
									1		Unmasks SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		$\overline{\text{SD_FR_CHNG_MSK}}$			0						Masks SD_FR_CHNG_Q bit	
					1						Unmasks SD_FR_CHNG_Q bit	
		$\overline{\text{MV_PS_CS_MSK}}$		0							Masks MV_PS_CS_Q bit	
				1							Unmasks MV_PS_CS_Q bit	
		Reserved	x								Not used	

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x45	Raw Status 2 (read only)	CCAPD								0	No CCAPD data detected—VBI System 2	These bits are status bits only; they cannot be cleared or masked; Register 0x46 is used for this purpose
										1	CCAPD data detected—VBI System 2	
		Reserved					x	x	x			
		EVEN_FIELD				0					Current SD field is odd numbered	
						1					Current SD field is even numbered	
		Reserved		x	x							
		MPU_STIM_INTRQ	0								MPU_STIM_INTRQ = 0	
			1								MPU_STIM_INTRQ = 1	
0x46	Interrupt Status 2 (read only)	CCAPD_Q								0	Closed captioning not detected in the input video signal—VBI System 2	These bits can be cleared or masked by Register 0x47 and Register 0x48, respectively; note that the interrupt in Register 0x46 for the CCAP, Gemstar, CGMS, and WSS data uses the Mode 1 data slicer
										1	Closed captioning data detected in the video input signal—VBI System 2	
		GEMD_Q							0		Gemstar data not detected in the input video signal—VBI System 2	
									1		Gemstar data detected in the input video signal—VBI System 2	
		Reserved					x	x				
		SD_FIELD_CHNGD_Q				0					SD signal has not changed field from odd to even or vice versa	
						1					SD signal has changed Field from odd to even or vice versa	
		Reserved			x						Not used	
		Reserved		x							Not used	
		MPU_STIM_INTRQ_Q	0								Manual interrupt not set	
			1								Manual interrupt set	
0x47	Interrupt Clear 2 (write only)	CCAPD_CLR								0	Do not clear—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, Gemstar, CGMS, and WSS data uses the Mode 1 data slicer
										1	Clears CCAPD_Q bit—VBI System 2	
		GEMD_CLR							0		Do not clear	
									1		Clears GEMD_Q bit	
		Reserved					0	0				
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q bit	
		Reserved		x	x						Not used	
		MPU_STIM_INTRQ_CLR	0								Do not clear	
			1								Clears MPU_STIM_INTRQ_Q bit	
0x48	Interrupt Mask 2 (read/write)	$\overline{\text{CCAPD_MSK}}$								0	Masks CCAPD_Q bit—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, Gemstar, CGMS, and WSS data uses the Mode 1 data slicer
										1	Unmasks CCAPD_Q bit—VBI System 2	
		$\overline{\text{GEMD_MSK}}$							0		Masks GEMD_Q bit—VBI System 2	
									1		Unmasks GEMD_Q bit—VBI System 2	
		Reserved					0	0			Not used	
		$\overline{\text{SD_FIELD_CHNGD_MSK}}$				0					Masks SD_FIELD_CHNGD_Q bit	
						1					Unmasks SD_FIELD_CHNGD_Q bit	
		Reserved		0	0						Not used	
		$\overline{\text{MPU_STIM_INTRQ_MSK}}$	0								Masks MPU_STIM_INTRQ_Q bit	
			1								Unmasks MPU_STIM_INTRQ_Q bit	
0x49	Raw Status 3 (read only)	SD_OP_50Hz; SD 60 Hz/50 Hz frame rate at output								0	SD 60 Hz signal output	These bits are status bits only; they cannot be cleared or masked; Register 0x4A is used for this purpose
										1	SD 50 Hz signal output	
		SD_V_LOCK							0		SD vertical sync lock not established	
									1		SD vertical sync lock established	
		SD_H_LOCK						0			SD horizontal sync lock not established	
								1			SD horizontal sync lock established	
		Reserved					x				Not used	
		SCM_LOCK				0					SECAM lock not established	
						1					SECAM lock established	
		Reserved	x	x	x						Not used	

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x4A	Interrupt Status 3 (read only)	SD_OP_CHNG_Q; SD 60 Hz/50 Hz frame rate at output								0	No change in SD signal standard detected at the output	These bits can be cleared and masked by Register 0x4B and Register 0x4C, respectively
										1	A change in SD signal standard is detected at the output	
		SD_V_LOCK_CHNG_Q							0		No change in SD VSYNC lock status	
									1		SD VSYNC lock status has changed	
		SD_H_LOCK_CHNG_Q						0			No change in HSYNC lock status	
								1			SD HSYNC lock status has changed	
		SD_AD_CHNG_Q; SD autodetect changed					0				No change in AD_RESULT[2:0] bits in Status 1 register	
							1				AD_RESULT[2:0] bits in Status 1 register have changed	
		SCM_LOCK_CHNG_Q; SECAM lock				0					No change in SECAM lock status	
						1					SECAM lock status has changed	
		PAL_SW_LK_CHNG_Q			0						No change in PAL swinging burst lock status	
					1						PAL swinging burst lock status has changed	
		Reserved	x	x							Not used	
0x4B	Interrupt Clear 3 (write only)	SD_OP_CHNG_CLR								0	Do not clear	
										1	Clears SD_OP_CHNG_Q bit	
		SD_V_LOCK_CHNG_CLR							0		Do not clear	
									1		Clears SD_V_LOCK_CHNG_Q bit	
		SD_H_LOCK_CHNG_CLR						0			Do not clear	
								1			Clears SD_H_LOCK_CHNG_Q bit	
		SD_AD_CHNG_CLR					0				Do not clear	
							1				Clears SD_AD_CHNG_Q bit	
		SCM_LOCK_CHNG_CLR				0					Do not clear	
						1					Clears SCM_LOCK_CHNG_Q bit	
		PAL_SW_LK_CHNG_CLR			0						Do not clear	
					1						Clears PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	
0x4C	Interrupt Mask 3 (read/write)	$\overline{\text{SD_OP_CHNG_MSK}}$								0	Masks SD_OP_CHNG_Q bit	
										1	Unmasks SD_OP_CHNG_Q bit	
		$\overline{\text{SD_V_LOCK_CHNG_MSK}}$							0		Masks SD_V_LOCK_CHNG_Q bit	
									1		Unmasks SD_V_LOCK_CHNG_Q bit	
		$\overline{\text{SD_H_LOCK_CHNG_MSK}}$						0			Masks SD_H_LOCK_CHNG_Q bit	
								1			Unmasks SD_H_LOCK_CHNG_Q bit	
		$\overline{\text{SD_AD_CHNG_MSK}}$					0				Masks SD_AD_CHNG_Q bit	
							1				Unmasks SD_AD_CHNG_Q bit	
		$\overline{\text{SCM_LOCK_CHNG_MSK}}$				0					Masks SCM_LOCK_CHNG_Q bit	
						1					Unmasks SCM_LOCK_CHNG_Q bit	
		$\overline{\text{PAL_SW_LK_CHNG_MSK}}$			0						Masks PAL_SW_LK_CHNG_Q bit	
					1						Unmasks PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	
0x4E	Interrupt Status 4 (read only)	VDP_CCAPD_Q								0	Closed captioning not detected	These bits can be cleared and masked by Register 0x4F and Register 0x50, respectively; note that an interrupt in Register 0x4E for the CCAP, Gemstar, CGMS, WSS, VPS, PDC, UTC, and VITC data uses the VDP data slicer
										1	Closed captioning detected	
		Reserved							x			
		VDP_CGMS_WSS_CHNGD_Q; see 0x9C Bit 4 of user sub map to determine whether interrupt is issued for a change in detected data or for when data is detected regardless of content						0			CGMS/WSS data is not changed/ not available	
								1			CGMS/WSS data is changed/available	
		Reserved					x					
		VDP_GS_VPS_PDC_UTC_CHNG_Q; see 0x9C Bit 5 of User Sub Map to determine whether interrupt is issued for a change in detected data or for when data is detected regardless of content				0					Gemstar/PDC/VPS/UTC data is not changed/not available	
						1					Gemstar/PDC/VPS/UTC data is changed/available	
		Reserved			x							
		VDP_VITC_Q		0							VITC data is not available in the VDP	
				1							VITC data is available in the VDP	
		Reserved	x									

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x4F	Interrupt Clear 4 (write only)	VDP_CCAPD_CLR								0	Do not clear	Note that an interrupt in Register 0x4E for the CCAP, Gemstar, CGMS, WSS, VPS, PDC, UTC, and VITC data uses the VDP data slicer
										1	Clears VDP_CCAPD_Q	
		Reserved							0			
		VDP_CGMS_WSS_CHNGD_CLR						0			Do not clear	
								1			Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		VDP_GS_VPS_PDC_UTC_CHNG_CLR				0					Do not clear	
						1					Clears VDP_GS_VPS_PDC_UTC_CHNG_Q	
		Reserved			0							
		VDP_VITC_CLR		0							Do not clear	
				1							Clears VDP_VITC_Q	
		Reserved	0									
0x50	Interrupt Mask 4	$\overline{\text{VDP_CCAPD_MSK}}$								0	Masks VDP_CCAPD_Q	Note that an interrupt in Register 0x4E for the CCAP, Gemstar, CGMS, WSS, VPS, PDC, UTC, and VITC data uses the VDP data slicer
										1	Unmasks VDP_CCAPD_Q	
		Reserved							0			
		$\overline{\text{VDP_CGMS_WSS_CHNGD_MSK}}$						0			Masks VDP_CGMS_WSS_CHNGD_Q	
								1			Unmasks VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		$\overline{\text{VDP_GS_VPS_PDC_UTC_CHNG_MSK}}$				0					Masks VDP_GS_VPS_PDC_UTC_CHNG_Q	
						1					Unmasks VDP_GS_VPS_PDC_UTC_ CHNG_Q	
		Reserved			0							
		$\overline{\text{VDP_VITC_MSK}}$		0							Masks VDP_VITC_Q	
				1							Unmasks VDP_VITC_Q	
		Reserved	0									
0x60	VDP_Config_1	VDP_TTXT_TYPE_MAN[1:0]							0	0	PAL: Teletext-ITU-BT.653-625/50-A, NTSC: reserved	
									0	1	PAL: Teletext-ITU-BT.653-625/50-B (WST), NTSC: Teletext-ITU-BT.653-525/60-B	
									1	0	PAL: Teletext-ITU-BT.653-625/50-C, NTSC: Teletext-ITU-BT.653-525/60-C, or EIA516 (NABTS)	
									1	1	PAL: Teletext-ITU-BT.653-625/50-D, NTSC: Teletext-ITU-BT.653-525/60-D	
		VDP_TTXT_TYPE_MAN_ENABLE						0			User programming of teletext type disabled	
								1			User programming of teletext type enabled	
		WST_PKT_DECODE_DISABLE					0				Enable hamming decoding of WST packets	
							1				Disable hamming decoding of WST packets	
		Reserved	1	0	0	0						
0x61	VDP_Config_2	Reserved					x	x	0	0		
		AUTO_DETECT_GS_TYPE				0					Disable autodetection of Gemstar type	
						1					Enable autodetection of Gemstar type	
		Reserved	0	0	0							
0x62	VDP_ADF_Config_1	ADF_DID[4:0]				1	0	1	0	1	User-specified DID sent in the ancillary data stream with VDP decoded data	
		ADF_MODE[1:0]		0	0						Nibble mode	
				0	1						Byte mode, no code restrictions	
				1	0						Byte mode with 0x00 and 0xFF prevented	
				1	1						Reserved	
		ADF_ENABLE	0								Disable insertion of VBI decoded data into ancillary 656 stream	
			1								Enable insertion of VBI decoded data into ancillary 656 stream	
0x63	VDP_ADF_Config_2	ADF_SDID[5:0]			1	0	1	0	1	0	User-specified SDID sent in the ancillary data stream with VDP decoded data	
		Reserved		x								
		DUPLICATE_ADF	0								Ancillary data packet is spread across the Y and C data streams	
			1								Ancillary data packet is duplicated on the Y and C data streams	

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x64	VDP_LINE_00E	VBI_DATA_P318[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 318 (PAL), NTSC—N/A	
		Reserved		0	0	0						
		MAN_LINE_PGM	0								Decode default standards on the lines indicated in Table 69	
			1								Manually program the VBI standard to be decoded on each line; see Table 70	If set to 1, all VBI_DATA_Px_Ny bits can be set as desired
0x65	VDP_LINE_00F	VBI_DATA_P319_N286[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 319 (PAL), Line 286 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P6_N23[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 6 (PAL), Line 23 (NTSC)	
0x66	VDP_LINE_010	VBI_DATA_P320_N287[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 320 (PAL), Line 287 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 7 (PAL), Line 24 (NTSC)	
0x67	VDP_LINE_011	VBI_DATA_P321_N288[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 321 (PAL), Line 288 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 8 (PAL), Line 25 (NTSC)	
0x68	VDP_LINE_012	VBI_DATA_P322[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 322 (PAL), NTSC—N/A	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 9 (PAL), NTSC—N/A	
0x69	VDP_LINE_013	VBI_DATA_P323[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 323 (PAL), NTSC—N/A	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 10 (PAL), NTSC—N/A	
0x6A	VDP_LINE_014	VBI_DATA_P324_N272[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 324 (PAL), Line 272 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 11 (PAL); NTSC—N/A	
0x6B	VDP_LINE_015	VBI_DATA_P325_N273[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 325 (PAL), Line 273 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 12 (PAL), Line 10 (NTSC)	
0x6C	VDP_LINE_016	VBI_DATA_P326_N274[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 326 (PAL), Line 274 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 13 (PAL), Line 11 (NTSC)	
0x6D	VDP_LINE_017	VBI_DATA_P327_N275[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 327 (PAL), Line 275 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 14 (PAL), Line 12 (NTSC)	
0x6E	VDP_LINE_018	VBI_DATA_P328_N276[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 328 (PAL), Line 276 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 15 (PAL), Line 13 (NTSC)	
0x6F	VDP_LINE_019	VBI_DATA_P329_N277[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 329 (PAL), Line 277 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 16 (PAL), Line 14 (NTSC)	
0x70	VDP_LINE_01A	VBI_DATA_P330_N278[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 330 (PAL), Line 278 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 17 (PAL), Line 15 (NTSC)	
0x71	VDP_LINE_01B	VBI_DATA_P331_N279[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 331 (PAL), Line 279 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 18 (PAL), Line 16 (NTSC)	
0x72	VDP_LINE_01C	VBI_DATA_P332_N280[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 332 (PAL), Line 280 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 19 (PAL), Line 17 (NTSC)	
0x73	VDP_LINE_01D	VBI_DATA_P333_N281[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 333 (PAL), Line 281 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 20 (PAL), Line 18 (NTSC)	

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x74	VDP_LINE_01E	VBI_DATA_P334_N282[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 334 (PAL), Line 282 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 21 (PAL), Line 19 (NTSC)	
0x75	VDP_LINE_01F	VBI_DATA_P335_N283[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 335 (PAL), Line 283 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 22 (PAL), Line 20 (NTSC)	
0x76	VDP_LINE_020	VBI_DATA_P336_N284[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 336 (PAL), Line 284 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 23 (PAL), Line 21 (NTSC)	
0x77	VDP_LINE_021	VBI_DATA_P337_N285[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 337 (PAL), Line 285 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P24_N22[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 24 (PAL), Line 22 (NTSC)	
0x78	VDP_STATUS (read only)	CC_AVL								0	Closed captioning not detected	CC_CLEAR resets the CC_AVL bit
										1	Closed captioning detected	
		CC_EVEN_FIELD							0		Closed captioning decoded from odd field	
									1		Closed captioning decoded from even field	
		CGMS_WSS_AVL						0			CGMS/WSS not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
								1			CGMS/WSS detected	
		Reserved					0					
		GS_PDC_VPS_UTC_AVL				0					GS/PDC/VPS/UTC not detected	GS_PDC_VPS_UTC_CLEAR resets the GS_PDC_VPS_UTC_AVL bit
						1					GS/PDC/VPS/UTC detected	
		GS_DATA_TYPE			0						Gemstar_1× detected	
					1						Gemstar_2× detected	
		VITC_AVL		0							VITC not detected	VITC_CLEAR resets the VITC_AVL bit
				1							VITC detected	
		TTXT_AVL	0								Teletext not detected	
			1								Teletext detected	
	VDP_STATUS_CLEAR (write only)	CC_CLEAR								0	Does not reinitialize the CCAP readback registers	This is a self-clearing bit
										1	Reinitializes the CCAP readback registers	
		Reserved							0			
		CGMS_WSS_CLEAR						0			Does not reinitialize the CGMS/WSS readback registers	This is a self-clearing bit
								1			Reinitializes the CGMS/WSS readback registers	
		Reserved					0					
		GS_PDC_VPS_UTC_CLEAR				0					Does not reinitialize the GS/PDC/VPS/UTC readback registers	This is a self-clearing bit
						1					Refreshes the GS/PDC/VPS/UTC readback registers	
		Reserved			0							
		VITC_CLEAR		0							Does not reinitialize the VITC readback registers	This is a self-clearing bit
				1							Reinitializes the VITC readback registers	
		Reserved	0									
0x79	VDP_CCAP_DATA_0 (read only)	CCAP_BYTE_1[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 1 of CCAP	
0x7A	VDP_CCAP_DATA_1 (read only)	CCAP_BYTE_2[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 2 of CCAP	
0x7D	VDP_CGMS_WSS_DATA_0 (read only)	CGMS_CRC[5:2]					x	x	x	x	Decoded CRC sequence for CGMS	
		Reserved	0	0	0	0						
0x7E	VDP_CGMS_WSS_DATA_1 (read only)	CGMS_WSS[13:8]			x	x	x	x	x	x	Decoded CGMS/WSS data	
		CGMS_CRC[1:0]	x	x							Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_WSS_DATA_2 (read only)	CGMS_WSS[7:0]	x	x	x	x	x	x	x	x	Decoded CGMS/WSS data	
0x84	VDP_GS_VPS_PDC_UTC_0 (read only)	GS_VPS_PDC_UTC_BYTE_0[7:0]	x	x	x	x	x	x	x	x	Decoded Gemstar/VPS/PDC/UTC data	
0x85	VDP_GS_VPS_PDC_UTC_1 (read only)	GS_VPS_PDC_UTC_BYTE_1[7:0]	x	x	x	x	x	x	x	x	Decoded Gemstar/VPS/PDC/UTC data	

Interrupt and VDP Map			Bit (Shading Indicates Default State)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x86	VDP_GS_VPS_PDC_UTC_2 (read only)	GS_VPS_PDC_UTC_BYTE_2[7:0]	x	x	x	x	x	x	x	x	Decoded Gemstar/VPS/PDC/UTC data	
0x87	VDP_GS_VPS_PDC_UTC_3 (read only)	GS_VPS_PDC_UTC_BYTE_3[7:0]	x	x	x	x	x	x	x	x	Decoded Gemstar/VPS/PDC/UTC data	
0x88	VDP_VPS_PDC_UTC_4 (read only)	VPS_PDC_UTC_BYTE_4[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x89	VDP_VPS_PDC_UTC_5 (read only)	VPS_PDC_UTC_BYTE_5[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8A	VDP_VPS_PDC_UTC_6 (read only)	VPS_PDC_UTC_BYTE_6[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8B	VDP_VPS_PDC_UTC_7 (read only)	VPS_PDC_UTC_BYTE_7[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8C	VDP_VPS_PDC_UTC_8 (read only)	VPS_PDC_UTC_BYTE_8[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8D	VDP_VPS_PDC_UTC_9 (read only)	VPS_PDC_UTC_BYTE_9[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8E	VDP_VPS_PDC_UTC_10 (read only)	VPS_PDC_UTC_BYTE_10[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x8F	VDP_VPS_PDC_UTC_11 (read only)	VPS_PDC_UTC_BYTE_11[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x90	VDP_VPS_PDC_UTC_12 (read only)	VPS_PDC_UTC_BYTE_12[7:0]	x	x	x	x	x	x	x	x	Decoded VPS/PDC/UTC data	
0x92	VDP_VITC_DATA_0 (read only)	VITC_DATA_0[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x93	VDP_VITC_DATA_1 (read only)	VITC_DATA_1[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x94	VDP_VITC_DATA_2 (read only)	VITC_DATA_2[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x95	VDP_VITC_DATA_3 (read only)	VITC_DATA_3[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x96	VDP_VITC_DATA_4 (read only)	VITC_DATA_4[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x97	VDP_VITC_DATA_5 (read only)	VITC_DATA_5[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x98	VDP_VITC_DATA_6 (read only)	VITC_DATA_6[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x99	VDP_VITC_DATA_7 (read only)	VITC_DATA_7[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x9A	VDP_VITC_DATA_8 (read only)	VITC_DATA_8[7:0]	x	x	x	x	x	x	x	x	Decoded VITC data	
0x9B	VDP_VITC_CALC_CRC (read only)	VITC_CRC[7:0]	x	x	x	x	x	x	x	x	Decoded VITC CRC data	
0x9C	VDP_OUTPUT_SEL	Reserved					0	0	0	0		
		WSS_CGMS_CB_CHANGE				0					Disable content-based updating of CGMS and WSS data	The available bit shows the availability of data only when its content has changed
						1					Enable content-based updating of CGMS and WSS data	
		GS_VPS_PDC_UTC_CB_CHANGE			0						Disable content-based updating of Gemstar, VPS, PDC, and UTC data	
					1						Enable content-based updating of Gemstar, VPS, PDC, and UTC data	
		I²C_GS_VPS_PDC_UTC[1:0]	0	0							Gemstar_1×/Gemstar_2×	Standard expected to be decoded
			0	1							VPS	
			1	0							PDC	
			1	1							UTC	

[1] Shading indicates default values.
[2] x indicates a bit that keeps the last written value.

PCB LAYOUT RECOMMENDATIONS

The ADV7180 is a high precision, high speed, mixed-signal device. To achieve the maximum performance from the part, it is important to have a well laid out PCB. The following is a guide for designing a board using the ADV7180.

ANALOG INTERFACE INPUTS

Take care when routing the inputs on the PCB. Keep track lengths to a minimum, and use 75 Ω trace impedances when possible. In addition, trace impedances other than 75 Ω increase the chance of reflections.

POWER SUPPLY DECOUPLING

It is recommended to decouple each power supply pin with 0.1 µF and 10 nF capacitors. The fundamental idea is to have a decoupling capacitor within about 0.5 cm of each power pin. In addition, avoid placing the capacitor on the opposite side of the PCB from the ADV7180 because doing so interposes inductive vias in the path. The decoupling capacitors must be located between the power plane and the power pin. Current must flow from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. Placing a via underneath the 100 nF capacitor pads, down to the power plane, is the best approach (see Figure 56).

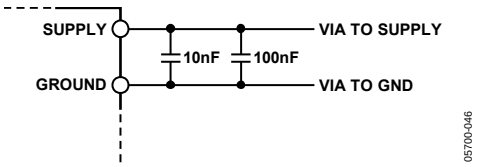


Figure 56. Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of P_{VDD}. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (A_{VDD}, D_{VDD}, D_{VDDIO}, and P_{VDD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least P_{VDD}, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended.

Experience repeatedly shows that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

PLL

Place the PLL loop filter components as close as possible to the ELPF pin. It must also be placed on the same side of the PCB as the ADV7180. Do not place any digital or other high frequency traces near these components. Use the values suggested in this data sheet with tolerances of 10% or less.

VREFN AND VREFP

Place the circuit associated with these pins as close as possible and on the same side of the PCB as the ADV7180.

DIGITAL OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7180. If series resistors are used, place them as close as possible to the ADV7180 pins. However, try not to add vias or extra length to the output trace to place the resistors closer.

If possible, limit the capacitance that each of the digital outputs drives to less than 15 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7180, creating more digital noise on its power supplies.

The 40-lead and 32-lead LFCSP have an exposed metal paddle on the bottom of the package. This paddle must be soldered to PCB ground for proper heat dissipation and for noise and mechanical strength benefits.

DIGITAL INPUTS

The digital inputs on the ADV7180 are designed to work with 1.8 V to 3.3 V signals and are not tolerant of 5 V signals. Extra components are needed if 5 V logic signals are required to be applied to the decoder.

TYPICAL CIRCUIT CONNECTION

Examples of how to connect the 40-lead LFCSP, 64-lead LQFP, 48-lead LQFP, and 32-lead LFCSP video decoders are shown in Figure 57, Figure 58, Figure 59, and Figure 60. For a detailed schematic of the ADV7180 evaluation boards, contact a local Analog Devices field applications engineer or an Analog Devices distributor.

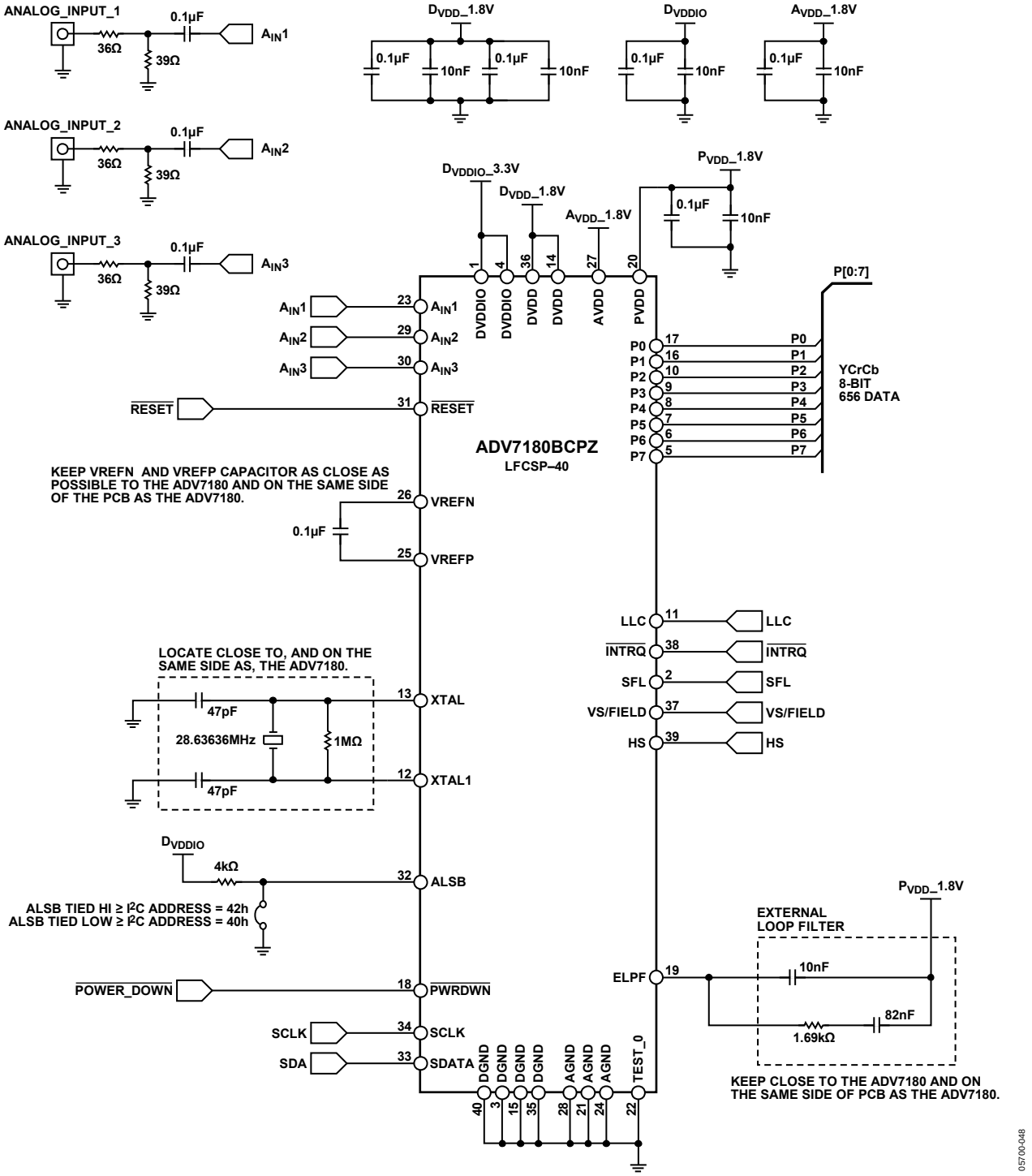


Figure 57. 40-Lead LFCSP Typical Connection Diagram

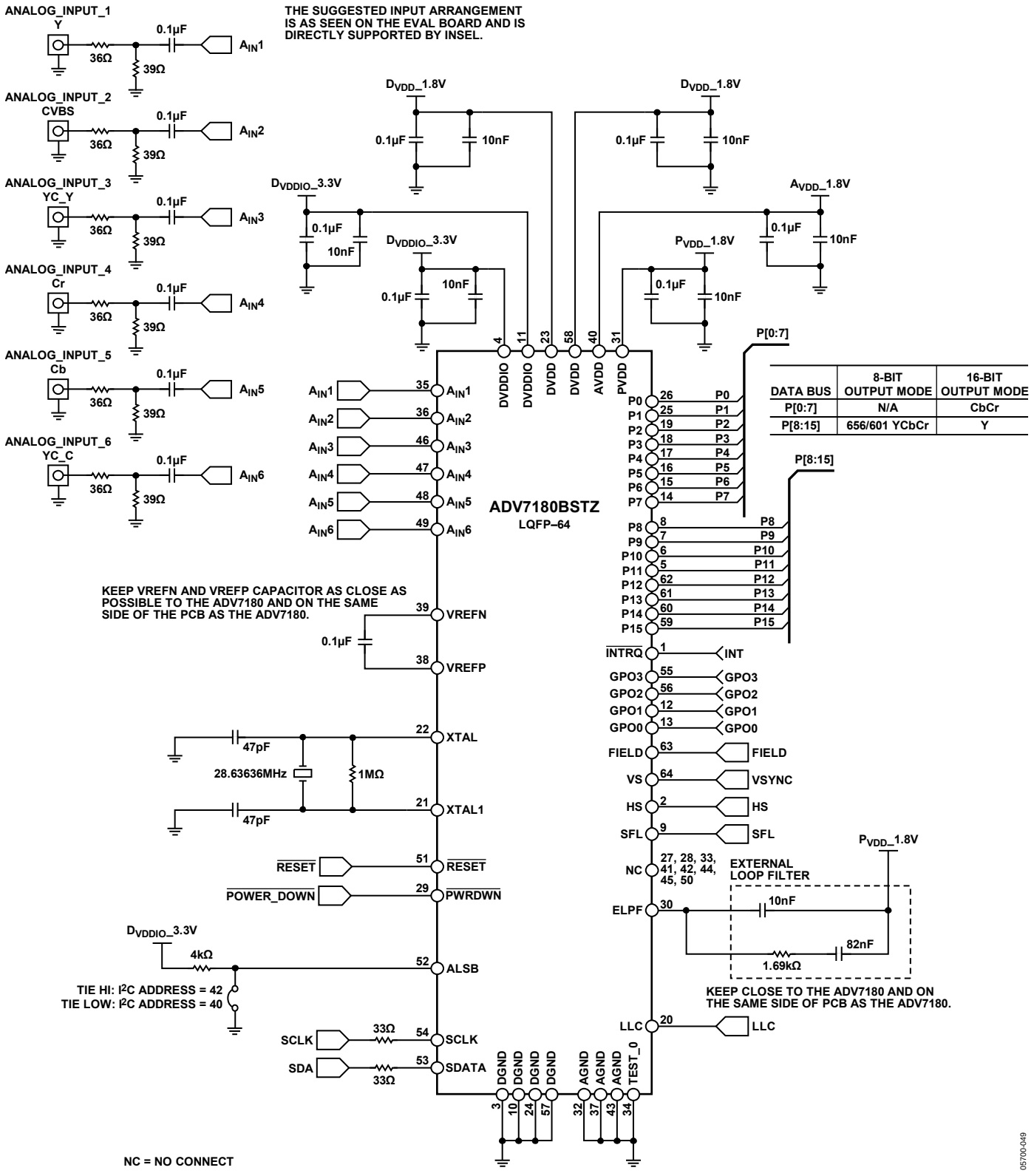
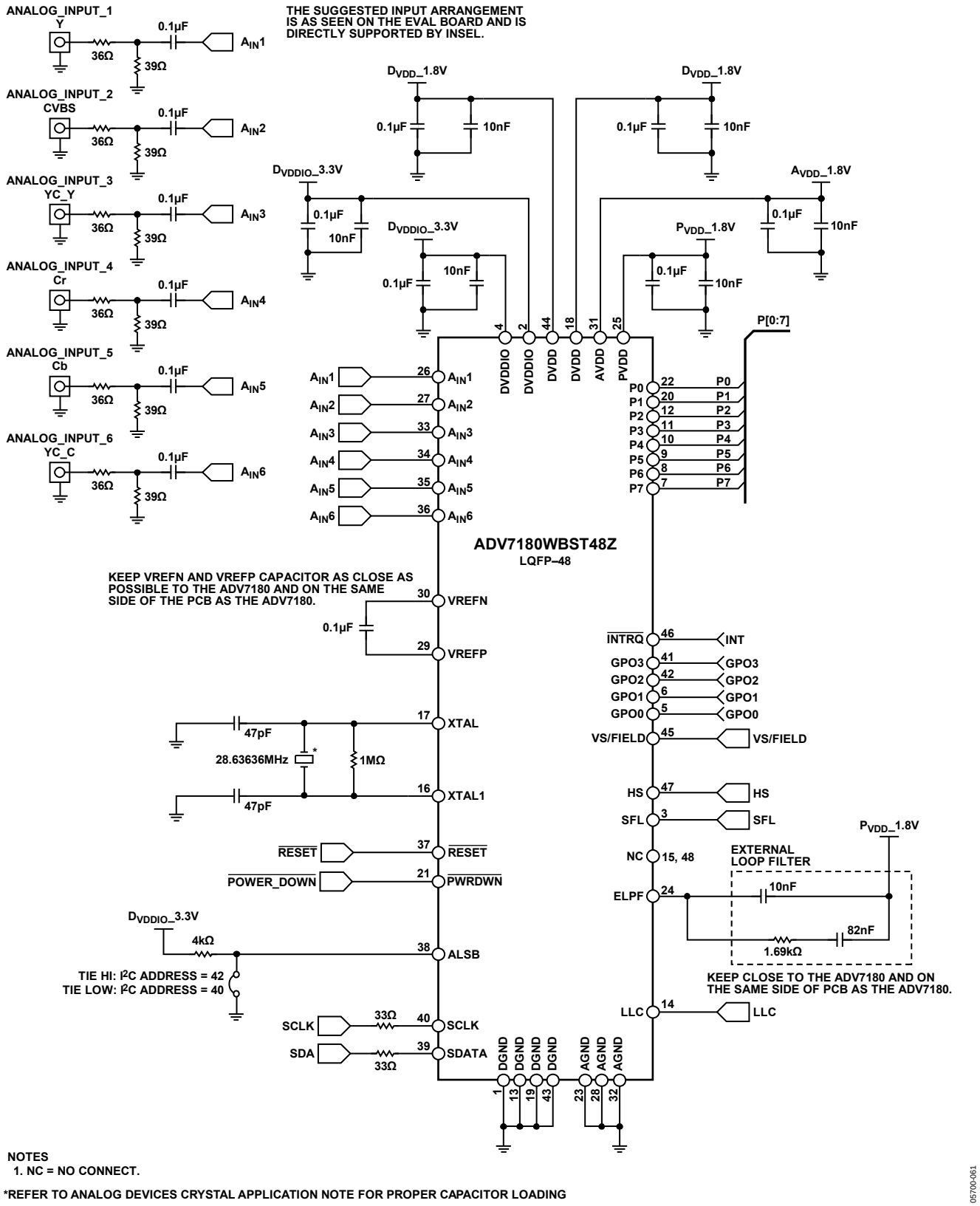


Figure 58. 64-Lead LQFP Typical Connection Diagram



NOTES
1. NC = NO CONNECT.

*REFER TO ANALOG DEVICES CRYSTAL APPLICATION NOTE FOR PROPER CAPACITOR LOADING

Figure 59. 48-Lead LQFP Typical Connection Diagram

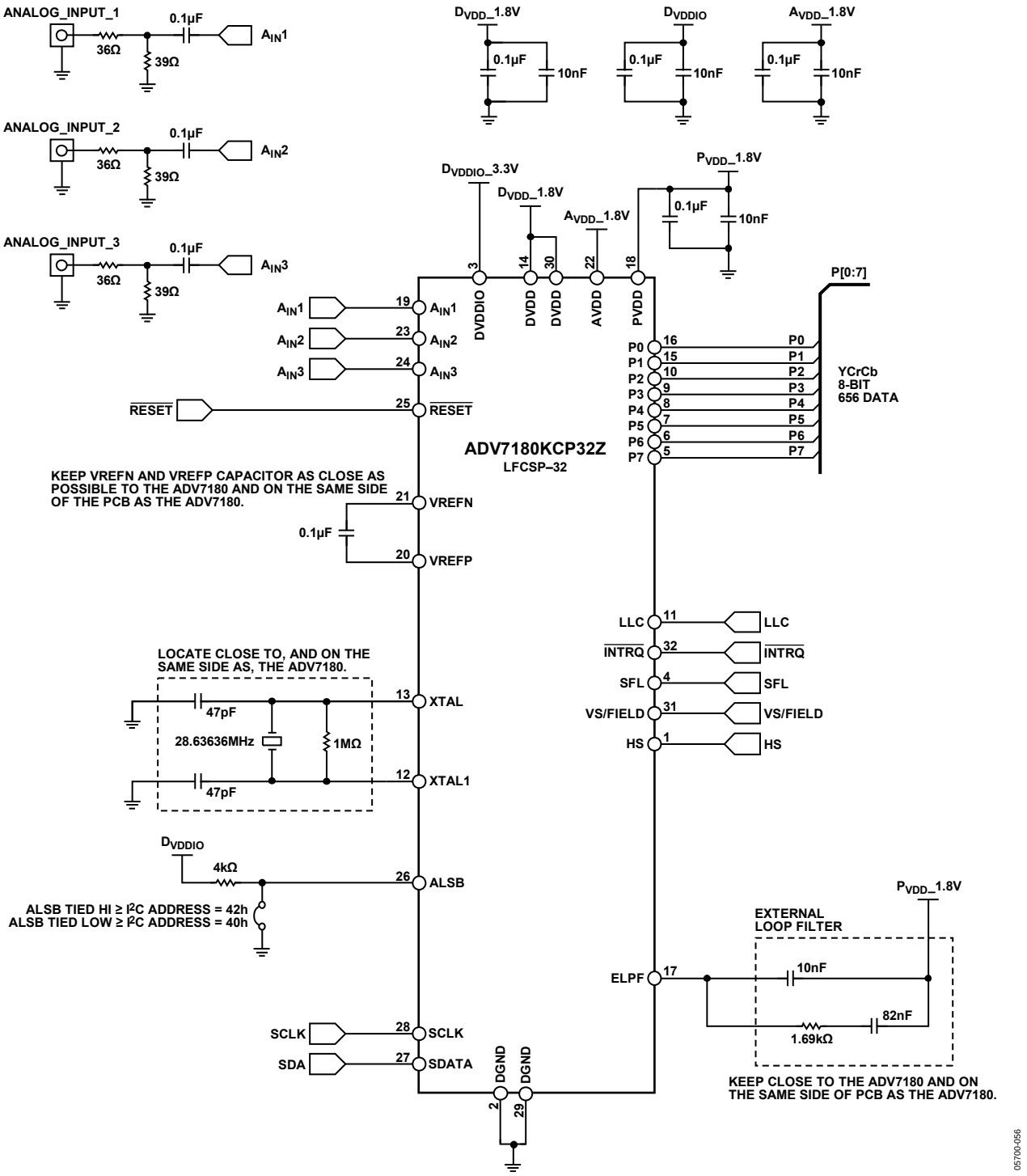
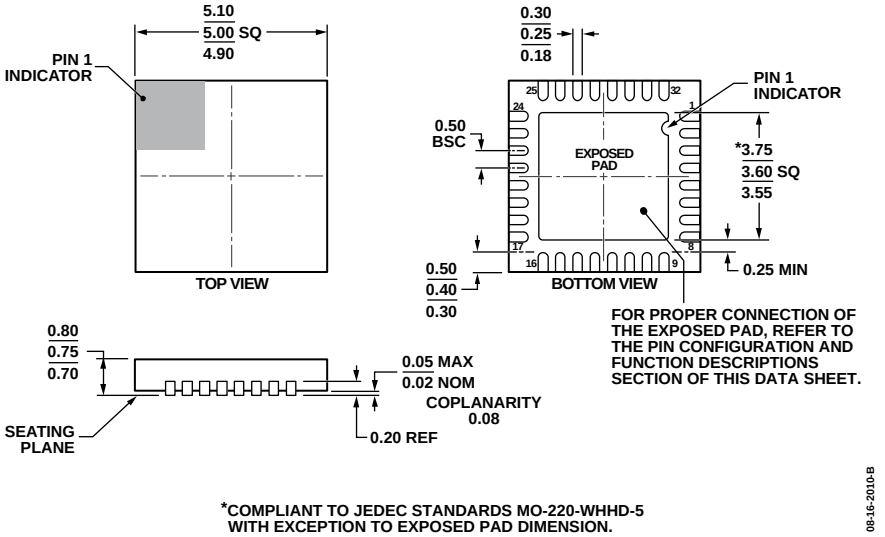


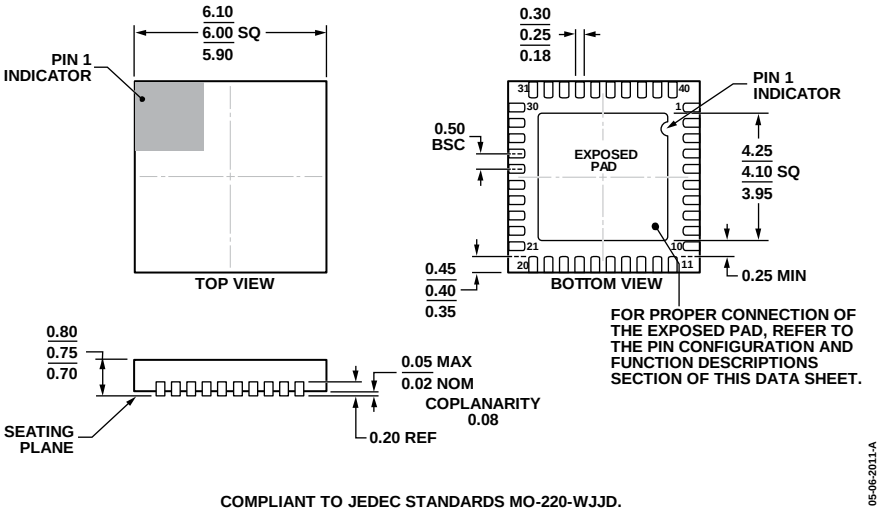
Figure 60. 32-Lead LFCSP Typical Connection Diagram

OUTLINE DIMENSIONS



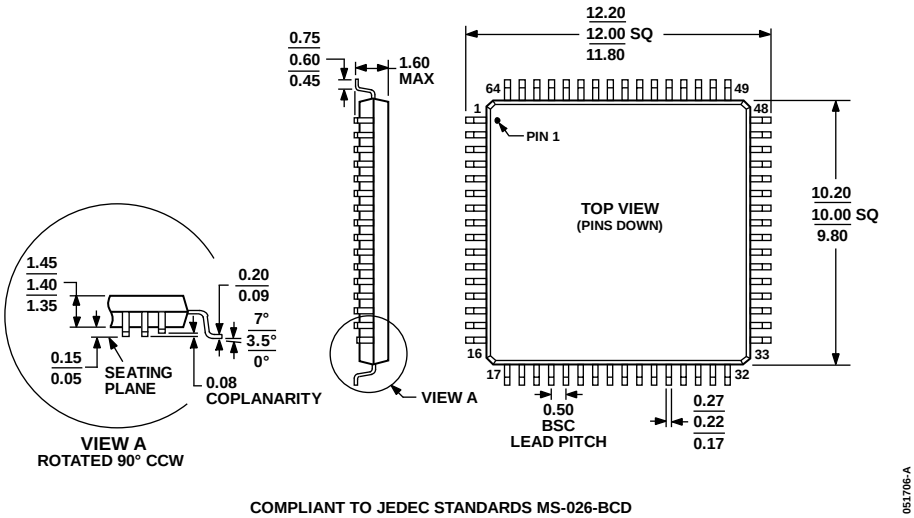
*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 61. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters



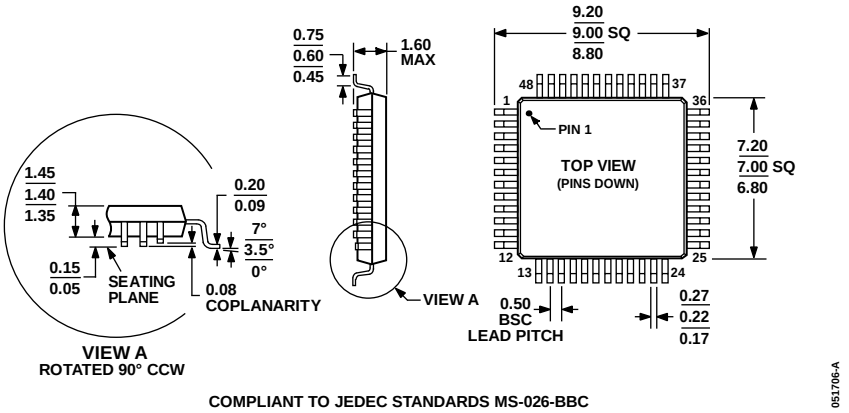
COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 62. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 63. 64-Lead Low Profile Quad Flat Package [LQFP]
10 mm × 10 mm Body
(ST-64-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 64. 48-Lead Low Profile Quad Flat Package [LQFP]
7 mm × 7 mm Body
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7180KCP32Z	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7180KCP32Z-RL	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7180BCPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
ADV7180BCPZ-REEL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
ADV7180BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7180BSTZ-REEL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7180WBCP32Z	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7180WBCP32Z-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7180WBCPZ	−40°C to +125°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
ADV7180WBCPZ-REEL	−40°C to +125°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
ADV7180WBSTZ	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7180WBSTZ-REEL	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7180WBST48Z	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180WBST48Z-RL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180KST48Z	−10°C to +70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180KST48Z-RL	−10°C to +70°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180BST48Z	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180BST48Z-RL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
ADV7180BCP32Z	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7180BCP32Z-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-ADV7180LQEBZ		Evaluation Board for the 64-Lead LQFP	
EVAL-ADV7180LFEBZ		Evaluation Board for the 40-Lead LFCSP	
EVAL-ADV7180-32EBZ		Evaluation Board for the 32-Lead LFCSP	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7180W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models, and designers should review the product Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific automotive reliability reports for these models.

Note that the ADV7180 is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C (±5°C).

In addition, it is backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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