HDMI/DVI TMDS Equalizer

ADV3003

FEATURES

- One input, one output HDMI/DVI high speed signal equalizer/driver
- Enables HDMI 1.3 receive-compliant input
  - Four TMDS channels per input/output
  - Supports 250 Mbps to 2.25 Gbps data rates
  - Supports 25 MHz to 225 MHz pixel clocks
  - Fully buffered unidirectional inputs/outputs
  - Equalized inputs for operation with long HDMI cables (20 meters at 2.25 Gbps)
  - Pre-emphasized outputs
  - Matched 50 Ω input and output on-chip terminations
  - Low added jitter
  - Transmitter disable feature
    - Reduces power dissipation
    - Disables input terminations
- Single-supply operation (3.3 V)
- Standards compliant: HDMI receiver, DVI
- 40-lead, 6 mm × 6 mm, RoHS-compliant LFCSP

APPLICATIONS

- Multiple input displays
- Advanced television set (HDTV) front panel connectors
- HDMI/DVI cable extenders

FUNCTIONAL BLOCK DIAGRAM

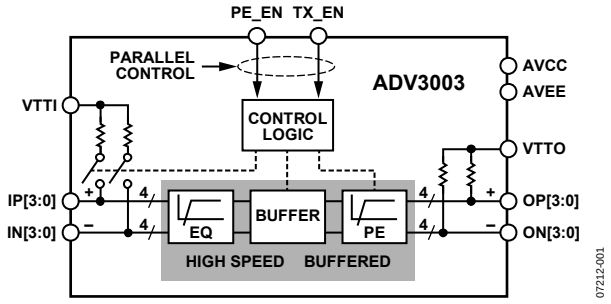


Figure 1.

TYPICAL APPLICATION DIAGRAM

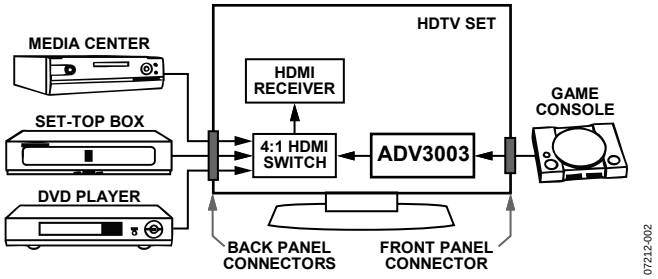


Figure 2.

GENERAL DESCRIPTION

The ADV3003 is a 4-channel transition minimized differential signaling (TMDS) buffer featuring equalized inputs and pre-emphasized outputs. The ADV3003 features 50 Ω input and output terminations, providing full-swing output signal recovery and minimizing reflections for improved system signal integrity. The ADV3003 is targeted at HDMI™/DVI applications and is ideal for use in systems with long cable runs, long PCB traces, and designs with interior cabling.

The ADV3003 is provided in a 40-lead, LFCSP, surface-mount, RoHS-compliant, plastic package and is specified to operate over the −40°C to +85°C temperature range.

PRODUCT HIGHLIGHTS

1. Supports data rates up to 2.25 Gbps, enabling 1080p deep color (12-bit color) HDMI formats and greater than UXGA (1600 × 1200) DVI resolutions.
2. The 12 dB input cable equalizer enables the use of long cables at the input. For a typical 24 AWG cable, the ADV3003 compensates for more than 20 meters at data rates up to 2.25 Gbps.
3. The selectable 6 dB of output pre-emphasis allows the ADV3003 to drive high loss output cables or long PCB traces.
4. Matched 50 Ω on-chip input and output terminations improve system signal integrity.
5. An external control pin, PE_EN, sets the output pre-emphasis to either 0 dB or 6 dB.
6. An external control pin, TX_EN, simultaneously disables both the transmitter and the on-chip input terminations. This feature reduces the power dissipation of the ADV3003 and indicates to a connected source when the ADV3003 is disabled.

Rev. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2008 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

2/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Maximum Data Rate (DR) per Channel	NRZ	2.25			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			10^{-9}	
Added Deterministic Jitter	DR ≤ 2.25 Gbps, PRBS $2^7 - 1$		25		ps (p-p)
Added Random Jitter			1		ps (rms)
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew[1]	At output		50		ps
EQUALIZATION PERFORMANCE					
Receiver (Fixed Setting)[2]	Boost frequency = 1.125 GHz		12		dB
Transmitter (Pre-Emphasis On)[3]	Boost frequency = 1.125 GHz		6		dB
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage (V_{ICM})		AVCC − 800		AVCC	mV
OUTPUT CHARACTERISTICS[4]					
High Voltage Level	Single-ended high speed channel	AVCC − 200		AVCC + 10	mV
Low Voltage Level	Single-ended high speed channel	AVCC − 600		AVCC − 400	mV
Rise/Fall Time (20% to 80%)		75		178	ps
TERMINATION					
Input Termination Resistance	Single-ended		50		Ω
Output Termination Resistance	Single-ended		50		Ω
POWER SUPPLY					
AVCC	Operating range (3.3 V ± 10%)	3	3.3	3.6	V
QUIESCENT CURRENT					
AVCC	Output disabled		20	40	mA
	Output enabled, pre-emphasis off		32	50	mA
	Output enabled, pre-emphasis on		66	80	mA
VTTI	Input termination on[5]		40	54	mA
VTTO	Output termination on, pre-emphasis off		40	50	mA
	Output termination on, pre-emphasis on		80	100	mA
	Output disabled		0	1	mA
POWER DISSIPATION[6]					
	Output disabled		66	148	mW
	Output enabled, pre-emphasis off		370	553	mW
	Output enabled, pre-emphasis on		686	937	mW
PARALLEL CONTROL INTERFACE	TX_EN, PE_EN				
Input High Voltage, V_{IH}		2			V
Input Low Voltage, V_{IL}				0.8	V

[1] Differential interpair skew is measured between the TMDS pairs of the HDMI/DVI link.
[2] ADV3003 output meets the transmitter eye diagram mask as defined in the HDMI Standard Version 1.3a and the DVI Standard Version 1.0.
[3] Cable output meets the receiver eye diagram mask as defined in the HDMI Standard Version 1.3a and the DVI Standard Version 1.0.
[4] PE = 0 dB.
[5] Typical value assumes the HDMI/DVI link is active with nominal signal swings. Minimum and maximum limits are measured at the extremes of input termination resistance and input voltage swing, respectively .
[6] The total power dissipation excludes power dissipated in the 50 Ω off-chip loads.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVCC to AVEE	3.7 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
Internal Power Dissipation	2.0 W
High Speed Input Voltage	AVCC − 1.4 V < V_{IN} < AVCC + 0.6 V
High Speed Differential Input Voltage	2.0 V
Parallel Interface (TX_EN, PE_EN)	AVEE − 0.3 V < V_{IN} < AVCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a 4-layer JEDEC circuit board for surface-mount packages. $_{JC}$ is specified for the exposed pad soldered to the circuit board with no airflow.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	31.9	2.6	°C/W

MAXIMUM POWER DISSIPATION

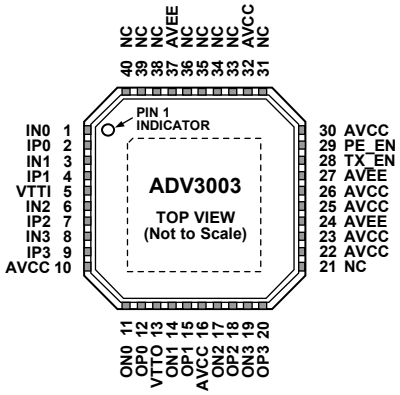
The maximum power that can be safely dissipated by the ADV3003 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating as determined by the thermal resistance coefficients.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE ADV3003 LFCSP HAS AN EXPOSED PADDLE (ePAD) ON THE UNDERSIDE OF THE PACKAGE, WHICH AIDS IN HEAT DISSIPATION. THE ePAD MUST BE ELECTRICALLY CONNECTED TO THE AVEE SUPPLY PLANE TO MEET ELECTRICAL AND THERMAL SPECIFICATIONS.

07212-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	IN0	HS, I	High Speed Input Complement.
2	IP0	HS, I	High Speed Input.
3	IN1	HS, I	High Speed Input Complement.
4	IP1	HS, I	High Speed Input.
5	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
6	IN2	HS, I	High Speed Input Complement.
7	IP2	HS, I	High Speed Input.
8	IN3	HS, I	High Speed Input Complement.
9	IP3	HS, I	High Speed Input.
10, 16, 22, 23, 25, 26, 30, 32	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
11	ON0	HS, O	High Speed Output Complement.
12	OP0	HS, O	High Speed Output.
13	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
14	ON1	HS, O	High Speed Output Complement.
15	OP1	HS, O	High Speed Output.
17	ON2	HS, O	High Speed Output Complement.
18	OP2	HS, O	High Speed Output.
19	ON3	HS, O	High Speed Output Complement.
20	OP3	HS, O	High Speed Output.
24, 27, 37, ePAD	AVEE	Power	Negative Analog Supply. 0 V nominal.
28	TX_EN	Control	High Speed Output Enable Parallel Interface.
29	PE_EN	Control	High Speed Pre-Emphasis Enable Parallel Interface.
21, 31, 33, 34, 35, 36, 38, 39, 40	NC	NC	No Connect.

[1] HS = high speed, I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

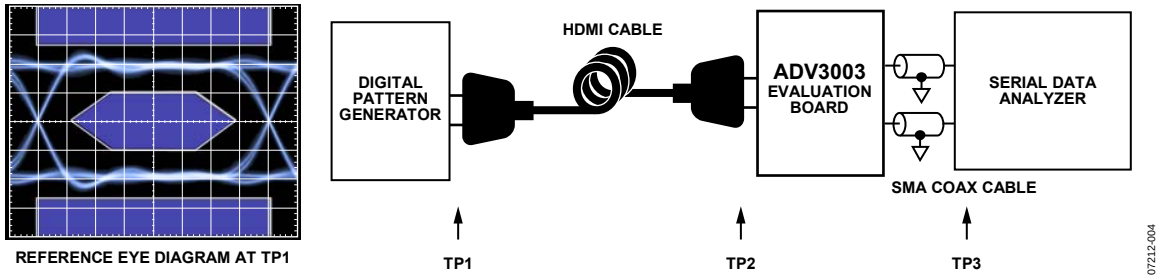


Figure 4. Test Circuit Diagram for Rx Eye Diagrams

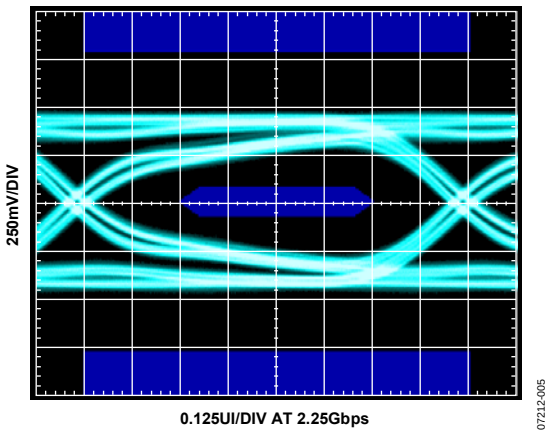


Figure 5. Rx Eye Diagram at TP2 (Cable = 2 Meters, 24 AWG)

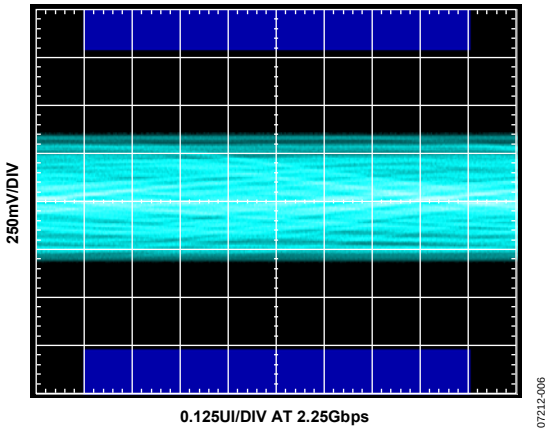


Figure 6. Rx Eye Diagram at TP2 (Cable = 20 Meters, 24 AWG)

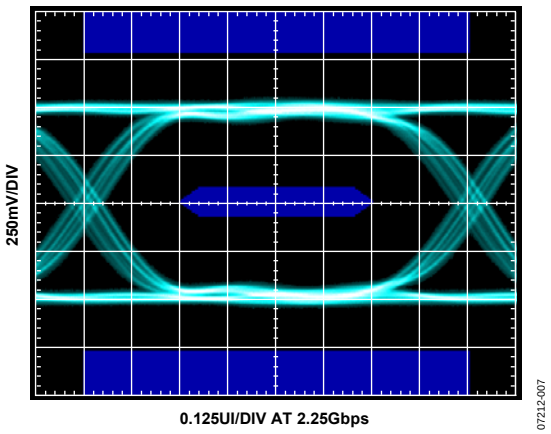


Figure 7. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 2 Meters, 24 AWG)

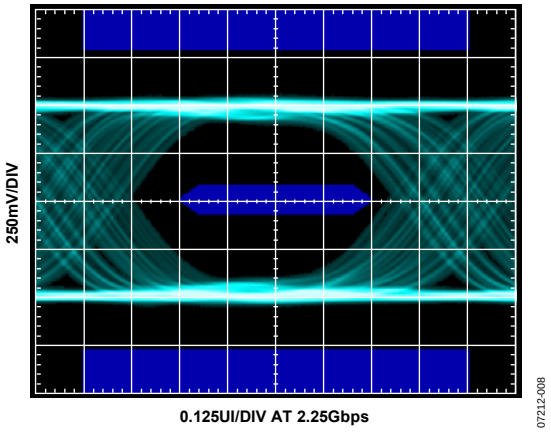


Figure 8. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 20 Meters, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

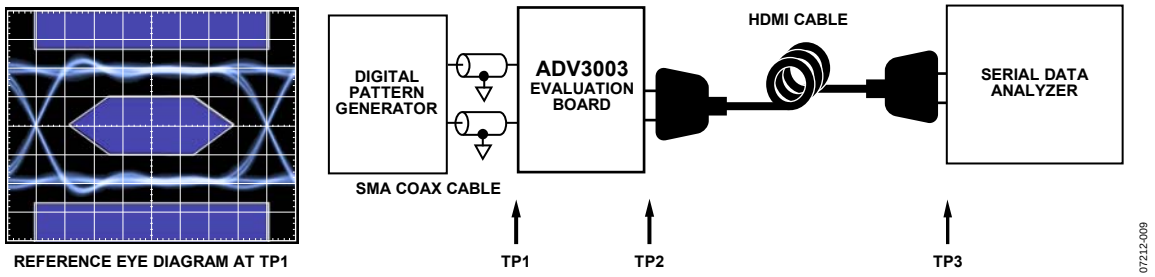


Figure 9. Test Circuit Diagram for Tx Eye Diagrams

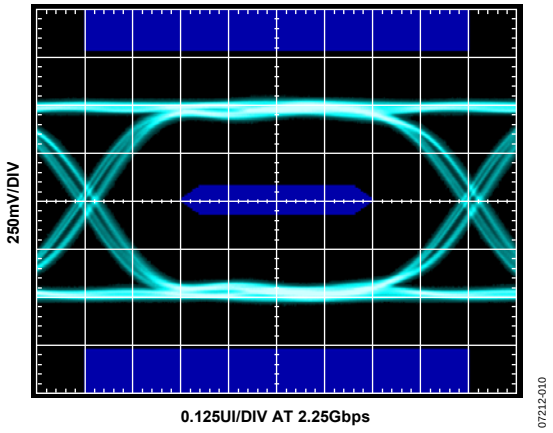


Figure 10. Tx Eye Diagram at TP2, PE = 0 dB

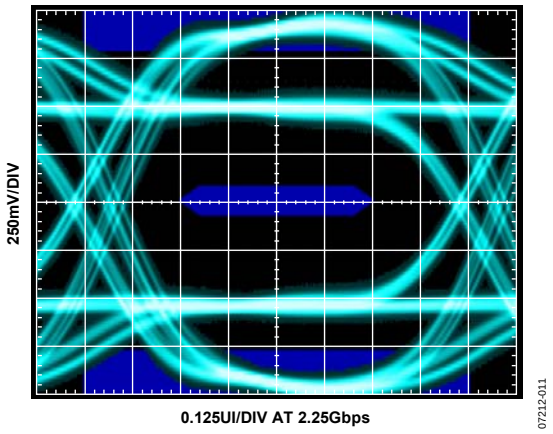


Figure 11. Tx Eye Diagram at TP2, PE = 6 dB

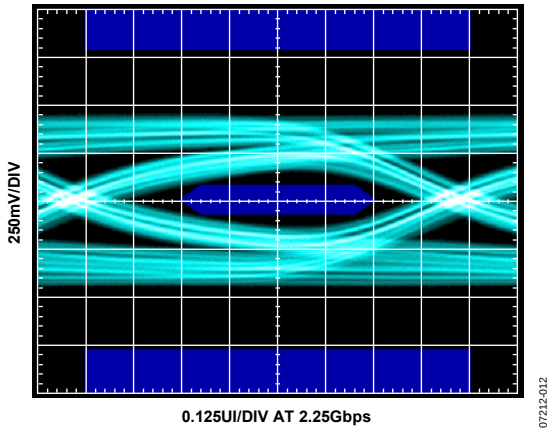


Figure 12. Tx Eye Diagram at TP3, PE = 0 dB (Cable = 6 Meters, 24 AWG)

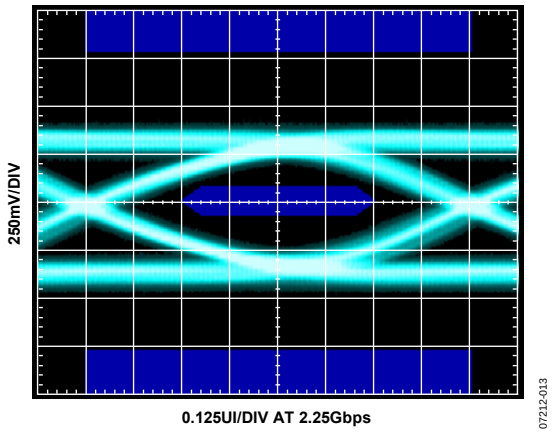


Figure 13. Tx Eye Diagram at TP3, PE = 6 dB (Cable = 10 Meters, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

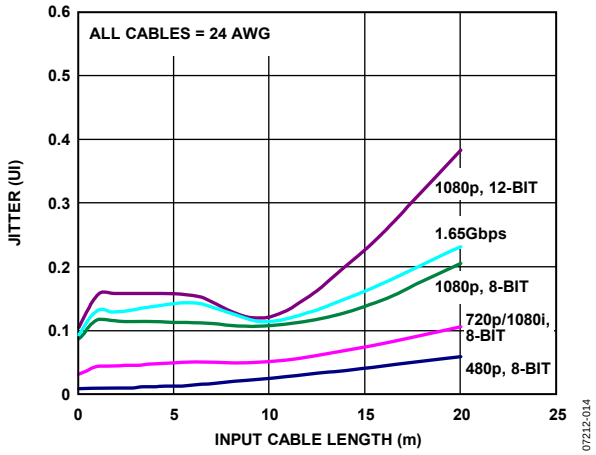


Figure 14. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

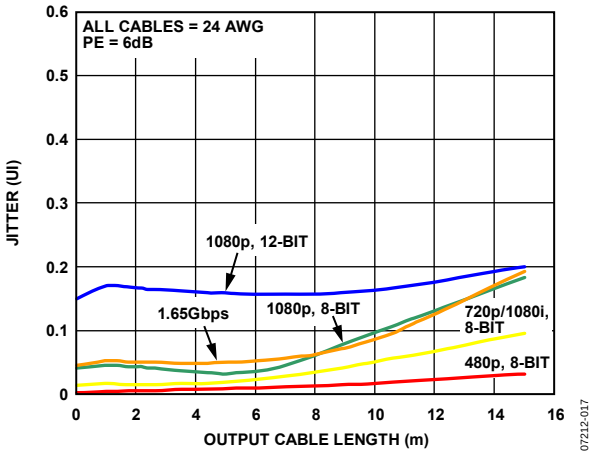


Figure 17. Jitter vs. Output Cable Length (See Figure 9 for Test Setup)

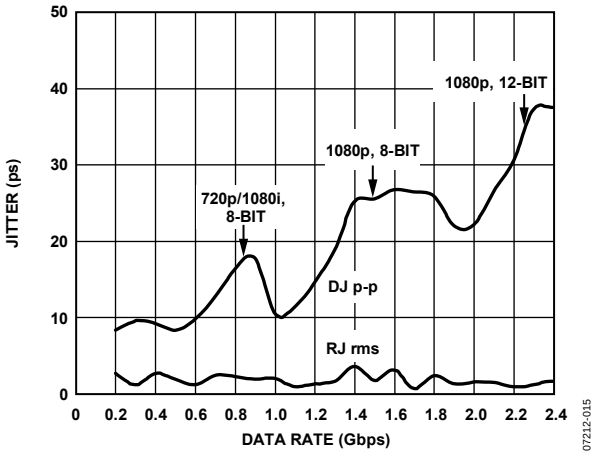


Figure 15. Jitter vs. Data Rate

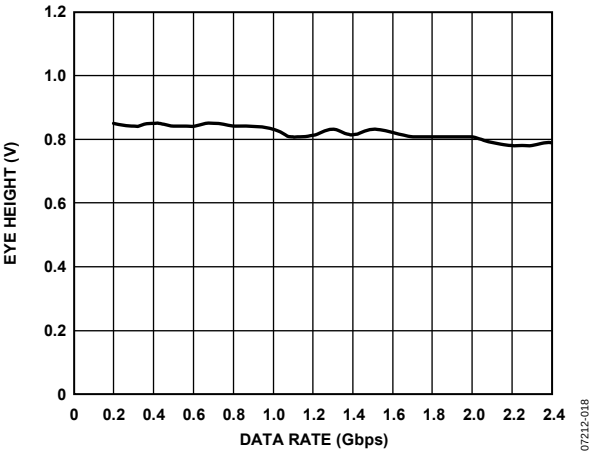


Figure 18. Eye Height vs. Data Rate

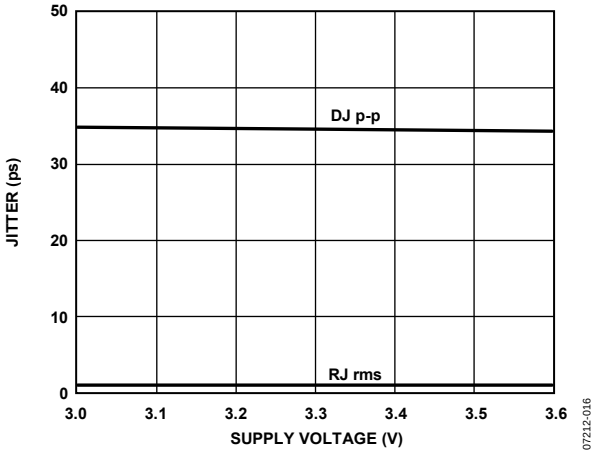


Figure 16. Jitter vs. Supply Voltage

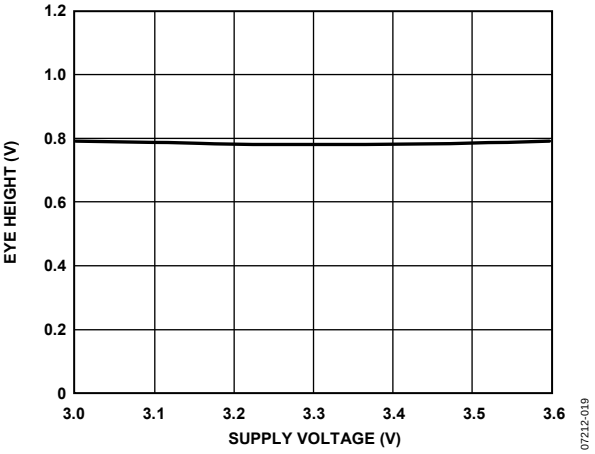


Figure 19. Eye Height vs. Supply Voltage

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

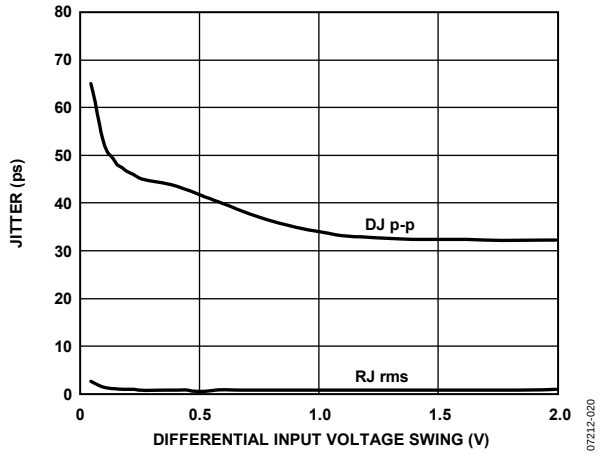


Figure 20. Jitter vs. Differential Input Voltage Swing

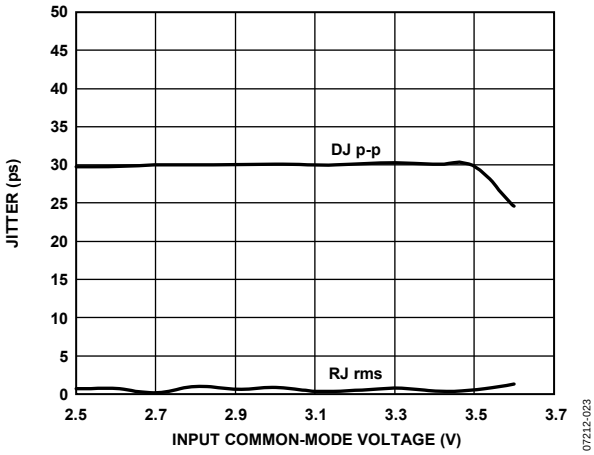


Figure 23. Jitter vs. Input Common-Mode Voltage

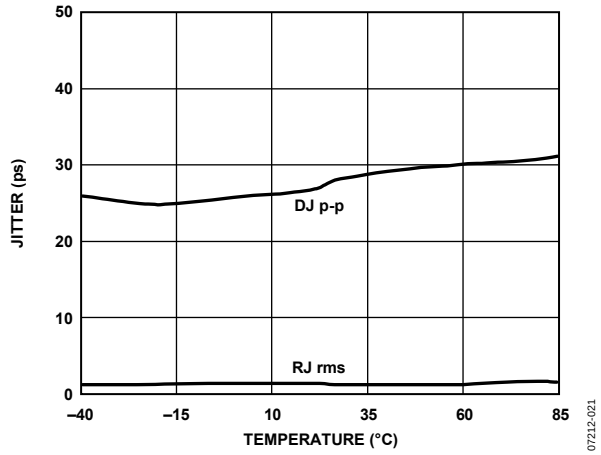


Figure 21. Jitter vs. Temperature

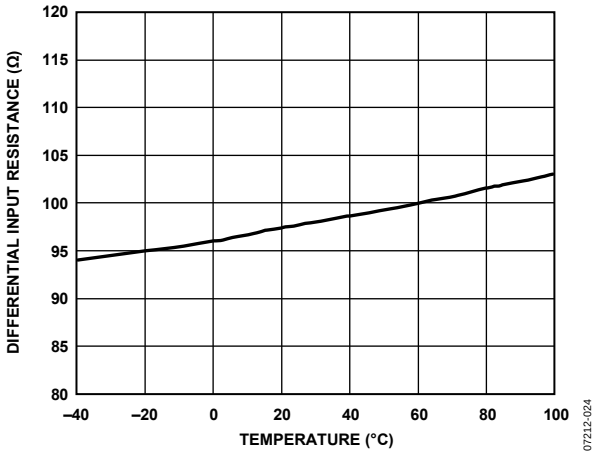


Figure 24. Differential Input Resistance vs. Temperature

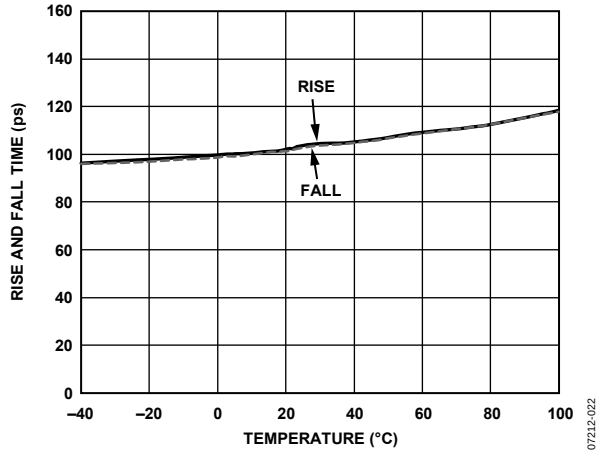


Figure 22. Rise and Fall Time vs. Temperature

THEORY OF OPERATION

INTRODUCTION

The primary function of the ADV3003 is to buffer the four high speed channels of a single HDMI or DVI link. The HDMI/DVI link consists of four differential, high speed channels and four auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 2.25 Gbps.

All four high speed TMDS channels on the ADV3003 are identical; that is, the pixel clock can be run on any of the four TMDS channels. Receive channel compensation (12 dB of fixed equalization) is provided for the high speed channels to support long input cables. The ADV3003 also includes selectable pre-emphasis for driving high loss output cables or long PCB traces.

In the intended application, the ADV3003 is placed between a source and a sink, with long cable runs at both the input and the output.

INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 25. When the transmitter of the ADV3003 is disabled by setting the TX_EN control pin as shown in Table 5, the input termination resistors are also disabled to provide a high impedance node at the inputs. Disabling the input terminations when the transmitter is disabled indicates to any connected HDMI sources that the link through the ADV3003 is inactive.

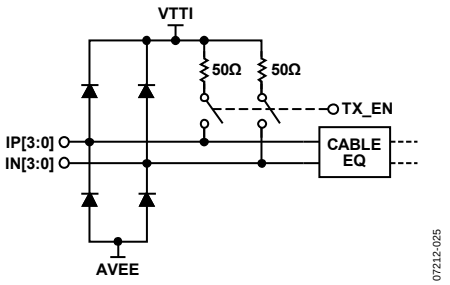


Figure 25. High Speed Input Simplified Schematic

The input equalizer provides 12 dB of high frequency boost. No specific cable length is suggested for this equalization level because cable performance varies widely among manufacturers; however, in general, the ADV3003 does not degrade input signals, even for short input cables. The ADV3003 can equalize more than 20 meters of a 24 AWG cable at 2.25 Gbps, for reference cables that exhibit an insertion loss of −15 dB at the fundamental frequency of this data rate.

OUTPUT CHANNELS

Each high speed output differential pair of the ADV3003 terminates to the 3.3 V VTTO power supply through two single-ended 50 Ω on-chip resistors, as shown in Figure 26.

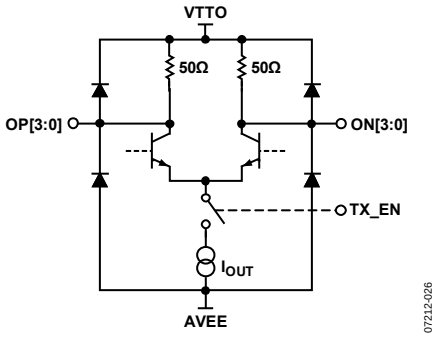


Figure 26. High Speed Output Simplified Schematic

The output termination resistors of the ADV3003 back-terminate the output TMDS transmission lines. These back-terminations, as recommended in the HDMI 1.3 specification, act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the ADV3003 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

The ADV3003 has an external control pin, TX_EN. The TX_EN pin must be connected to either a logic high (1) or low (0), in accordance with the logic values set forth in Table 1. The use of the TX_EN pin is described in Table 5. When the transmitter is enabled by setting TX_EN to 1, both the input and output terminations are enabled. Setting TX_EN to 0 disables the transmitter, reducing power when the transmitter is not in use. When the transmitter is disabled, the input termination resistors are also disabled to present a high impedance state at the input and indicate to any connected HDMI sources that the link through the ADV3003 is inactive.

Table 5. Transmitter Enable Setting

TX_EN	Input Termination	Transmitter State	Output Termination
0	Off	Off	On
1	On	On	On

The ADV3003 also includes two levels of programmable output pre-emphasis, 0 dB and 6 dB. The output pre-emphasis level can be manually configured by setting the PE_EN pin. The PE_EN pin must be connected to either a logic high (1) or low (0), in accordance with the logic values set forth in Table 1. The use of the PE_EN pin is described in Table 6. No specific cable length is suggested for use with either pre-emphasis setting, because cable performance varies widely among manufacturers.

Table 6. Pre-Emphasis Enable Setting

PE_EN	Boost
0	0 dB
1	6 dB

In a typical application, the output of the ADV3003 is connected to the input of an HDMI/DVI receiver, which provides a second set of matched terminations in accordance with the HDMI 1.3 specification. If neither receiver nor receiver termination is connected to the output of the ADV3003 in the end-application, each ADV3003 output pin should be tied to 3.3 V through a 50 Ω resistor.

APPLICATION NOTES

The ADV3003 is a TMDS buffer featuring equalized inputs and pre-emphasized outputs. It is intended for use as a buffer in HDMI/DVI systems with long input cable runs, and is fully HDMI 1.3 receive-compliant.

PINOUT

The ADV3003 is designed to have an HDMI/DVI receiver pinout at its input and a transmitter pinout at its output. This makes the ADV3003 ideal for use in advanced TV front-panel connectors and AVR-type applications where a designer routes both the inputs and the outputs directly to HDMI/DVI connectors—all of the high speed signals can be routed on one side of the board.

The ADV3003 provides 12 dB of input equalization, so it can compensate for the signal degradation of long input cables. In addition, the ADV3003 can also provide up to 6 dB of pre-emphasis that boosts the output TMDS signals and allows the ADV3003 to precompensate when driving long PCB traces or high loss output cables. The net effect of the input equalization and output pre-emphasis is that the ADV3003 can compensate for signal degradation of both the input and output cables; it acts to reopen a closed input data eye and transmit a full-swing HDMI signal to an end receiver.

CABLE LENGTHS AND EQUALIZATION

The 12 dB equalizer of the ADV3003 is optimized for video data rates of 2.25 Gbps and can equalize more than 20 meters of 24 AWG HDMI cable at the input at 2.25 Gbps, the data rate corresponding to the video format 1080p with 12-bit deep color.

The length of cable that can be used in a typical HDMI/DVI application depends on a large number of factors including

- Cable quality: The quality of the cable in terms of conductor wire gauge and shielding. Thicker conductors have lower signal degradation per unit length.
- Data rate: The data rate being sent over the cable. The signal degradation over HDMI cables increases with data rate.
- Edge rates: The edge rates of the source. Slower input edges result in more significant data eye closure at the end of a cable.
- Receiver sensitivity: The sensitivity of the terminating receiver.

Because of these considerations, specific cable types and lengths are not recommended for use with this equalizer. The ADV3003 equalizer does not degrade signal integrity, even for short input cables.

PRE-EMPHASIS

The pre-emphasis of the ADV3003 acts to boost the initial voltage swing of the output signals. Pre-emphasis provides a distinct advantage in systems where the ADV3003 is driving either high loss cables or long PCB traces, because the added boost helps to ensure that the data eye at the far end of the output cables or PCB traces meets the HDMI receive mask. The use of pre-emphasis in a system is highly application specific.

PCB LAYOUT GUIDELINES

The ADV3003 is a 4-channel TMDS buffer, targeted for use in HDMI and DVI video applications. Although the HDMI/DVI link consists of four differential, high speed channels and four single-ended, low speed auxiliary control signals, the ADV3003 buffers only the high speed signals.

The high speed signals carry the audiovisual (AV) data, which is encoded by a technique called TMDS. For HDMI, the TMDS data is further encrypted in accordance with the high bandwidth digital content protection (HDCP) standard.

The TMDS signals are differential, unidirectional, and high speed (up to 2.25 Gbps). The channels that carry the video data must have a controlled impedance, be terminated at the receiver, and be capable of operating up to at least 2.25 Gbps. It is especially important to note that the PCB traces that carry the TMDS signals should be designed with a controlled differential impedance of 100 Ω. The ADV3003 provides single-ended 50 Ω terminations on chip for both its inputs and outputs. Transmitter termination is not fully specified by the HDMI standard, but its inclusion in the ADV3003 improves the overall system signal integrity.

TMDS Signals

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. In DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data is also interleaved with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock, which runs at one-tenth the speed of the video data channels.

The four high speed channels of the ADV3003 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock, so any channel can be used for any TMDS signal; the user chooses which signal is routed over which channel. In addition, the TMDS channels are symmetric; therefore, the p and n of a given differential pair are interchangeable, provided the inversion is consistent across all inputs and outputs of the ADV3003.

The ADV3003 buffers the TMDS signals; therefore, the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces is more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the ADV3003, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

Layout for the TMDS Signals

The TMDS differential pairs can either be microstrip traces, routed on the outer layer of a board, or stripline traces, routed on an internal layer of the board. If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stack-up. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100 Ω. The characteristic impedance of a differential pair is a function of several variables including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PC board binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path; therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. In addition, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together to establish the required 100 Ω differential impedance. Enough space should be left between the differential pairs of a given group so that the n of one pair does not couple to the p of another pair. For example, one technique is to make the interpair distance 4× to 10× wider than the intrapair spacing.

Any group of four TMDS channels (input or output) should have closely matched trace lengths to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

The length of the TMDS traces should be minimized to reduce overall signal degradation. Commonly used PC board material such as FR4 is lossy at high frequencies, so long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through intersymbol interference (ISI).

Controlling the Characteristic Impedance of a TMDS Differential Pair

The characteristic impedance of a differential pair depends on a number of variables including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask.

Many combinations can produce the correct characteristic impedance. It is generally required to work with the PC board fabricator to obtain a set of parameters to produce the desired results.

One consideration is how to guarantee a differential pair with a differential impedance of 100 Ω over the entire length of the trace. One technique to accomplish this is to change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a 100 Ω differential impedance. When the traces split apart, for example, to go into a connector, and are no longer so strongly coupled, the width of the traces should be increased to yield a differential impedance of 100 Ω in the new configuration.

Ground Current Return

In some applications, it may be necessary to invert the output pin order of the ADV3003. This requires routing of the TMDS traces on multiple layers of the PCB. When routing differential pairs on multiple layers, it is also necessary to reroute the corresponding reference plane to provide one continuous ground current return path for the differential signals. Standard plated through-hole vias are acceptable for both the TMDS traces and the reference plane. An example of this routing is illustrated in Figure 27. To lower the impedance between the two ground planes, additional through-hole vias should be used to stitch the planes together, as space allows.

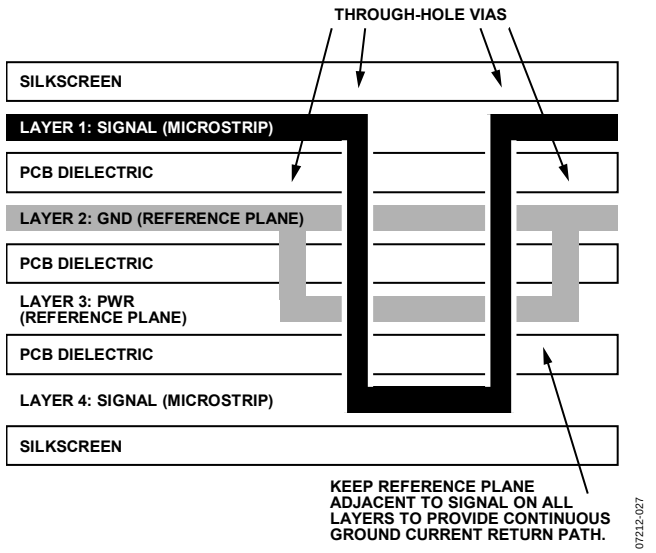


Figure 27. Example Routing of Reference Plane

TMDS Terminations

The ADV3003 provides internal 50 Ω single-ended terminations for all its high speed inputs and outputs. The output termination resistors are always enabled and act to back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the ADV3003 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

In a typical application, the ADV3003 output is connected to an HDMI/DVI receiver or another device with a 50 Ω single-ended input termination. It is recommended that the outputs be terminated with external 50 Ω on-board resistors when the ADV3003 is not connected to another device.

Auxiliary Control Signals

There are four low-speed, single-ended control signals associated with each source or sink in an HDMI/DVI application. These control signals are hot plug detect (HPD), consumer electronics control (CEC), and two display data channel (DDC) lines. The two signals on the DDC bus are serial data and serial clock (SDA and SCL, respectively). The ADV3003, which is a TMDS-only part, does not buffer these low speed signals. If the end application requires it, use other means to buffer these signals.

Power Supplies

The ADV3003 has three separate power supplies referenced to a single ground, AVEE. The supply/ground pairs are as follows: AVCC/AVEE, VTTI/AVEE, and VTTO/AVEE.

The AVCC/AVEE supply (3.3 V) powers the core of the ADV3003. The VTTI/AVEE supply (3.3 V) powers the input termination (see Figure 25). Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination (see Figure 26).

In a typical application, all pins labeled AVEE, including the ePAD, should be connected directly to ground. All pins labeled AVCC, VTTI, or VTTO should be connected to 3.3 V. The supplies can also be powered individually, but care must be taken to ensure that each stage of the ADV3003 is powered correctly.

Power Supply Bypassing

The ADV3003 requires minimal supply bypassing. When powering the supplies individually, place a 0.01 µF capacitor between each 3.3 V supply pin (AVCC, VTTI, and VTTO) and ground to filter out supply noise. Generally, bypass capacitors should be placed near the power pins and should connect directly to the relevant supplies (without long intervening traces). For example, to improve the parasitic inductance of the power supply decoupling capacitors, minimize the trace length between capacitor landing pads and the vias as shown in Figure 28.

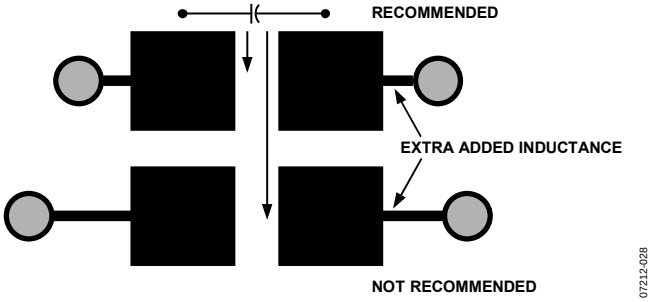
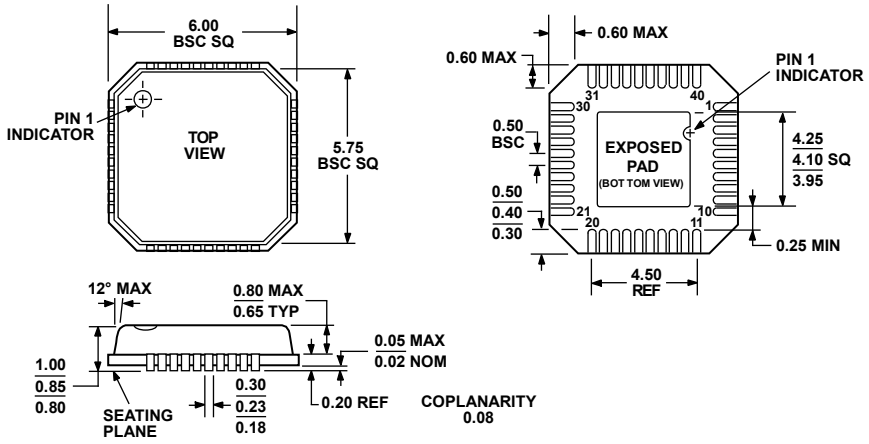


Figure 28. Recommended Pad Outline for Bypass Capacitors

In applications where the ADV3003 is powered by a single 3.3 V supply, it is recommended to use two reference supply planes and bypass the 3.3 V reference plane to the ground reference plane with one 220 pF, one 1000 pF, two 0.01 µF, and one 4.7 µF capacitors. The capacitors should via down directly to the supply planes and be placed within a few centimeters of the ADV3003.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

*THE ADV3003 HAS A CONDUCTIVE HEAT SLUG (ePAD) TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL HDMI/DVI TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO AVEE. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO AN AVEE POWER PLANE REDUCES THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

012808-A

Figure 29. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADV3003ACPZ[1]	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1	490
ADV3003ACPZ-R7[1]	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Reel 7	CP-40-1	1500
ADV3003-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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