

Instruction Set

Data Transfer Operations

	bytes	OSC periods
MOV A,Rn	1	1
MOV A,@Ri	1	2
MOV A,direct	2	2
MOV A,#data	2	2
MOV Rn,A	1	1
MOV Rn,direct	2	2
MOV Rn,#data	2	2
MOV direct,A	2	2
MOV direct,Rn	2	2
MOV direct,@Ri	2	2
MOV direct,direct	3	3
MOV direct,#data	3	3
MOV @Ri,A	1	2
MOV @Ri,direct	2	2
MOV @Ri,#data	2	2
MOV DPTR,#data16	3	3
MOVC A,@A+DPTR	1	4
MOVC A,@A+PC	1	4
MOVV A,@Ri	1	4
MOVV A,@DPTR	1	4
MOVV @Ri,A	1	4
MOVV @DPTR,A	1	4
PUSH direct	2	2
POP direct	2	2
XCH A,Rn	1	1
XCH A,@Ri	1	2
XCH A,direct	2	2
XCHD A,@Ri	1	2

Arithmetic Operations

	bytes	OSC periods
ADD A,Rn	1	1
ADD A,@Ri	1	2
ADD A,direct	2	2
ADD A,#data	2	2
ADDC A,Rn	1	1
ADDC A,@Ri	1	2
ADDC A,direct	2	2
ADDC A,#data	2	2
SUBB A,Rn	1	1
SUBB A,@Ri	1	2
SUBB A,direct	2	2
SUBB A,#data	2	2
INC A	1	1
INC Rn	1	1
INC @Ri	1	2
INC direct	2	2
INC DPTR	1	3
DEC A	1	1
DEC Rn	1	1
DEC @Ri	1	2
DEC direct	2	2
MUL AB	1	9
DIV AB	1	9
DA A	1	2

Logical Operations

	bytes	OSC periods
ANL A,Rn	1	1
ANL A,@Ri	1	2
ANL A,direct	2	2
ANL A,#data	2	2
ANL direct,A	2	2
ANL direct,#data	3	3
ORL A,Rn	1	1
ORL A,@Ri	1	2
ORL A,direct	2	2
ORL A,#data	2	2
ORL direct,A	2	2
ORL direct,#data	3	3
XRL A,Rn	1	1
XRL A,@Ri	1	2
XRL A,direct	2	2
XRL A,#data	2	2
XRL direct,A	2	2
XRL direct,#data	3	3
CLR A	1	1
CPL A	1	1
RL A	1	1
RLC A	1	1
RR A	1	1
RRC A	1	1
SWAP A	1	1

Boolean Variable Manipulation

	bytes	OSC periods
CLR C	1	1
CLR bit	2	2
SETB C	1	1
SETB bit	2	2
CPL C	1	1
CPL bit	2	2
ANL C,bit	2	2
ANL C,bit AND bit with C	2	2
ORL C,bit	2	2
ORL C,bit OR bit with C	2	2
ORL C,bit OR (NOTbit) with C	2	2
MOV bit,C	2	2
MOV bit,C	2	2

Program Branching

	bytes	OSC periods
ACALL addr11	2	3
LCALL addr16	3	4
RET	1	4
RETI	1	4
AJMP addr11	2	3
LJMP addr16	3	4
SJMP rel	2	3
JMP @A+DPTR	1	3
JC rel	2	3
JNC rel	2	3
JB bit,rel	3	4
JNB bit,rel	3	4
JBC bit,rel	3	4
JZ rel	2	3
JNZ rel	2	3
CJNE A,direct,rel	3	4
CJNE A,#data,rel	3	4
CJNE Rn,#data,rel	3	4
CJNE @Ri,#data,rel	3	4
DJNZ Rn,rel	2	3
DJNZ direct,rel	3	4
NOP	1	1

Instructions That Affect Flags

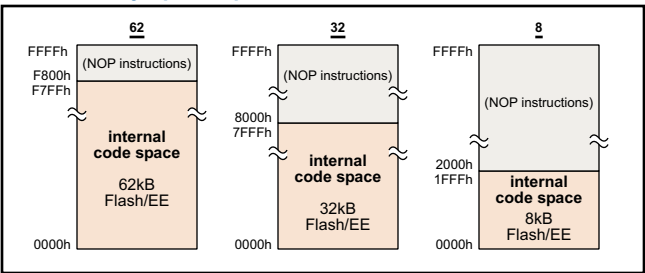
ADD A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	DA A C = C or (x>100) RRC A C = ACC.7 RLC A C = ACC.0
ADDC A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	SETB C C = 1 CLR C C = 0
SUBB A,x	C = borrow into bit 7 AC = borrow into bit 3 OV = borrow into bit 6, but not 7	ANL C,bit C = C and bit ANL C,bit C = C and NOTbit ORL C,bit C = C or bit ORL C,bit C = C or NOTbit
MUL AB	C = 0 OV = (result>255)	MOV C,bit C = bit CJNE x,y,rel C = (x<y)
DIV AB	C = 0 OV = divide by zero	

Pin Functions

Pin	Function
2	P1.1 / AIN2
3	P1.2 / AIN3 / REFIN2+
4	P1.3 / AIN4 / REFIN2-
5	AV _{DD}
- 5	AGND
6	AGND
7	REFIN-
8	REFIN+
9	P1.4 / AIN5
10	P1.5 / AIN6
11	P1.6 / AIN7 / IEXC1
12	P1.7 / AIN8 / IEXC2
13	AINCOM / DAC
14	DAC

Pin	Function
- 15	AIN9 (CSP package only)
- 16	AIN10 (CSP package only)
15	RESET
16	P3.0 / RxD
17	P3.1 / TxD
18	P3.2 / INT0
19	P3.3 / INT1
20	DV _{DD}
21	DGND
22	P3.4 / T0
23	P3.5 / T1
24	P3.6 / WR
25	P3.7 / RD
26	SCLK (I ² C)

Code Memory Space Options



Interrupt Vector Addresses

Interrupt Bit	Interrupt Name	Vector Address	Relative Priority
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
RDY0/RDY1	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I ² C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

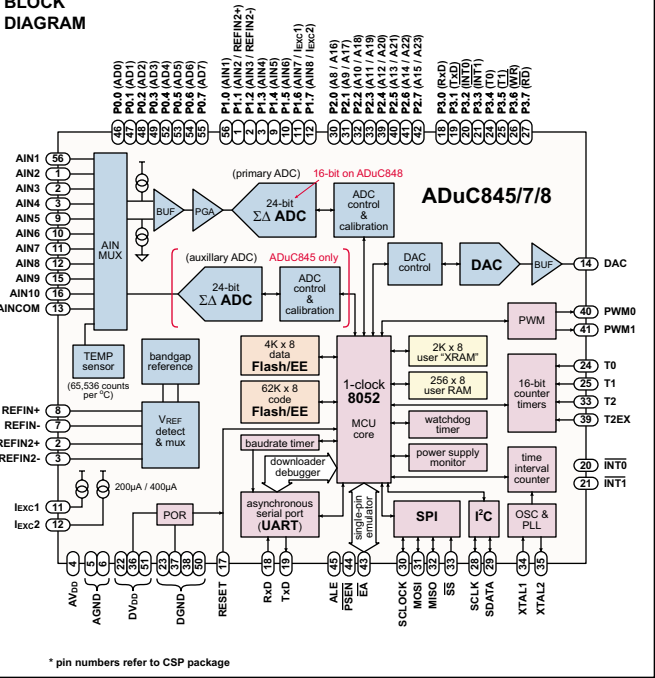
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ADuC845/ADuC847/ADuC848 MicroConverter® Quick Reference Guide

FUNCTIONAL BLOCK DIAGRAM



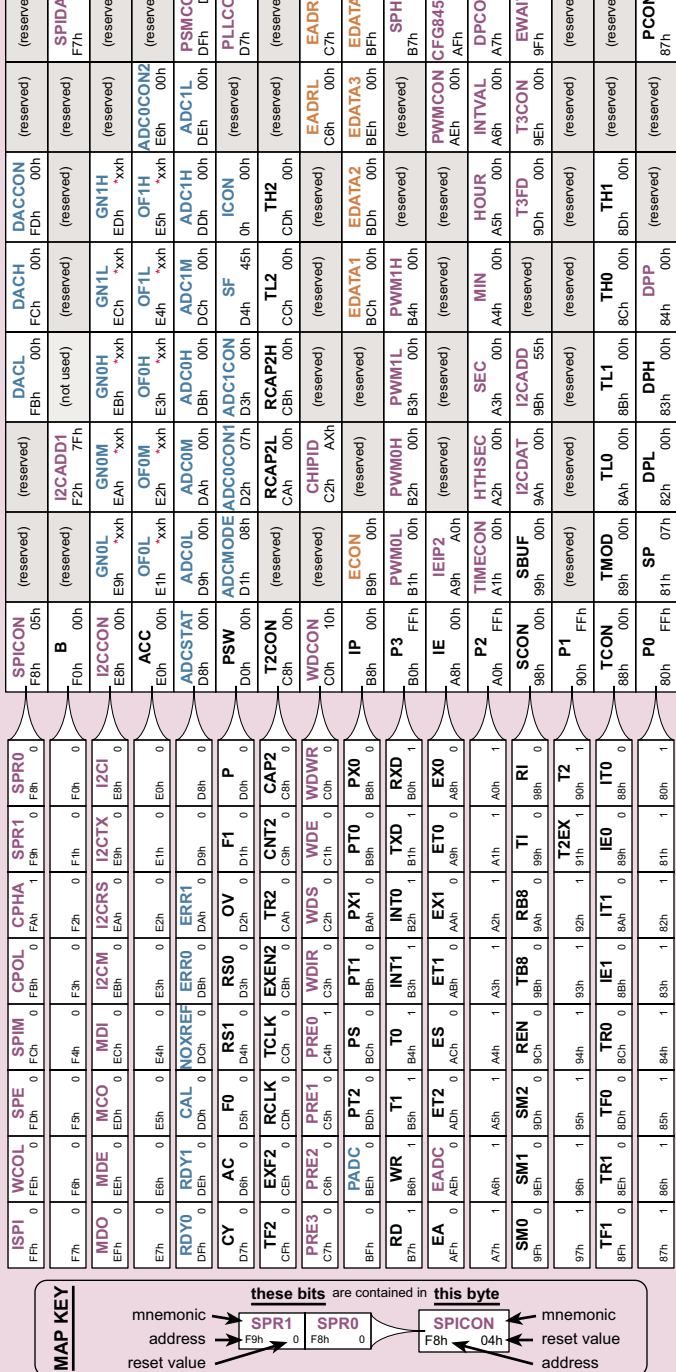
A Precision Analog Flash MCU

The ADuC845/ADuC847/ADuC848 is:
ADC: 24-bit* primary ADC, differential w/ programmable gain 24-bit auxiliary ADC, single-ended w/ fixed gain (ADuC845 only) 10-channel input mux (*ADC is 16bit on ADuC848)
DAC: 12-bit, 15µs, voltage output <1LSB DNL
Flash/EEPROM: up to 62kB Flash/EE program memory 4kB Flash/EE data memory
Microcontroller: "single-cycle" 8052, up to 12.6MIPS 32 I/O lines, programmable PLL clock (98.3kHz to 12.6MHz from 32kHz crystal)
Embedded Tools Support: on-chip download/debug & single-pin emulation functions
Other on-chip features: temperature sensor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8-/16-bit PWM, power-on-reset



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decimal address	HEX address		Lower RAM									
127	7Fh	General Purpose Area	MSB address	(bit addresses)								LSB address
...	...											
48	30h											
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h		
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h		
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h		
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h		
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h		
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h		
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h		
40	28h		47h	46h	45h	44h	43h	42h	41h	40h		
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h		
38	26h		37h	36h	35h	34h	33h	32h	31h	30h		
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h		
36	24h		27h	26h	25h	24h	23h	22g	21h	20h		
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h		
34	22h		17h	16h	15h	14h	13h	12h	11g	10h		
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h		
32	20h		07h	06h	05h	04h	03h	02h	01h	00h		



MAP KEY		these bits are contained in this byte															
mnemonic	address	reset value	SPR1		SPR0		SPICON										mnemonic
			F9h		F8h		F8h										
ISPI	WCOL	SPE	SPIM	CPOL	CPHA	SPR1	SPR0										
		F9h	0	FCh	0	F9h	1	F9h	0	F9h	0	F9h	0	F8h	0	05h	SPICON
		F7h	0	F8h	0	F5h	0	F4h	0	F3h	0	F2h	0	F1h	0	F0h	00h
		F7h	0	F8h	0	F5h	0	F4h	0	F3h	0	F2h	0	F1h	0	F0h	00h
MDO	MDE	MCO	MDI	I2CM	I2CRS	I2CTX	I2CI										
		EFh	0	EEh	0	EDh	0	ECh	0	EBh	0	EAh	0	E9h	0	E8h	00h
		E7h	0	E6h	0	E5h	0	E4h	0	E3h	0	E2h	0	E1h	0	E0h	00h
		E7h	0	E6h	0	E5h	0	E4h	0	E3h	0	E2h	0	E1h	0	E0h	00h
RDY0	RDY1	CAL	NOXREF	ERR0	ERR1												
		DFh	0	DEh	0	DCb	0	DBh	0	DAh	0	D9h	0	D8h	0	D7h	00h
CY	AC	F0	RS1	RS0	OV	F1	P										
		D7h	0	D6h	0	D5h	0	D4h	0	D3h	0	D2h	0	D1h	0	D0h	00h
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	GN2	CAP2										
		CFh	0	CEh	0	CDh	0	CCb	0	CBh	0	CAh	0	C9h	0	C8h	00h
PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR										
		C7h	0	C6h	0	C5h	0	C4h	1	C3h	0	C2h	0	C1h	0	C0h	00h
	PAUC	P2	PS	PT1	PT0	EX0	PX0										
		BFh	0	BEh	0	BDh	0	BCb	0	BBh	0	BAh	0	B9h	0	B8h	00h
RD	WR	T1	T0	INT1	INT0	TXD</											

ADCMODE	ADC Mode register	T3CON	Timer 3 Control register
ADCON0	60kHz reset filter enable (0=disable)	T3CON.7	Timer 3 baud rate enable (0=Disable)
ADCONMODE0	primary ADC enable bit (0=disable)	T3CON.2	binary divide factor (DIV)
ADCONMODE1	auxiliary ADC enable bit (0=disable)	T3CON.1	12-bit logarithmic (16 baudrate) / log2
ADCONMODE3	chop mode disable bit (1=disable)	T3CON.0	(rounded down)
ADCONMODE2	zero cal mode (0=normal, continuous/conc)	T3FD	Timer 3 Fractional Divider register
ADCONMODE0	adc calib. fs-cal, sys-zero-cal, sys-fs-cal	T3FD = (2^{T3CON.7} / baudrate) × 2^(T3CON.1) - 64	
ADCSSTA	ADC Status register	CHIPID	Chip ID Register (AX hex = AD-B485/7B)
ADCSSTA.0	ADCON ready	CFG845/CFG847/CFG848	Config. Register
RDY1	ADC1 ready indicator flag	CFG84.7	extended stack-pointer enable (0=Disable)
CAL	calibration start control bit (set to begin cal)	CFG84x.0	internal XRAM select (0=external XRAM)
ADCSSTA.1	external ADIF error flag (only valid if ADC active)	WDCON	Watchdog Timer control register
ADCSSTA.2	primary ADC error flag (indicates result is clamped)	WDTCON.7	Watchdog timer prescaler bit
ADCSSTA.3	auxiliary ADC error flag (indicates result is clamped)	PRE2	0-7=15, 8-31: 2.625, 125,250,500, 1000,2000ms
ADCSSTA.4	0=normal, 1=chop, 2=continuous/conc	WDTCON.6	8-0ms (immediate reset)
ADCSSTA.5	0=normal, 1=chop, 2=continuous/conc	WDR1	watchdog interrupt response bit
ADCSSTA.6	0=normal, 1=chop, 2=continuous/conc	WDR2	watchdog timer timeout (enable watchdog timeout)
ADCSSTA.7	0=normal, 1=chop, 2=continuous/conc	WDE	watchdog enable control (0=disabled)
ADCSSTA.8	0=normal, 1=chop, 2=continuous/conc	WDEEN	watchdog write enable bit (set to enable write)
ADCSSTA.9	0=normal, 1=chop, 2=continuous/conc	PSMCON	Power-Supply Monitor control register
ADCSSTA.10	0=normal, 1=chop, 2=continuous/conc	PSMCON.7	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.11	0=normal, 1=chop, 2=continuous/conc	PSMCON.6	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.12	0=normal, 1=chop, 2=continuous/conc	PSMCON.5	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.13	0=normal, 1=chop, 2=continuous/conc	PSMCON.4	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.14	0=normal, 1=chop, 2=continuous/conc	PSMCON.3	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.15	0=normal, 1=chop, 2=continuous/conc	PSMCON.2	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.16	0=normal, 1=chop, 2=continuous/conc	PSMCON.1	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.17	0=normal, 1=chop, 2=continuous/conc	PSMCON.0	AVDD status bit (1=above / 0=below trip point)
ADCSSTA.18	0=normal, 1=chop, 2=continuous/conc	SP	Stack Pointer
ADCSSTA.19	0=normal, 1=chop, 2=continuous/conc	SPH	Stack Pointer High byte
ADCSSTA.20	0=normal, 1=chop, 2=continuous/conc	IEA	Interrupt Enable register #1
ADCSSTA.21	0=normal, 1=chop, 2=continuous/conc	IEA.0	enable interrupts (0=all interrupts disabled)
ADCSSTA.22	0=normal, 1=chop, 2=continuous/conc	ET2	enable TF2/EXF2 (Timer2 overflow interrupt)
ADCSSTA.23	0=normal, 1=chop, 2=continuous/conc	ET1	enable TF1 (Timer1 overflow interrupt)
ADCSSTA.24	0=normal, 1=chop, 2=continuous/conc	EX0	enable IE0 (external interrupt 0)
ADCSSTA.25	0=normal, 1=chop, 2=continuous/conc	EX1	enable IE1 (external interrupt 1)
ADCSSTA.26	0=normal, 1=chop, 2=continuous/conc	EX2	enable IE2 (external interrupt 2)
ADCSSTA.27	0=normal, 1=chop, 2=continuous/conc	EX3	enable IE3 (external interrupt 3)
ADCSSTA.28	0=normal, 1=chop, 2=continuous/conc	EX4	enable IE4 (external interrupt 4)
ADCSSTA.29	0=normal, 1=chop, 2=continuous/conc	EX5	enable IE5 (external interrupt 5)
ADCSSTA.30	0=normal, 1=chop, 2=continuous/conc	EX6	enable IE6 (external interrupt 6)
ADCSSTA.31	0=normal, 1=chop, 2=continuous/conc	EX7	enable IE7 (external interrupt 7)
ADCSSTA.32	0=normal, 1=chop, 2=continuous/conc	EX8	enable IE8 (external interrupt 8)
ADCSSTA.33	0=normal, 1=chop, 2=continuous/conc	EX9	enable IE9 (external interrupt 9)
ADCSSTA.34	0=normal, 1=chop, 2=continuous/conc	EX10	enable IE10 (external interrupt 10)
ADCSSTA.35	0=normal, 1=chop, 2=continuous/conc	EX11	enable IE11 (external interrupt 11)
ADCSSTA.36	0=normal, 1=chop, 2=continuous/conc	EX12	enable IE12 (external interrupt 12)
ADCSSTA.37	0=normal, 1=chop, 2=continuous/conc	EX13	enable IE13 (external interrupt 13)
ADCSSTA.38	0=normal, 1=chop, 2=continuous/conc	EX14	enable IE14 (external interrupt 14)
ADCSSTA.39	0=normal, 1=chop, 2=continuous/conc	EX15	enable IE15 (external interrupt 15)
ADCSSTA.40	0=normal, 1=chop, 2=continuous/conc	EX16	enable IE16 (external interrupt 16)
ADCSSTA.41	0=normal, 1=chop, 2=continuous/conc	EX17	enable IE17 (external interrupt 17)
ADCSSTA.42	0=normal, 1=chop, 2=continuous/conc	EX18	enable IE18 (external interrupt 18)
ADCSSTA.43	0=normal, 1=chop, 2=continuous/conc	EX19	enable IE19 (external interrupt 19)
ADCSSTA.44	0=normal, 1=chop, 2=continuous/conc	EX20	enable IE20 (external interrupt 20)
ADCSSTA.45	0=normal, 1=chop, 2=continuous/conc	EX21	enable IE21 (external interrupt 21)
ADCSSTA.46	0=normal, 1=chop, 2=continuous/conc	EX22	enable IE22 (external interrupt 22)
ADCSSTA.47	0=normal, 1=chop, 2=continuous/conc	EX23	enable IE23 (external interrupt 23)
ADCSSTA.48	0=normal, 1=chop, 2=continuous/conc	EX24	enable IE24 (external interrupt 24)
ADCSSTA.49	0=normal, 1=chop, 2=continuous/conc	EX25	enable IE25 (external interrupt 25)
ADCSSTA.50	0=normal, 1=chop, 2=continuous/conc		