

INSTRUCTION SET

Arithmetic Operations

Instruction	Operation	Bytes	Clock Periods
ADD A,source	add source to A	1,2	12
ADD A,#data		2	12
ADDC A,source	add with carry	1,2	12
ADDC A,#data		2	12
SUBB A,source	subtract from A with borrow	1,2	12
SUBB A,#data		2	12
INC A	increment	1	12
INC source		1,2	12
INC DPTR*		1	24
DEC A	decrement	1	12
DEC source		1,2	12
MUL AB	multiply A by B	1	48
DIV AB	divide A by B	1	48
DA A	decimal adjust	1	12

Legend

Symbol	Description
Rn	register addressing using R0-R7
direct	8bit internal address (00h-FFh)
@Ri	indirect addressing using R0 or R1
source	any of [Rn, direct, @Ri]
dest	any of [Rn, direct, @Ri]
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address

* INC DPTR increments the 24bit value DPP/DPH/DPL

Logical Operations

Instruction	Operation	Bytes	Clock Periods
ANL A,source	logical AND	1,2	12
ANL A,#data		2	12
ANL direct,A		3	24
ANL direct,#data	logical OR	2	12
ORL A,source		1,2	12
ORL A,#data		2	12
ORL direct,A	logical XOR	2	12
ORL direct,#data		3	24
XRL A,source		1,2	12
XRL A,#data	logical XOR	2	12
XRL direct,A		2	12
XRL direct,#data		3	24
CLR A	clear A to zero	1	12
CPL A	complement A	1	12
RL A	rotate A left	1	12
RLC A	...through C	1	12
RR A	rotate A right	1	12
RRC A	...through C	1	12
SWAP A	swap nibbles	1	12

Data Transfer Operations

Instruction	Operation	Bytes	Clock Periods
MOV A,source	move source to destination	1,2	12
MOV A,#data		2	12
MOV dest,A		1,2	12
MOV dest,source		1,2,3	24
MOV dest,#data		2,3	12,24
MOV DPTR,#data16		3	24
MOVC A,@A+DPTR	move from code memory	1	24
MOVC A,@A+PC		1	24
MOVX A,@Ri	move to/from data memory	1	24
MOVX A,@DPTR		1	24
MOVX @Ri,A		1	24
MOVX @DPTR,A		1	24
PUSH direct	push onto stack	2	24
POP direct	pop from stack	2	24
XCH A,source	exchange bytes	1,2	12
XCHD A,@Ri	exchg low digits	1	12

Program Branching

Instruction	Operation	Bytes	Clock Periods
ACALL addr11	call subroutine	2	24
LCALL addr16		3	24
RET	return from sub.	1	24
RETI	return from int.	1	24
AJMP addr11	jump	2	24
LJMP addr16		3	24
SJMP rel		2	24
JMP @A+DPTR	jump if A = 0	1	24
JZ rel		2	24
JNZ rel		2	24
CJNE A,direct,rel	compare and jump if not equal	3	24
CJNE A,#data,rel		3	24
CJNE Rn,#data,rel		3	24
CJNE @Ri,#data,rel	decrement and jump if not zero	3	24
DJNZ Rn,rel		2	24
DJNZ direct,rel		3	24
NOP	no operation	1	12

Boolean Variable Manipulation

Instruction	Operation	Bytes	Clock Periods
CLR C	clear bit to zero	1	12
CLR bit		2	12
SETB C	set bit to one	1	12
SETB bit		2	12
CPL C	complement bit	1	12
CPL bit		2	12
ANL C,bit	AND bit with C	2	24
ANL C,#data	...NOTbit with C	2	24
ORL C,bit	OR bit with C	2	24
ORL C,#data	...NOTbit with C	2	24
MOV C,bit	move bit to bit	2	12
MOV bit,C		2	24
JC rel	jump if C set	2	24
JNC rel	jmp if C not set	2	24
JB bit,rel	jump if bit set	3	24
JNB bit,rel	jmp if bit not set	3	24
JBC bit,rel	jmp&clear if set	3	24

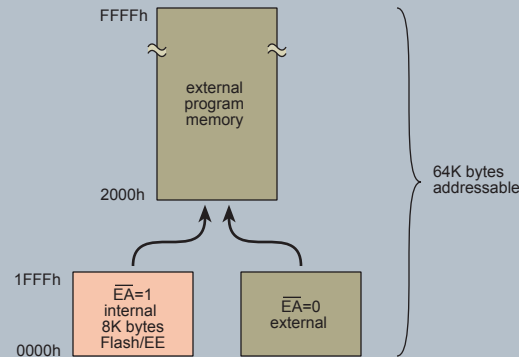
ASSEMBLER DIRECTIVES

EQU	define symbol	DW	store word values in program memory
DATA	define internal memory symbol	ORG	set segment location counter
IDATA	define indirect addressing symbol	END	end of assembly source file
XDATA	define external memory symbol	CSEG	select program memory space
BIT	define internal bit memory symbol	XSEG	select external data memory space
CODE	define program memory symbol	DSEG	select internal data memory space
DS	reserve bytes of data memory	ISEG	select indirectly addressed internal data memory space
DBIT	reserve bits of bit memory	BSEG	select bit addressable memory space
DB	store byte values in program memory		

PIN FUNCTIONS

Pin	Function
1	56 P1.0 / T2
2	1 P1.1 / T2EX
3	2 P1.2 / IEXC1 / DAC
4	3 P1.3 / IEXC2 / AIN5
5	4,5 AV _{DD}
6	6,7,8 AGND
7	9 REFIN-
8	10 REFIN+
9	11 P1.4 / AIN1
10	12 P1.5 / AIN2
11	13 P1.6 / AIN3
12	14 P1.7 / AIN4 / DAC
13	15 SS
14	16 MISO
15	17 RESET
16	18 P3.0 / RxD
17	19 P3.1 / TxD
18	20 P3.2 / INT0
19	21 P3.3 / INT1
20	22 DV _{DD}
21	23 DGND
22	24 P3.4 / T0
23	25 P3.5 / T1
24	26 P3.6 / WR
25	27 P3.7 / RD
26	28 SCLOCK / D0
27	29 MOSI / D1
28	30 P2.0 / A8 / A16
29	31 P2.1 / A9 / A17
30	32 P2.2 / A10 / A18
31	33 P2.3 / A11 / A19
32	34 XTAL1 (in)
33	35 XTAL2 (out)
34	36 DV _{DD}
35	37,38 DGND
36	39 P2.4 / A12 / A20
37	40 P2.5 / A13 / A21
38	41 P2.6 / A14 / A22
39	42 P2.7 / A15 / A23
40	43 EA
41	44 PSEN
42	45 ALE
43	46 P0.0 / AD0
44	47 P0.1 / AD1
45	48 P0.2 / AD2
46	49 P0.3 / AD3
47	50 DGND
48	51 DV _{DD}
49	52 P0.4 / AD4
50	53 P0.5 / AD5
51	54 P0.6 / AD6
52	55 P0.7 / AD7

PROGRAM MEMORY SPACE (read only)



INTERRUPT VECTOR ADDRESSES

Interrupt Bit	Interrupt Name	Vector Address	Priority within Level
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
RDY0/RDY1	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI	SPI Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

MicroConverter® Quick Reference Guide

a "Data Acquisition System on a Chip"

the ADuC824 is: ADC: 24bit $\Sigma\Delta$ with programmable gain, plus 16bit $\Sigma\Delta$ auxiliary ADC

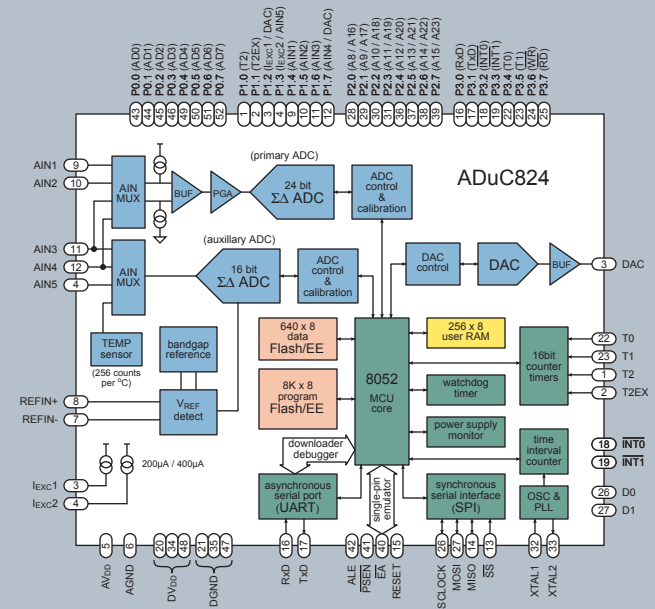
DAC: 12bit, 15 μ s, voltage output, rail-to-rail <1LSB DNL

EEPROM: 8K bytes Flash/EE program memory
640 bytes Flash/EE data memory

microcontroller: industry standard 8052
32 I/O lines, programmable PLL clock (98KHz to 12MHz from 32KHz crystal)

other on-chip features: calibrated temperature sensor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter

FUNCTIONAL BLOCK DIAGRAM



PRINTED IN U.S.A.

decimal address		HEX address	LOWER RAM									
127	7Fh	General Purpose Area	MSB address	(bit addresses)								LSB address
...	...											
48	30h											
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h		
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h		
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h		
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h		
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h		
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h		
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h		
40	28h		47h	46h	45h	44h	43h	42h	41h	40h		
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h		
38	26h		37h	36h	35h	34h	33h	32h	31h	30h		
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h		
36	24h		27h	26h	25h	24h	23h	22g	21h	20h		
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h		
34	22h		17h	16h	15h	14h	13h	12h	11g	10h		
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h		
32	20h		07h	06h	05h	04h	03h	02h	01h	00h		

(bit addresses)

127	7Fh	General Purpose Area	MSB address	(bit addresses)								LSB address
...	...											
48	30h											
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h		
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h		
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h		
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h		
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h		
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h		
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h		
40	28h		47h	46h	45h	44h	43h	42h	41h	40h		
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h		
38	26h		37h	36h	35h	34h	33h	32h	31h	30h		
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h		
36	24h		27h	26h	25h	24h	23h	22g	21h	20h		
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h		
34	22h		17h	16h	15h	14h	13h	12h	11g	10h		
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h		
32	20h		07h	06h	05h	04h	03h	02h	01h	00h		

The diagram illustrates the memory architecture. On the left, internal memory components are shown: a top section (9Fh to 00h) for 640 bytes of Flash/EE data (160 pages) accessible through SFRs; a middle section (FFh to 00h) for 256 bytes of RAM (128 bytes upper, 128 bytes lower); and a bottom section (00h to 000000h) for 0 bytes. On the right, a large block represents external data memory (16MEG addressable) from FFFFFFFh to 0000000h. An arrow points from the Flash/EE data section to the SFRs section, indicating that SFRs are used to access the Flash/EE data.

FFh	128 bytes upper RAM (indirect addressing only)
00h	128 bytes lower RAM (direct or indirect addressing)

SFR details

SPICON										(reserved)	(reserved)	DAICON	(reserved)	(reserved)
B										(reserved)	(reserved)	(reserved)	SPIDAT	
F0h 00h										(reserved)	(reserved)	F7h 00h	(reserved)	
DCON										(reserved)	(reserved)	(reserved)	(reserved)	
E8h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
GNOL										(reserved)	(reserved)	(reserved)	(reserved)	
E9h ~55h										(reserved)	(reserved)	(reserved)	(reserved)	
ACC										(reserved)	(reserved)	(reserved)	(reserved)	
E0h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
ADDCSTAT										(reserved)	(reserved)	(reserved)	(reserved)	
D8h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
PSW										(reserved)	(reserved)	(reserved)	(reserved)	
D0h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
T2CON										(reserved)	(reserved)	(reserved)	(reserved)	
C8h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
WDCON										(reserved)	(reserved)	(reserved)	(reserved)	
C0h 10h										(reserved)	(reserved)	(reserved)	(reserved)	
IP										(reserved)	(reserved)	(reserved)	(reserved)	
B8h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
P3										(reserved)	(reserved)	(reserved)	(reserved)	
B0h FFh										(reserved)	(reserved)	(reserved)	(reserved)	
IE										(reserved)	(reserved)	(reserved)	(reserved)	
A8h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
P2										(reserved)	(reserved)	(reserved)	(reserved)	
A0h FFh										(reserved)	(reserved)	(reserved)	(reserved)	
SCON										(reserved)	(reserved)	(reserved)	(reserved)	
98h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
P1										(reserved)	(reserved)	(reserved)	(reserved)	
90h FFh										(reserved)	(reserved)	(reserved)	(reserved)	
TCON										(reserved)	(reserved)	(reserved)	(reserved)	
88h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
P0										(reserved)	(reserved)	(reserved)	(reserved)	
80h FFh										(reserved)	(reserved)	(reserved)	(reserved)	
SP										(reserved)	(reserved)	(reserved)	(reserved)	
81h 07h										(reserved)	(reserved)	(reserved)	(reserved)	
DPL										(reserved)	(reserved)	(reserved)	(reserved)	
00h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
DPH										(reserved)	(reserved)	(reserved)	(reserved)	
83h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
DPP										(reserved)	(reserved)	(reserved)	(reserved)	
84h 00h										(reserved)	(reserved)	(reserved)	(reserved)	
PCON										(reserved)	(reserved)	(reserved)	(reserved)	
87h 00h										(reserved)	(reserved)	(reserved)	(reserved)	

MAP KEY

these bits are contained in this byte

The diagram shows three registers: SPR1, SPR0, and SPICON. SPR1 and SPR0 are grouped together, with a callout indicating their bits are contained in the SPICON byte. Arrows indicate the mapping of mnemonics to addresses and reset values.

Register	Mnemonic	Address	Reset Value
SPR1		F9h	0
SPR0		F8h	0
SPICON		F8h	00h

* calibration coefficients are preconfigured at power-up to factory calibrated values

ADCSTAT	ADC Status Register	PSMCON	Power Supply Monitor control register
RDY1	primary ADC ready flag	PSMCON.6	DVno compare bit (=fault)
CAL	auxiliary ADC ready flag	PSMCON.5	AVno compare bit (=fault)
NORREF	no external reference flag	PSMCON.4	PSM interrupt bit
ERR1	primary ADC error flag	PSMCON.3	DVno trip point select bits
	auxiliary ADC error flag	PSMCON.2	{4.63V, 3.08V, 2.93V, 2.63V}
		PSMCON.1	AVno trip point select bits
		PSMCON.0	{4.63V, 3.08V, 2.93V, 2.63V}
ADCMODE	ADC Mode Register		PSM powerdown control (=on / =off)
ADMODE.5	primary ADC enable bit	SP	Stack Pointer
ADMODE.4	auxiliary ADC enable bit	IE	Interrupt Enable register #1
ADMODE.2	mode bits	enable RDYn	enable interrupts (=0=all interrupts disabled)
ADMODE.1	{powerdown, idle, snrgl-conv, conv-conv, self-test, fs-self-test, zero-self-test, fs-syscal}	ET2	enable RT2X/EF2 (Timer2 overflow interrupt)
		ET1	enable RT1 (serial port overflow interrupt)
ADCON0	Primary ADC Control Register	EX1	enable IE1 (external interrupt 1)
ADCON.7	this bit must contain zero (=0=internal ref)	ET0	enable TF0 (Timer0 overflow interrupt)
ADCON.6	external reference select bit (=0=internal ref)	IE1	enable IE0 (external interrupt 0)
ADCON.5	channel selection bits:		
ADCON.4	{AIN1-AIN2, AIN3-AIN4, AIN2-AIN3, AIN2-AIN2}	IEIP2	Interrupt Enable/Priority register #2
ADCON.3	unipolar select bit (=0=bipolar)	IEIP2.6	(not used)
ADCON.2	range select bits:	IEIP2.5	priority of TI1 interrupt (timer interval)
ADCON.1	{±20mV, ±40mV, ±80mV ±160mV, ±320mV, ±640mV, ±1280mV, ±2560V}	IEIP2.5	priority of PSM1 interrupt (power supply monitor)
		IEIP2.4	priority of ISPI1 (serial port interface)
		IEIP2.3	this bit must contain zero
		IEIP2.2	enable TI interrupt (timer interval)
		IEIP2.1	enable PSM interrupt (power supply monitor)
		IEIP2.0	enable ISPI interrupt (serial interface)
SF	Sync Filter Register: $f_{ADC} = 4,096\text{Hz} \cdot (3 - SF)$	IP	Interrupt Priority register
OF0H,OF0M,OF0L	ADC offset coefficient	IP.7	(not used)
OF1H,OF1L	ADC1 offset coefficient	PADC	priority of RDY0/RDY1 (ADC interrupt)
GN0H,GN0M,GN0L	ADC0 gain coefficient	TF2	priority of RT2X/EF2 (Timer2 overflow interrupt)
GN1H,GN1L	ADC1 gain coefficient	RT1	priority of RT1 (serial port overflow interrupt)
ADCON.0	ADCON data	TF1	priority of TF1 (Timer1 overflow interrupt)
ADCOH,ADCOM,ADCOL	ADCO data	PX1	priority of IE1 (external INT1)
ADC1H,ADC1L	ADC1 data	PT0	priority of TF0 (Timer0 overflow interrupt)
ICON	Current Source Control Register	PX0	priority of IE0 (external INT0)
ICON.6	burnout current enable bit	TMOD	Timer Mode register
ICON.5	ADC1 current correction bit (=0=correction off)	TMOD.3/7	gate controller bit (=0=ignore INTx)
ICON.4	ADC0 current correction bit (=0=correction off)	TMOD.2/6	counter/timer select bit (=0=timer)
ICON.3	12 pin select bit (=0pin14 + 1pin13)	TMOD.1/5	timer mode selection bits
ICON.2	11 pin select bit (=0pin13 + 1pin14)	TMOD.0/4	{13bit, 16bitIC, 18bitIC, 20bitIC, 2x8bitT}
ICON.1	2 enable bit (=0=disable)		(upper nibble = Timer1, lower nibble = Timer0)
ICON.0	11 enable bit (=0=disable)		
DACCON	DAC Control Register	TCON	Timer Control register
DACCON.4	DAC pin select bit (=0pin13 + 1pin12)	TR1	Timer1 overflow flag
DACCON.3	ModeSelect (=0=12bit, 1=8bit)	TR0	Timer1 run control (=0=off, 1=run)
DACCON.2	RangeSelect (=0=2.5V, 1=4Vno)	TR0	Timer0 overflow flag
DACCON.1	Clear DAC (=0=0V, 1=normal operation)	TR0	Timer0 run control (=0=off, 1=run)
DACCON.0	Powerdown DAC (=0=off, 1=on)	IE1	external INT1 flag
		IE1	IE1 type (=0=level trig, 1=edge trig)
		IE0	external INT0 flag
		IE0	IE0 type (=0=level trig, 1=edge trig)
DACH,DACL	DAC data registers	TH0,TL0	Timer0 registers
		TH1,TL1	Timer1 registers
PLLCON	PLL Control Register	TH2,TL2	Timer2 Control-register
PLLCON.7	oscillator powerdown control bit (=0=normal)	TF2	overflow flag
PLLCON.6	PLL lock indicator flag (=0=not of lock)	EXF2	external flag
PLLCON.5	this bit must contain zero	RCLK	receive clock enable (=0=Timer1 used for Rx0 clk)
PLLCON.4	EA detect status bit (=0=not detect of EA pin)	TCLK	transmit clock enable (=0=Timer1 used for Tx0 clk)
PLLCON.3	"fast interrupt" control value, "CD" (default=3):	TX2EX	external event flag
PLLCON.2	3-bit clock divider value, "CD" (default=3):	run control	run control (=0=stop, 1=run)
PLLCON.1	1 enable bit (=0=disable)	CR2	timer/counter select (=0=timer, 1=counter)
PLLCON.0	$f_{CORE} = 12,552.912\text{Hz} \cdot 2^{CD}$	capture/reload	capture/reload select (=0=reload, 1=capture)
TIMECON	Time Interval Counter Control Register	TH2,TL2	Timer2 register
TIMECON.6	24hour select bit (=0=255hour)	RCAP2H,RCAP2L	Timer2 Reload/Capture
TIMECON.5	timebase selection bit		
TIMECON.4	{128th sec, seconds, minutes, hours}	P0	Port0 register
TIMECON.3	single time interval control bit (=0=reload&restart)	P1	Port1 register
TIMECON.2	time interval interrupt bit, "TI"	P1.2-1.7	analog/digital pins (1=analog function, 0=digital input)
TIMECON.1	time interval enable bit (=0=disable&reload)	TX2EX	timer/counter 2 capture/reload trigger (or digital I/O)
TIMECON.0	time clock register bit (=0=disable)	P2	Port2 register
INTVAL	TIC Interval Register	P3	Port3 register
HTHSEC	TIC Elapsed 128th Second Register	RD0	external data memory read strobe
SEC	TIC Elapsed Seconds Register	external data memory write strobe	
MIN	TIC Elapsed Minutes Register	T1	timer/counter 1 external input

B	auxiliary math register
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