ADS8881x 18-Bit, 1-MSPS, Serial Interface, microPower, Miniature, True-Differential Input, SAR Analog-to-Digital Converter

1 Features

- Sample Rate: 1 MHz
- No Latency Output
- Unipolar, True-Differential Input Range: $-V_{REF}$ to $+V_{REF}$
- Wide Common-Mode Voltage Range: 0 V to V_{REF} with 90-dB CMRR (min)
- SPI™-Compatible Serial Interface with Daisy-Chain Option
- Excellent AC and DC Performance:
  - ADS8881C:
    INL: ±1 LSB (typ), ±2.0 LSB (max)
    DNL: ±1.0 LSB (max), 18-Bit NMC
    SNR: 100 dB, THD: –115 dB
  - ADS8881I:
    INL: ±1.5 LSB (typ), ±3.0 LSB (max)
    DNL: +1.5 and –1 LSB (max), 18-Bit NMC
    SNR: 100 dB, THD: –115 dB
- Wide Operating Range:
  - AVDD: 2.7 V to 3.6 V
  - DVDD: 2.7 V to 3.6 V (Independent of AVDD)
  - REF: 2.5 V to 5 V (Independent of AVDD)
  - Operating Temperature:
    ADS8881C : 0°C to +70°C
    ADS8881I : –40°C to +85°C
- Low-Power Dissipation:
  - 5.5 mW at 1 MSPS
  - 0.55 mW at 100 kSPS
  - 55 µW at 10 kSPS
- Power-Down Current (AVDD): 50 nA
- Full-Scale Step Settling to 18 Bits: 290 ns
- Packages: MSOP-10 and VSON-10

2 Applications

- Automatic Test Equipment (ATE)
- Instrumentation and Process Controls
- Precision Medical Equipment
- Low-Power, Battery-Operated Instruments

3 Description

The ADS8881 is an 18-bit, 1-MSPS, true-differential input, analog-to-digital converter (ADC). The device operates with a 2.5-V to 5-V external reference, offering a wide selection of signal ranges without additional input signal scaling. The reference voltage setting is independent of, and can exceed, the analog supply voltage (AVDD).

The device offers an SPI-compatible serial interface that also supports daisy-chain operation for cascading multiple devices. An optional busy-indicator bit makes synchronizing with the digital host easy.

The device supports unipolar, true-differential analog input signals with a differential input swing of $-V_{REF}$ to V_{REF}. This true-differential analog input structure allows for a common-mode voltage of any value in the range of 0 V to V_{REF} (when both inputs are within the operating input range of –0.1 V to V_{REF} + 0.1 V).

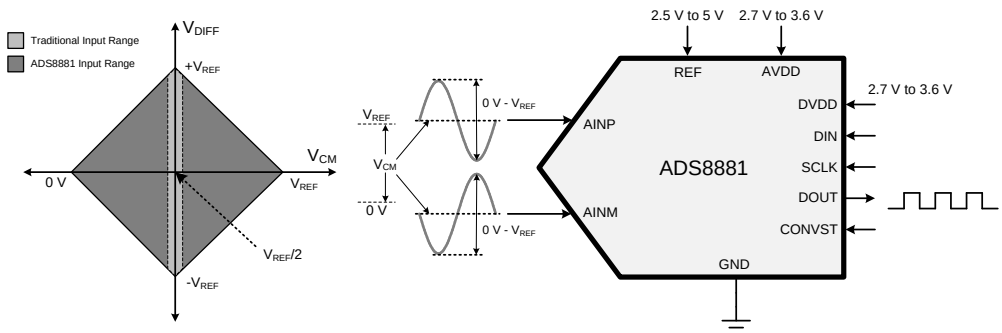
Device operation is optimized for very low-power operation. Power consumption directly scales with speed. This feature makes the ADS8881 excellent for lower-speed applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8881x	VSSOP (10)	3.00 mm × 3.00 mm
	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

True-Differential Input Range



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Companion Products ... 4
6 Device Comparison ... 5
7 Pin Configurations and Functions ... 6
8 Specifications ... 7
8.1 Absolute Maximum Ratings ... 7
8.2 ESD Ratings ... 7
8.3 Recommended Operating Conditions ... 7
8.4 Thermal Information ... 7
8.5 Electrical Characteristics ... 8
8.6 Timing Requirements: 3-Wire Operation ... 10
8.7 Timing Requirements: 4-Wire Operation ... 11
8.8 Timing Requirements: Daisy-Chain ... 12
8.9 Typical Characteristics ... 13
9 Parametric Measurement Information ... 20
9.1 Equivalent Circuits ... 20
10 Detailed Description ... 21
10.1 Overview ... 21
10.2 Functional Block Diagram ... 21
10.3 Feature Description ... 21
10.4 Device Functional Modes ... 24
11 Application and Implementation ... 33
11.1 Application Information ... 33
11.2 Typical Applications ... 36
12 Power-Supply Recommendations ... 45
12.1 Power-Supply Decoupling ... 45
12.2 Power Saving ... 45
13 Layout ... 47
13.1 Layout Guidelines ... 47
13.2 Layout Example ... 47
14 Device and Documentation Support ... 48
14.1 Device Support ... 48
14.2 Documentation Support ... 48
14.3 Receiving Notification of Documentation Updates 48
14.4 Community Resources ... 48
14.5 Trademarks ... 49
14.6 Electrostatic Discharge Caution ... 49
14.7 Glossary ... 49
15 Mechanical, Packaging, and Orderable Information ... 49

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2014) to Revision D **Page**

- Added *Companion Products* and *Device Comparison* sections ... 4
- Changed ESD Ratings table to current standards, added HBM and CDM data ... 7
- Added timing specifications for different operating temperature ranges for the t_{conv}, $t_{d\text{-}CK\text{-}DO}$, and t_{quiet} parameters in the *Timing Requirements: 3-Wire Operation* table ... 10
- Added timing specifications for different operating temperature ranges for the t_{conv} parameter in *Timing Requirements: 4-Wire Operation* table ... 11
- Added timing specifications for different operating temperature ranges for the t_{conv} parameter in *Timing Requirements: Daisy-Chain* table ... 12

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Changes from Revision B (December 2014) to Revision C **Page**

- Changed format to meet latest data sheet standards; added new sections, moved existing sections 1
- Changed ADS8881 to ADS8881C, added ADS8881I 1
- Separated ADS8881C and ADS8881I specifications in *Excellent AC and DC Performance* Features bullet 1
- Changed Device Information table to current standards 1
- Added Recommended Operating Conditions table 7
- Changed LSB footnote to include how to convert LSB to ppm 8
- Changed f_{SCLK} parameter maximum specification from 66.6 MHz to 70 MHz in Timing Requirements: 3-Wire Operation table. 10
- Changed t_{SCLK} parameter minimum specification from 15 ns to 14.3 ns in Timing Requirements: 3-Wire Operation table. 10
- Added more information about validity of data on SCLK edges in all interface modes 25
- Changed diagrams and text for better explanation of the daisy-chain feature in the *Daisy-Chain Mode* section 30
- Changed Equation 2 and Equation 3 34
- Added *Layout Guidelines* section 47

Changes from Revision A (July 2013) to Revision B **Page**

- Changed *Wide Common-Mode Voltage Range* Features bullet 1
- Added note 2 to Family Information table 5
- Changed External Reference Input, *Reference input current* parameter typical specification from 350 to 300 8
- Added External Reference Input, *Reference leakage current* parameter to Electrical Characteristics 8
- Changed Power-Supply Requirements, *Power-supply voltage* parameter digital interface supply range as a function of SCLK in Electrical Characteristics 9
- Added Digital Inputs, *Digital input leakage current* parameter to Electrical Characteristics 9
- Added true-differential input feature details to *Analog Input* section 22
- Deleted shading from Figure 64 35
- Deleted shading from Figure 65 36
- Deleted shading from Figure 67 38
- Deleted shading from Figure 69 40
- Deleted shading from Figure 70 40
- Deleted shading from Figure 72 43
- Added power scaling with throughput feature details to *Power Saving* section 45

Changes from Original (May 2013) to Revision A **Page**

- Changed document status to Production Data; pre-RTM changes made throughout document 1

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5 Companion Products

PART NUMBER	NAME
REF5045	Low Noise, Very Low Drift, Precision Voltage Reference
THS4281	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
REF2925	2.5V 100ppm/Degrees C, 50uA in SOT23-3 Series (Bandgap) Voltage Reference
AFE5808A	Fully Integrated, 8 Channel Ultrasound Analog Front End with Passive CW Mixer
LMK04803	Low Noise Clock Jitter Cleaner With Dual Cascaded PLLs and Integrated 1.9 GHz VCO

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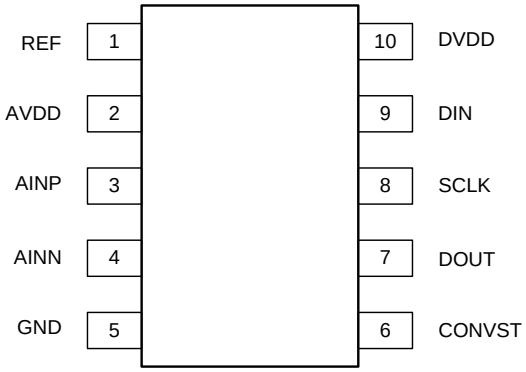
6 Device Comparison

THROUGHPUT	18-BIT, TRUE-DIFFERENTIAL	16-BIT, SINGLE-ENDED	16-BIT, TRUE-DIFFERENTIAL
100 kSPS	ADS8887	ADS8866	ADS8867
250 kSPS	—	ADS8339	—
400 kSPS	ADS8885	ADS8864	ADS8865
500 kSPS	—	ADS8319	ADS8318
680 kSPS	ADS8883	ADS8862	ADS8863
1 MSPS	ADS8881	ADS8860	ADS8861

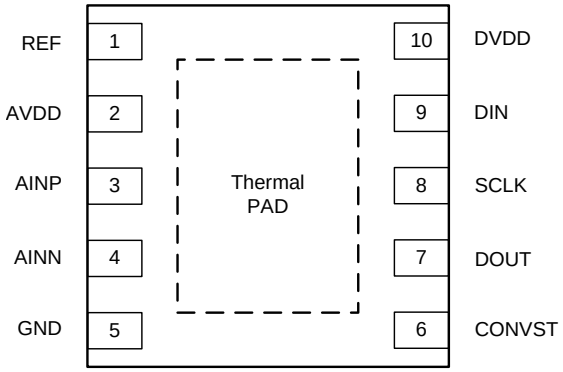
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7 Pin Configurations and Functions

DGS Package
VSSOP-10
Top View, Not to Scale



DRC Package
VSON-10
Top View, Not to Scale



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINN	4	Analog input	Inverting analog signal input
AINP	3	Analog input	Noninverting analog signal input
AVDD	2	Analog	Analog power supply. This pin must be decoupled to GND with a 1-μF capacitor.
CONVST	6	Digital input	Convert input. This pin also functions as the $\overline{CS}$ input in 3-wire interface mode; see the *Description* and *Timing Requirements* sections for more details.
DIN	9	Digital input	Serial data input. The DIN level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode; see the *Description* and *Timing Requirements* sections for more details.
DOUT	7	Digital output	Serial data output
DVDD	10	Power supply	Digital interface power supply. This pin must be decoupled to GND with a 1-μF capacitor.
GND	5	Analog, digital	Device ground. Note that this pin is a common ground pin for both the analog power supply (AVDD) and digital I/O supply (DVDD). The reference return line is also internally connected to this pin.
REF	1	Analog	Positive reference input. This pin must be decoupled with a 10-μF or larger capacitor.
SCLK	8	Digital input	Clock input for serial interface. Data output (on DOUT) are synchronized with this clock.
Thermal pad	—	Thermal pad	Exposed thermal pad **(only for the DRC package option)**. Texas Instruments recommends connecting the thermal pad to the printed circuit board (PCB) ground.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AINP to GND or AINN to GND		–0.3	REF + 0.3	V
AVDD to GND or DVDD to GND		–0.3	4	V
REF to GND		–0.3	5.7	V
Digital input voltage to GND		–0.3	DVDD + 0.3	V
Digital output to GND		–0.3	DVDD + 0.3	V
Operating temperature, T_A	ADS8881C	0	70	°C
	ADS8881I	–40	85	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		3		V
DVDD	Digital power supply		3		V
V_{REF}	Reference voltage		5		V

8.4 Thermal Information

THERMAL METRIC		ADS8881		UNIT
		DGS (VSSOP)	DRC (VSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.9	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	45.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.9	45.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

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8.5 Electrical Characteristics

All minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, V_{CM} = V_{REF} / 2 V, and f_{SAMPLE} = 1 MSPS, over the operating free-air temperature range, unless otherwise noted. Typical specifications are at T_A = 25°C, AVDD = 3 V, and DVDD = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)(2)	AINP – AINN	$-V_{REF}$		V_{REF}	V
	Operating input range(1)(2)	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		V_{REF} + 0.1	
V_{CM}	Input common-mode range		0	V_{REF} / 2	V_{REF}	V
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
EXTERNAL REFERENCE INPUT						
V_{REF}	Input range	ADS8881C	3		5	V
		ADS8881I	2.5		5	
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300		µA
	Reference leakage current			250		nA
C_{REF}	Decoupling capacitor at the REF input		10	22		µF
	Input leakage current	During acquisition for dc input		5		nA
SYSTEM PERFORMANCE						
	Resolution			18		Bits
NMC	No missing codes		18			Bits
DNL	Differential linearity	ADS8881C	–0.99	±0.6	1	LSB(3)
		ADS8881I	–0.99	±0.7	1.5	
INL	Integral linearity(4)	ADS8881C	–2	±1.2	2	LSB(3)
		ADS8881I	–3	±1.5	3	
E_O	Offset error(5)		–4	±1	4	mV
	Offset error drift with temperature			±1.5		µV/°C
E_G	Gain error		–0.01	±0.005	0.01	%FSR
	Gain error drift with temperature			±0.15		ppm/°C
CMRR	Common-mode rejection ratio		90	100		dB
PSRR	Power-supply rejection ratio	At mid-code		80		dB
	Transition noise			0.7		LSB
SAMPLING DYNAMICS						
t_{conv}	Conversion time		500		710	ns
t_{ACQ}	Acquisition time		290			ns
	Maximum throughput rate with or without latency				1000	kHz
	Aperture delay			4		ns
	Aperture jitter, RMS			5		ps
	Step response	Settling to 18-bit accuracy		290		ns
	Overvoltage recovery	Settling to 18-bit accuracy		290		ns

(1) Ideal input span, does not include gain or offset error.
(2) Specified for V_{CM} = V_{REF} / 2; see the *Analog Input* section for the effect of V_{CM} on the full-scale input range.
(3) LSB = least significant bit. 1 LSB at 18-bits is approximately 3.8 ppm.
(4) This parameter is the endpoint INL, not best-fit.
(5) Measured relative to actual measured reference.

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Electrical Characteristics (continued)

All minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, V_{CM} = V_{REF} / 2 V, and f_{SAMPLE} = 1 MSPS, over the operating free-air temperature range, unless otherwise noted.
Typical specifications are at T_A = 25°C, AVDD = 3 V, and DVDD = 3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
SINAD	Signal-to-noise + distortion(6)		At 1 kHz, V_{REF} = 5 V	98	99.9		dB
			At 10 kHz, V_{REF} = 5 V		98.7		
			At 100 kHz, V_{REF} = 5 V		93.3		
SNR	Signal-to-noise ratio(6)		At 1 kHz, V_{REF} = 5 V	98.5	100		dB
			At 10 kHz, V_{REF} = 5 V		99.5		
			At 100 kHz, V_{REF} = 5 V		93.5		
THD	Total harmonic distortion(6)(7)		At 1 kHz, V_{REF} = 5 V		–115		dB
			At 10 kHz, V_{REF} = 5 V		–112		
			At 100 kHz, V_{REF} = 5 V		–102		
SFDR	Spurious-free dynamic range(6)		At 1 kHz, V_{REF} = 5 V		115		dB
			At 10 kHz, V_{REF} = 5 V		112		
			At 100 kHz, V_{REF} = 5 V		102		
BW_{-3dB}	–3-dB small-signal bandwidth				30		MHz
POWER-SUPPLY REQUIREMENTS							
	Power-supply voltage	AVDD	Analog supply	2.7	3	3.6	V
		DVDD	Digital supply range for SCLK > 40 MHz	2.7	3	3.6	
			Digital supply range for SCLK < 40 MHz	1.65	1.8	3.6	
	Supply current	AVDD	1-MHz sample rate, AVDD = 3 V		1.8	2.4	mA
P_{VA}	Power dissipation		1-MHz sample rate, AVDD = 3 V		5.5	7.2	mW
			100-kHz sample rate, AVDD = 3 V		0.55		
			10-kHz sample rate, AVDD = 3 V		55		µW
IA_{PD}	Device power-down current(8)				50		nA
DIGITAL INPUTS: LOGIC FAMILY (CMOS)							
V_{IH}	High-level input voltage		1.65 V < DVDD < 2.3 V	0.8 × DVDD		DVDD + 0.3	V
			2.3 V < DVDD < 3.6 V	0.7 × DVDD		DVDD + 0.3	
V_{IL}	Low-level input voltage		1.65 V < DVDD < 2.3 V	–0.3		0.2 × DVDD	V
			2.3 V < DVDD < 3.6 V	–0.3		0.3 × DVDD	
I_{LK}	Digital input leakage current				±10	±100	nA
DIGITAL OUTPUTS: LOGIC FAMILY (CMOS)							
V_{OH}	High-level output voltage		I_O = 500-µA source, C_{LOAD} = 20 pF	0.8 × DVDD		DVDD	V
V_{OL}	Low-level output voltage		I_O = 500-µA sink, C_{LOAD} = 20 pF	0		0.2 × DVDD	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature		ADS8881C	0		70	°C
			ADS8881I	–40		85	

(6) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(7) Calculated on the first nine harmonics of the input frequency.
(8) The device automatically enters a power-down state at the end of every conversion, and remains in power-down during the acquisition phase.

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8.6 Timing Requirements: 3-Wire Operation

All specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range, unless otherwise noted.

			MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time		290			ns
t_{conv}	Conversion time	T_A in the range –40°C to 85°C	500		710	ns
		T_A in the range 0°C to 70°C	500		700	
t_{conv}	Conversion time		500			ns
$1/f_{sample}$	Time between conversions		1000			ns
t_{wh-CNV}	Pulse duration: CONVST high		10			ns
f_{SCLK}	SCLK frequency				70	MHz
t_{SCLK}	SCLK period		14.3			ns
t_{clkl}	SCLK low time		0.45		0.55	t_{SCLK}
t_{clkh}	SCLK high time		0.45		0.55	t_{SCLK}
$t_{h-CK-DO}$	SCLK falling edge to current data invalid		3			ns
$t_{d-CK-DO}$	SCLK falling edge to next data valid delay	T_A in the range –40°C to 85°C			13.4	ns
		T_A in the range 0°C to 70°C			11.7	
		T_A in the range 25°C to 50°C			10.7	
$t_{d-CNV-DO}$	Enable time: CONVST low to MSB valid				12.3	ns
$t_{d-CNV-DOhz}$	Disable time: CONVST high or last SCLK falling edge to DOUT 3-state ($\overline{CS}$ mode)				13.2	ns
t_{quiet}	Quiet time	T_A in the range –40°C to 85°C	20			ns
		T_A in the range 0°C to 70°C	13			

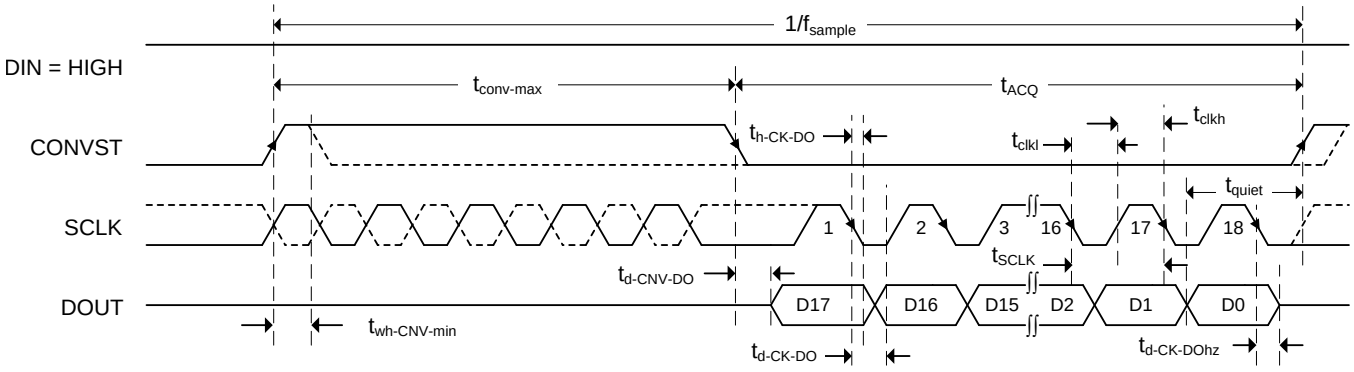


Figure 1. 3-Wire Operation: CONVST Functions as Chip Select

NOTE: Figure 1 shows the timing diagram for the *3-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Timing Requirements: 3-Wire Operation are also applicable for the *3-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

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8.7 Timing Requirements: 4-Wire Operation

All specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range, unless otherwise noted.

			MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time		290			ns
t_{conv}	Conversion time	T_A in the range –40°C to 85°C	500		710	ns
		T_A in the range 0°C to 70°C	500		700	
t_{conv}	Conversion time		500			ns
$1/f_{sample}$	Time between conversions		1000			ns
t_{wh-DI}	Pulse duration: DIN high		10			ns
t_{wl-CNV}	Pulse width: CONVST low		20			ns
$t_{d-DI-DO}$	Delay time: DIN low to MSB valid				12.3	ns
$t_{d-DI-DOhz}$	Delay time: DIN high or last SCLK falling edge to DOUT 3-state				13.2	ns
$t_{su-DI-CNV}$	Setup time: DIN high to CONVST rising edge		7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN high from CONVST rising edge (see Figure 63)		0			ns

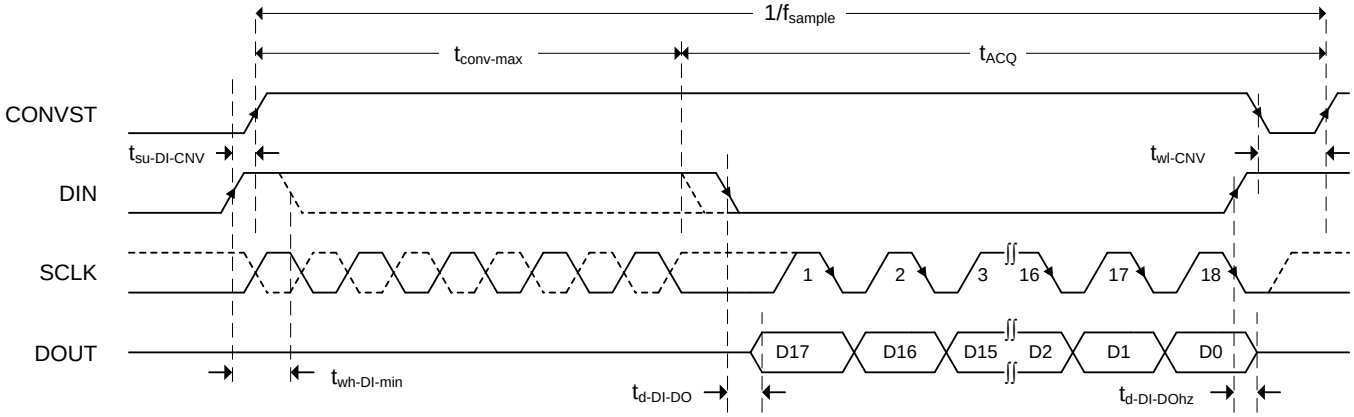


Figure 2. 4-Wire Operation: DIN Functions as Chip Select

NOTE: Figure 2 shows the timing diagram for the *4-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Timing Requirements: 4-Wire Operation are also applicable for the *4-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

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8.8 Timing Requirements: Daisy-Chain

All specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range, unless otherwise noted.

			MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time		290			ns
t_{conv}	Conversion time	T_A in the range -40°C to 85°C	500		710	ns
		T_A in the range 0°C to 70°C	500		700	
t_{conv}	Conversion time		500			ns
$1/f_{sample}$	Time between conversions		1000			ns
$t_{su-CK-CNV}$	Setup time: SCLK valid to CONVST rising edge		5			ns
$t_{h-CK-CNV}$	Hold time: SCLK valid from CONVST rising edge		5			ns
$t_{su-DI-CNV}$	Setup time: DIN low to CONVST rising edge (see Figure 2)		7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN low from CONVST rising edge (see Figure 63)		0			ns
$t_{su-DI-CK}$	Setup time: DIN valid to SCLK falling edge		1.5			ns

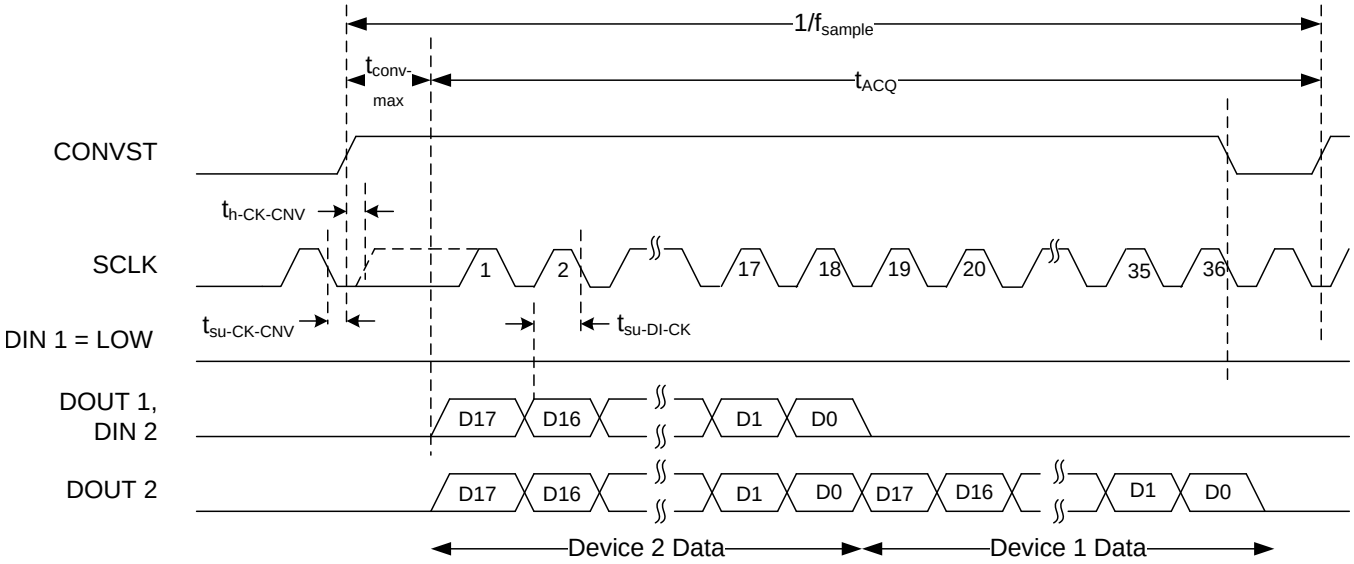


Figure 3. Daisy-Chain Operation: Two Devices

NOTE: Figure 3 shows the timing diagram for the *Daisy-Chain Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Timing Requirements: Daisy-Chain are also applicable for the *Daisy-Chain Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

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8.9 Typical Characteristics

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

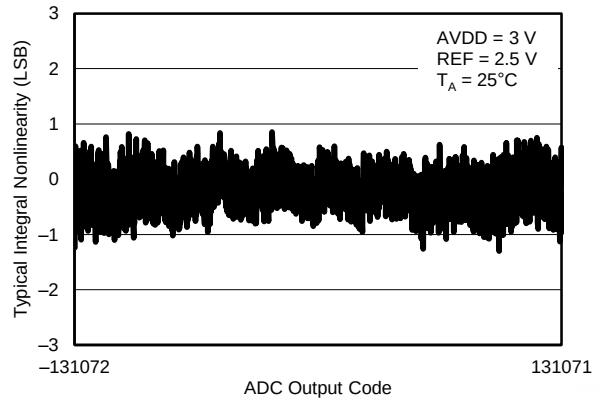


Figure 4. Typical INL (V_{REF} = 2.5 V)

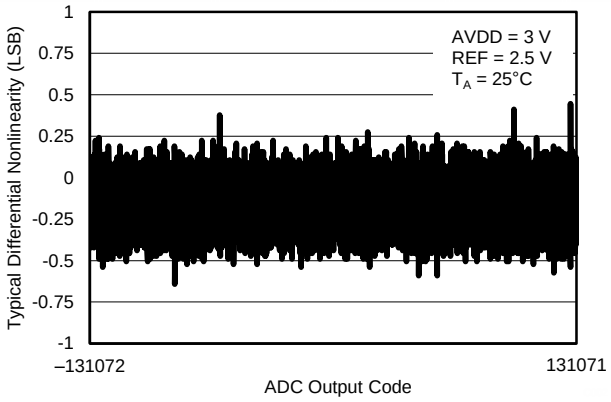


Figure 5. Typical DNL (V_{REF} = 2.5 V)

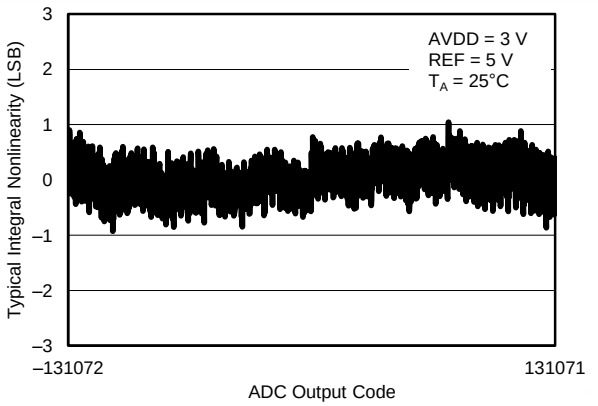


Figure 6. Typical INL (V_{REF} = 5 V)

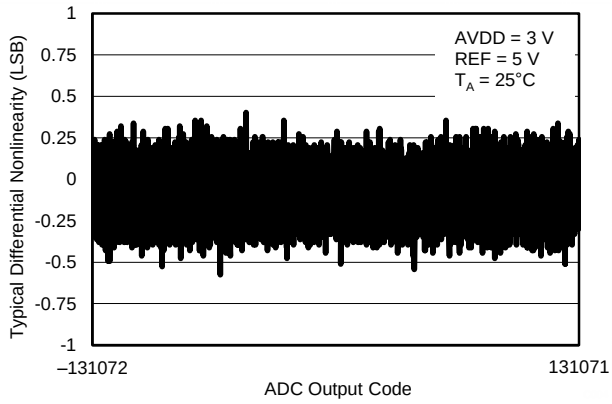


Figure 7. Typical DNL (V_{REF} = 5 V)

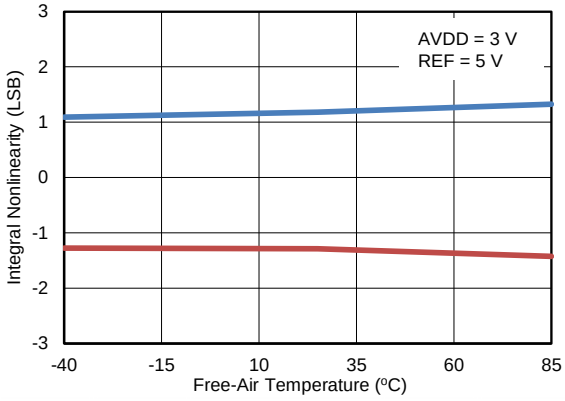


Figure 8. INL vs Temperature

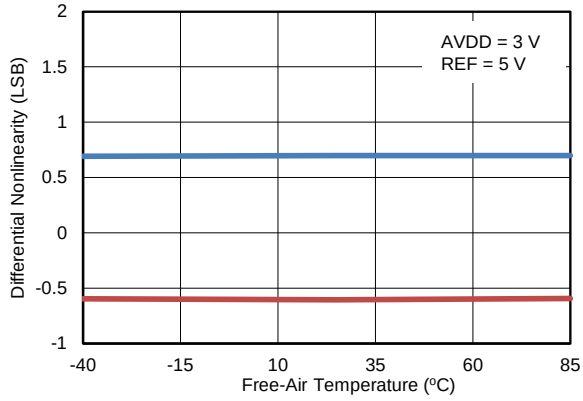


Figure 9. DNL vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

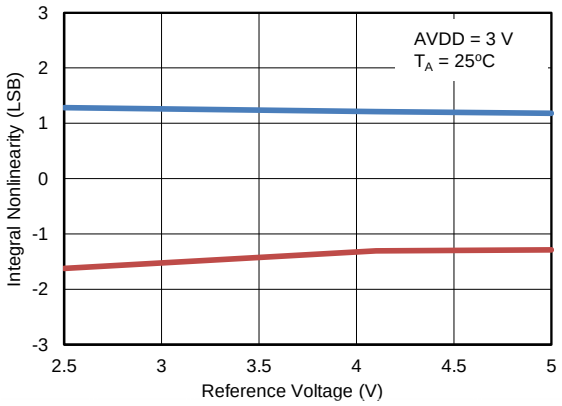


Figure 10. INL vs Reference Voltage

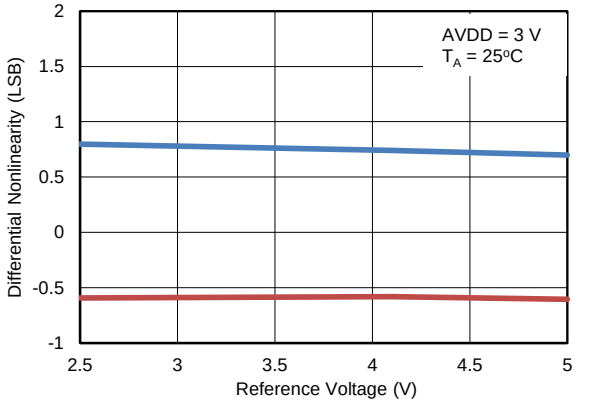


Figure 11. DNL vs Reference Voltage

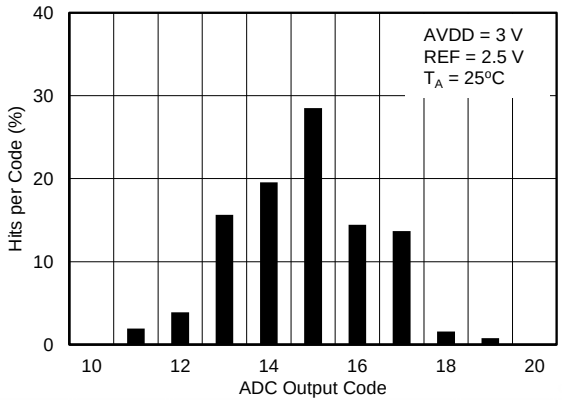


Figure 12. DC Input Histogram (V_{REF} = 2.5 V)

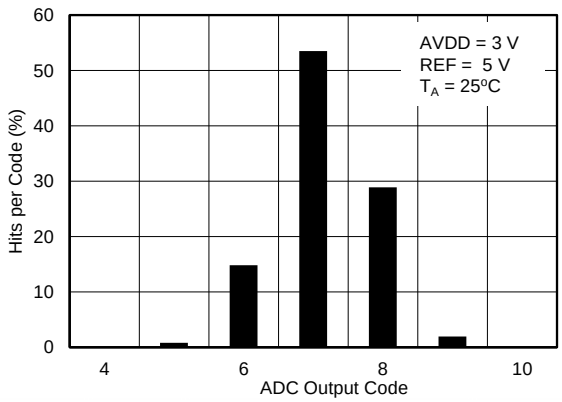


Figure 13. DC Input Histogram (V_{REF} = 5 V)

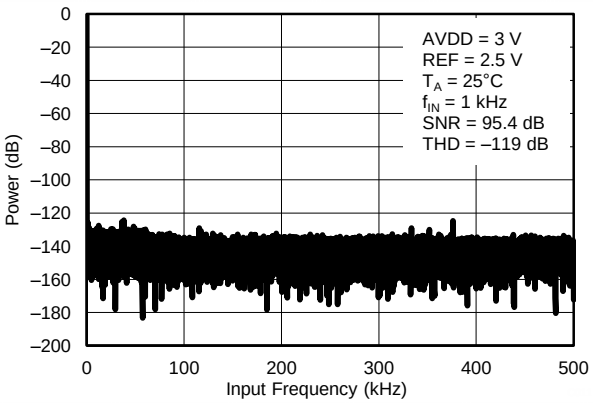


Figure 14. Typical FFT (V_{REF} = 2.5 V)

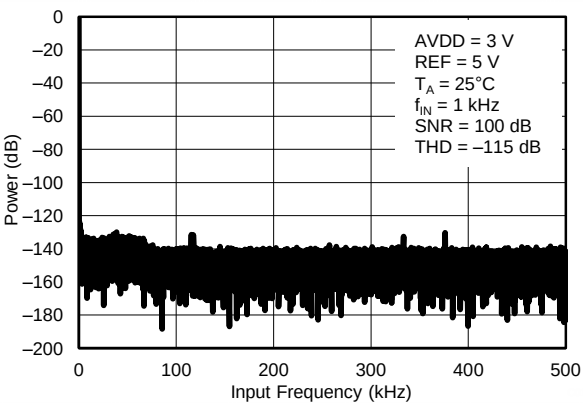


Figure 15. Typical FFT (V_{REF} = 5 V)

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

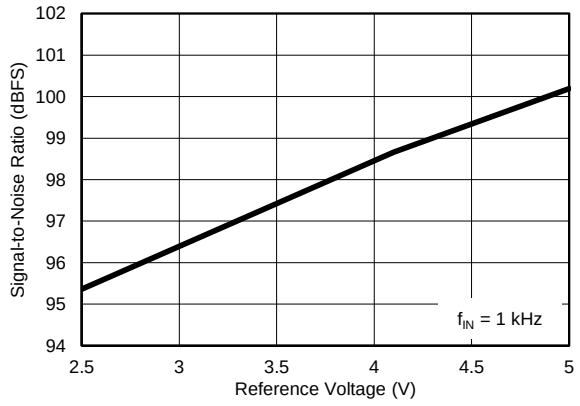


Figure 16. SNR vs Reference Voltage

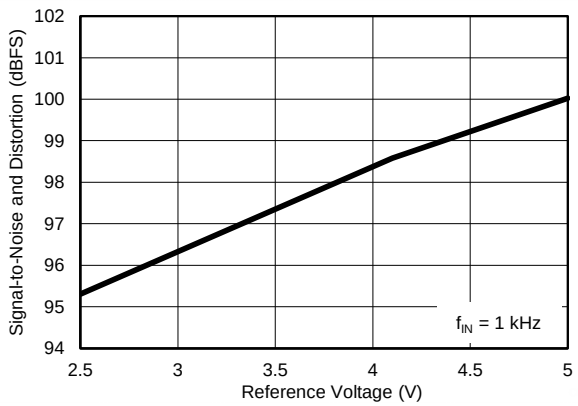


Figure 17. SINAD vs Reference Voltage

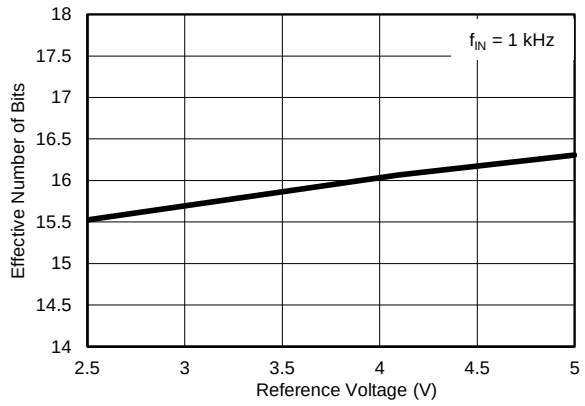


Figure 18. ENOB vs Reference Voltage

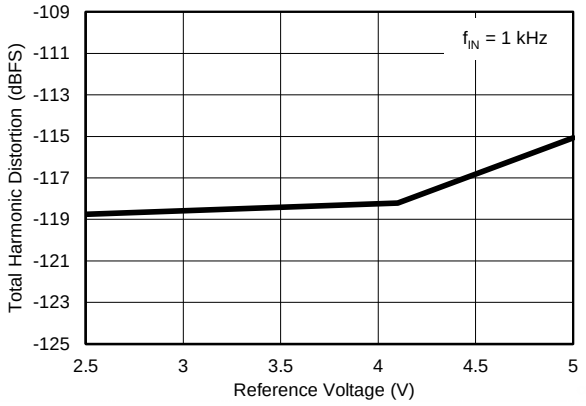


Figure 19. THD vs Reference Voltage

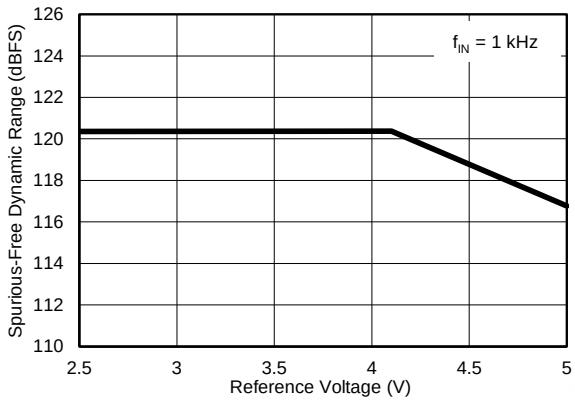


Figure 20. SFDR vs Reference Voltage

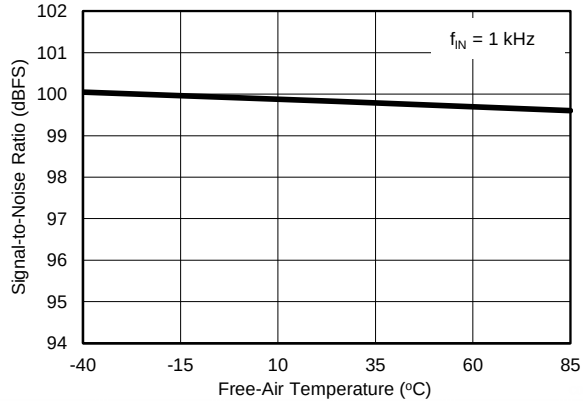


Figure 21. SNR vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

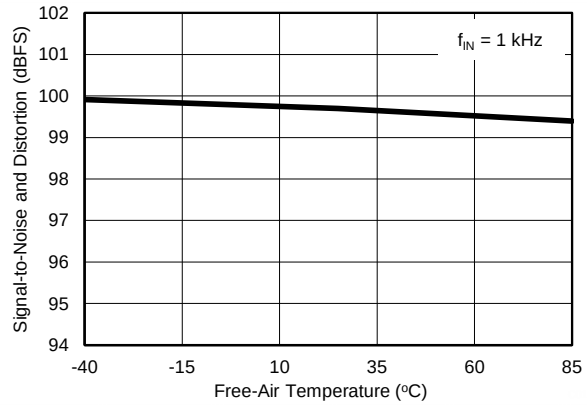


Figure 22. SINAD vs Temperature

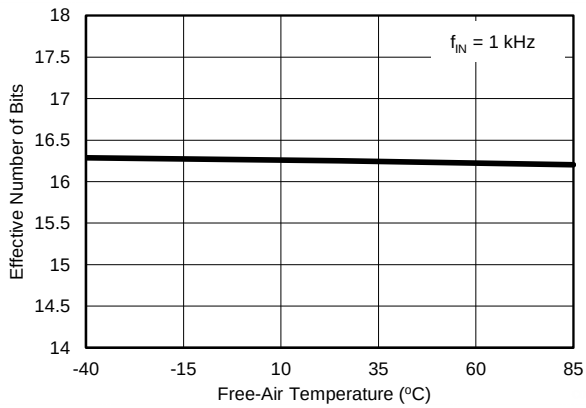


Figure 23. ENOB vs Temperature

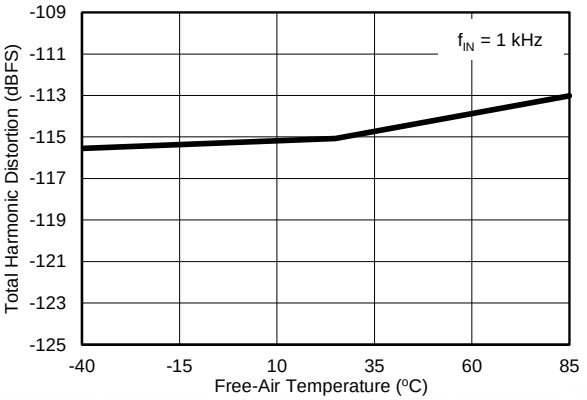


Figure 24. THD vs Temperature

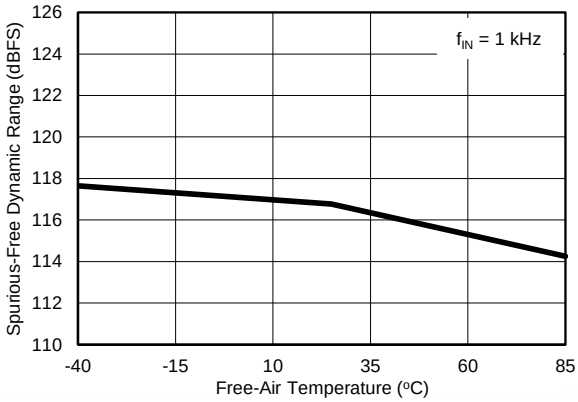


Figure 25. SFDR vs Temperature

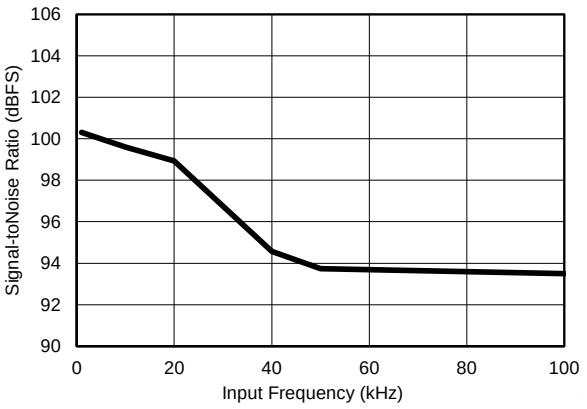


Figure 26. SNR vs Input Frequency

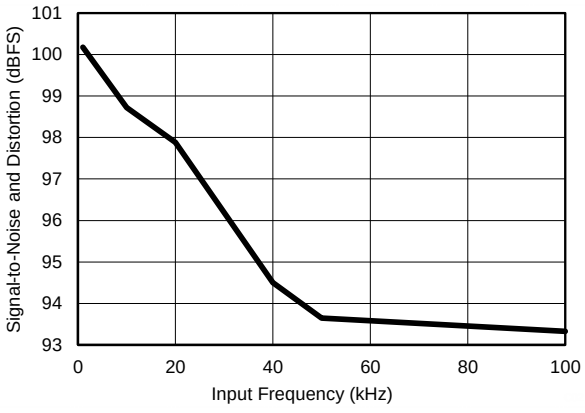


Figure 27. SINAD vs Input Frequency

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

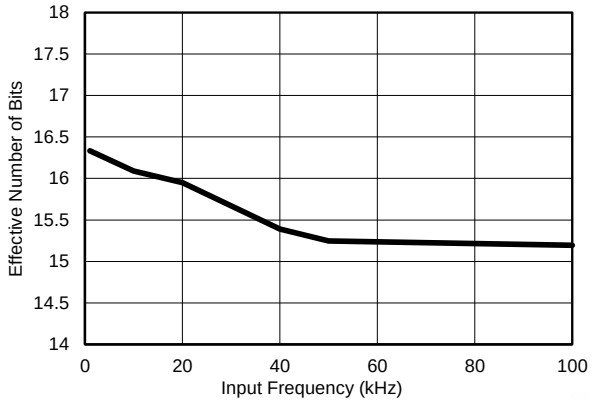


Figure 28. ENOB vs Input Frequency

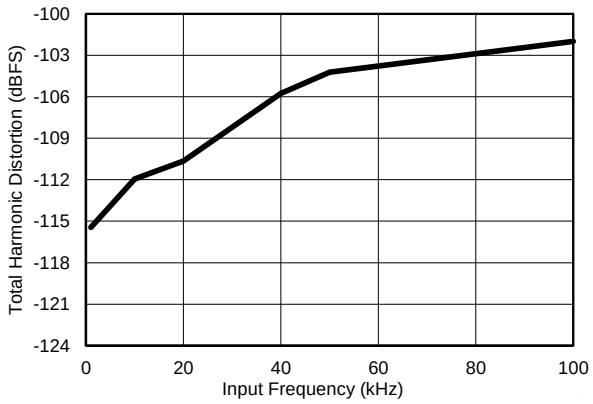


Figure 29. THD vs Input Frequency

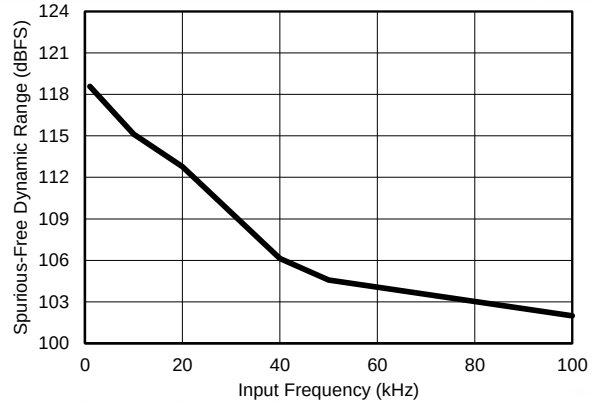


Figure 30. SFDR vs Input Frequency

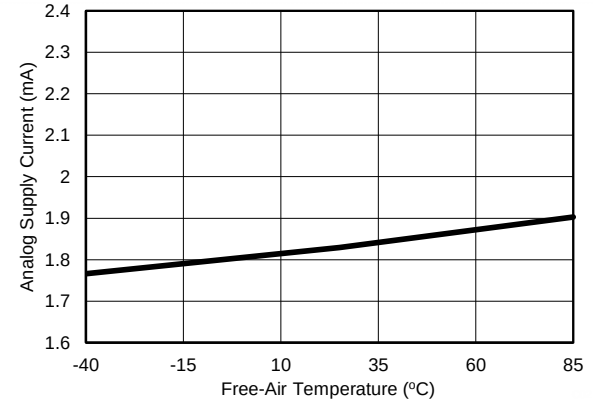


Figure 31. Supply Current vs Temperature

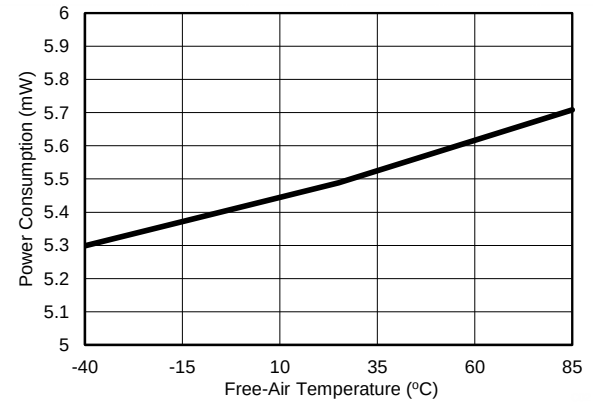


Figure 32. Power Consumption vs Temperature

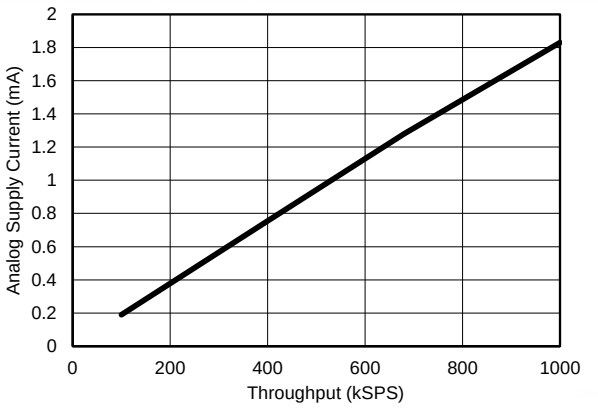


Figure 33. Supply Current vs Throughput

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

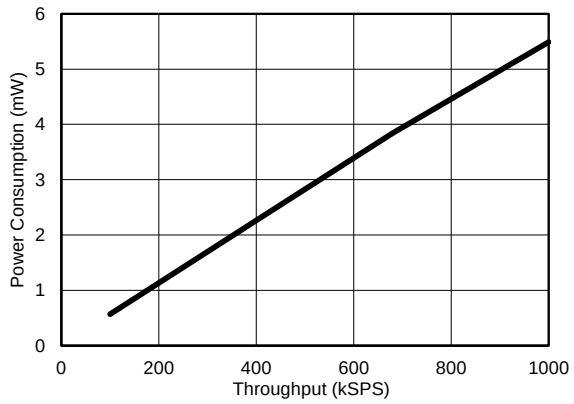


Figure 34. Power Consumption vs Throughput

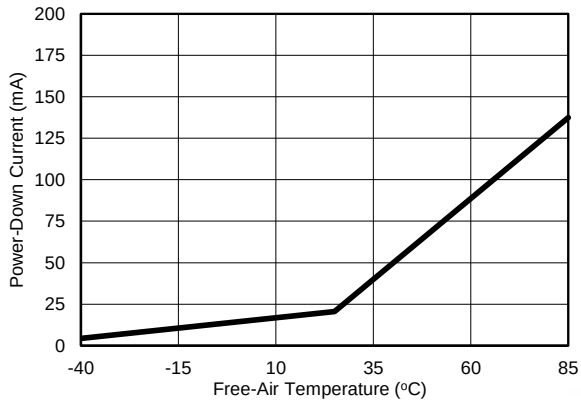


Figure 35. Power-Down Current vs Temperature

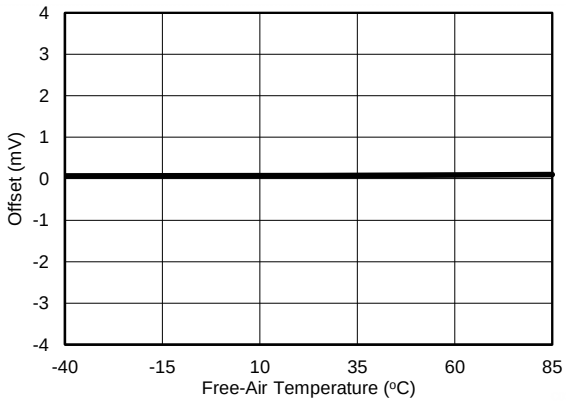


Figure 36. Offset vs Temperature

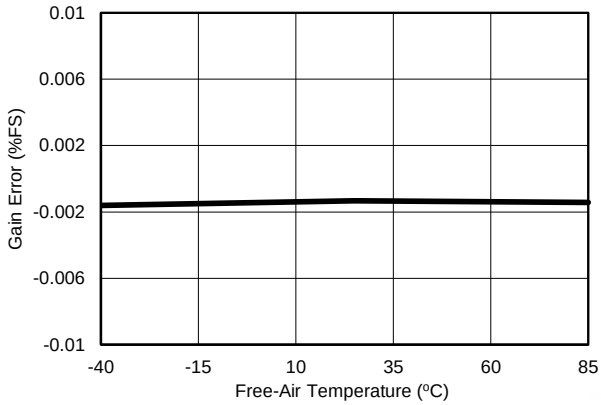


Figure 37. Gain Error vs Temperature

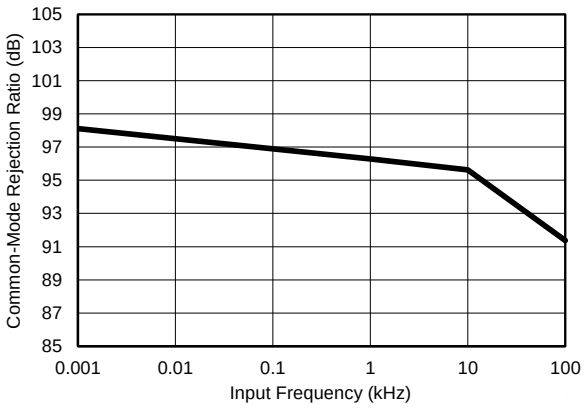


Figure 38. CMRR vs Input Frequency

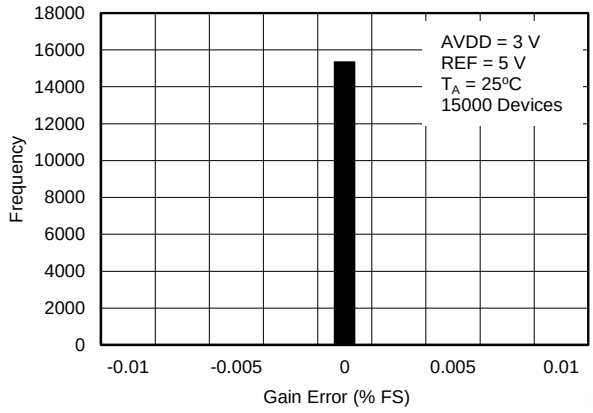


Figure 39. Typical Distribution of Gain Error

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

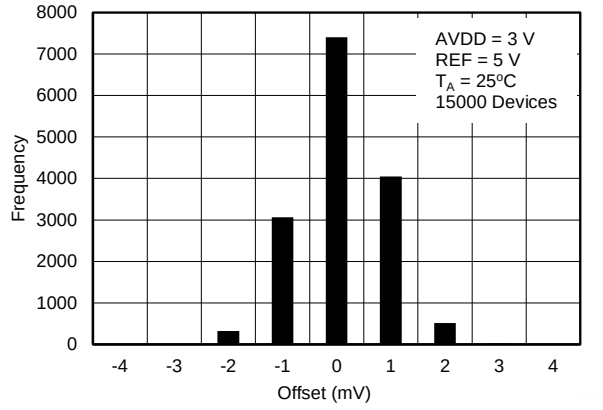


Figure 40. Typical Distribution of Offset Error

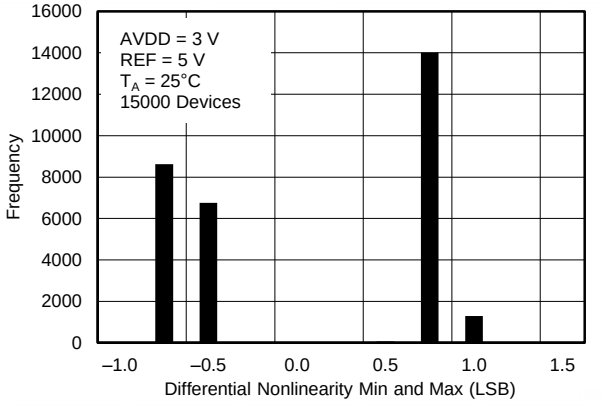


Figure 41. Typical Distribution of Differential Nonlinearity (Minimum and Maximum)

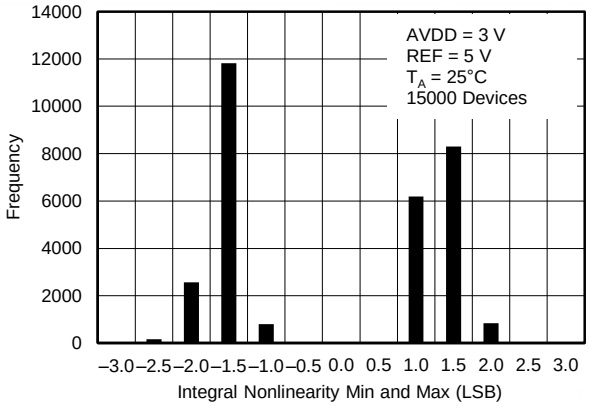


Figure 42. Typical Distribution of Integral Nonlinearity (Minimum and Maximum)

9 Parametric Measurement Information

9.1 Equivalent Circuits

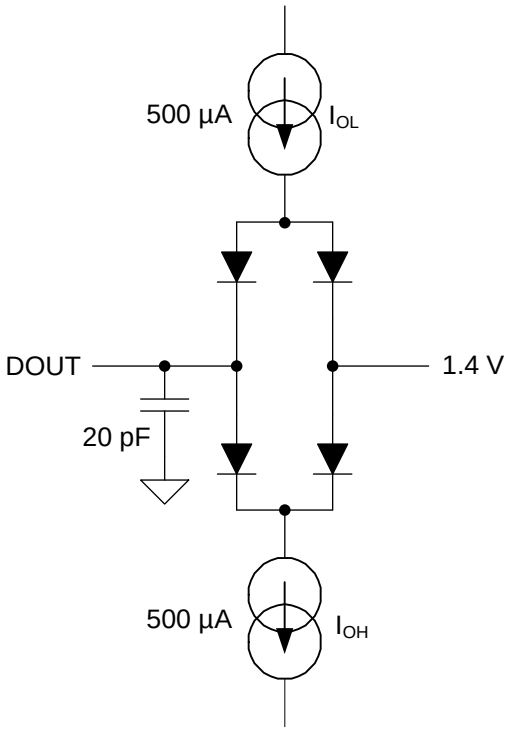


Figure 43. Load Circuit for Digital Interface Timing

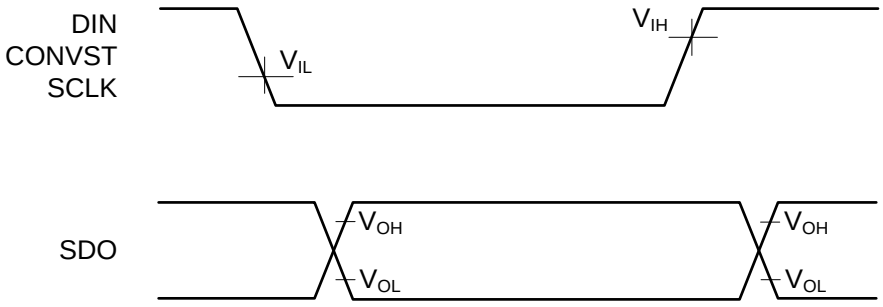


Figure 44. Voltage Levels for Timing

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10 Detailed Description

10.1 Overview

The ADS8881 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) from a 16- and 18-bit device family. This compact device features high performance. Power consumption is inherently low and scales linearly with sampling speed. The architecture is based on charge redistribution that inherently includes a sample-and-hold (S/H) function.

The ADS8881 supports a true-differential analog input across two pins (INP and INN). When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the INP and INN inputs are disconnected from the internal circuit.

The ADS8881 uses an internal clock to perform conversions. The device reconnects the sampling capacitors to the INP and INN pins after conversion and then enters an acquisition phase. During the acquisition phase, the device is powered down and the conversion result can be read.

The device digital output is available in SPI-compatible format, thus making interfacing with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs) easy.

10.2 Functional Block Diagram

Figure 45 shows the detailed functional block diagram for the device.

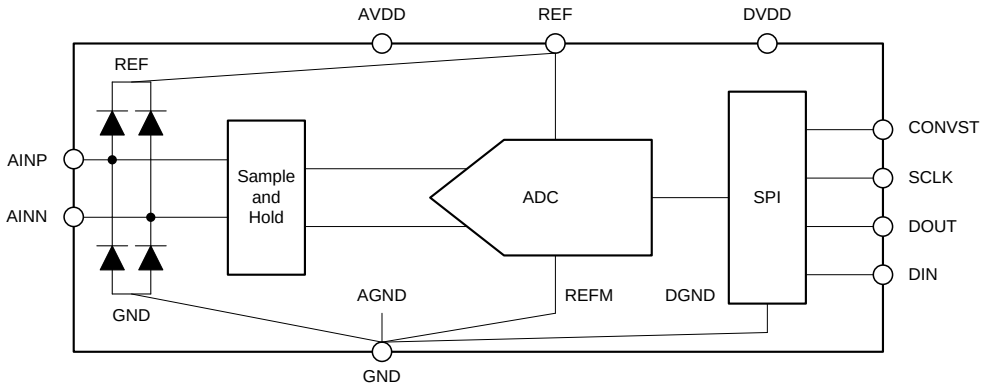


Figure 45. Detailed Block Diagram

10.3 Feature Description

10.3.1 Analog Input

As shown in Figure 45, the device features a differential analog input. Both positive and negative inputs are individually sampled on 55-pF sampling capacitors and the device converts for the voltage difference between the two sampled values: $V_{INP} – V_{INN}$.

Feature Description (continued)

Most differential input SAR ADCs prohibit the input common-mode voltage, V_{CM} (that is, the average voltage between the inputs), at AINP or AINM from varying more than approximately 10% beyond the mid-scale input value. As shown in Figure 46, the device has a unique common-mode voltage detection and rejection block that does not have this restriction and thus allows V_{CM} to be set to any value between 0 V and V_{REF} without degrading device performance.

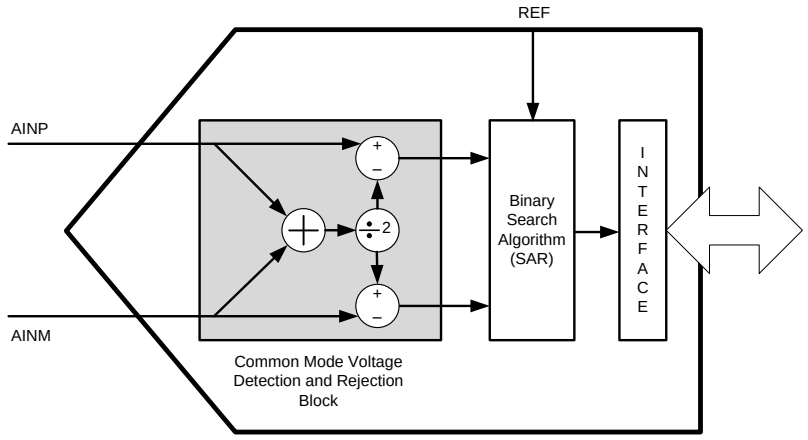


Figure 46. Conceptual Diagram: True Differential Input Structure

Table 1 shows the full-scale input range of the device as a function of input common-mode voltage. The device offers a maximum dynamic range for $V_{CM} = V_{REF} / 2$. The differential input with wide common-mode range allows connecting differential signals from sensors without any signal conditioning.

Table 1. Full-Scale Input Range

V_{CM}	ABSOLUTE INPUT RANGE		FULL SCALE INPUT RANGE (V_{FS})
	V_{AINP}	V_{AINN}	
$V_{CM} < V_{REF} / 2$	0 to $2 \times V_{CM}$	0 to $2 \times V_{CM}$	$(-2 \times V_{CM})$ to $(2 \times V_{CM})$
$V_{CM} = V_{REF} / 2$	0 to V_{REF}	0 to V_{REF}	$(-V_{REF})$ to (V_{REF})
$V_{CM} > V_{REF} / 2$	$(2 \times V_{CM} - V_{REF})$ to V_{REF}	$(2 \times V_{CM} - V_{REF})$ to V_{REF}	$[-2 \times (V_{CM} - V_{REF})]$ to $[2 \times (V_{CM} - V_{REF})]$

Figure 47 shows an equivalent circuit of the input sampling stage. The sampling switch is represented by a 96-Ω resistance in series with the ideal switch; see the *ADC Input Driver* section for more details on the recommended driving circuits.

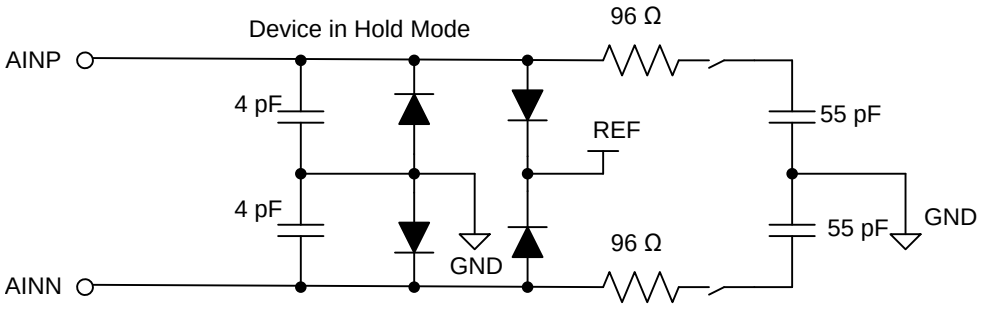


Figure 47. Input Sampling Stage Equivalent Circuit

Figure 45 and Figure 47 illustrate electrostatic discharge (ESD) protection diodes to REF and GND from both analog inputs. Make sure that these diodes do not turn on by keeping the analog inputs within the specified range.

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10.3.2 Reference

The device operates with an external reference voltage and switches binary-weighted capacitors onto the reference terminal (REF pin) during the conversion process. The switching frequency is proportional to the internal conversion clock frequency but the dynamic charge requirements are a function of the absolute value of the input voltage and reference voltage. This dynamic load must be supported by a reference driver circuit without degrading the noise and linearity performance of the device. During the acquisition process, the device automatically powers down and does not take any dynamic current from the external reference source. The basic circuit diagram for such a reference driver circuit for precision ADCs is shown in Figure 48; see the *ADC Reference Driver* section for more details on the application circuits.

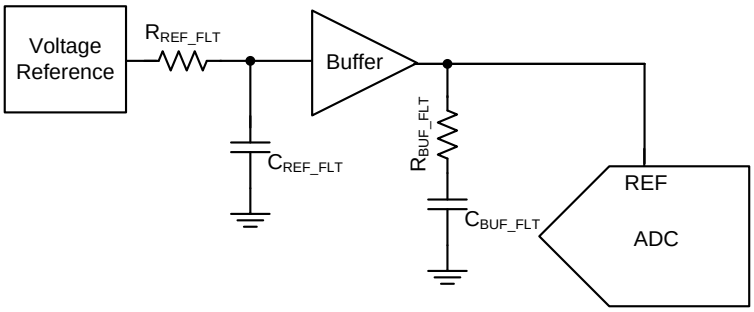


Figure 48. Reference Driver Schematic

10.3.3 Clock

The device uses an internal clock for conversion. Conversion duration may vary but is bounded by the minimum and maximum value of t_{conv}, as specified in the *Timing Requirements* section. An external SCLK is only used for a serial data read operation. Data are read after a conversion completes and when the device is in acquisition phase for the next sample.

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10.3.4 ADC Transfer Function

The ADS8881 is a unipolar, differential input device. The device output is in twos compliment format.

Figure 49 shows ideal characteristics for the device. The full-scale range for the ADC input (AINP – AINN) is equal to twice the reference input voltage to the ADC ($2 \times V_{REF}$). The LSB for the ADC is given by Equation 1.

$$1\ LSB = [2 \times (V_{REF} / 2^{18})] \quad (1)$$

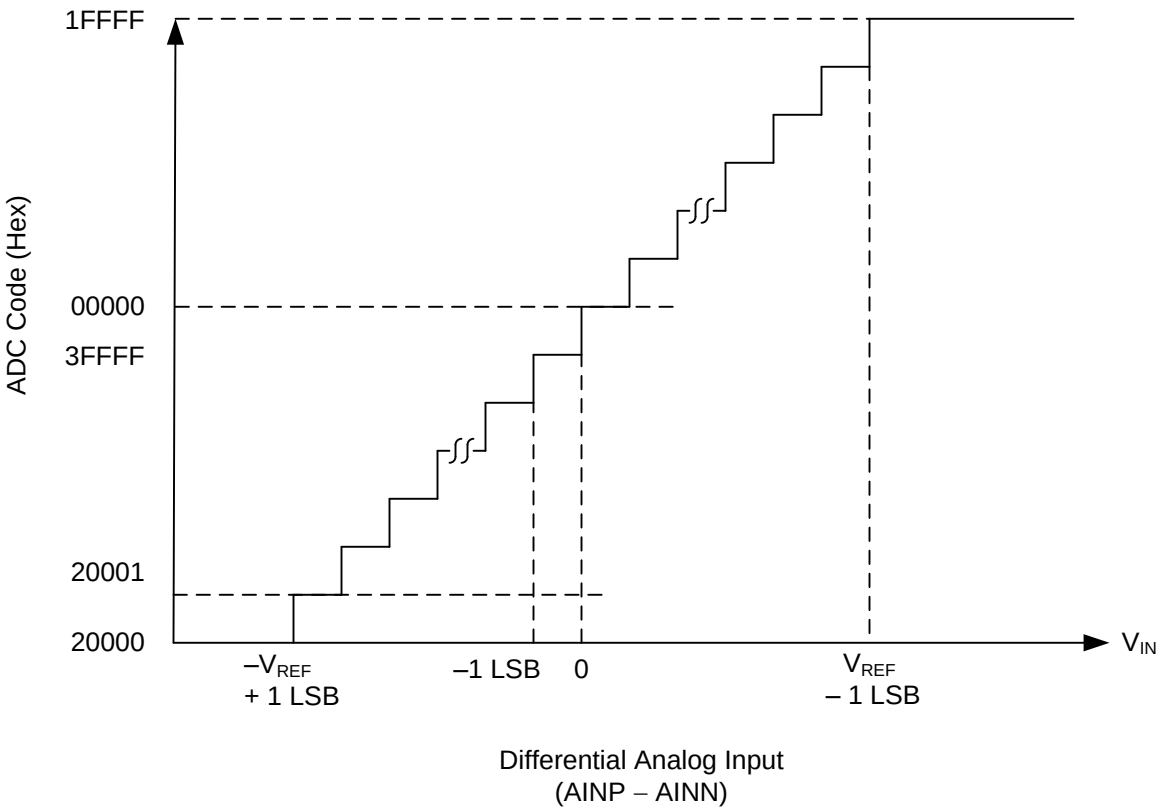


Figure 49. Differential Transfer Characteristics

10.4 Device Functional Modes

The ADS8881 is a low pin-count device. However, the device offers six different options for interfacing with the digital host.

These options can be broadly classified as being either $\overline{CS}$ *mode* (in either a 3- or 4-wire interface) or *daisy-chain mode*. The device operates in $\overline{CS}$ mode if DIN is high at the CONVST rising edge. If DIN is low at the CONVST rising edge, or if DIN and CONVST are connected together, the device operates in daisy-chain mode. In both modes, the device can either operate with or without a *busy indicator*, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

The 3-wire interface in $\overline{CS}$ mode is useful for applications that need galvanic isolation on-board. The 4-wire interface in $\overline{CS}$ mode allows the user to sample the analog input independent of the serial interface timing and, therefore, allows easier control of an individual device while having multiple, similar devices on-board. The daisy-chain mode is provided to hook multiple devices in a chain similar to a shift register and is useful in reducing component count and the number of signal traces on the board.

10.4.1 $\overline{CS}$ Mode

$\overline{CS}$ mode is selected if DIN is high at the CONVST rising edge. There are four different interface options available in this mode: 3-wire $\overline{CS}$ mode without a busy indicator, 3-wire $\overline{CS}$ mode with a busy indicator, 4-wire $\overline{CS}$ mode without a busy indicator, and 4-wire $\overline{CS}$ mode with a busy indicator. The following sections discuss these interface options in detail.

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Device Functional Modes (continued)

10.4.1.1 3-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 50). As shown in Figure 51, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must return high before the minimum conversion time ($t_{conv-min}$) elapses and is held high until the maximum possible conversion time ($t_{conv-max}$) elapses. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

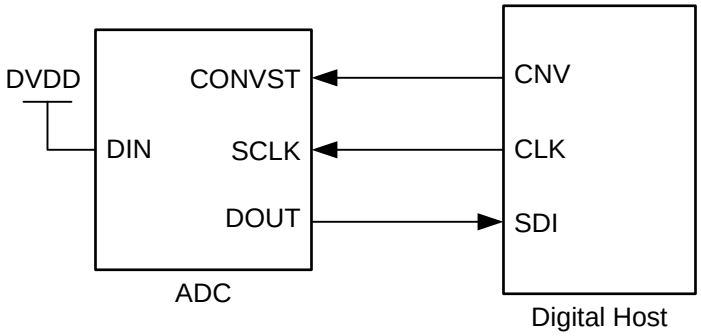


Figure 50. Connection Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (DIN = 1)

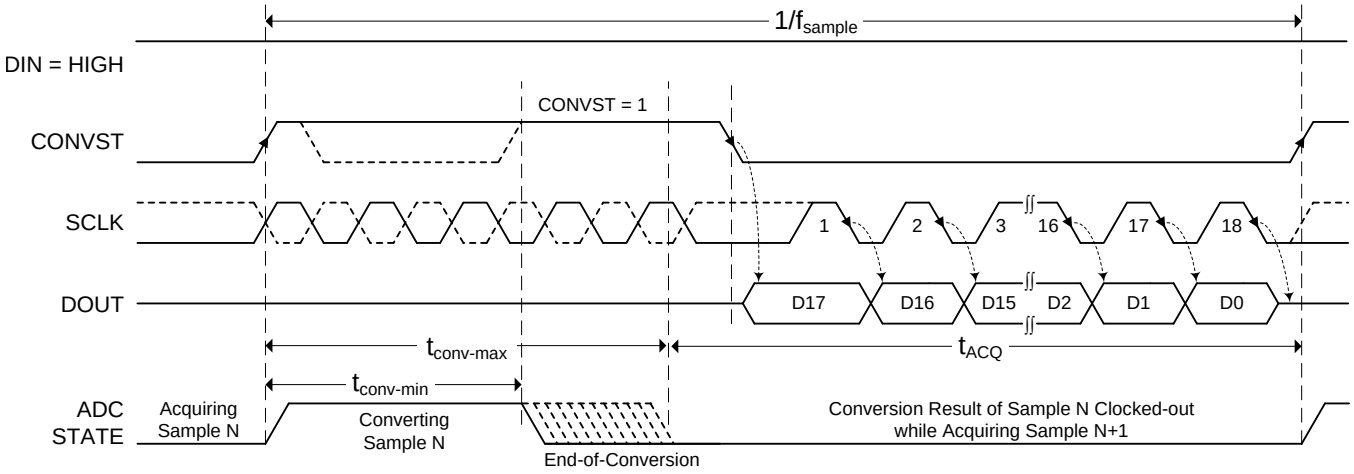


Figure 51. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down. CONVST (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv-max}$) elapses. On the CONVST falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO-min}$ time frame. DOUT goes to 3-state after the 18th SCLK falling edge or when CONVST goes high, whichever occurs first.

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Device Functional Modes (continued)

10.4.1.2 3-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 52). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 53, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must be pulled low before the minimum conversion time ($t_{conv-min}$) elapses and must remain low until the maximum possible conversion time ($t_{conv-max}$) elapses. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.

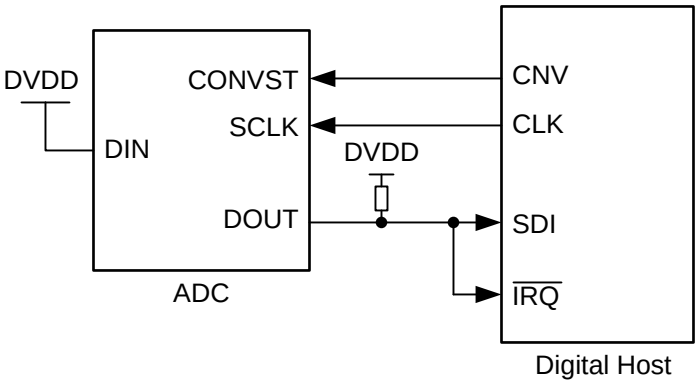


Figure 52. Connection Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator

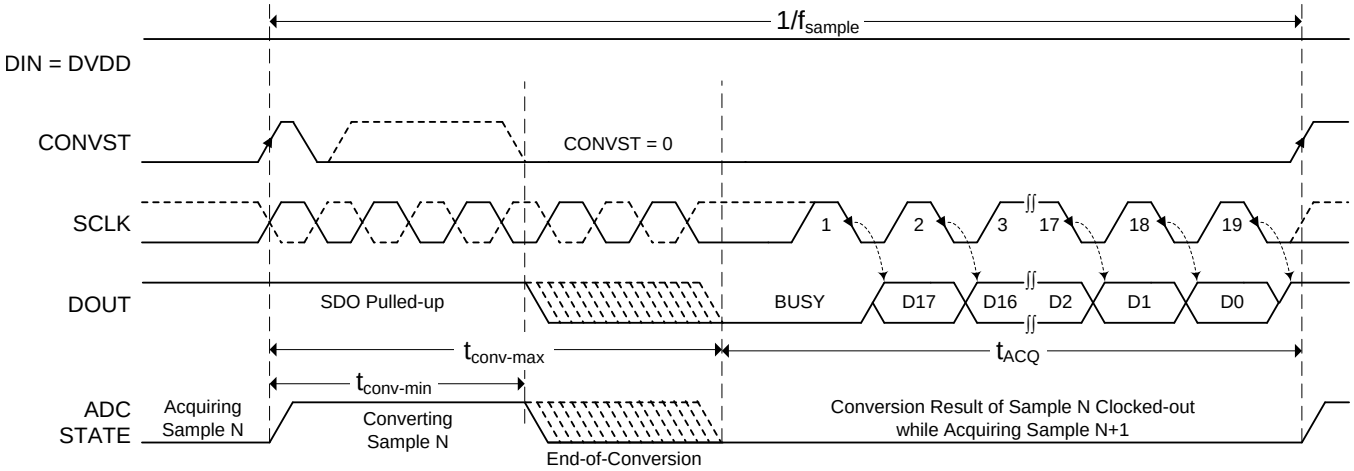


Figure 53. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO-min}$ time frame. DOUT goes to 3-state after the 19th SCLK falling edge or when CONVST goes high, whichever occurs first.

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Device Functional Modes (continued)

10.4.1.3 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is useful when one or more ADCs are connected to an SPI-compatible digital host. Figure 54 shows the connection diagram for single ADC; see Figure 56 for the connection diagram for two ADCs.

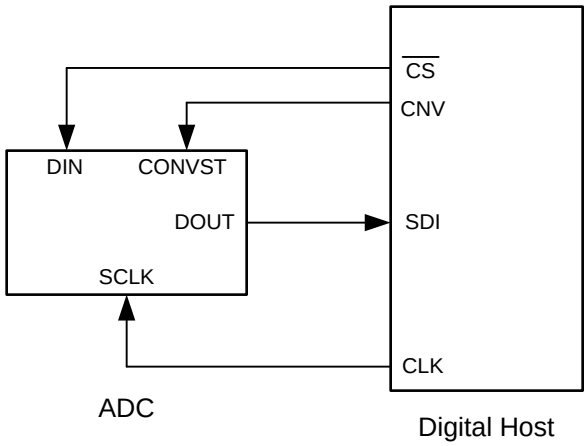


Figure 54. Connection Diagram: Single ADC With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$. As shown in Figure 55, with DIN high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (functioning as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled high before the minimum conversion time ($t_{conv-min}$) elapses and remains high until the maximum possible conversion time ($t_{conv-max}$) elapses. A high level on DIN at the end of the conversion ensures the device does not generate a busy indicator.

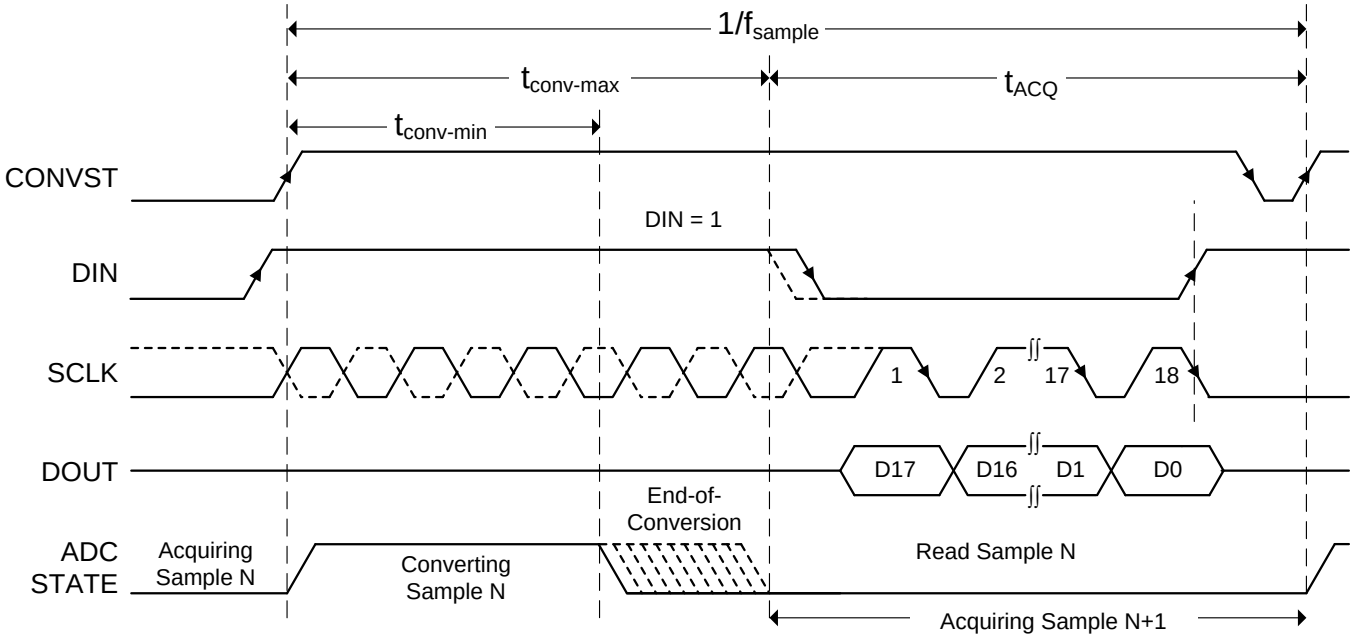


Figure 55. Interface Timing Diagram: Single ADC With 4-Wire $\overline{CS}$ Mode

Device Functional Modes (continued)

When conversion is complete, the device enters acquisition phase and powers down. DIN (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv-max}$) elapses. On the DIN falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO-min}$ time frame. DOUT goes to 3-state after the 18th SCLK falling edge or when DIN goes high, whichever occurs first.

As shown in Figure 56, multiple devices can be hooked together on the same data bus. In this case, as shown in Figure 57, the DIN of the second device (functioning as $\overline{CS}$ for the second device) can go low after the first device data are read and the DOUT of the first device is in 3-state.

Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

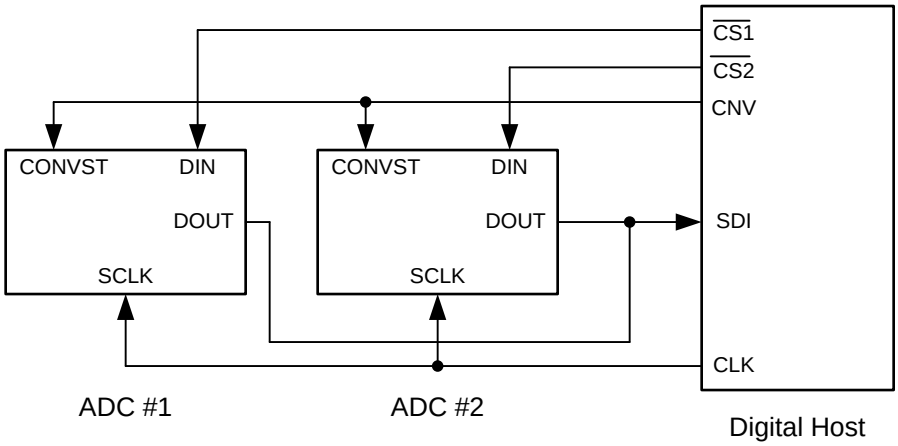


Figure 56. Connection Diagram: Two ADCs With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

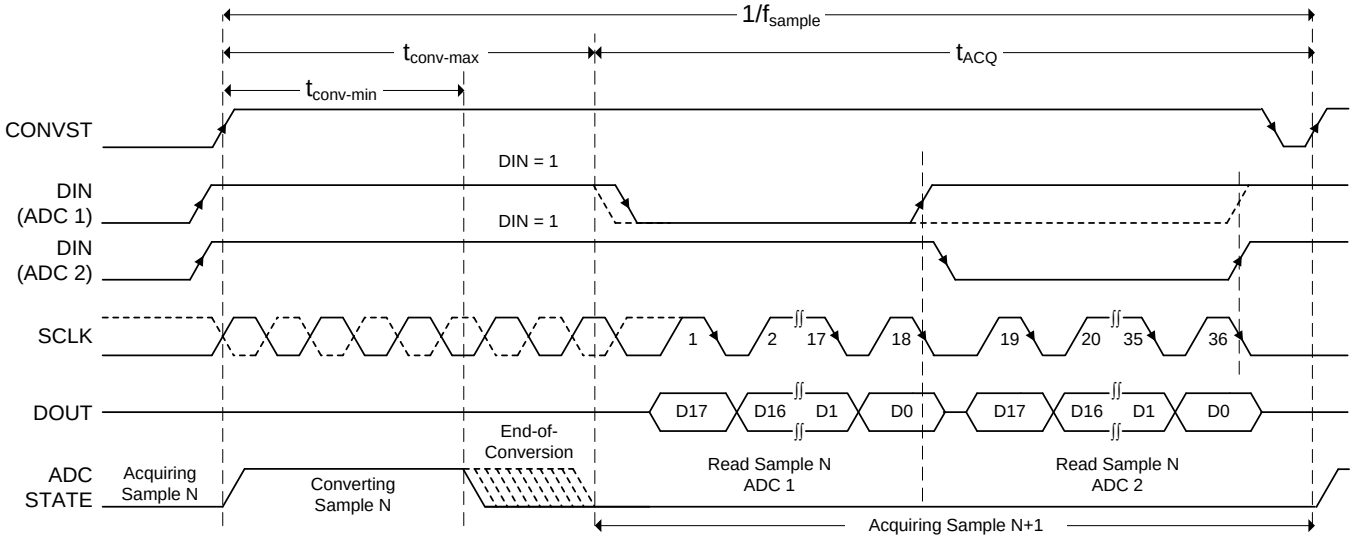


Figure 57. Interface Timing Diagram: Two ADCs With 4-Wire $\overline{CS}$ Mode

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Device Functional Modes (continued)

10.4.1.4 4-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, the analog sample is least affected by clock jitter because the CONVST signal (used to sample the input) is independent of the data read operation. In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$ (as shown in Figure 58). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 59, when DIN is high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held high from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (acting as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled low before the minimum conversion time ($t_{conv-min}$) elapses and remains low until the maximum possible conversion time ($t_{conv-max}$) elapses. A low level on the DIN input at the end of a conversion ensures the device generates a busy indicator.

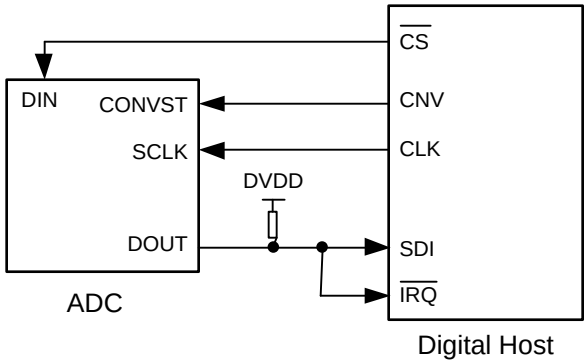


Figure 58. Connection Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

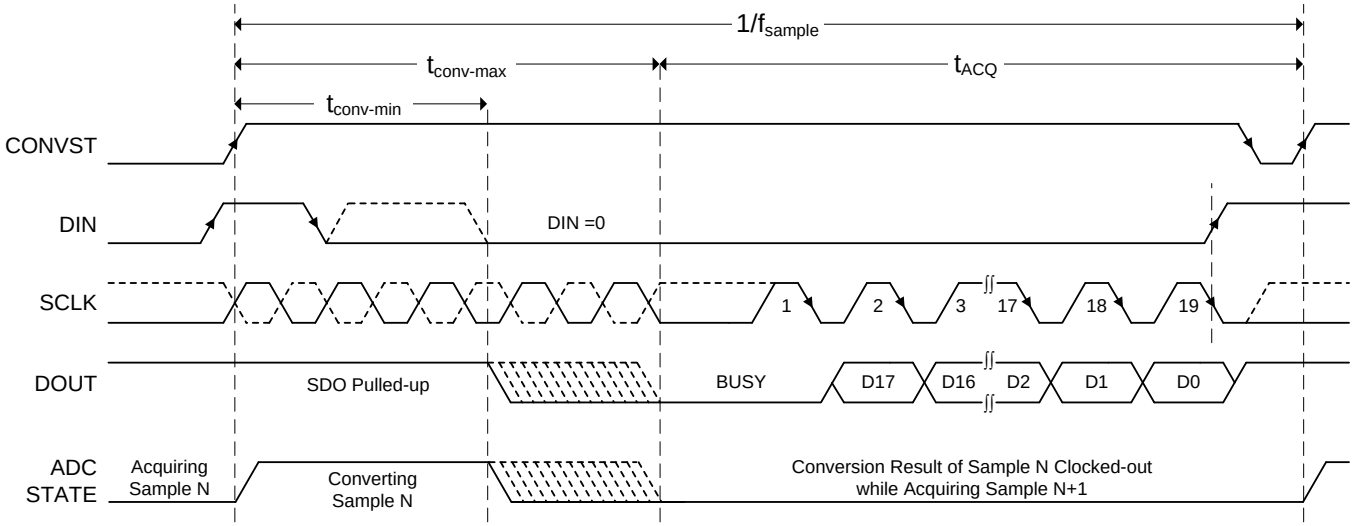


Figure 59. Interface Timing Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

Device Functional Modes (continued)

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO\text{-}min}$ time frame. DOUT goes to 3-state after the 19th SCLK falling edge or when DIN goes high, whichever occurs first. Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

10.4.2 Daisy-Chain Mode

Daisy-chain mode is selected if DIN is low at the time of a CONVST rising edge or if DIN and CONVST are connected together. Similar to $\overline{CS}$ mode, this mode features operation with or without a busy indicator. The following sections discuss these interface modes in detail.

10.4.2.1 Daisy-Chain Mode Without a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability. Figure 60 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to GND. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI pin of the digital host.

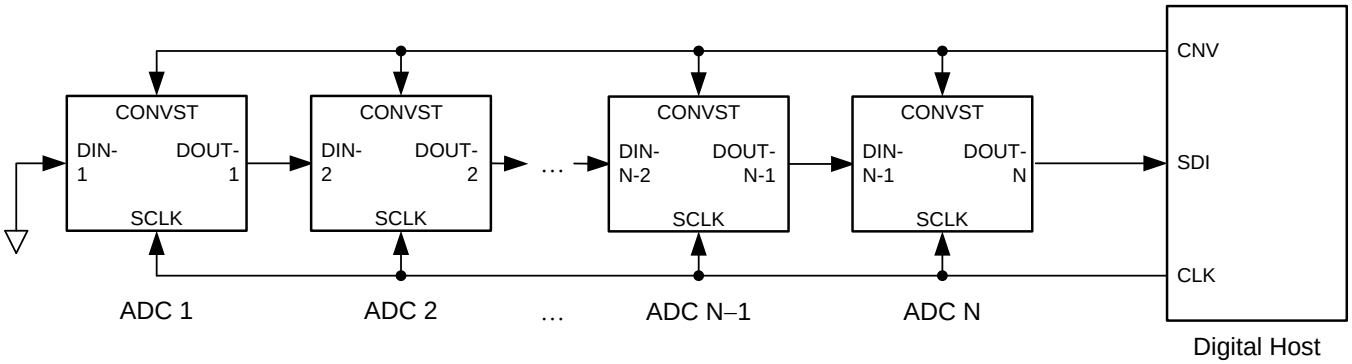


Figure 60. Connection Diagram: Daisy-Chain Mode Without a Busy Indicator (DIN = 0)

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Device Functional Modes (continued)

As shown in Figure 61, the device DOUT pin is driven low when DIN and CONVST are low together. With DIN low, a CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be low at the CONVST rising edge so that the device does not generate a busy indicator at the end of the conversion.

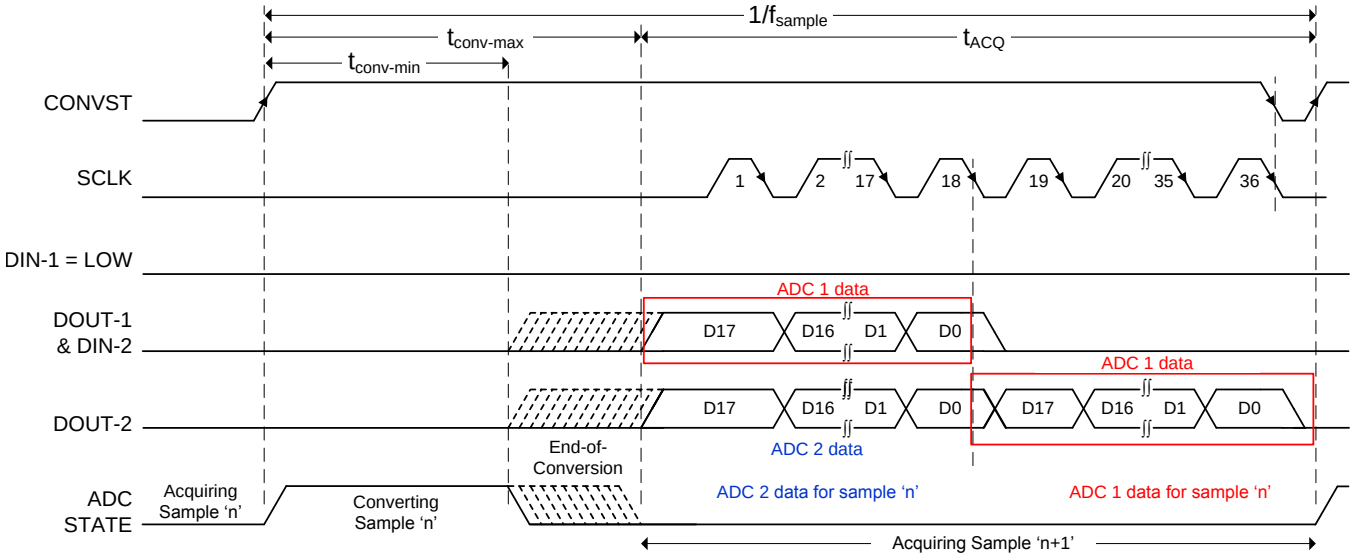


Figure 61. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 18-bit, shift register and also outputs the MSB bit of this conversion result on its own DOUT pin. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the data of ADC N, followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of 18 x *N* SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO\text{-}min}$ time frame.

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Device Functional Modes (continued)

10.4.2.2 Daisy-Chain Mode With a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability and an interrupt-driven data transfer is desired. Figure 62 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to its CONVST. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI and IRQ pins of the digital host.

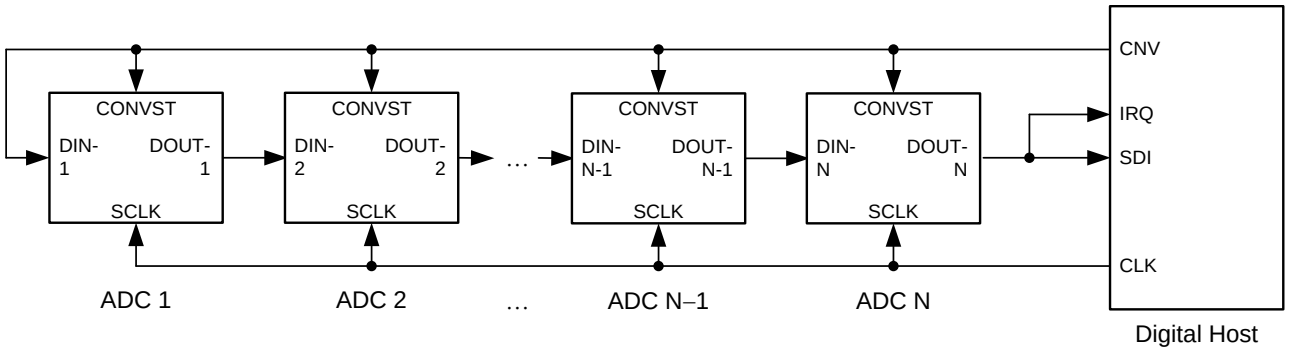


Figure 62. Connection Diagram: Daisy-Chain Mode With a Busy Indicator (DIN = 0)

As shown in Figure 63, the device DOUT pin is driven low when DIN and CONVST are low together. A CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be high at the CONVST rising edge so that the device generates a busy indicator at the end of the conversion.

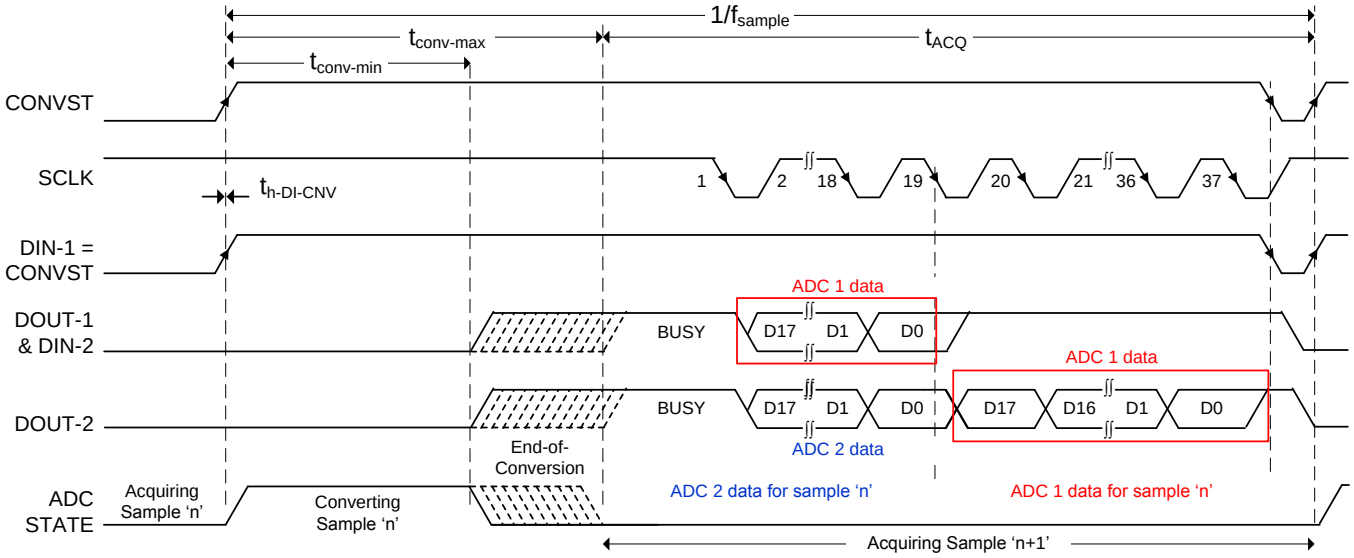


Figure 63. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode With a Busy Indicator

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Device Functional Modes (continued)

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 18-bit, shift register and also forces its DOUT pin high, thereby providing a low-to-high transition on the IRQ pin of the digital host. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the interrupt signal followed by the data of ADC N followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of (18 × N) + 1 SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Fast sampling rates require a high-frequency SCLK and data must be read at the SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at the SCLK falling edge requires the digital host to clock in the data during the $t_{h_CK_DO\text{-}min}$ time frame. Note that the busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

NOTE: For SCLK ≤ 36 MHz, SPI mode-3 (CPOL = 1, CPHA = 1) allows reading the conversion results of N ADCs in 18 × N SCLK cycles because the busy indicator bit is not clocked in by the host.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by some application circuits designed using the ADS8881.

11.1.1 ADC Reference Driver

The external reference source to the ADS8881 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few hundred μV_{RMS}. Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of V_{REF} stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor, C_{BUF_FLT} (see Figure 48) for regulating the voltage at the reference input of the ADC. The amplifier selected to drive the reference pin must have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pin without any stability issues.

11.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 18-bit ADC such as the ADS8881.

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Application Information (continued)

11.1.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (see the *Antialiasing Filter* section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier bandwidth as described in Equation 2:

$$Unity-Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (2)$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in Equation 3.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \quad \leq \quad \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (3)$$

where:

- $V_{1\ /\ f_AMP_PP}$ is the peak-to-peak flicker noise in µV,
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration.

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in Equation 4.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \quad (4)$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA™-SPICE simulations before selecting the amplifier.

11.1.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the inputs of the ADC during the small acquisition time window. For ac signals, keep the filter bandwidth low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.

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Application Information (continued)

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A differential filter capacitor, C_{FLT}, is connected across the inputs of the ADC (as shown in Figure 64). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor must be at least 10 times the specified value of the ADC sampling capacitance. For the ADS8881, the input sampling capacitance is equal to 59 pF, thus the value of C_{FLT} must be greater than 590 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

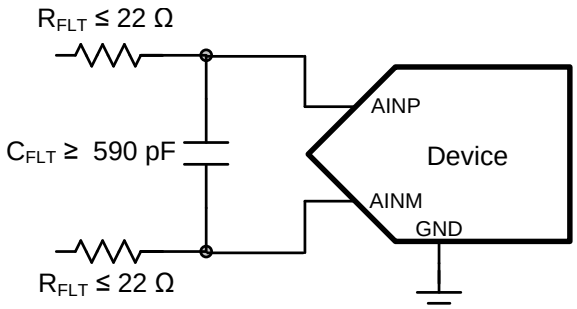


Figure 64. Antialiasing Filter

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS8881, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth must be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

This section describes some common application circuits using the ADS8881. These data acquisition (DAQ) blocks are optimized for specific input types and performance requirements of the system. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the *Power Supply* section for suggested guidelines.

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11.2 Typical Applications

11.2.1 DAQ Circuit for a 1-µs, Full-Scale Step Response

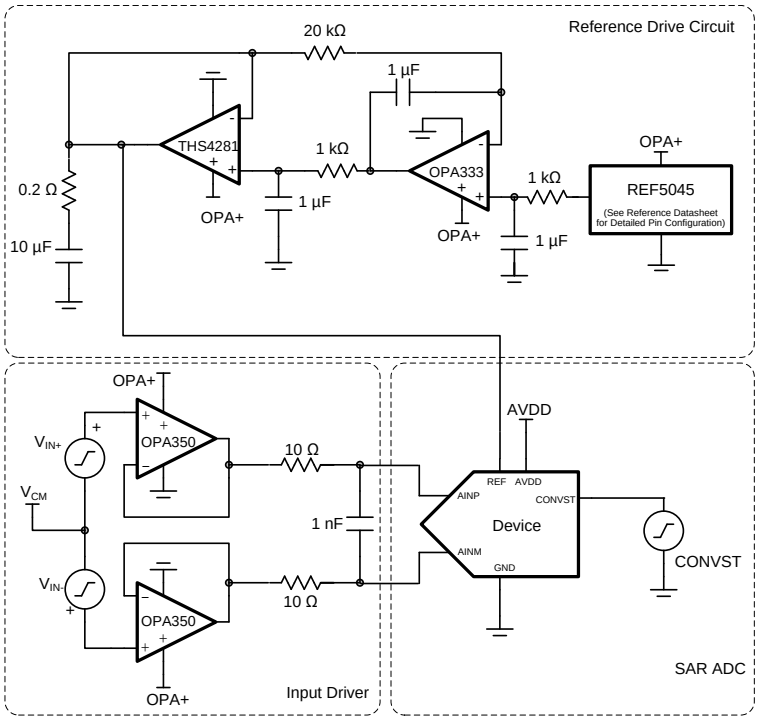


Figure 65. DAQ Circuit for a 1-µs, Full-Scale Step Response

11.2.1.1 Design Requirements

Step input signals are common in multiplexed applications when switching between different channels. In a worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched.

Design an application circuit optimized for using the ADS8881 to achieve

- full-scale step input settling to 18-bit accuracy and
- INL of < ±2 LSB and
- maximum specified throughput of 1 MSPS

11.2.1.2 Detailed Design Procedure

The application circuit is shown in Figure 65.

In such applications, the primary design requirement is to ensure that the full-scale step input signal settles to 18-bit accuracy at the ADC inputs. This condition is critical to achieve the excellent linearity specifications of the ADC. Therefore, the bandwidth of the antialiasing RC filter must be large enough to allow optimal settling of the input signal during the ADC acquisition time. The filter capacitor helps reduce the sampling charge injection at the ADC inputs, but degrades the phase margin of the driving amplifier, thereby leading to stability issues. Amplifier stability is maintained by the series isolation resistor.

The application circuit in Figure 65 shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

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Typical Applications (continued)

The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

For the input driving amplifiers, key specifications include rail-to-rail input and output swing, high bandwidth, high slew rate, and fast settling time. The OPA350 CMOS amplifier meets all these specification requirements for this circuit with a single-supply and low quiescent current. The component values of the antialiasing filter are selected to meet the settling requirements of the system as well as to maintain the stability of the input driving amplifiers.

11.2.1.3 Application Curve



18-bit INL

Figure 66. Limited Point Linearity

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response* (TIDU012).

11.2.2 Low-Power DAQ Circuit for Excellent Dynamic Performance at 1 MSPS

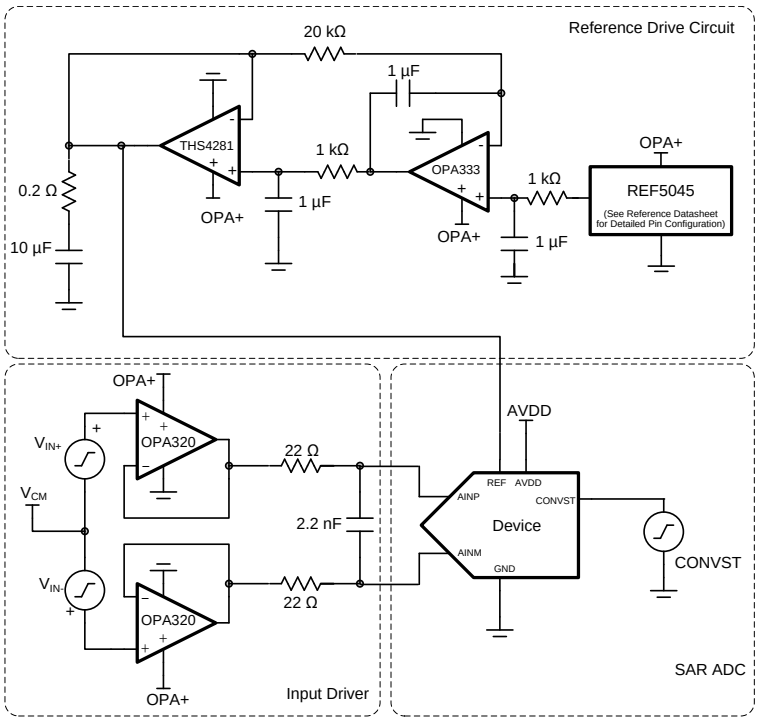


Figure 67. DAQ Circuit for Lowest Power and Excellent Dynamic Performance at 1 MSPS

11.2.2.1 Design Requirements

Design an application circuit optimized for using the ADS8881 to achieve

- ENOB > 17 bits and
- < 35 mW of total power consumption and
- maximum specified throughput of 1 MSPS

11.2.2.2 Detailed Design Procedure

The application circuit in Figure 67 shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

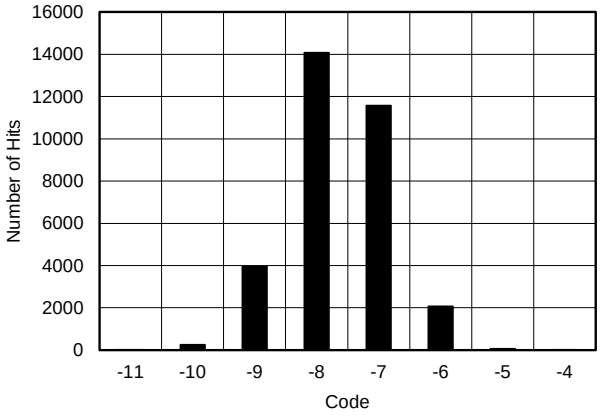
The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

In such applications, the input driver must be low in power and noise as well as able to support rail-to-rail input and output swing with a single supply. A high amplifier bandwidth is also preferred to help attenuate high-frequency distortion. However, oftentimes bandwidth and noise are traded off with the power consumption of the amplifier. This circuit uses the OPA320 as the front-end driving amplifier because this device has a relatively low noise density of 7 nV/$\sqrt{\text{Hz}}$ for a maximum-specified quiescent current of 1.45 mA per channel.

The noise contribution from the front-end amplifier is band-limited by the 3-dB bandwidth of the RC filter and is designed to be 1.65 MHz in this application. Again, the component values of the antialiasing filter are carefully selected to maintain the stability of the input driving amplifiers.

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11.2.2.3 Application Curve



V_{diff} close to 0 V, 32768 data points, standard deviation = 0.82 bits,
ENOB (dc) = 17.18 bits

Figure 68. DC Input Histogram

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power* (SLAU513).

11.2.3 DAQ Circuit for Lowest Distortion and Noise Performance at 1 MSPS

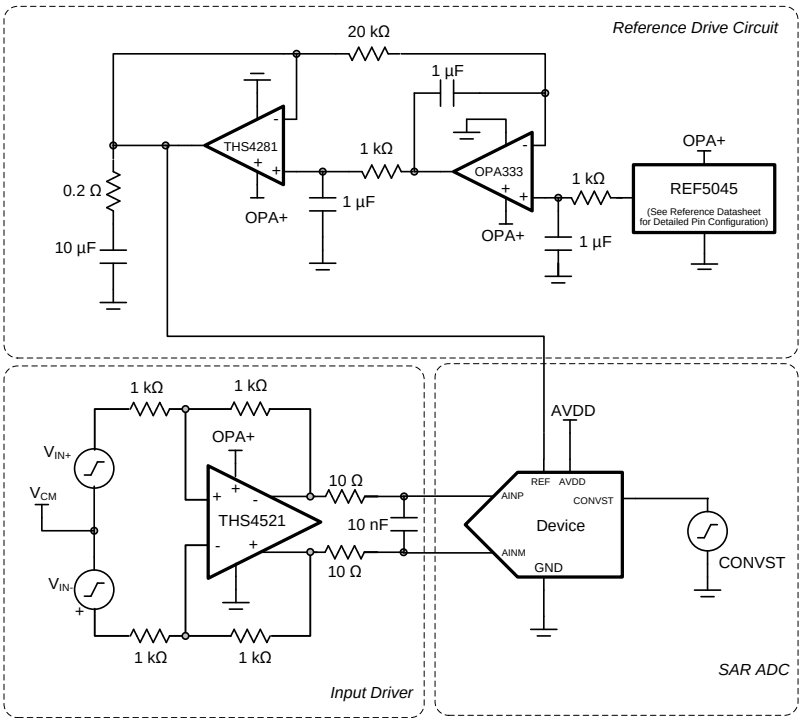


Figure 69. Differential Input DAQ Circuit for Lowest Distortion and Noise at 1 MSPS

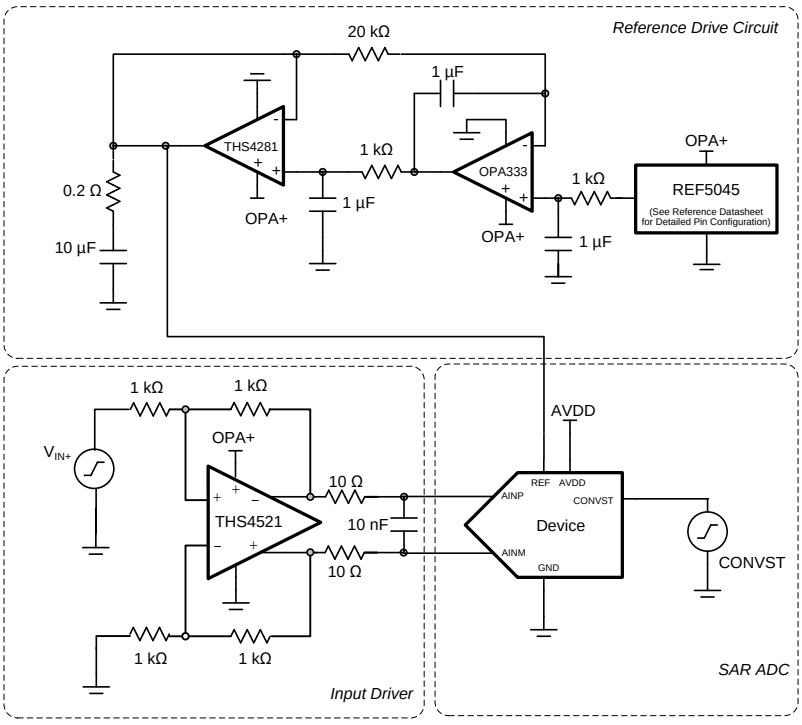


Figure 70. Single-Ended to Differential DAQ Circuit for Lowest Distortion and Noise at 1 MSPS

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11.2.3.1 Design Requirements

Design an application circuit optimized for using the ADS8881 to achieve

- > 98.5-dB SNR, < –110-dB THD and
- ± 1.5-LSB linearity and
- maximum specified throughput of 1 MSPS

11.2.3.2 Detailed Design Procedure

The application circuits are shown in Figure 69 and Figure 70. In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in an inverting gain configuration and a low-pass RC filter before being fed into the ADC.

The reference driver circuit, shown in Figure 69 and Figure 70, generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8881 at higher sampling rates up to 1 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

As a rule of thumb, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power THS4521 as an input driver that provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications.

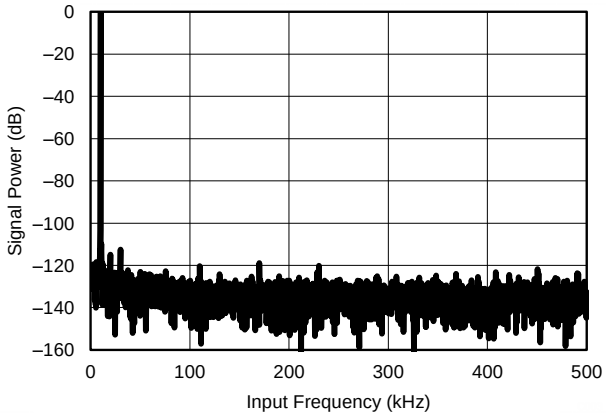
In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

The circuit in Figure 69 shows a fully-differential DAQ block optimized for low distortion and noise using the THS4521 and ADS8881. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4521 (not shown in Figure 69). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider. However, note that the ADS8881 allows the common-mode input voltage (V_{CM}) to be set to any value in the range of 0 V to V_{REF}.

The circuit in Figure 70 shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4521 and the ADS8881. This front-end circuit configuration requires a single-ended ac signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4521 (not shown in Figure 70). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider. However, note that the ADS8881 allows the common-mode input voltage (V_{CM}) to be set to any value in the range of 0 V to V_{REF}.

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11.2.3.3 Application Curve



f_{IN} = 10 kHz, SNR = 99 dB, THD = –112 dB

Figure 71. FFT Plot

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Distortion and Noise* (SLAU515).

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11.2.4 Ultralow-Power DAQ Circuit at 10 kSPS

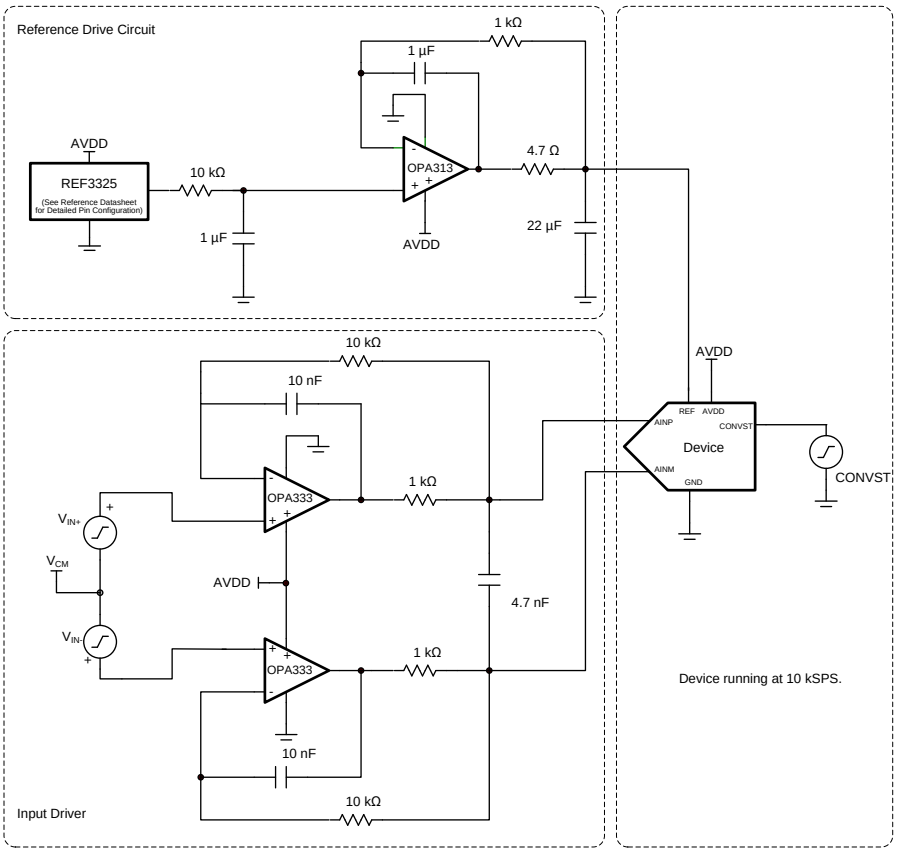


Figure 72. Ultralow-Power DAQ Circuit at 10 kSPS

11.2.4.1 Design Requirements

Portable and battery-powered applications require ultralow-power consumption and do not need very high throughput from the ADC.

Design a single-supply, data acquisition circuit optimized for using the ADS8881 to achieve

- ENOB > 16 bits and
- Ultralow-power consumption of < 1 mW at throughput of 10 kSPS.

11.2.4.2 Detailed Design Procedure

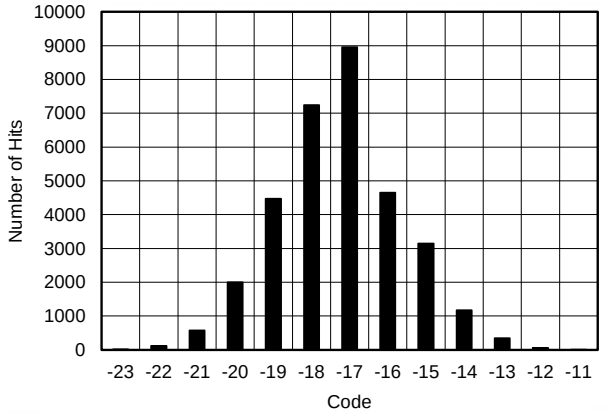
The application circuit in Figure 72 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5 V dc using a single 3.3-V supply. This ultralow power reference block is suitable to drive the ADS8881 for power-sensitive applications at a relatively lower throughput. This design uses the high-precision REF3325 circuit that provides an accurate 2.5-V reference voltage at an extremely low quiescent current of 5 µA. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

The reference buffer is designed with the low-power OPA313 that can operate from a 3.3-V supply at an extremely low quiescent current of 50 µA. The wideband noise contribution from the amplifier is limited by a lowpass filter of a cutoff frequency equal to 1.5 kHz, formed by a 4.7-Ω resistor in combination with a 22-µF capacitor. The 4.7-Ω series resistor creates an additional drop in the reference voltage that is corrected by a dual-feedback configuration.

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The input driver circuit uses extremely low-power, dual amplifiers (such as the OPA2333) with a maximum quiescent current of 28 µA per channel to drive the ADC inputs. The input amplifiers are configured in a modified unity-gain buffer configuration. The filter capacitor at the ADC inputs attenuates the sampling charge-injection noise from the ADC but effects the stability of the input amplifiers by degrading the phase margin. This attenuation requires a series isolation resistor to maintain amplifier stability. The value of the series resistor is directly proportional to the open-loop output impedance of the driving amplifier to maintain stability, which is high (in the order of kΩ) in the case of low-power amplifiers such as the OPA333. Therefore, a high value of 1 kΩ is selected for the series resistor at the ADC inputs. However, this series resistor creates an additional voltage drop in the signal path, thereby leading to linearity and distortion issues. The dual-feedback configuration used in Figure 72 corrects for this additional voltage drop and maintains system performance at ultralow-power consumption.

11.2.4.3 Application Curve



V_{diff} close to 0 V, 32768 data points, standard deviation = 1.7 bits,
ENOB (dc) = 16.3 bits

Figure 73. DC Input Histogram

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *18-Bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1mW* (SLAU514).

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12 Power-Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

12.1 Power-Supply Decoupling

Decouple the AVDD and DVDD pins with GND, using individual 1-µF decoupling capacitors placed in close proximity to the pin, as shown in Figure 74.

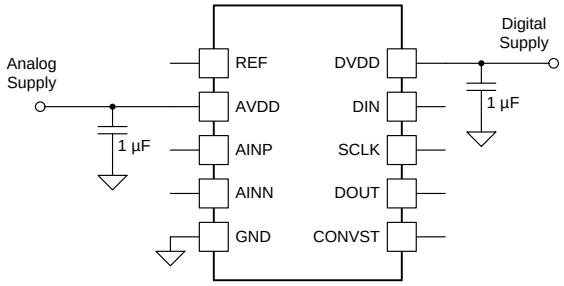


Figure 74. Supply Decoupling

12.2 Power Saving

The device has an auto power-down feature that powers down the internal circuitry at the end of every conversion. Referring to Figure 75, the input signal is acquired on the sampling capacitors when the device is in a power-down state (t_{acq}); at the same time, the result for the previous conversion is available for reading. The device powers up on the start of the next conversion. During conversion phase (t_{conv}), the device also consumes current from the reference source (connected to the REF pin).

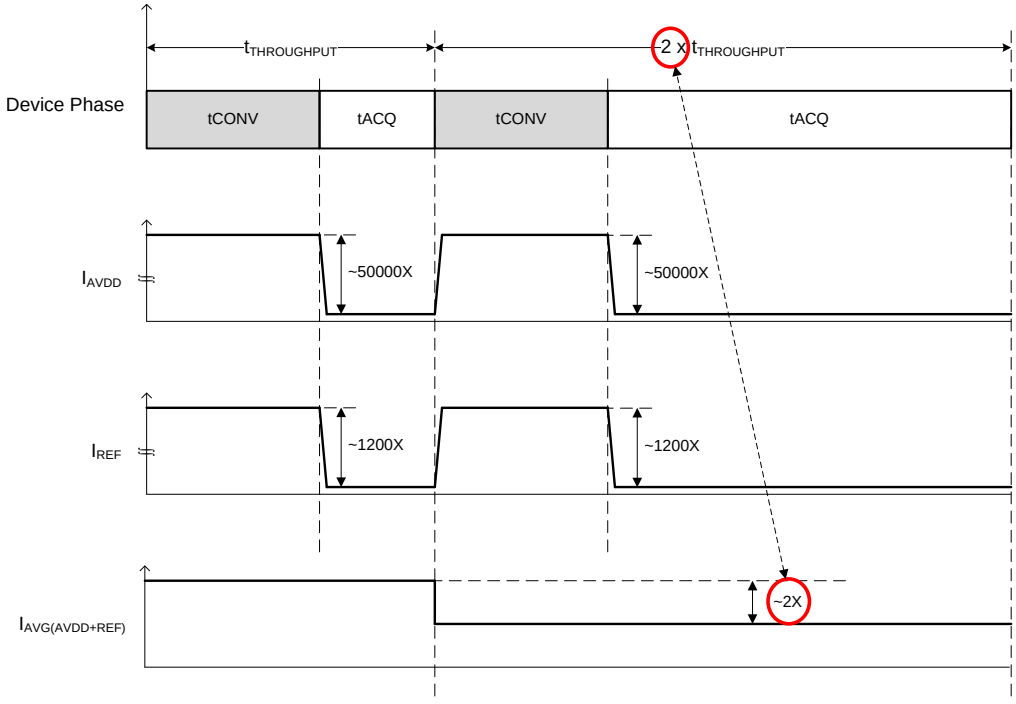


Figure 75. Power Scaling With Throughput

Power Saving (continued)

The conversion time, t_{conv}, is independent of the SCLK frequency. When operating the device at speeds lower than the maximum rated throughput, the conversion time, t_{conv}, does not change; the device spends more time in power-down state. Therefore, as shown in Figure 76, the device power consumption from the AVDD supply and the external reference source is directly proportional to the speed of operation. Extremely low AVDD power-down current (50 nA, typical) and extremely low external reference leakage current (250 nA, typical), make this device ideal for very low throughput applications (such as pulsed measurements).

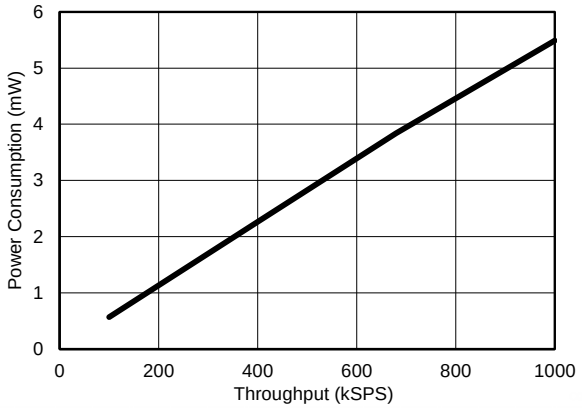


Figure 76. Power Scaling With Throughput

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13 Layout

13.1 Layout Guidelines

Figure 77 shows a board layout example for the device. Appropriate layout that interconnects accompanying capacitors and converters with low inductance is critical for achieving optimum performance. Thus, a PCB board with at least four layers is recommended to keep all critical components on the top layer and interconnected to a solid (low inductance) analog ground plane at the subsequent inner layer using 15-mil vias. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 77, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

As a result of dynamic currents during conversion and data transfer, each supply pin (AVDD and DVDD) must have a decoupling capacitor to keep the supply voltage stable. To maximize decoupling capabilities, inductance between each supply capacitor and the supply pin of the converter is kept less than 5 nH by placing the capacitor within 0.2-inches from the pin and connecting it with 20-mil traces and a 15-mil grounding via, as shown in Figure 77. TI recommends using one 1-μF ceramic capacitor at each supply pin. Avoid placing vias between the supply pin and its decoupling capacitor.

Dynamic currents are also present at the REF pin during the conversion phase and very good decoupling is critical to achieve optimum performance. The inductance between the reference capacitor and the REF pin is kept less than 2 nH by placing the capacitor within 0.1-inches from the pin and connecting it with 20-mil traces and multiple 15-mil grounding vias, as shown in Figure 77. A single, 10-μF, X7R-grade, 0805-size, ceramic capacitor with at least a 10-V rating is recommended for good performance over the rated temperature range. Avoid using additional lower value capacitors because the interactions between multiple capacitors may affect the ADC performance at higher sampling rates. A small, 0.1-Ω to 0.47-Ω, 0603-size resistor placed in series with the reference capacitor (as shown in Figure 77) keeps the overall impedance low and constant, especially at very high frequencies.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

13.2 Layout Example

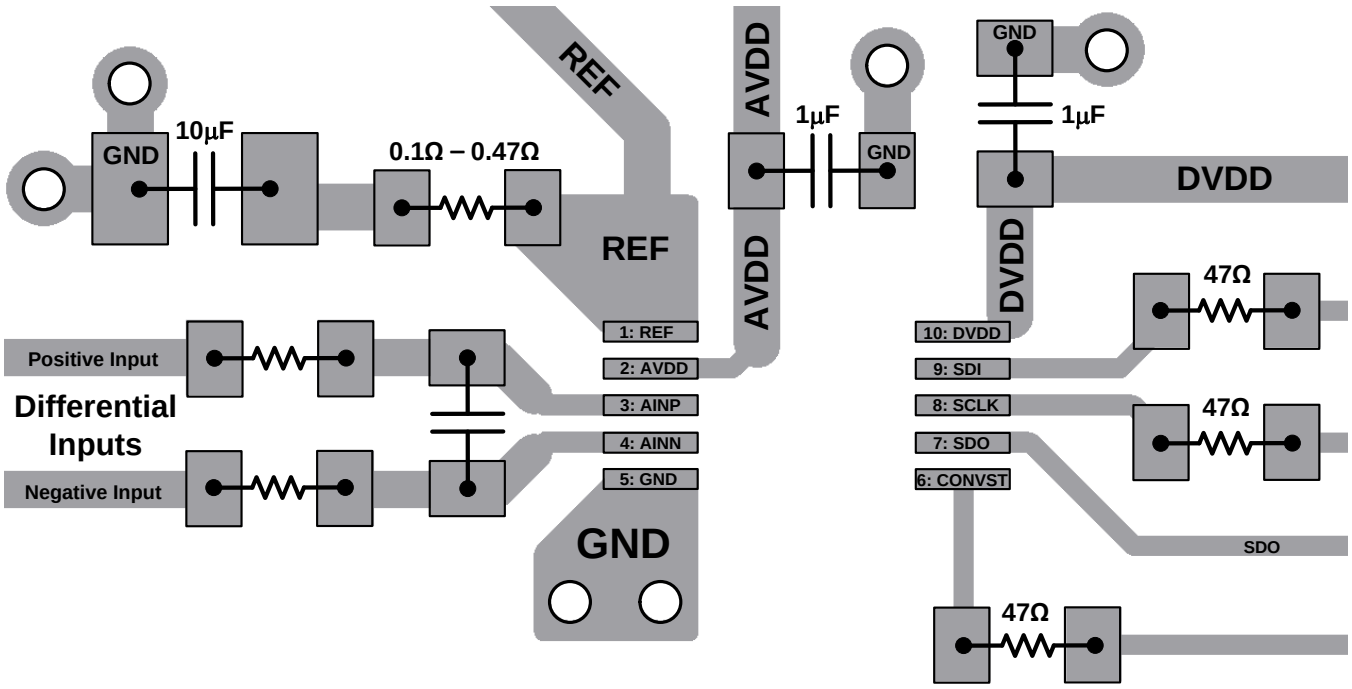


Figure 77. Recommended Layout

14 Device and Documentation Support

14.1 Device Support

14.1.1 Development Support

- Using SAR ADC TINA Models: Static behavior, power scaling
- Using SAR ADC TINA Models: Much ado about settling
- SAR ADC Response Times: Respond quickly, control quickly
- Input Considerations for SAR ADCs

14.2 Documentation Support

14.2.1 Related Documentation

For related documentation see the following:

- *OPAx333 1.8-V, microPower, CMOS Operational Amplifiers, Zero-Drift Series* Data Sheet (SBOS351)
- *THS452x Very Low Power, Negative Rail Input, Rail-To-Rail Output, Fully Differential Amplifier* Data Sheet (SBOS458)
- *THS4281 Very Low-Power, High-Speed, Rail-to-Rail Input and Output Voltage-Feedback Operational Amplifier* Data Sheet (SLOS432)
- *1-MHz, Micro-Power, Low-Noise, RRIO,1.8-V CMOS Operational Amplifier Precision Value Line Series* Data Sheet (SBOS649)
- *OPAx350 High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series* Data Sheet (SBOS099)
- *1.8V, 7MHz, 90dB CMRR, Single-Supply, Rail-to-Rail I/O Operational Amplifier* Data Sheet (SBOS259)
- *18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response* TI Precision Design (TIDU012)
- *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power* TI Precision Design (SLAU513)
- *18 bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1 mW* TI Precision Design (SLAU514)
- *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* TI Precision Design (SLAU515)
- *Ultra Low Power, 18 bit Precision ECG Data Acquisition System* TI Precision Design (SLAU516)
- *ADS8881 IBIS Model* (SBAM172)
- *ADS8881 TINA-TI Reference Design* (SBAM173)
- ADS8881EVM-PDK User's Guide (SBAU211)

14.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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14.5 Trademarks

E2E is a trademark of Texas Instruments.
TINA is a trademark of Texas Instruments Inc..
SPI is a trademark of Motorola Inc.
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14.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8881CDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	Samples
ADS8881CDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	Samples
ADS8881CDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	Samples
ADS8881CDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	8881C	Samples
ADS8881IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	Samples
ADS8881IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	Samples
ADS8881IDRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	Samples
ADS8881IDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8881	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

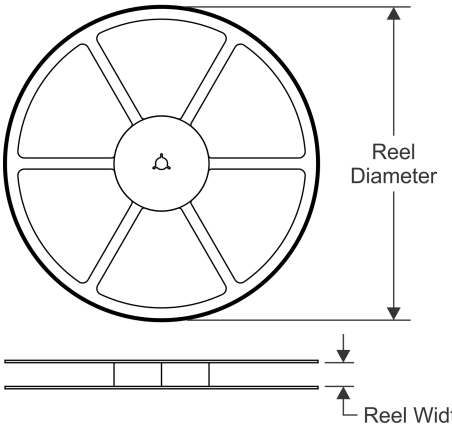
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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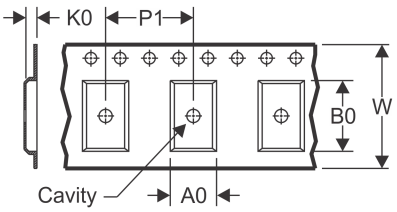
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

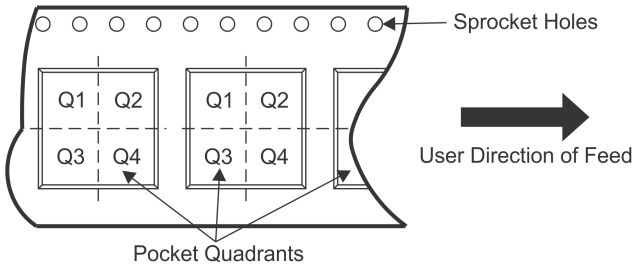


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

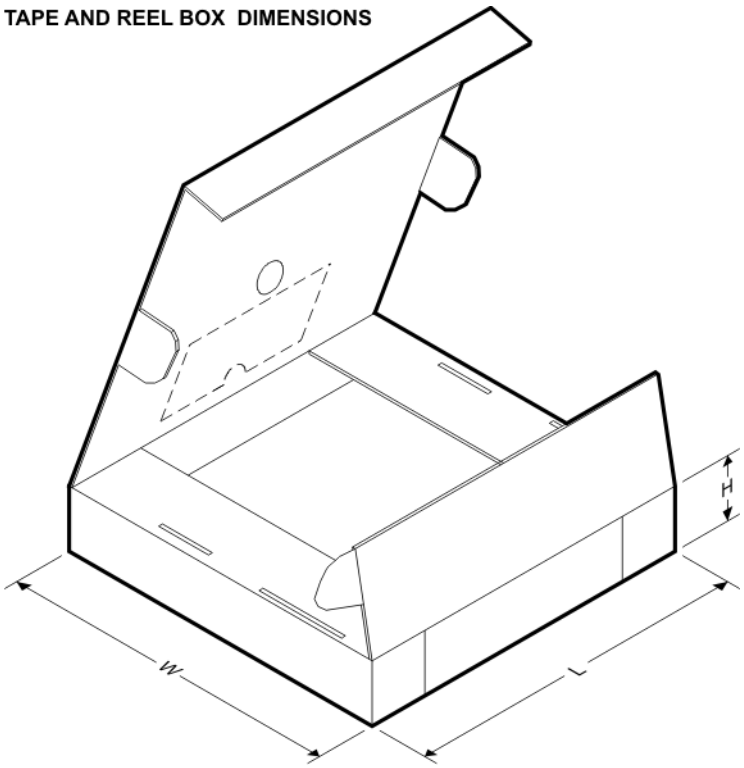
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8881CDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8881CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8881IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8881IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

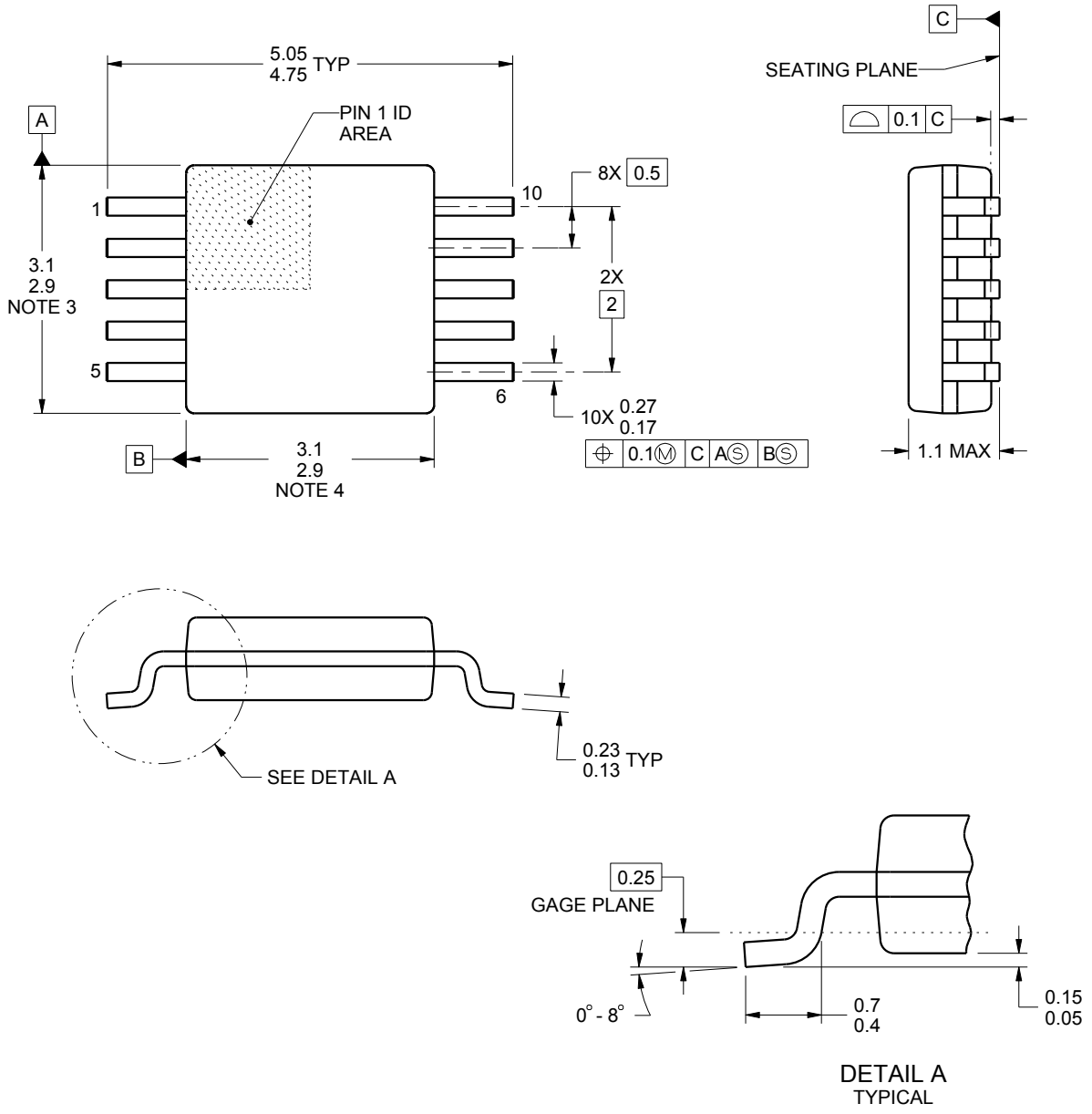
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8881CDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8881CDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8881CDRCT	VSON	DRC	10	250	210.0	185.0	35.0
ADS8881IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8881IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8881IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

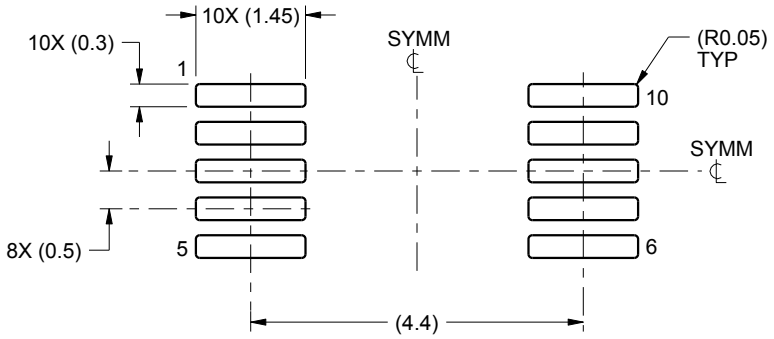
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

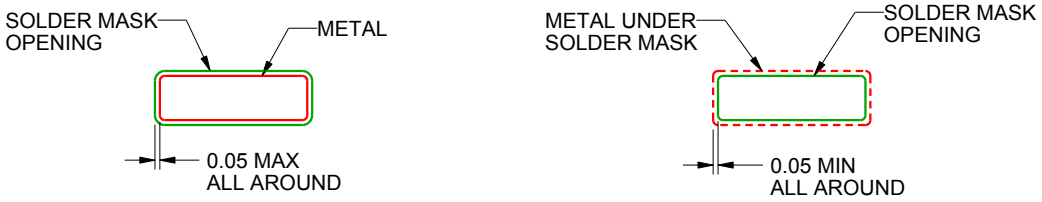


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

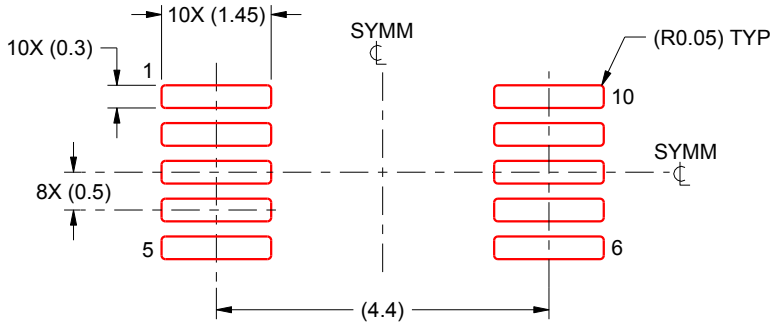


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

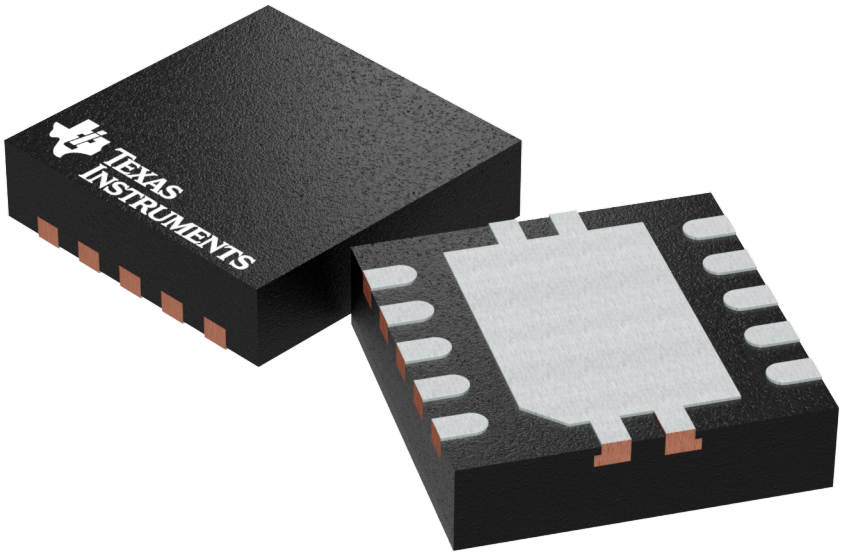
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRC 10

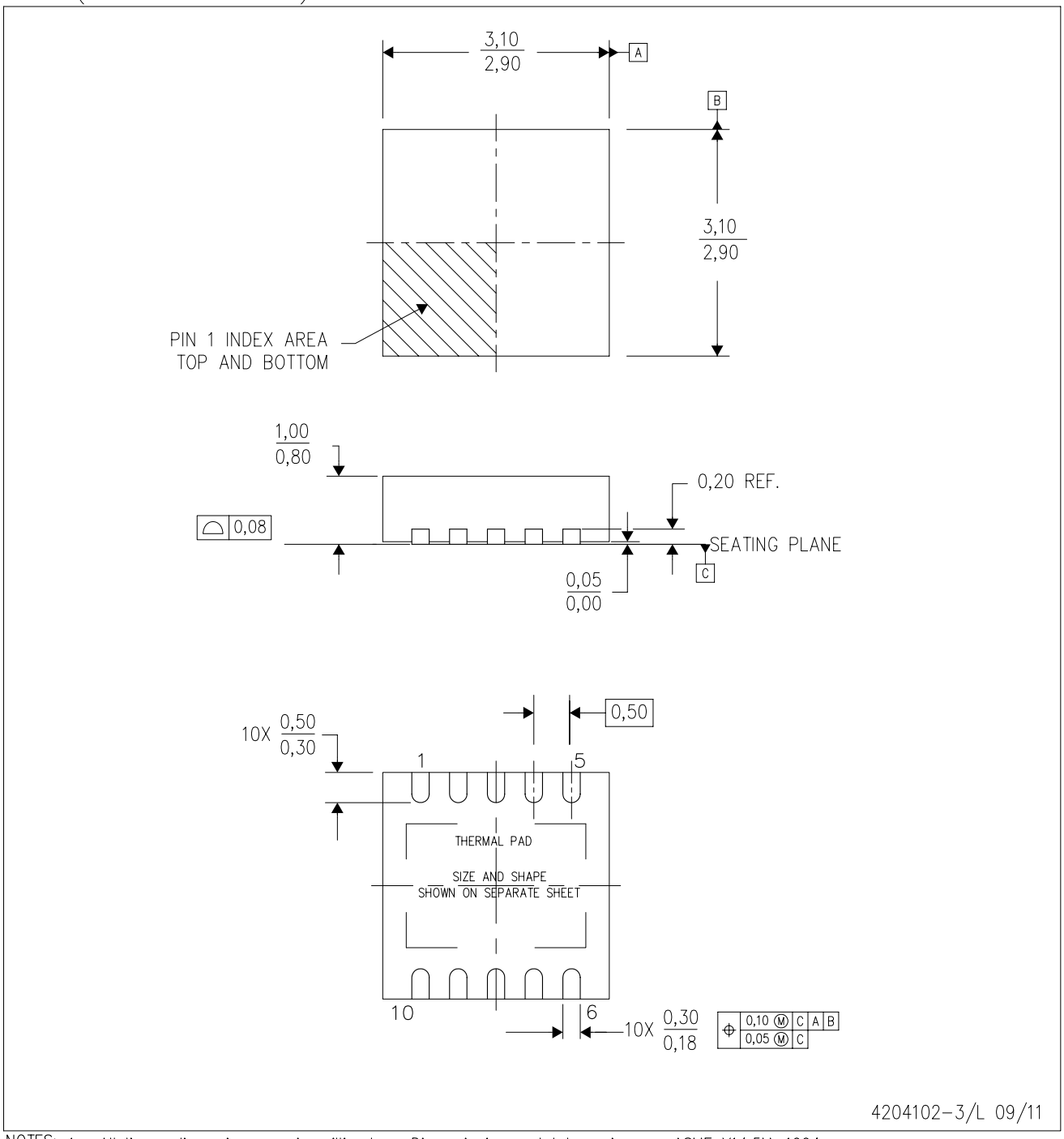
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

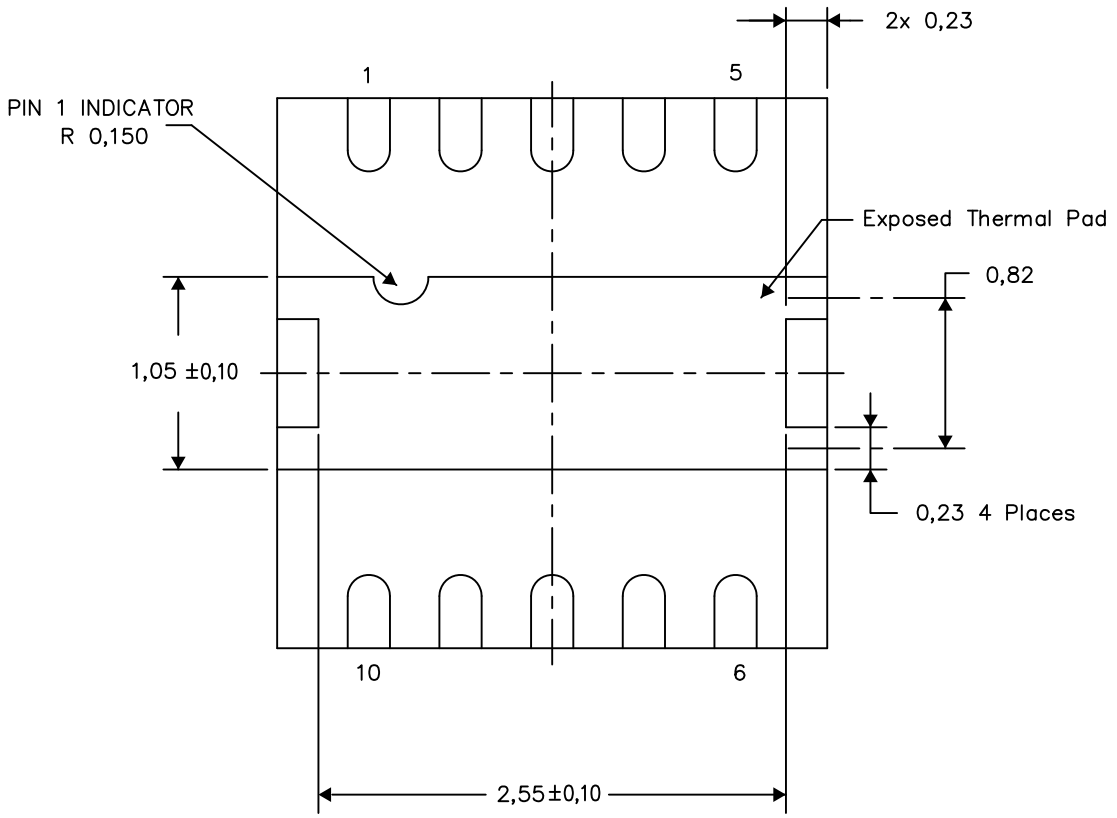
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206565–6/Y 08/15

NOTE: A. All linear dimensions are in millimeters

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