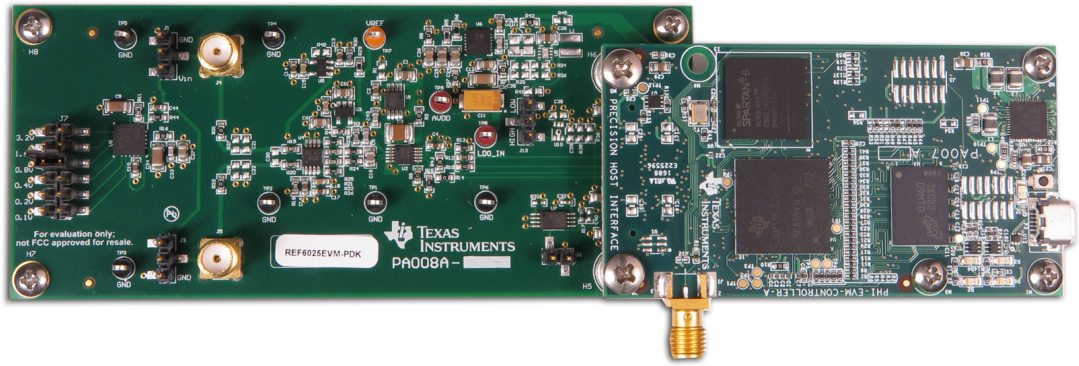
ADS8881EVMV2-PDK User's Guide



This user's guide describes the characteristics, operation, and use of the ADS8881EVMV2 (evaluation module) paired with a TI Precision Host Interface (PHI) Controller. This board is an evaluation platform for the ADS8881 and can also be used to evaluate the REF6045 device. The ADS8881 is an 18-bit true-differential unipolar successive approximation register (SAR) analog-to-digital converter (ADC) with a maximum throughput of 1 MSPs. The device is a very-low-power ADC with excellent noise and distortion performance for AC or DC signals. The REF6045 is a high-precision voltage reference with an integrated high-bandwidth buffer designed specifically to drive the REF pin of a SAR ADC. On this EVM, the REF6045 drives the reference of the ADS8881. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

The PHI eases EVM evaluation using additional hardware and software by providing computer connectivity through the universal serial bus (USB) interface.

The following related documents are available through the Texas Instruments website at www.ti.com.

Related Documentation

Device	Literature Number
ADS8881	SBAS547D
REF6045	SBOS708B
THS4551	SBOS778B
OPA333	SBOS351
OPA320	SBOS513F
LP38798	SNOSCT6
REF5045	SBOS410H
TPS78833	SLVU059

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1 Overview

The ADS8881EVMV2 is a platform that evaluates the performance of both devices onboard: the ADS8881 and the REF6045. The EVM includes all the peripheral circuits and components necessary to demonstrate the performance of the SAR ADC and the voltage reference. When paired with the precision host interface (PHI) controller board and a USB cable to connect to a computer, the capture and analyzation of data is supported.

The PHI board serves three primary functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the required digital input and output signals to communicate with the EVM
- Supplies power to all active circuitry on the EVM board

Along with the ADS8881EVM, an A-to-micro-B USB cable and a *Quick Start* guide is included to aid with system setup

1.1 ADS8881EVMV2 Features

The ADS8881EVMV2 includes the following features:

- Onboard 18-bit, 1-MSPs, serial interface, true-differential input, SAR ADC
- Low-noise and low distortion ADC input drivers optimized to meet ADC performance
- Input common-mode of 2.35 V generated onboard that allows unipolar and bipolar inputs
- Low-noise, low-drift reference (REF6045) with jumper-selectable resistor divider network for DC test signal generation
- Low-dropout (LDO) regulator that provides supply voltages to the ADC and drive circuits

1.2 ADS8881EVMV2-PDK Features

The performance development kit(PDK) includes the following features:

- Hardware and software for diagnostic testing that demonstrates accurate performance evaluation of the ADS8881 SAR ADC and REF6045 voltage reference
- USB powered with no external power supply required
- PHI controller that provides a convenient interface to the EVM over a USB 2.0 (or higher) for power delivery and digital input and output
- Easy-to-use evaluation software for Microsoft Windows 7®, and Windows 8® 64-bit operating systems
- Software suite including graphical tools for data capture, histogram analysis, and spectral analysis (FFT) (The software suite has a provision for exporting data to a text file for post-processing.)

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2 EVM Analog Interface

The ADS8881EVMV2 is designed for easy interfacing to multiple analog sources through SMA connectors that allow input signals through coaxial cables. The jumper connector provides a convenient 4-pin, dual-row resistor divider network combination at JP1 for fixed DC inputs. All analog inputs are buffered by the THS4551 high-speed fully-differential amplifier to properly drive the ADS8881 ADC inputs.

Most SAR ADCs (and a few delta-sigma ADCs) switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. To support this dynamic load and preserve the ADC linearity, distortion, and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx voltage reference family has integrated low-output impedance buffers that enable the user to directly drive the REF pin of a SAR ADC, while preserving the performance of the ADC. The output voltage of the REF60xx does not drop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is extremely useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems.

2.1 ADC Analog Input Signal Path and Options

In Figure 3, the signal path for the differential signal applied at the board inputs is shown. The board input impedance is 1-kΩ with 10-nF differential filtering that keeps noise in external cabling common. The overall signal path bandwidth is limited to 1.6 MHz by the charge kickback filter formed from 4.99-Ω resistors and a 10-nF capacitor between the amplifier output and ADC input.

The ADS8881EVMV2 uses the THS4551 fully-differential amplifier to drive the ADC input. The THS4551 is a very-low-power, fully-differential op amp with rail-to-rail output and an input common-mode range that includes the negative rail. The amplifier is designed for low-power data acquisition systems where power dissipation is a critical requirement. The amplifier provides exceptional AC performance that meets the very low distortion and high slew rate required from the input driver.

The ADS8881EVMV2 is designed for easy interfacing to multiple analog sources through SMA connectors allowing for input signals through coaxial cables. 100-mil headers provide a convenient option to connect an external analog source or the configurable onboard DC source. This DC source is provided through a convenient 4-pin, dual-row resistor divider network combination at JP1. All analog inputs are buffered by the THS4551 high-speed fully-differential amplifier to drive the ADS8881 ADC inputs. Use appropriate caution when handling these pins.

Table 1 lists the analog inputs.

Table 1. Analog Input Options on the ADS8881EVMV2

Pin Number	100-mil Header	Signal	Description
J1	JP3.2	AIN(–)	Negative differential input. Ground this pin for single-ended signals.
J2	JP2.2	AIN(+)	Positive differential input or input for single-ended signals

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2.2 Differential Input Signal Configuration

The ADS8881 can convert differential signals with a common-mode between 0 V and V_{REF}, but the THS4551 can condition a bipolar signal by changing the common-mode. This board sets the THS4551 output common-mode to 2.35 V, which corresponds to V_{REF} / 2 + 0.1 V. As a result, when a bipolar differential signal with a common-mode of 0 V is applied at the A0(–) and A0(+) EVM inputs, the THS4551 shifts the common-mode to 2.35 V. Figure 1 illustrates an input signal of 2.5-V differential with 0-V common-mode (where the common-mode is changed from 0 V to 2.35 V) to present a 5-V differential signal, while maintaining a 100-mV headroom from the amplifier power rails in order to provide linear operation.

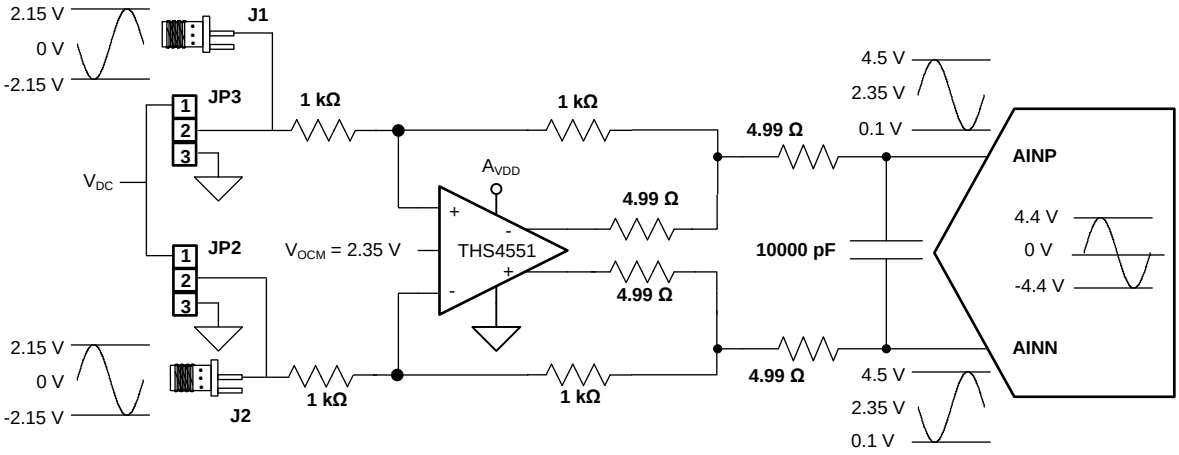

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Figure 1. Differential Input Example

2.3 Single-Ended Signal Configuration

The ADS8881 can only convert single-ended signals between 0 V and V_{REF}. The THS4551 can condition a single-ended signal to a differential signal, which allows for a larger input voltage range to the EVM input AIN(+) .The THS4551 can condition a single-ended input signal to a differential signal allowing a 0 V to 5 V or –2.5 V to 2.5 V input voltage range at the A0(+) EVM input. The EVM AIN(–) input must be grounded for single-ended signals, which can be accomplished by inserting a shunt from JP3.2 and JP3.3, as shown in Figure 2.

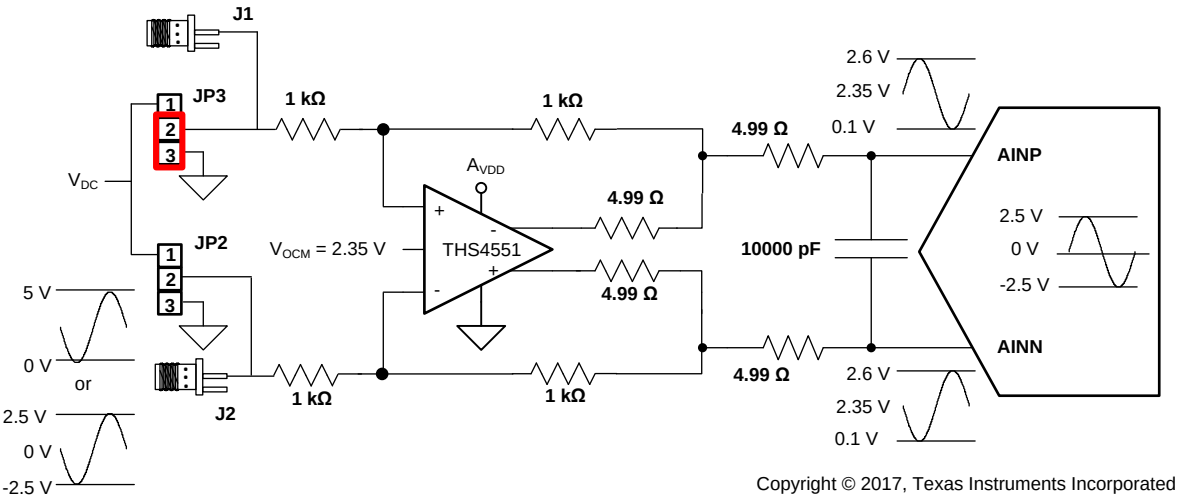

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Figure 2. Single-Ended Signal Example

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2.4 Onboard DC Input Configuration

This EVM includes the low-noise, low drift user-configurable REF6045 reference that can generate DC voltages at the inputs of the THS4551 without requiring an external source.

The resistor divider network includes a set of four fixed DC voltages that can be configured through JP1 jumper pins. By inserting a single shunt on the JP1 header, the DC voltage is divided down to the output, as listed in Table 2.

Table 2. DC Input Configuration

V_{DC} (in Volts)	Close
0.1	JP1.1 – JP1.2
2.5	JP1.3 – JP1.4
3.5	JP1.5 – JP1.6
4.4	JP1.7 – JP1.8

CAUTION

Make sure that the DC voltage provided at the input of the THS4551 never exceeds the 4.5 V_{REF} set by REF6045. To avoid damaging the ADS8881, strictly use the jumper combinations listed in Table 2.

3 Onboard Voltage ADC Reference

Since the circuitry is powered by a 5-V supply, the reference voltage must be less than 5 V. The REF6045 generates the 4.5-V reference for the ADS8881. Unlike typical ADC reference configurations, this EVM does not require any additional active circuitry to drive the ADC reference, since the reference input signal path is entirely self-contained on the REF6045. Figure 3 illustrates the schematic.

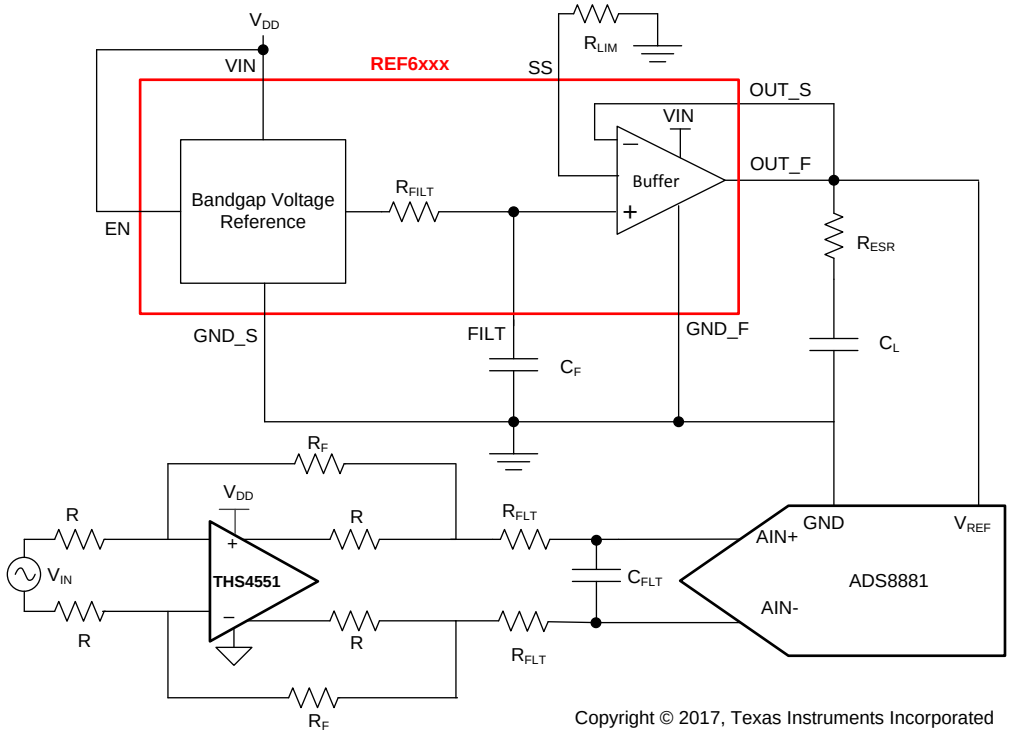

Figure 3. ADS8881EVMV2 Schematic Block Diagram

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4 Power Supplies

The PHI provides multiple power supplies to the EVM that are derived from the USB supply of the computer.

The EEPROM and the digital section of the ADC are powered by two separate 3.3-V supplies generated directly by the PHI. The REF6045 and analog input drive circuits are powered by the 5 V generated by the LP38798 onboard the EVM, which is a low-noise linear regulator that uses the 5.5-V supply out of a switching regulator on the PHI to generate a cleaner 5-V output. The TPS78833 on the EVM generates the 3.3-V supply for the ADC.

The power supply for each active component on the EVM has a ceramic bypassed capacitor placed close to the component. The EVM layout uses thick traces or large copper fill areas whenever possible between bypass capacitors and the loads that minimize inductance along the load current path.

5 ADS8881EVMV2 Initial Setup with PHI

This section explains the initial hardware and software setup procedure that must be completed for the proper operation the ADS8881EVMV2 paired with the PHI.

5.1 Default Jumper Settings

When unpacking, the EVM must not have any jumper shunts installed. This is the correct setting for the standard DC and AC tests that are conducted on the EVM.

5.2 EVM Graphical User Interface (GUI) Software Installation

The EVM GUI that is required to power up and evaluate the performance of the EVM must be installed on the user's computer. This software is designed to be used with the PHI paired with the EVM. Download the latest version of the installer online from the *Software* section of the ADS8881EVM product folder.

The workstation that is used for the installation must be a Windows 7 or Windows 8 64-bit computer, with USB 2.0 (or higher) ports, and have 1 GB of hard disk space available. Log in with an administrator account and make sure the installation is run as administrator. Read and accept the license agreements and follow the on-screen instructions to complete the installation as shown in Figure 4.

CAUTION

Manually disable any anti-virus software running on the computer before running the EVM GUI installer. Depending on the anti-virus settings, an error message may appear or the installer .exe file may be deleted.

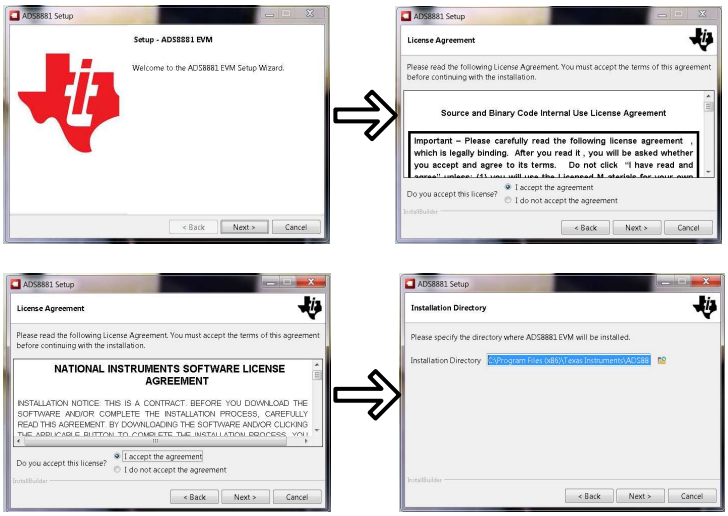

Figure 4. ADS8881 Software Installation Prompts

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As a part of the ADS8881EVM GUI installation and shown in Figure 5, a prompt with a *Device Driver Installation* appears on the screen. Click *Next* to proceed.

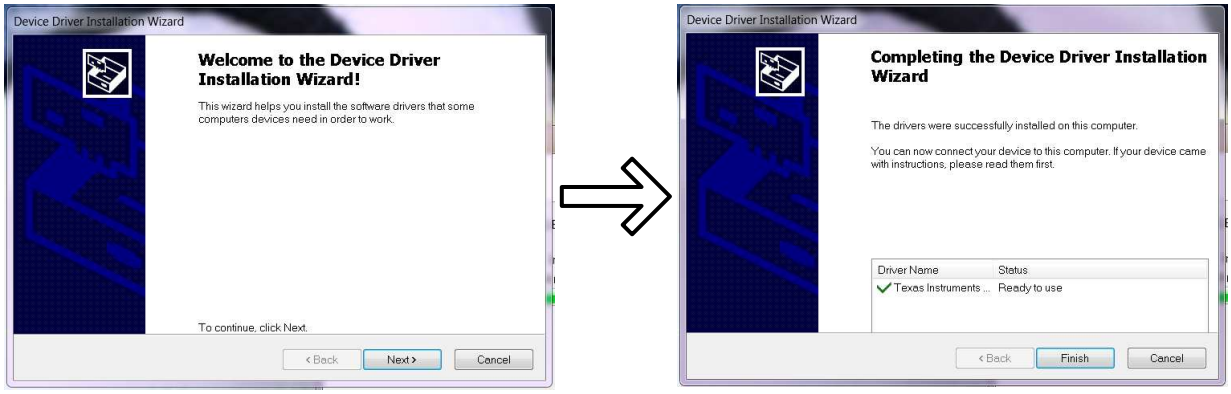

Figure 5. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that "Windows cannot verify the publisher of this driver software". Select *Install this driver software anyway*.

This software requires NI LabVIEW™ run-time engine and may prompt for the installation of this software if it is not already installed. At the end of these installations, make sure that the *Create Desktop Shortcut* and *Run ADS8881 EVM* options are selected, as shown in Figure 6.

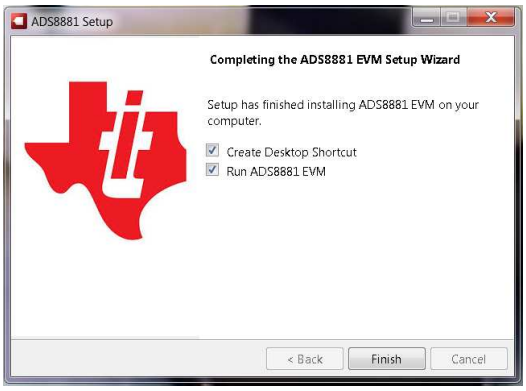

Figure 6. ADS8881EVM GUI Installation Final Step

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6 ADS8881EVMV2 Operation

The following instructions are a step-by-step guide to connecting the ADS8881EVMV2 to the computer and evaluating the performance of the devices:

1. Connect the ADS8881EVMV2 to the PHI. Install the two screws as shown in Figure 7.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI starts blinking, which indicates that the PHI is booted up and is attempting to communicate with the PC. The resulting LED indicators are shown in Figure 7.

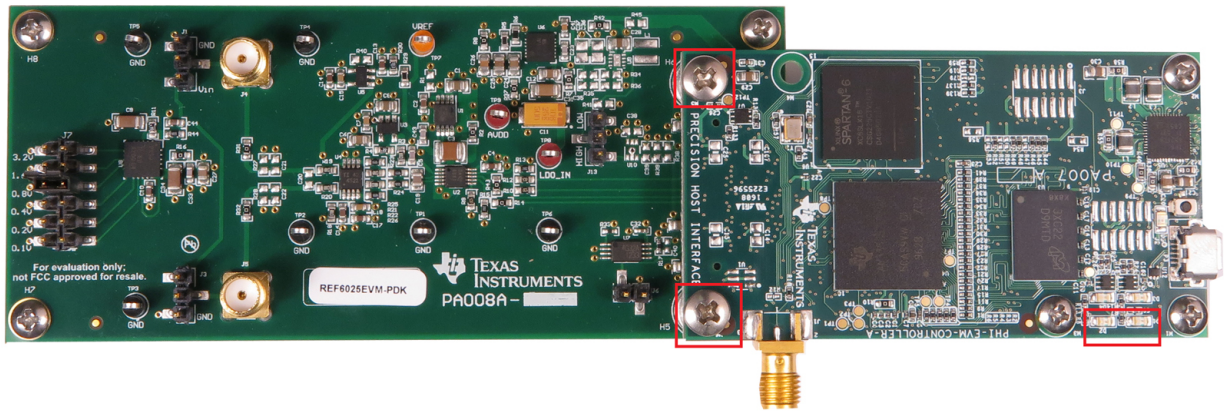

Figure 7. EVM Hardware Setup and LED Indicators

3. Launch the ADS8881EVM GUI software, as shown in Figure 8. The rate at which LED D2 blinks slows down, indicating that the GUI is successfully communicating with the ADS8881EVMV2.

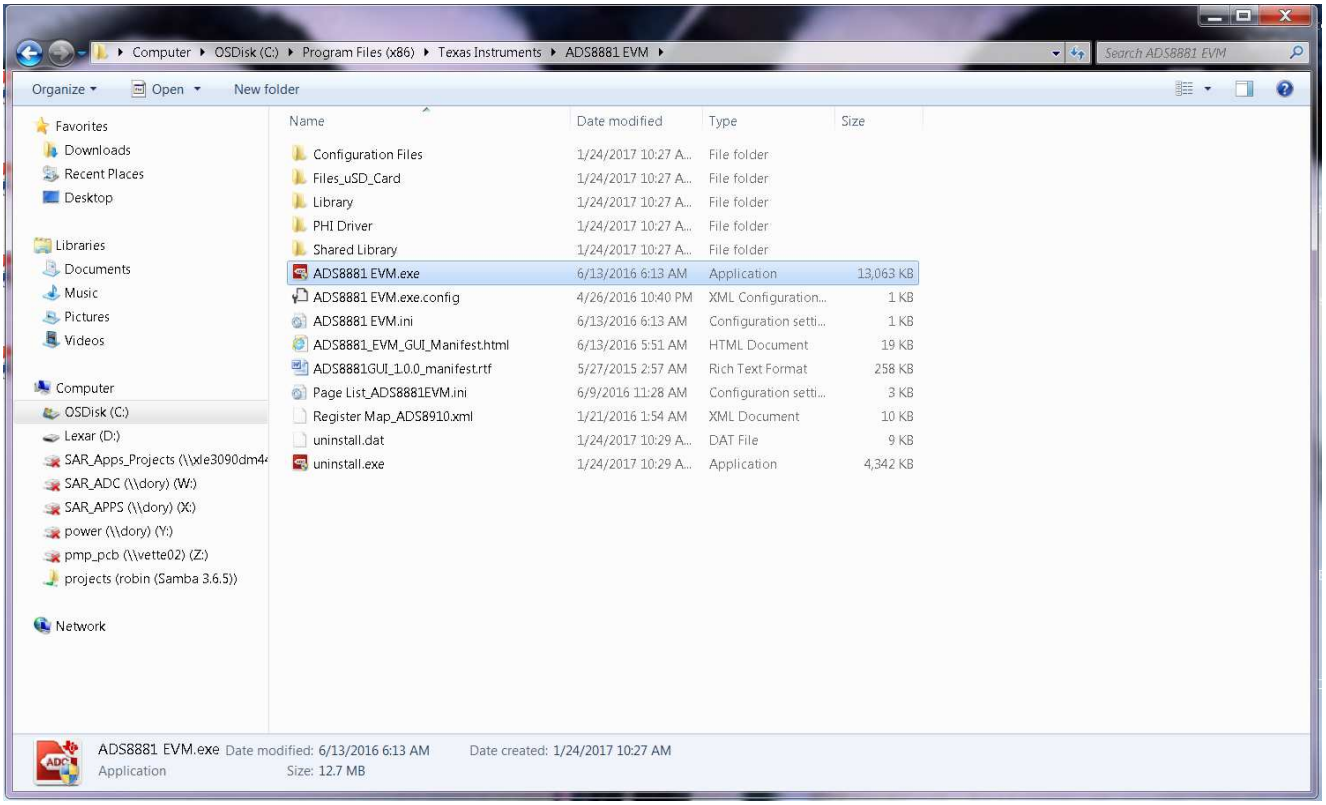

Figure 8. Launch the EVM GUI Software

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6.1 EVM GUI Global Settings for ADC Configuration and Data Capture

The ADS8881EVM GUI provides high-level control over the ADS8881 functions including interface modes, sampling rate, and the number of samples to capture. With the ADS8881EVM GUI, the performance of the REF6045 under different ADC operating conditions can be evaluated.

Figure 9 identifies the input parameters of the GUI and default values so the ADS8881 can function. These are global settings that persist across the GUI tools listed in the top left pane (or from one page to another).

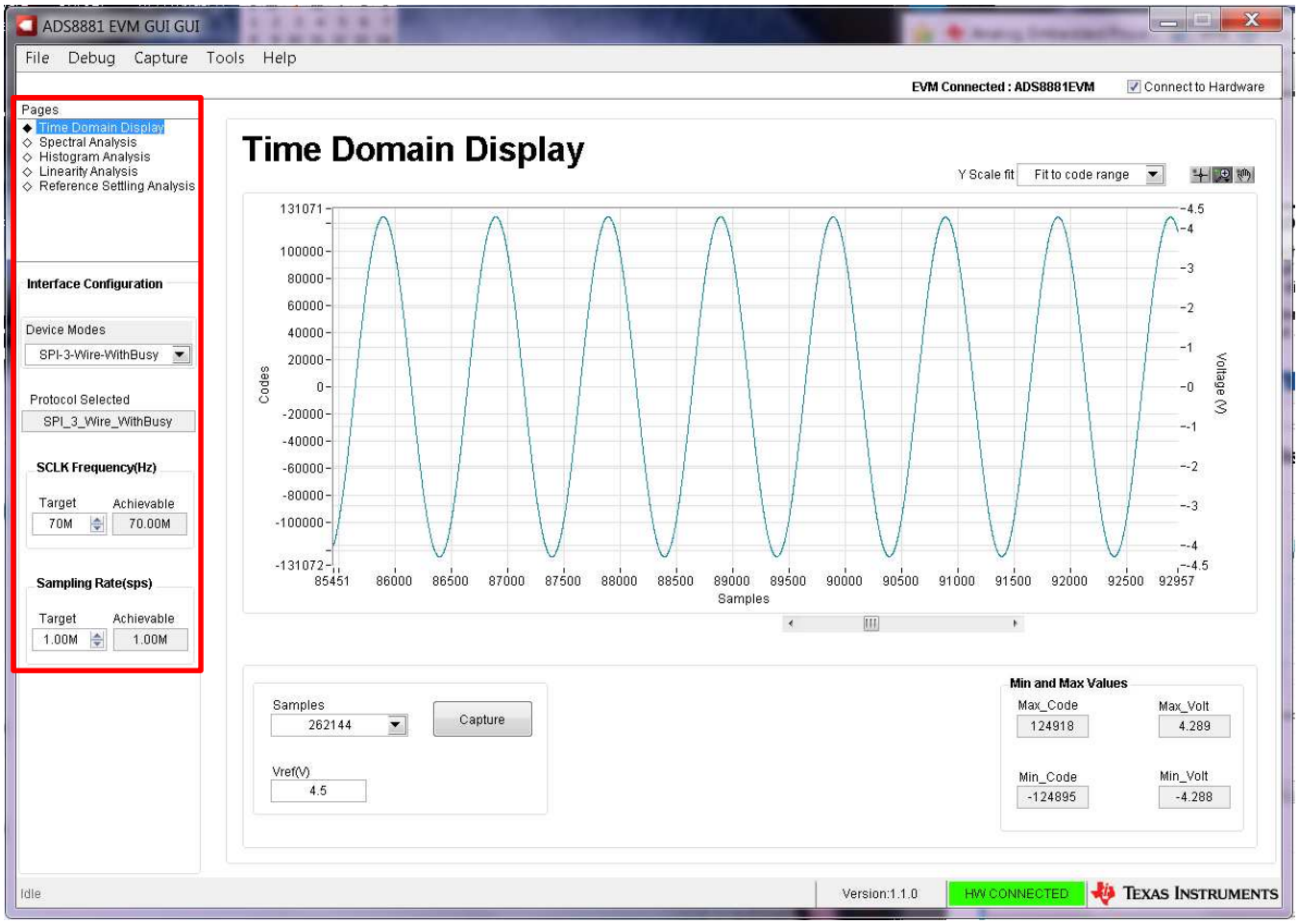

Figure 9. EVM GUI Global Input Parameters

The host configuration options in this pane allow user-configuration of the host interface of the ADS8881. In this pane, *SCLK Frequency(Hz)* and *Sampling Rate(sps)* can be selected. Using either of these two parameters, the GUI computes the best achievable values and considers the timing constraints of the selected device mode.

A target SCLK frequency (in Hz) can be specified and the GUI changes the PHI PLL settings to attempt to match this as closely as possible. The achievable frequency may differ slightly from the selected target value. Similarly, the sampling rate of the ADC can be adjusted by modifying the target sampling rate argument (in Hz). The achievable ADC sampling rate may differ from the target value depending on the applied SCLK frequency and the closest match that is displayed.

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6.2 Time Domain Display Tool

The *Time Domain Display* tool allows visualization of the ADC response to a given input signal. This tool is useful for studying the behavior of the ADC and to debug any gross problems with the ADC, input drive, or reference circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS8881 (as per the host configuration settings) using the capture button as shown in Figure 10. The sample indices are on the x-axis, and the two y-axes show the corresponding output codes and the equivalent analog voltages based on the reference voltage driven by the REF6045. Switching pages to any of the analysis tools shown in Section 6.3 and Section 6.4 triggers calculations that are performed on the same set of data.

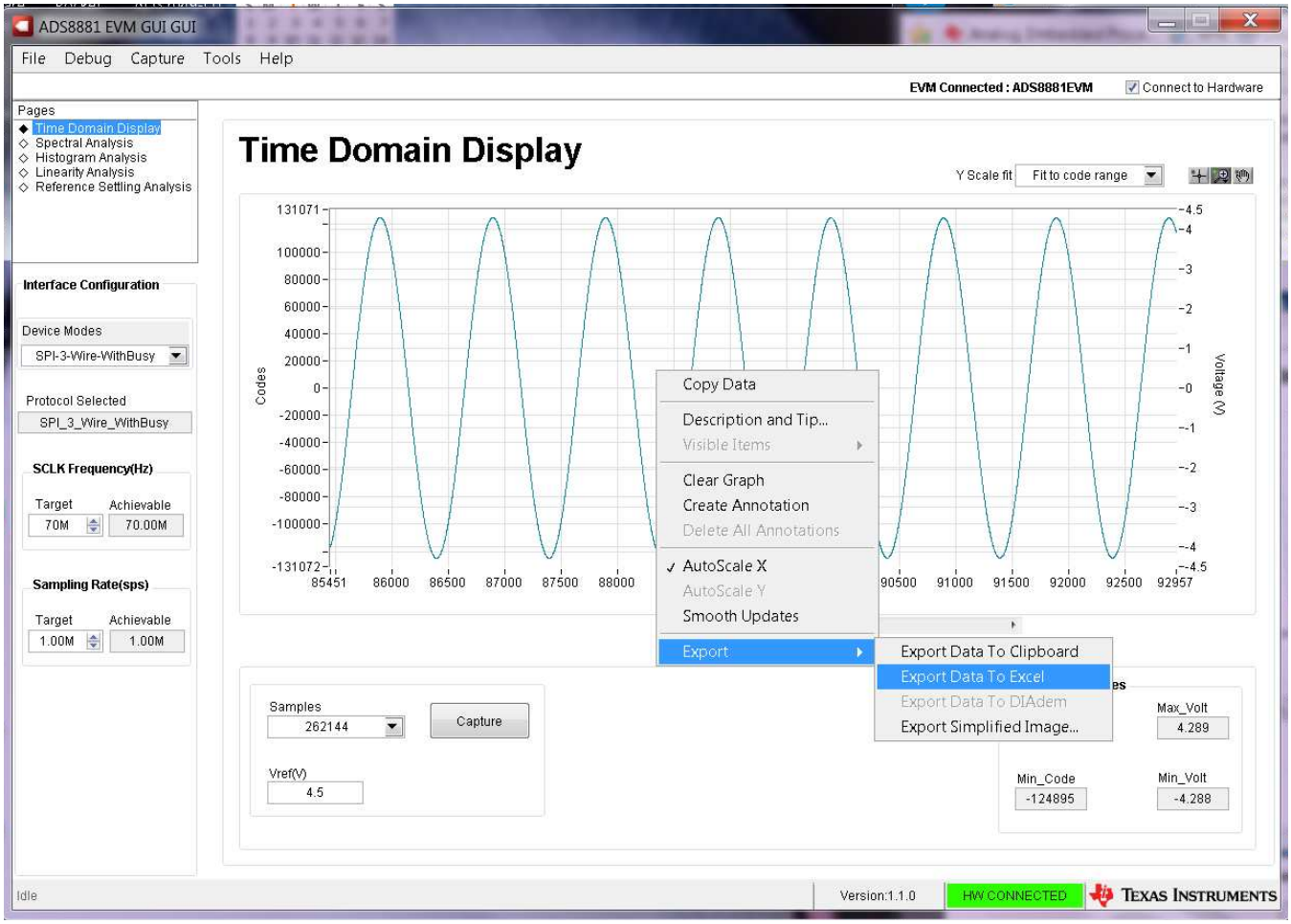

Figure 10. Time Domain Data Capture with Data Export Option

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6.3 Spectral Analysis Tool

The spectral analysis tool helps evaluate the dynamic performance of the ADS8881EVM through FFT analysis of the ADC output for time-varying inputs and computation of key dynamic range metrics (such as SNR, THD, SFDR, SINAD, and ENOB).

The expected ADC input is a sinusoidal signal of peak-to-peak amplitude close to the ADC full-scale input range (FSR). The RMS power of the input signal normalized to FSR is shown in the *signal power* (dB) field in Figure 11, and must be approximately –0.5 dBFS (or approximately 95% × FSR) to avoid input clipping.

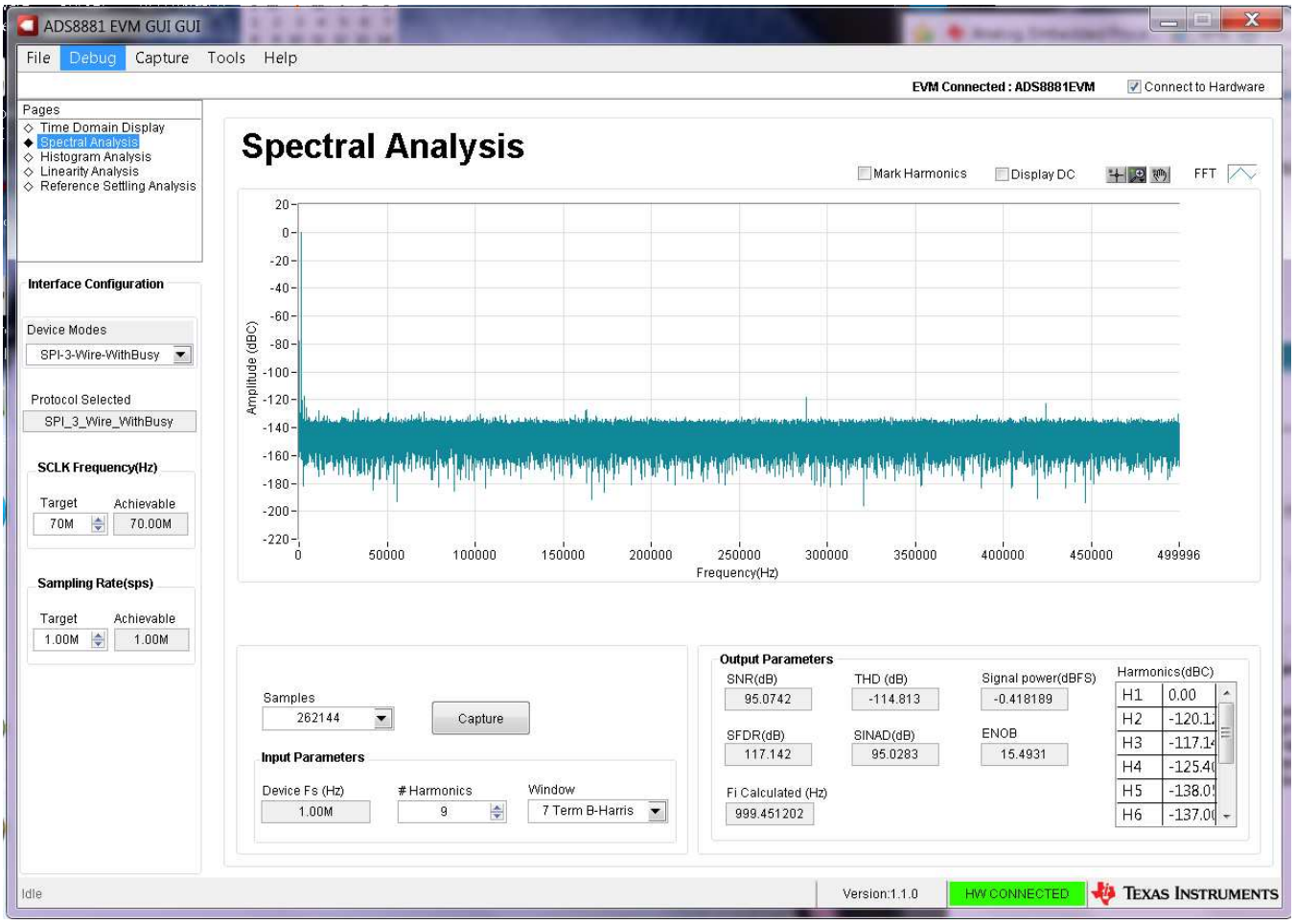

Figure 11. Spectral Analysis Tool

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling. (This discussion is beyond the scope of this document.) The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to the absence of a windowing function or using a rectangular window. TI does not recommend using this option.

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6.4 Histogram Tool

Noise degrades ADC resolution, and the histogram tool can estimate *effective resolution*. *Effective resolution* indicates the number of bits of ADC resolution losses resulting from noise that is generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram. The histogram is obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking on the **Capture** button as Figure 12 shows:

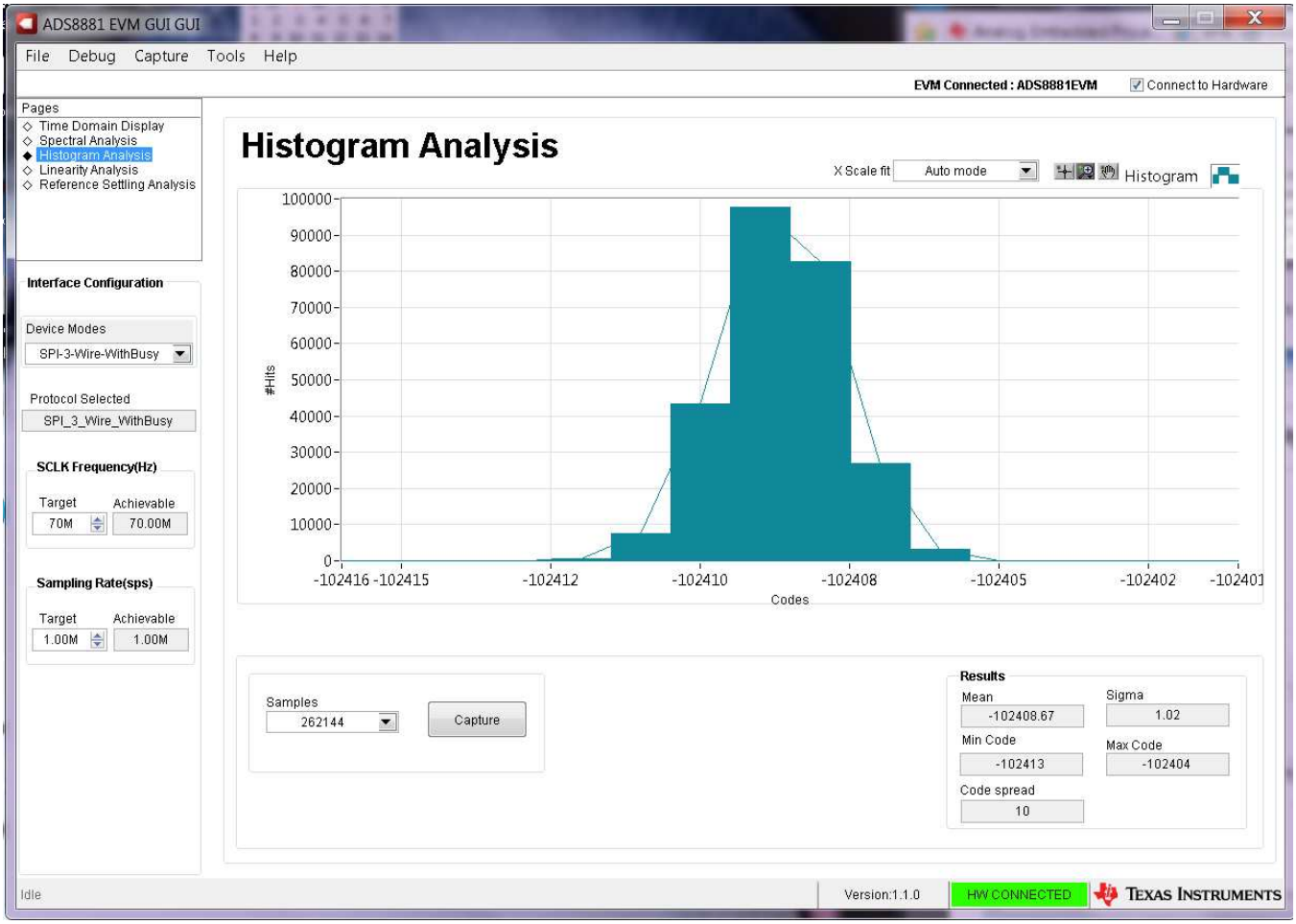

Figure 12. Histogram Analysis Tool

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6.5 Linearity Analysis Tool

The linearity analysis tool (see Figure 13) measures and generates the DNL and INL plots over code for the ADS8881. A 2-kHz sinusoidal input signal is required, which is slightly saturated (35 mV outside the full-scale range at each input or 0.13 dBFS) with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 3

Table 3. External Source Requirements for ADS8881 Evaluation

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Balanced differential
External source common-mode	0 V or floating
External source impedance (R_S)	10 Ω – 30 Ω
External source differential impedance (R_{S_DIFF} = 2 × R_S	20 Ω – 60 Ω
Source differential signal (V_{PP} amplitude for –0.1 dBFs)	(2 × R_S × 4.57 × 10^{-3}) + 9.14 V or (R_{S_DIFF} × 4.57 × 10^{-3}) + 9.14 V
Maximum noise	30 μV_{RMS}
Maximum SNR	100 dB
Maximum THD	–130 dB

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The number-of-hits setting depends on the external noise source. For a 110-dB SNR external source with approximately 10 µVrms of noise, the total number of hits must be 512. For a source with 100-dB SNR, TI recommends 1024 hits.

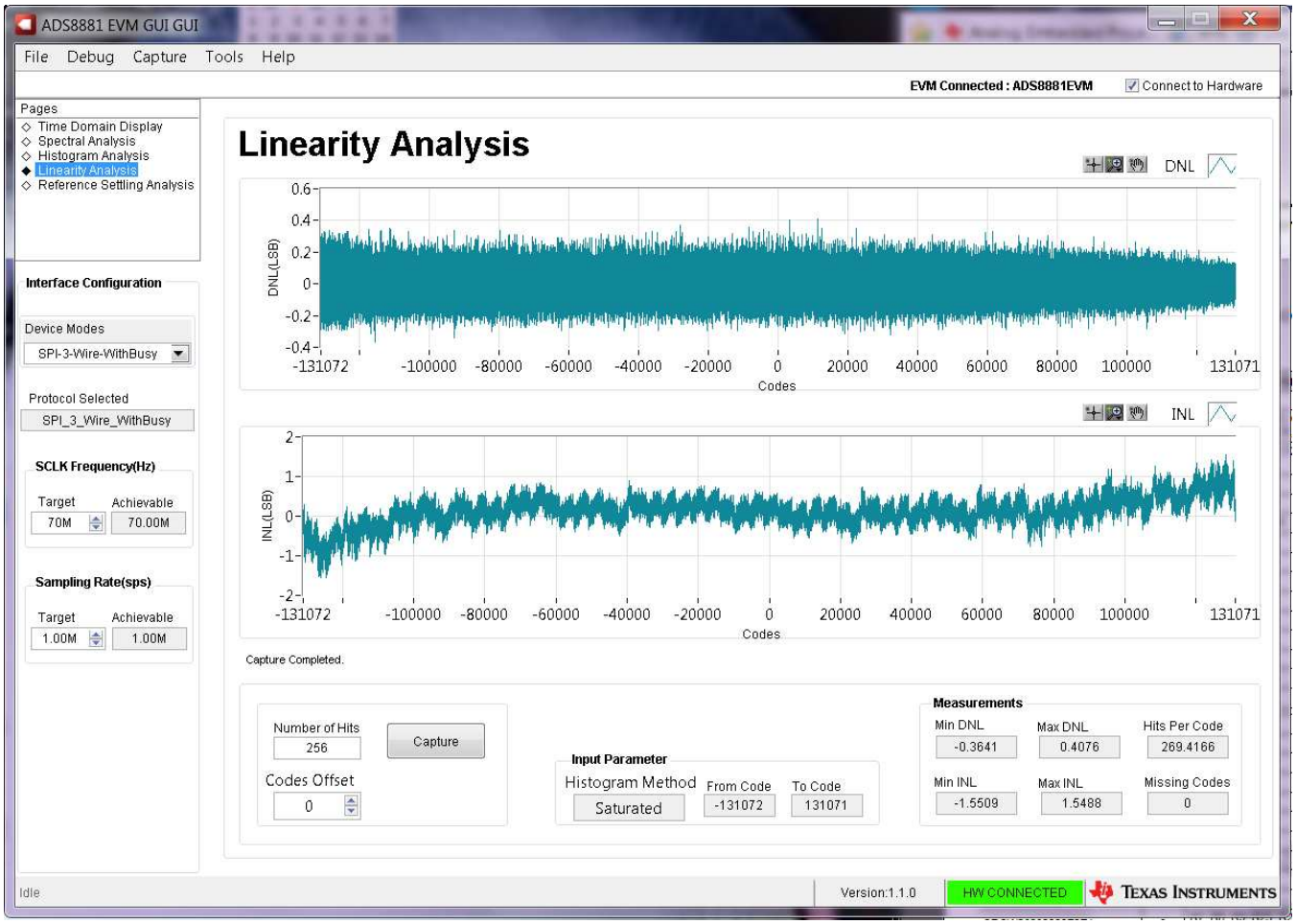

Figure 13. Linearity Analysis Tool

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6.6 Reference Settling Analysis

The ADS8881EVMV2 has the REF6045 driving the ADS8881 reference pin. The REF6045 has an integrated high-band-width buffer that is optimized to drive the reference pin of the ADC at the maximum possible load presented by the ADC. The REF6045 helps maintain the ADC reference within 1 LSB of the nominal voltage during burst mode of data conversion. This requirement applies from the first sample captured in each burst. The Reference Settling tool, as shown in Figure 14, helps showcase this performance of the ADC. Provide a low-noise DC differential input to the ADC. Set the parameters for the Reference Settling test. The various test parameters are:

- Samples: This parameter defines the number of consecutive samples to be captured in a single burst.
- Min Interset Delay (ms): This parameter defines the time interval between two consecutive bursts. No ADC conversion activity takes place during this time.
- Number of sets to average: This parameter defines number of bursts to capture that are averaged to arrive at the Reference Settling number.
- Initial samples to ignore: This parameter defines the number of samples to ignore in each burst from the beginning.

The tool captures the defined number of burst captures and performs the vertical averaging on the burst mode data. The difference between maximum and minimum codes from the averaged data defines the Reference Settling error.

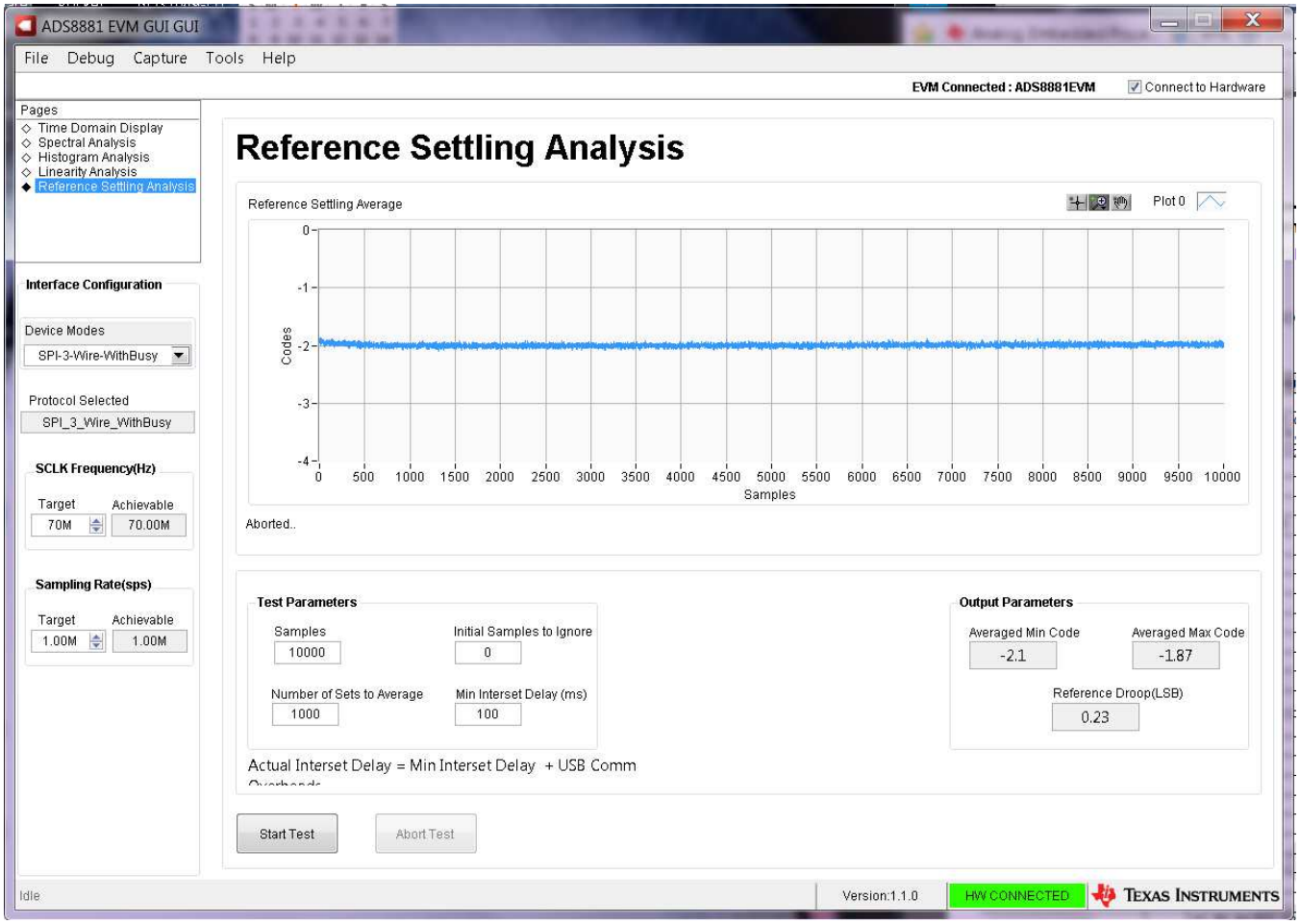

Figure 14. Reference Settling Tool

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7 Pairing With Precision Signal Injector EVM

The AC and DC performance of the ADS8881EVMV2 may be assessed using any signal generator capable of generating a test tone as listed in Table 3.

The Precision Signal Injector Evaluation Module (PSIEVM) facilitates the evaluation of single-ended, differential, and high-voltage SAR analog-to-digital converters by generating a very low distortion, low-noise signal. This signal generator is powered and controlled by the USB port through LabVIEW software.

The PSIEVM can be paired with the ADS8881EVMV2 and PHI to easily evaluate the AC and DC performance of the ADS8881EVMV2.

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8 Bill of Materials, PCB Layout, and Schematics

This section contains the Table 4, PCB layout, and the EVM schematics.

8.1 Bill of Materials

Table 4 lists the ADS8881EVMV2 BOM.

Table 4. ADS8881EVMV2 Bill of Materials

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
PA008	1	!PCB	Any	Printed Circuit Board
GRM21BR71A106KE51L	11	C1, C13, C17, C23, C28, C31, C36, C37, C38, C39, C40	Murata	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805
GRM188R71A105KA61D	9	C3, C4, C5 C10, C12, C15, C18, C22, C26	Murata	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603
GRM32ER71A476KE15L	1	C24	Murata	CAP, CERM, 47uF, 10V, +/-10%, X7R, 1210
GRM188R71E102KA01D	2	C19, C32	MuRata	CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0603
C0603X104K3RACTU	4	C6, C11, C14, C16	Kemet	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603
GCM31CR70J226KE23L	1	C2	Murata	CAP, CERM, 22uF, 6.3V, +/-10%, X7R
593D106X9025C2TE3	1	C29	Vishay-Sprague	CAP, TA, 10uF, 25V, +/-10%, 0.45 ohm, SMD
C0805C103F1GACTU	1	C20	Kemet	CAP, CERM, 0.01uF, 100V, +/-1%, C0G/NP0, 0805
C1608C0G1E103J	2	C7, C8, C9	TDK	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603
GRM21BR71C475KA73L	1	C27	Murata	CAP, CERM, 4.7uF, 16V, +/-10%, X7R, 0805
0805ZC105KAT2A	1	C25	AVX	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0805
GRM188R71E103KA01D	2	C21, C33	MuRata	CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0603
GMK316AB7106KL	1	C30	Taiyo Yuden	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206
GRM155R71E104KE14 D	2	C34,C35	TDK	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0402
1891	4	H7, H8, H9, H10	Keystone	3/16 Hex Female Standoff
9774050360R	2	H3, H4	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
PMSSS 440 0025 PH	4	H1, H2, H5, H6	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
RM3X4MM 2701	2	H11, H12	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
TSW-103-07-G-S	2	JP2, JP3	Samtec	Header, 100mil, 3x1, Gold, TH
QTH-030-01-L-D-A	1	J3	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
5-1814832-1	2	J1, J2	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
TSW-102-07-G-S	1	JP4	Samtec	Header, 100mil, 2x1, Gold, TH
TSM-104-01-L-DV	1	JP1	Samtec	Header, 2.54mm, 4x2, Gold, SMT
THT-14-423-10	1	LBL1	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
CRCW06030000Z0EA	9	R7, R8, R9, R25, R29, R30, R31, R33, R38	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
CRCW060310R0FKEA	1	R22	Vishay-Dale	RES, 10.0, 1%, 0.1 W, 0603
ERJ-3RQFR22V	2	R18, R24	Panasonic	RES, 0.22 ohm, 1%, 0.1W, 0603

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Table 4. ADS8881EVMV2 Bill of Materials (continued)

Manufacturer Part Number	Qty	Reference Designators	Manufacturer	Description
CRCW060347K5FKEA	1	R32	Vishay-Dale	RES, 47.5 k, 1%, 0.1 W, 0603
CRCW060315K0FKEA	1	R34	Vishay-Dale	RES, 15.0 k, 1%, 0.1 W, 0603
RC0603FR-0747RL	3	R27, R36, R37	Yageo America	RES, 47.0, 1%, 0.1 W, 0603
ERJ-3RSFR10V	1	R16	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
CRCW060320K0FKEA	2	R28, R35	Vishay-Dale	RES, 20.0 k, 1%, 0.1 W, 0603
CRCW040210K0FKED	2	R39, R41	Vishay-Dale	RES, 10.0k ohm, 1%, 0.063 W, 0402
CRCW06031K00FKEA	5	R12, R13, R14, R16, R17	Vishay-Dale	RES, 1.00k ohm, 1%, 0.1 W, 0603
CRCW06034R99FKEA	4	R19, R20, R42, R43	Vishay-Dale	RES, 4.99, 1%, 0.1 W, 0603
RC0603FR-0716KL	1	R23	Yageo America	RES, 16.0 k, 1%, 0.1 W, 0603
RC0603FR-0718KL	1	R21	Yageo America	RES, 18.0 k, 1%, 0.1 W, 0603
CRCW060349R9FKEA	2	R10, R11	Vishay-Dale	RES, 49.9, 1%, 0.1 W, 0603
RT0805BRD0744K2L	1	R2	Yageo America	RES, 44.2 k, 0.1%, 0.125 W, 0805
RT0805BRD073K52L	1	R3	Yageo America	RES, 3.52 k, 0.1%, 0.125 W, 0805
RT0805BRD071K26L	1	R4	Yageo America	RES, 1.26 k, 0.1%, 0.125 W, 0805
RT0805BRD0722R9L	1	R5	Yageo America	RES, 22.9, 0.1%, 0.125 W, 0805
MCR01MZPF1001	1	R6	Rohm	RES, 1 k, 1%, 0.063 W, 0402
RL0603FR-070R5L	1	R44	Yageo America	RES, 0.5, 1%, 0.1 W, 0603
5015	5	TP1, TP2, TP3, TP4, TP5	Keystone	Test Point, Miniature, SMT
REF6045IDGKR	1	U6	Texas Instruments	High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A
ADS8881IDGSR	1	U7	Texas Instruments	18-Bit, 1-MSPS, Serial Interface, microPower, Miniature, True-Differential Input, SAR Analog-to-Digital Converter, DGS0010A
TPS78833DBVR	1	U5	Texas Instruments	Single Output Low Noise LDO, 150 mA, Fixed 3.3 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), 0 to 70 degC
THS4551IDGKR	1	U3	Texas Instruments	Low-Noise, Precision, 150 MHz, Fully-Differential Amplifier, DGK0008A
OPA333AIDBVR	1	U4	Texas Instruments	17 uA, MicroPower, Precision, Zero Drift CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A)
LP38798SD-ADJ/NOPB	1	U8	Texas Instruments	Ultra Low Noise, 800 mA Linear Voltage Regulator for RF/Analog Circuits, DNT0012B
BR24G32FVT-3AGE2	1	U9	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
OPA320AIDBVT	1	U2	Texas Instruments	Precision, 20MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT-23
REF5045AIDGKT	1	U1	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin MSOP

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8.2 PCB Layout

Figure 15 through Figure 18 illustrate the EVM PCB layout.

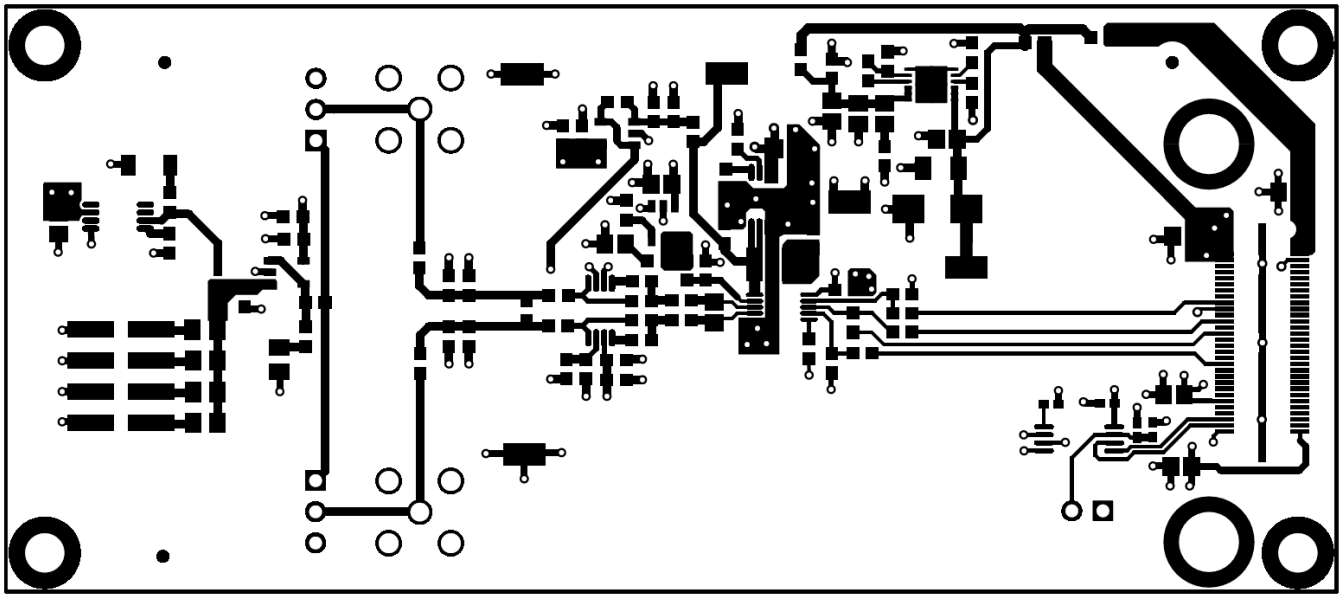

Figure 15. ADS8881EVMV2 PCB Layer 1: Top Layer

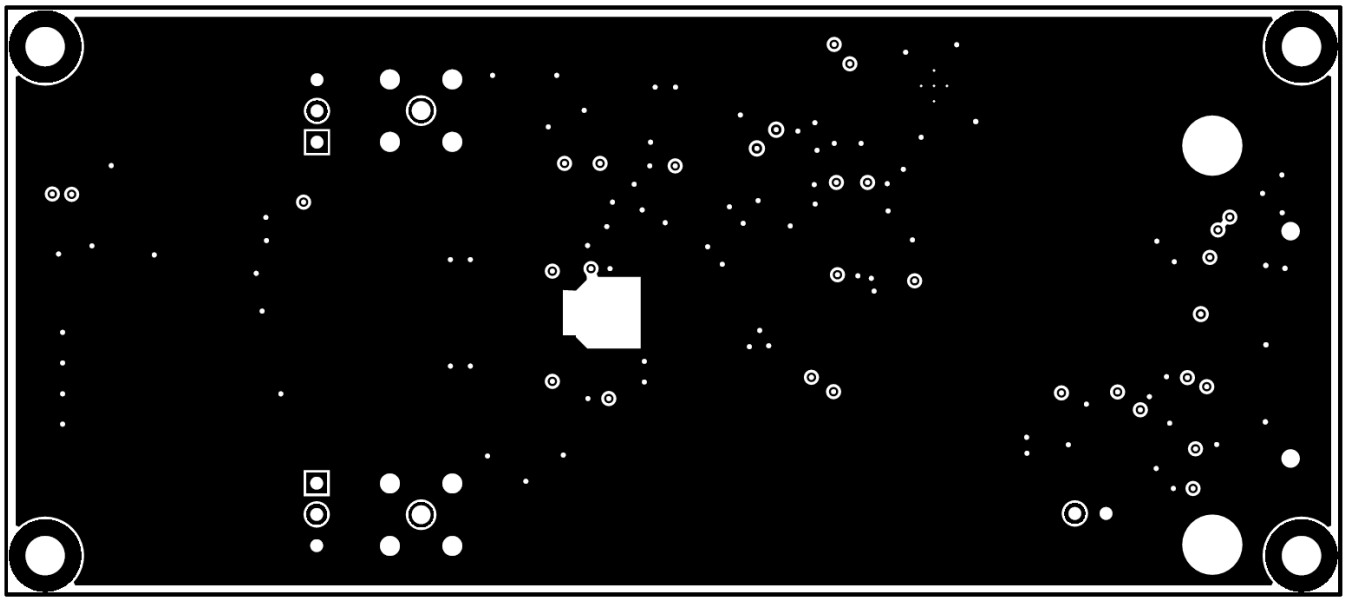

Figure 16. ADS8881EVMV2 PCB Layer 2: GND Plane

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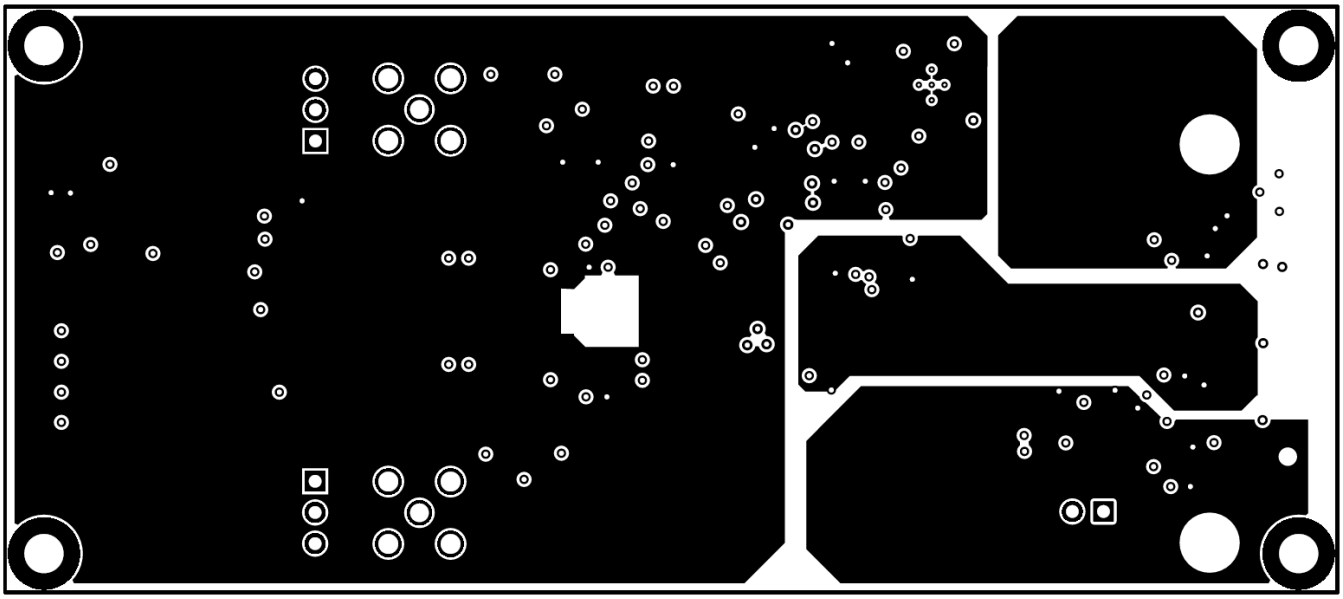

Figure 17. ADS8881EVMV2 PCB Layer 3: Power Planes

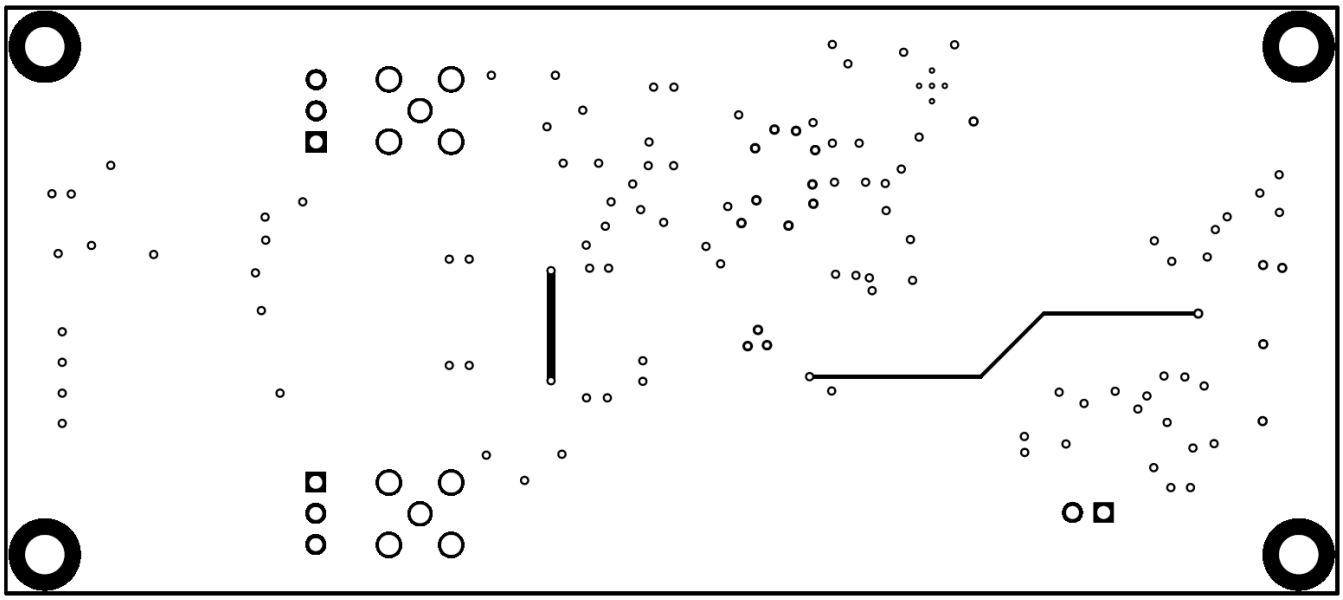

Figure 18. ADS8881EVMV2 PCB Layer 4: Bottom Layer

8.3 Schematic

Figure 19 and Figure 20 illustrate the EVM schematics.

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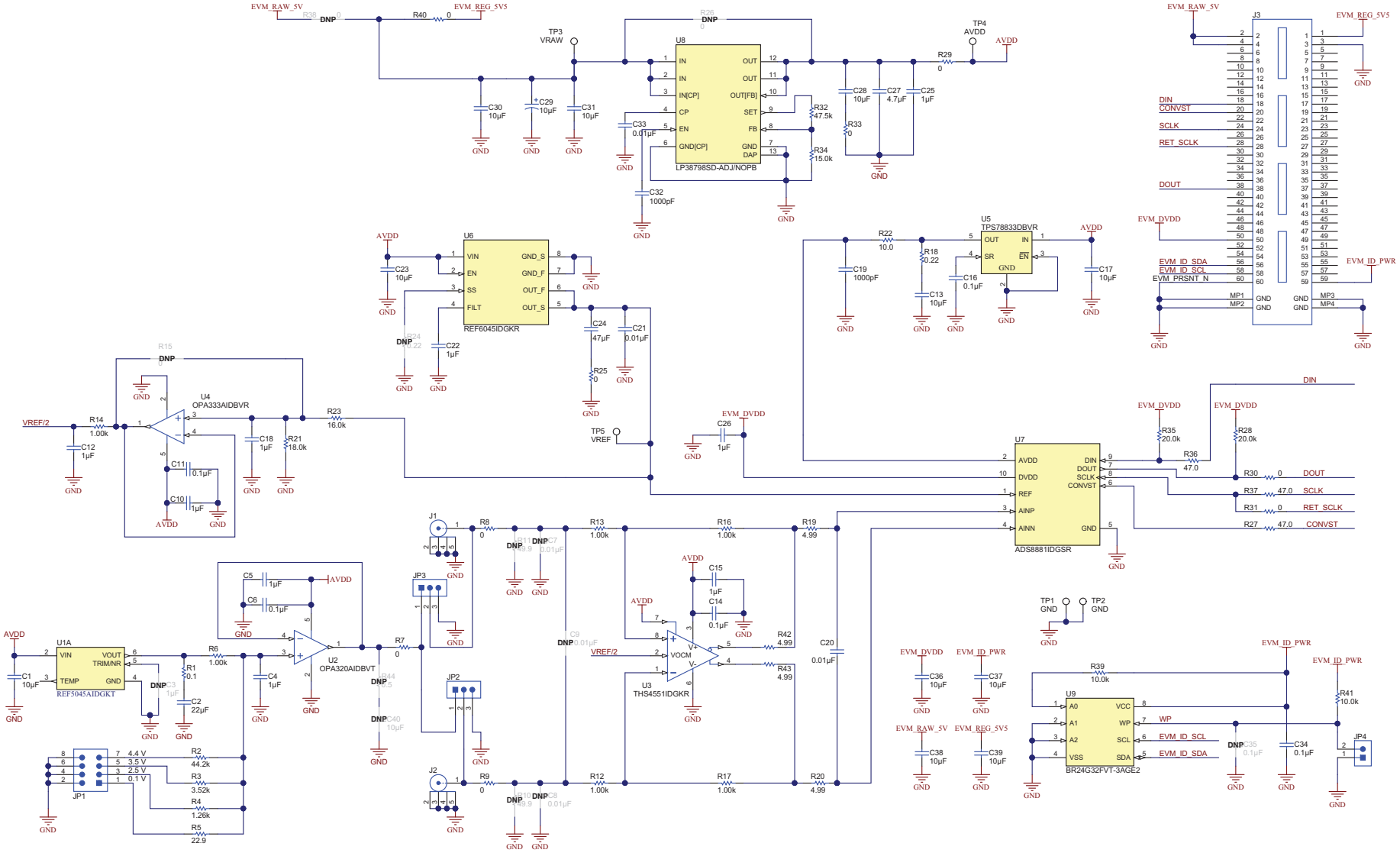

Figure 19. Schematic Diagram (Page 1) of ADS8881EVMV2 PCB

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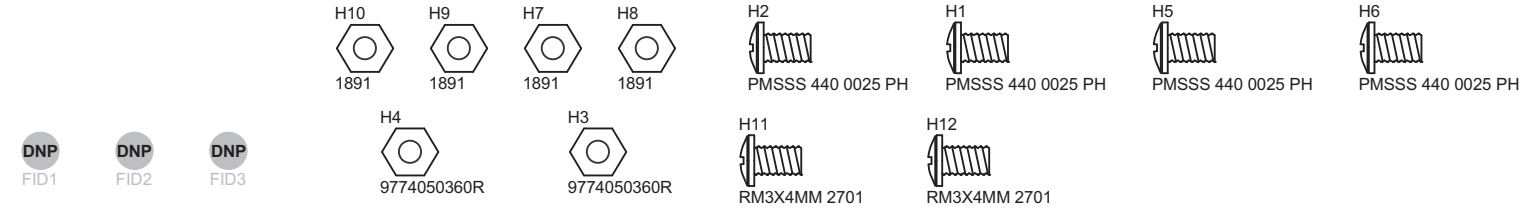

Label Table	
Variant	Label Text
001	REF6025EVM-PDK
002	ADS8881EVMV2-PDK

Figure 20. Schematic Diagram (Page 2) of the ADS8881EVMV2 PCB

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2017) to A Revision	Page
• Changed Figure 19	22
• Changed Figure 20	23

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   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

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   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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