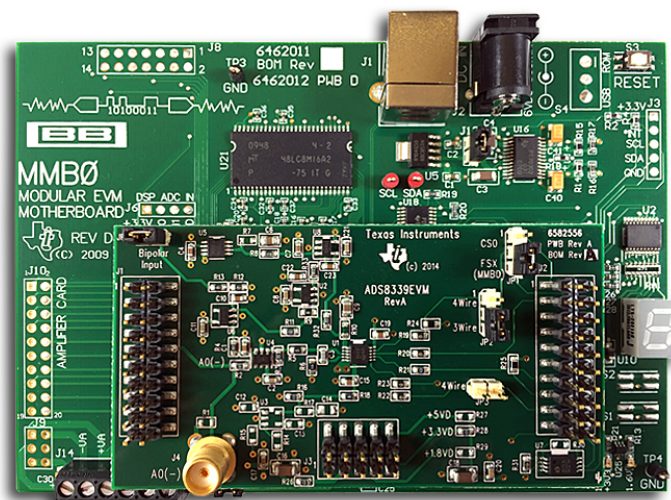


ADS8339EVM-PDK



ADS8339EVM-PDK

This user's guide describes the operation and use of the [ADS8339](#) evaluation module (EVM). The ADS8339 is a 16-bit, pseudo-differential, unipolar, successive approximation register (SAR), analog-to-digital converter (ADC) with a maximum throughput of 250-KSPS. The device is a very low-power ADC with excellent noise and distortion performance for ac or dc signals. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through a universal serial bus (USB). The [ADS8339EVM-PDK](#) includes the ADS8339EVM as a daughter card, MMB0 motherboard, and an A-to-B USB cable. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8339EVM daughter card. Throughout this document, the abbreviation EVM and the term evaluation module are synonymous with the ADS8339EVM-PDK.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS8339	SBAS677
OPA333	SBOS351
OPA376	SBOS406
OPA836	SLOS712
REF5045	SBOS410
THS4281	SLOS432

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Samtec is a trademark of Samtec, Inc.
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1 ADS8339EVM-PDK Overview

The ADS8339EVM is an evaluation module built to TI's modular EVM specifications; for more information, see [SLAA185](#), *Designing Modular EVMs for Data Acquisition Products*. The EVM by itself has no microprocessor and cannot run software. The EVM is available as part of the ADS8339EVM-PDK kit that combines the ADS8339EVM as a daughterboard with the digital signal processor (DSP) based MMB0 motherboard using ADCPro™ software as a graphical user interface (GUI).

ADCPro software collects, records, and analyzes data from ADC evaluation boards. ADCPro also runs different plug-in programs to easily expand testing and data collection capabilities. In combination with the ADS8339EVM plug-in program, ADCPro offers a comprehensive evaluation environment for the ADS8339. For more details on ADCPro, see [SBAU128](#), *ADCPro Analog-to-Digital Converter Evaluation Software User's Guide*, available for download from www.ti.com.

1.1 ADS8339EVM Daughterboard Features

- Includes support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI™)
- Serial interface header for easy connection to TI DSP-based communication systems
- Compatible with the TI Modular EVM system
- Designed for 5-V analog supply
- Onboard 4.5-V voltage reference
- Bipolar (–2.15 V to +2.15 V) or unipolar (0.1 V to 4.4 V) input range

1.2 ADS8339EVM-PDK Kit Additional Features

- USB port for computer interfacing
- Regulated 5-V and 3.3-V supplies for powering EVM daughterboard
- Easy-to-use evaluation software for Windows® operating system
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Easily expandable with new analysis plug-in tools from Texas Instruments

2 EVM Analog Interface

The ADS8339EVM is designed to easily interface to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, the Samtec™ connector provides a convenient 10-pin, dual-row, header and socket combination at J1. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. The analog inputs are buffered by an [OPA836](#) high-speed operational amplifier in order to properly drive the ADS8339 ADC input.

Use appropriate caution when handling these pins. [Table 1](#) summarizes the pinout for analog interface J1.

Table 1. Analog Inputs

Connector	Pin Number	Signal	Description
Samtec 10 × 2	J1.10	A0(–)	CH0 inverted EVM input
SMA	J4	A0(–)	CH0 inverted EVM input

2.1 Bipolar-Input Signal Configuration

With JP4 closed, the OPA836 positive input is biased with 1.125 V, created by dividing the 4.5-V onboard reference by four. This bias becomes a 2.25-V offset at the output of the OPA836 that allows input signals with a 0-V common mode voltage. To keep the OPA836 distortion as low as possible, limit the input signal swing from –2.15 V to +2.15 V, as shown in [Figure 1](#).

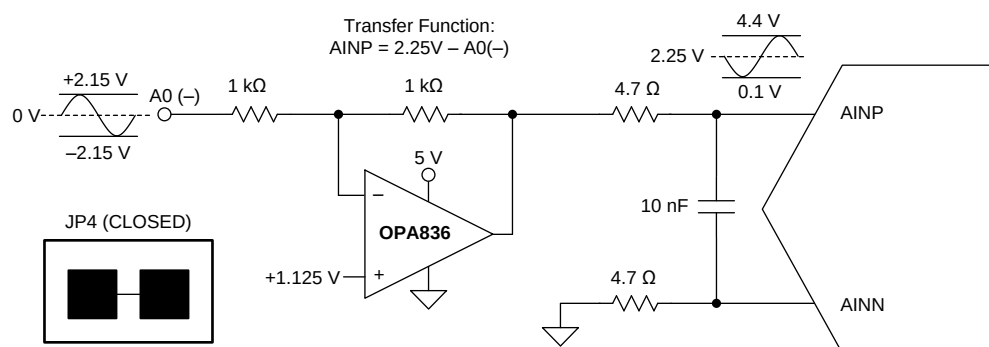


Figure 1. Bipolar-Input Signal Configuration

2.2 Unipolar-Input Signal Configuration

With JP4 open, the OPA836 positive input is biased with +2.25 V, created by dividing the 4.5-V onboard reference by two. This bias becomes a 4.5-V offset at the output of the OPA836 that allows input signals with a 2.25-V common mode voltage. To keep the OPA836 distortion as low as possible, limit the input signal swing from +0.1 V to +4.4 V, as shown in [Figure 2](#).

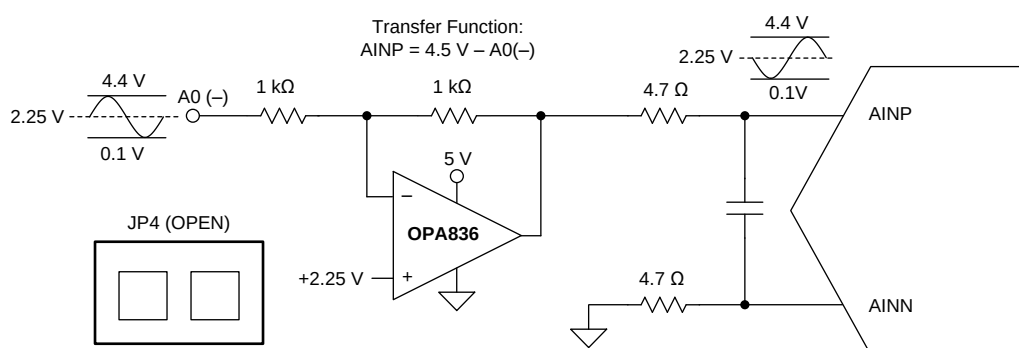


Figure 2. Unipolar-Input Signal Configuration

2.3 Voltage Reference

Because the EVM is powered by a 5-V analog supply, make sure to use a value below 5 V for the reference. This EVM uses a 4.5-V reference, created by the onboard [REF5045](#), as shown in [Figure 3](#). The REF5045 output is filtered by an RC filter with a 160-Hz cutoff frequency to minimize noise contribution. The EVM is buffered by the [THS4281](#), which drives the 10 μ F capacitor required at the ADC reference input. The [OPA333](#) with additional feedback is optional, but does complement the THS4281, and minimizes offset and drift.

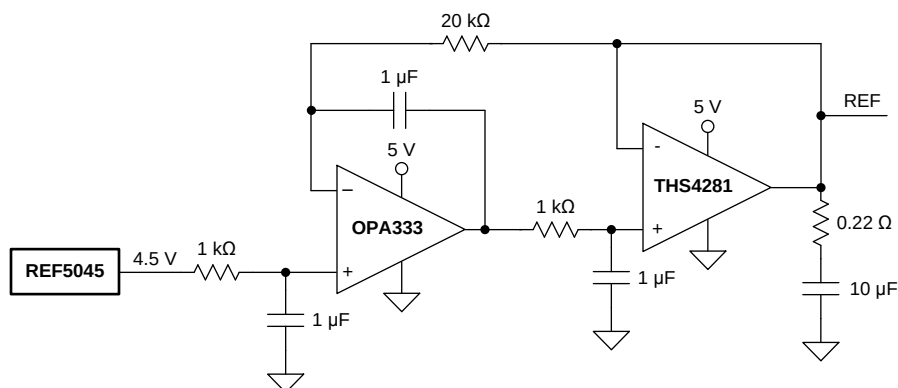


Figure 3. THS4281 Reference Driver with Complementary OPA333 for Drift and Offset Correction

3 EVM Digital Interface

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-L-DV-P provide convenient 10-pin, dual-row, header and socket combinations at P1. The header and socket provide access to the ADC digital control pins. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 2 summarizes the pinouts for digital interface J2.

Table 2. J2: Serial Interface Header

Pin Number	Signal	Description
J2.1	$\overline{\text{CS}}$ or CONVST	Chip-select input that can be used as a convert start
J2.3	SCLK	Serial clock input
J2.7	$\overline{\text{CS}}$ or CONVST	Input used as convert start by the MMB0 motherboard
J2:13	SDO or MISO	SDO or MISO output
J2.15	INT	Interrupt output for detecting end of conversion with BUSY bit
J2.17	CONVST	Direct connection to the convert start pin if JP3 is installed
J2.4, J2.10, and J2.18	GND	Grounded pins
J2.16, J2.20	I ² C bus	I ² C bus; used only to program the U4 EEPROM on the EVM board
J2.2, J2.5-6, J2.8-9, J2.11-12, J2.14, and J2:19	Unused	Unused

3.1 Serial Interface (SPI)

The ADS8339 ADC uses SPI serial communication to send conversion results to the MMB0 motherboard, and subsequently, to a computer using universal serial bus (USB). The serial clock signal (SCLK) is created by the MMB0 motherboard as the SPI host, with a frequency that is programmable up to 25-MHz to obtain the maximum sampling rate of 250-kSPS.

3.2 I²C Bus for Onboard EEPROM

The ADS8339EVM has an I²C bus used by the MMB0 motherboard to communicate with the onboard EEPROM. The bus is not used in any form by the ADS8339 converter.

4 EVM Power-Supply Inputs

J3 is the power-supply input connector. [Table 3](#) lists the configuration details for J3.

Table 3. J3: Power-Supply Interface Header

Pin Number	Pin Name	Function	Required
J3.3	+5VA	5-V analog supply	Yes
J3.5	GND	Analog and digital ground (single ground board)	Yes
J3.6	GND	Analog and digital ground (single ground board)	Yes
J3.7	+ 1.8VD	1.8-V digital supply	No
J3.9	+3.3VD	3.3-V digital supply	Yes
J3.10	+5VD	5-V digital supply	Optional
P3.1-2, P3.4, and P3.7-8	Unused	Unused	No

4.1 Analog Power Options

The ADS8339EVM board functions with a 5-V supply provided at J3.3 by the MMB0 motherboard, powering the onboard reference, op amps, and the analog supply of the ADS8339.

4.2 Digital Power Options

The ADS8339EVM connects the digital power supply of the ADS8339 to +3.3VD (J3.10) to match the 3.3-V logic level of the MMB0 motherboard.

4.3 Analog and Digital Grounds

The EVM only has one ground plane for all analog and digital supplies; pins J3.5 and J3.6 are tied together to this ground plane. Therefore, connect both supply grounds to pins J3.5 and J3.6 so they share the same ground.

5 EVM Digital Configuration

The EVM offers two jumpers (JP2 and JP3) to configure the EVM in either 3-wire SPI mode or 4-wire SPI mode.

5.1 SPI 3-Wire Mode (JP2:2–3 and JP3:OPEN)

This mode is used to communicate with the MMB0 motherboard. Use the chip-select signal to bring the ADS8339 digital output out of tri-state mode and initialize conversions. The rising edge of the chip-select signal starts a conversion, and after the conversion time, the falling edge of the chip-select signal brings the digital output out of tri-state mode. [Figure 4](#) shows the serial configuration for this mode.

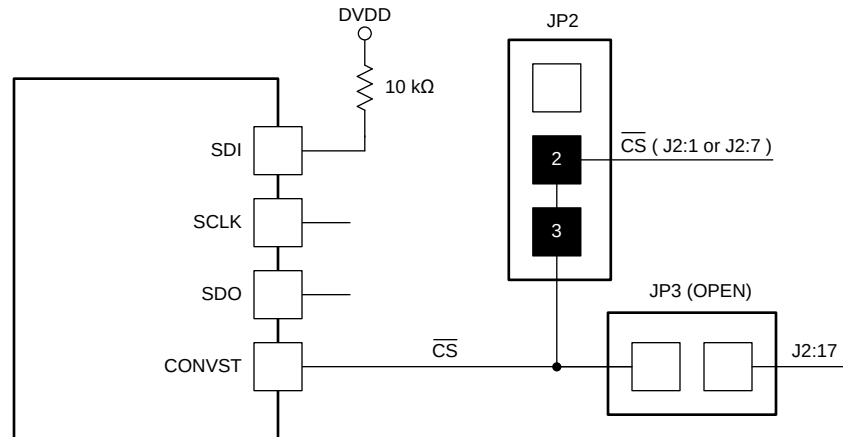


Figure 4. Serial 3-Wire Configuration

5.2 SPI 4-Wire Mode (JP2:1–2 and JP3:CLOSED)

The chip-select signal is used to bring the ADS8339 digital output out of tri-state. However, conversion is initialized from J3:17 as an independent signal. The rising edge of J3:17 (CONVST) starts a conversion, and after the conversion time, the falling edge of the chip-select signal brings the digital output out of tri-state. [Figure 5](#) shows the serial configuration for this mode.

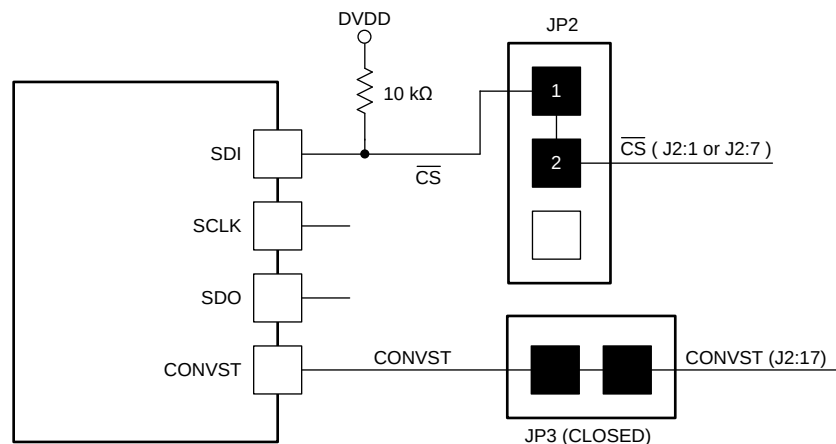


Figure 5. Serial 4-Wire Configuration

6 PDK Kit Setup

NOTE: Do not connect the ADS8339EVM-PDK to a PC before completing [Section 6](#). Failure to observe this caution may cause Microsoft Windows to disregard the ADS8339EVM-PDK as a connected device.

This section presents the steps required to setup the ADS8339EVM-PDK kit before operation. [Section 7](#) explains how to operate the kit to acquire and analyze data.

The steps to setup the kit are as follows and must be completed before attempting to capture data:

- Step 1. Download and install the ADCPro software (if not already installed) on a PC.
- Step 2. Download and install MMB0 motherboard drivers.
- Step 3. Download and install the ADS8339EVM-PDK EVM plug-in software.
- Step 4. Configure the ADS8339EVM-PDK hardware.
- Step 5. Power up the ADS8339EVM-PDK.

Each task is described in the subsequent sections of this document.

6.1 Install ADCPro Software

ADCPro is the primary program used to evaluate the ADS8339. ADCPro is available at www.ti.com/tool/adcpro. Refer to [SBAU128](#), *ADCPro User's Guide*, for detailed installation instructions.

6.2 Install MMB0 Motherboard Drivers

NOTE: The user must have administrator privileges before attempting to install the MMB0 motherboard drivers.

The driver installer is located at TI's FTP site:

ftp://ftp.ti.com/pub/data_acquisition/ADCPro2/misc/drivers/64bit/mmb0_driver_install_x64-v1.0.0.0.msi. Download and double-click the file, and then follow the instructions.

[Figure 6](#) shows the initial and completed installer screen shots.

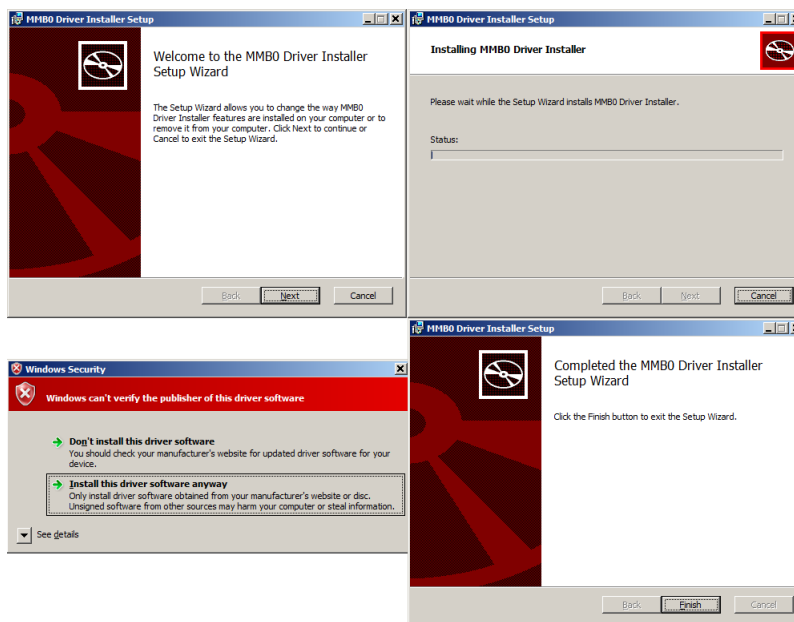


Figure 6. MMB0 Driver Installer

6.3 Install ADS8339EVM-PDK Plug-In Software

NOTE: Install ADCPro before installing the ADS8339EVM-PDK plug-in software.

The installation file link for the PDK plug-in is in the ADS8339EVM-PDK product folder at www.ti.com/tool/ADS8339evm-pdk. In the software section, look for a link with a file named **ads8339evm-adcproplugin-<version #>.exe**, where <version #> refers to the installation file version number, and increments with software version releases. Download and double-click the file, and then follow the instructions.

Figure 7 shows the initial and completed installer screen shots.

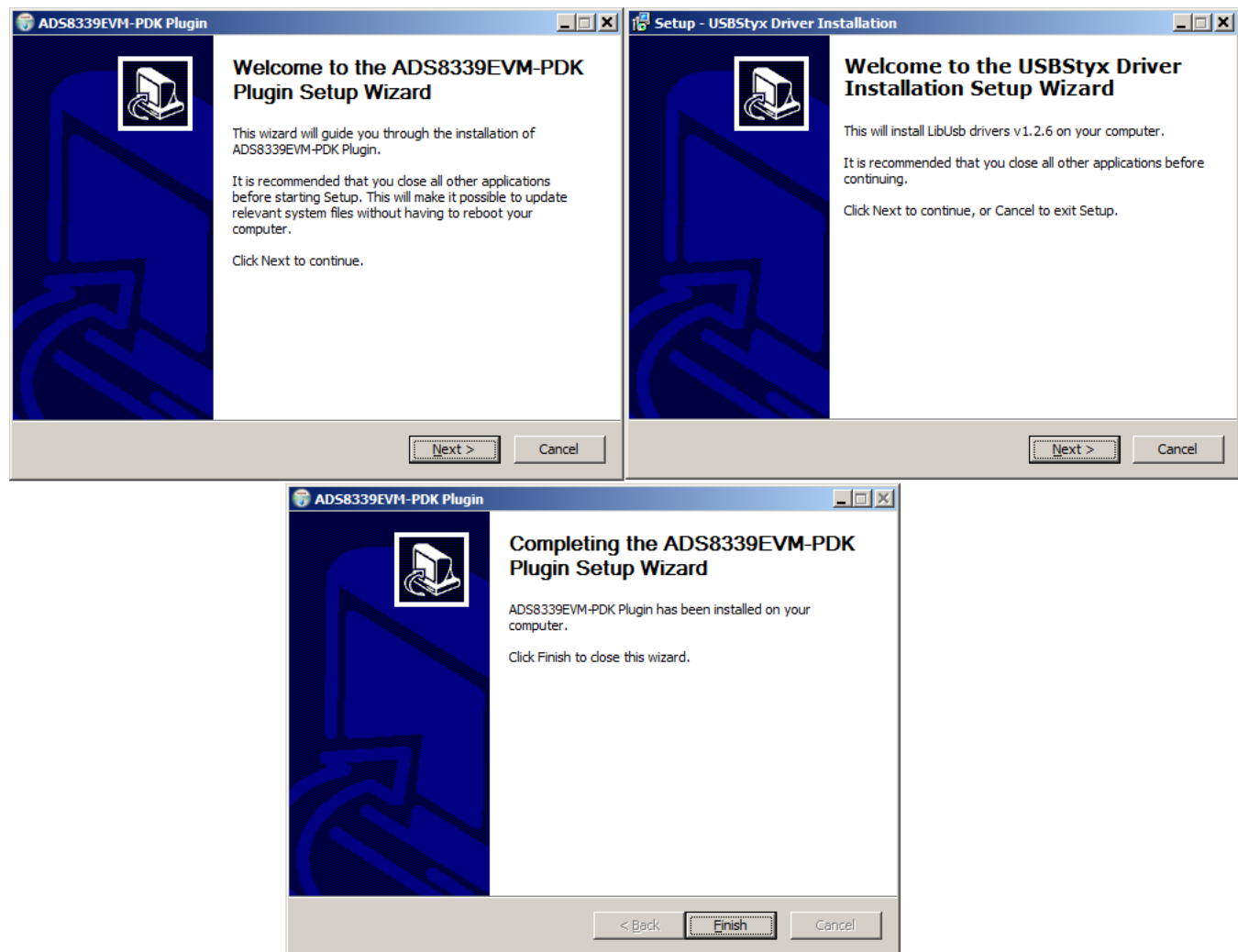


Figure 7. Plug-In Installer

6.4 Configure ADS8339EVM-PDK Hardware

The ADS8339EVM-PDK contains both the ADS8339EVM and the MMB0 motherboard; however, the devices may be shipped unconnected or configured incorrectly. Follow these steps to verify that the ADS8339EVM-PDK kit is properly configured and connected:

- Step 1. Unpack the ADS8339EVM-PDK kit.
- Step 2. Set J12 to closed, J13A to open, and J13B to closed on the MMB0, as shown in [Figure 8](#).
 - J12 must be closed. This setting allows the wall supply to power up the MMB0 and ADS8339EVM through J2 (6-VDC input), and the onboard LDOs to regulate the input down to 5 V, 3.3 V, and 1.8 V.
 - J13B must be closed. This setting connects the 5-V analog power supply with the 5-V digital power supply.
 - J13A must be opened. This setting allows the 5-V analog power supply to be regulated on board.

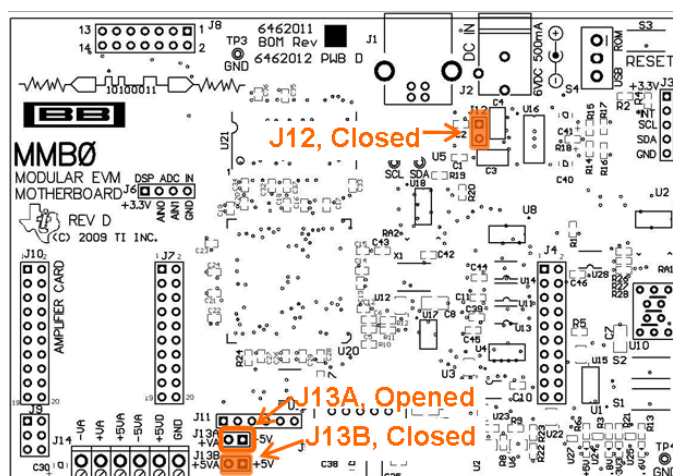


Figure 8. MMB0 Motherboard Jumper Configuration

- Step 3. Set JP1:2–3, JP2:2–3, JP3:open, and JP4:closed on the ADS8339EVM, as shown in [Figure 9](#).

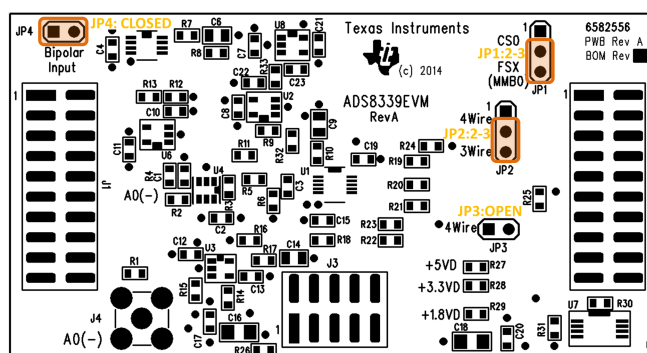


Figure 9. ADS8339EVM Jumper Configuration

- Step 4. Plug the ADS8339EVM into the MMB0.

CAUTION

To avoid damage to the EVM, do not misalign the pins when plugging the ADS8339EVM into the MMB0. Check the pin alignment carefully before applying power to the PDK.

6.5 Power Up ADS8339EVM-PDK

When the ADS8339EVM-PDK kit is configured, power can be applied to the MMB0. This power comes from a wall supply that delivers 6 VDC to the MMB0 through J2 on the MMB0 motherboard. The wall power supply adapter is not included with this PDK. TI recommends using an external power-supply adapter that complies with the applicable regional safety standards (such as UL, CSA, VDE, PSE, and so forth). The functional requirements of the power-supply adapter are as follows:

- Nom output voltage: 5.6 VDC to 15 VDC
- Current capacity: 500 mA or more
- Uses a 2.5-mm center positive barrel connector for mating with the on-board power jack

After the power supply is connected, four green light-emitting diodes (LEDs) in the bottom right-hand corner of the MMB0 motherboard light up. If these LEDs do not light up, disconnect the power and verify that J12 is closed on the MMB0 motherboard.

7 PDK Kit Operation

The evaluation software is based on ADCPro. This program operates with a variety of plug-ins. To use ADCPro, load an EVM plug-in and a test plug-in (select these plug-ins from the EVM and test menus, respectively). To unload a plug-in, select the unload option from the corresponding menu.

The following sections describe how to use ADCPro and the ADS8339EVM plug-in to acquire data.

7.1 About MMB0

The MMB0 is a modular EVM system motherboard. The MMB0 provides the USB interface between the PC and the ADS8339EVM. The MMB0 is designed around the [TMS320VC5509](#), a DSP with an onboard USB interface from Texas Instruments. The MMB0 also has 16 MB of SDRAM installed.

The MMB0 is not sold as a DSP development board, and is not available separately. TI cannot offer support for the MMB0 except as part of an EVM kit. For schematics or other information about the MMB0, contact Texas Instruments.

7.2 Load ADS8339EVM-PDK Plug-In

- Step 1. Make sure the PDK kit is configured and powered up, as explained in [Section 6](#). Then, press the *Reset* button on the MMB0 (in the top right-hand corner) one time to clear the board memory.
- Step 2. Connect the MMB0 to a PC using the USB cable provided with the kit.
- Step 3. Start ADCPro from the Windows *Start* menu.
- Step 4. Load the ADS8339EVM plug-in from the ADCPro *EVM* drop-down menu, as shown in [Figure 10](#). Note that only one EVM plug-in can be loaded at a time. If a different plug-in is selected, the previous plug-in is unloaded and the MMB0 restarted.

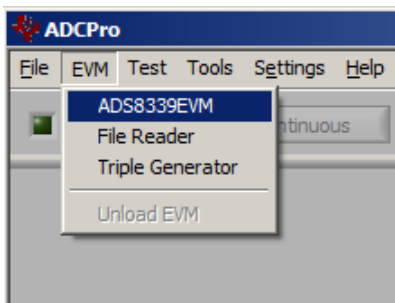


Figure 10. Loading EVM Plug-In

- Step 5. When the plug-in is loaded, the plug-in searches for the board. A series of messages in the status area indicates this action, eventually displaying *Connected to EVM*.

The plug-in is now loaded and ready to function with the ADS8339EVM.

7.3 ADS8339EVM Plug-In Operation

Figure 11 shows the device-configuration tab of the ADS8339EVM plug-in that is used to change acquisition parameters, such as sample rate and voltage reference.

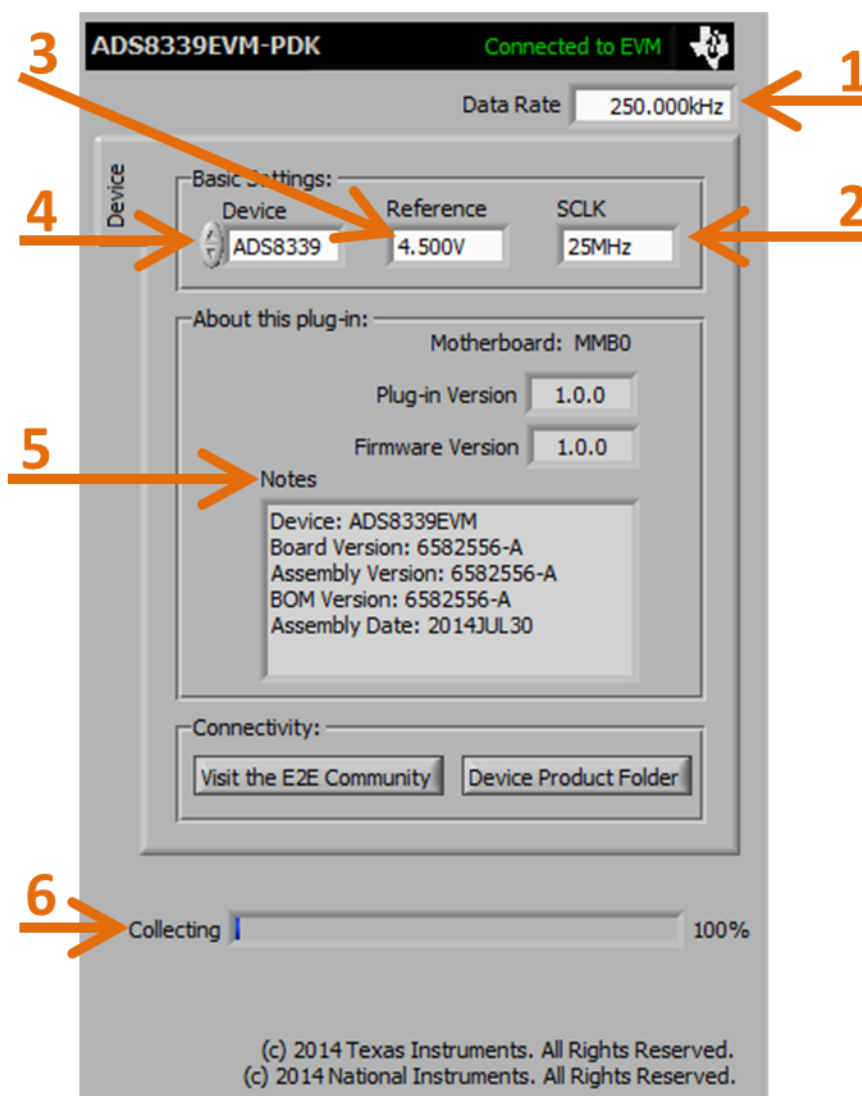


Figure 11. ADS8339EVM Plug-In: Device-Configuration Tab

The device-configuration tab contains the following controls:

1. **Data Rate:** By default, the data rate is at 250-KSPS. This control shows the data rate or sampling frequency used by the ADC to acquire data. With SCLK frequency at 25-MHz, set data rate to a value from 6.105-KSPS to 250-KSPS. With SCLK frequency at 400 KHz, set the data rate to a value from 3.960-kSPS to 21.052-kSPS.
2. **SCLK:** By default, SCLK is at 25-MHz. SCLK sets the clock frequency used by the SPI interface to capture data. Note that reducing SCLK frequency also reduces the maximum data rate.
3. **Reference:** 4.5 V is the default reference value, and matches the onboard reference of the EVM. To read accurate voltages, set the value of this control to be the exact value of the reference.
4. **Device:** ADS8339 is the only device available for this plug-in.
5. **About this plug-in:** This control shows the plug-in version, MMB0 firmware version, assembly date, and board revision information.
6. **Collecting:** This feature shows the percentage of data collected during an acquisition session.

7.4 Load Test Plug-in

When the ADS8339EVM plug-in is configured, to acquire data, use the *Test* drop-down menu to load one of the four test plug-ins, as shown in [Figure 12](#). Note that only one test plug-in can be loaded at a time. If a different plug-in is selected, the previous plug-in is unloaded.

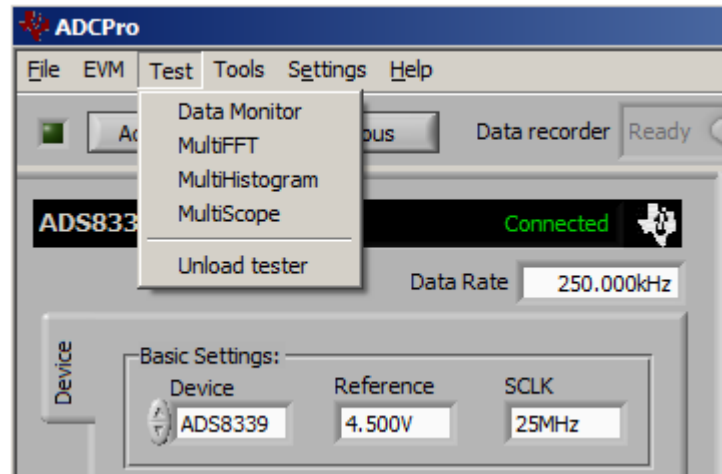


Figure 12. ADCPro Test Plug-ins

There are four different test options available for the ADS8339EVM:

- **Data Monitor:** This test option acquires and exports data in a table format as hexadecimal data.
- **MultiFFT:** This test option acquires data and create an FFT graph of power versus frequency to display data.
- **MultiHistogram:** This option acquires data and creates a histogram of code values.
- **MultiScope:** This feature acquires and displays data in a graph of voltage versus time.

For further details regarding how to set up and use the various test plug-ins, refer to [SBAU128](#), *ADCPro User's Guide*.

7.5 Acquire Data

When the ADS8339EVM is configured for the desired test scenario, press the *Acquire* button to start the data collection process. The software collects the number of data points located in the test plug-in *Block Size* field (512 by default; see [SBAU128](#)). During data acquisition, the ADS8339EVM plug-in disables all front-panel controls and the collection process bar displays the completion progress.

7.6 Troubleshooting

If the ADS8339EVM plug-in cannot find the ADS8339EVM-PDK, press the *RESET* button on the MMB0 and try again.

If ADCPro stops responding while the ADS8339EVM-PDK is connected, shut down and restart the ADCPro software. If restarting the software does not restore functionality, unplug the USB cable from the MMB0 and then plug the cable back in.

8 Bill of Materials, Layout, and Schematic

The bill of materials is provided in [Table 4](#). [Section 8.2](#) shows the printed circuit board (PCB) layout for the ADS8339EVM. [Section 8.3](#) shows the schematic for the ADS8339EVM.

8.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, refer to www.ti.com.)

Table 4. ADS8339EVM Bill of Materials

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
1	1	—		Printed Circuit Board, 3.2 in x 1.7 in. x 0.062 in.	Texas Instruments	6582556
2	8	1 μ F	C1, C4, C7, C10, C15, C19, C22, C23	Capacitor, X7R Ceramic +/-10%, 25WV, 0603	Murata	GRM188R71E105KA12D
3	4	0.1 μ F	C2, C8, C11, C21	Capacitor, X7R Ceramic +/-10%, 25WV, 0603	Murata	GRM188R71E104KA01D
4	1	10000 pF	C3	Capacitor, C0G Ceramic +/-5%, 50WV, 0603	TDK	C1608C0G1H103J
5	2	10 μ F	C6, C9	Capacitor, X7R Ceramic +/-10%, 10WV, 0805	Murata	GRM21BR71A106KE51L
6	3	—	C12, C13, C14	Do Not Install (DNI)	—	—
7	2	10 μ F	C16, C18	Capacitor, X7R Ceramic +/-10%, 16WV, 1206	TDK	C3216X7R1C106K
8	2	1000 pF	C17, C20	Capacitor, C0G Ceramic +/-5%, 50WV, 0603	Murata	GRM188SC1H102JA01D
9	2	—	J1, J2 (Top)	Header 20 Pin SMT Plug, .100" Gold (2x10)	Samtec	TSM-110-01-L-DV-P
10	2	—	J1, J2 (Bottom)	Header 20 Pin SMT Socket, .100" Gold (2x10)	Samtec	SSW-110-22-F-D-VS-K
11	1	—	J3 (Top)	Header 10 Pin SMT Plug, .100" Gold (2x5)	Samtec	TSM-105-01-L-DV-P
12	1	—	J3 (Bottom)	Header 10 Pin SMT Socket, .100" Gold (2x5)	Samtec	SSW-105-22-F-D-VS-K
13	1	—	J4	CONN SMA JACK STRAIGHT PCB	Amphenol	132134
14	2	—	JP1, JP2	Header Strip, 3 pin .100" Gold (1x3)	Samtec	TSW-103-07-L-S
15	2	—	JP3, JP4	Header Strip, 2 pin .100" Gold (1x2)	Samtec	TSW-102-07-L-S
16	7	—	R1, R14, R15, R17, R27, R29, R30	Do Not Install (DNI)	—	—
17	2	1k	R2, R3	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB102V
18	1	100	R4	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1000V
19	2	4.7	R5, R6	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW06034R70FKEA
20	2	0.22	R7, R10	Resistor, Thin Film Chip, 1%, 1/5W, 0603	Susumu	RL0816S-R22-F
21	2	1k	R8, R33	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1001V
22	2	10	R9, R18	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW060310R0FKEA
23	3	20k	R11, R12, R32	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB203V
24	1	10k	R13	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB103V
25	4	0	R16, R21, R26, R28	Resistor, Thick Film Chip, 1/10W, 0603	Panasonic	ERJ-3GEY0R00V
26	5	47	R19, R20, R22, R23, R31	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V
27	2	10k	R24, R25	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1002V
28	1	—	U1	IC ADC 16BIT 1MSPS PSEUDO-DIFF 10-MSOP	Texas Instruments	ADS8339IDGS
29	1	—	U2	IC OPAMP VFB R-R 95MHZ SOT23-5	Texas Instruments	THS4281DBV
30	1	—	U3	Do Not Install (DNI)	—	—
31	1	—	U4	IC OPAMP VFB RRO 205MHZ SOT23-6	Texas Instruments	OPA836IDBV
32	1	—	U5	IC VREF SERIES PREC 4.5V 8-MSOP	Texas Instruments	REF5045IDGK
33	1	—	U6	IC OPAMP GP 5.5MHZ SGL SOT23-5	Texas Instruments	OPA376AIDBV
34	1	—	U7	IC EEPROM 256KBIT 400KHZ 8TSSOP	Microchip	24LC256-I/ST
35	1	—	U8	IC OPAMP CHOP R-R 350KHZ SOT23-5	Texas Instruments	OPA333AIDBV

8.2 PCB Layout

Figure 13 through Figure 16 show the PCB layout for the ADS8339EVM.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS8339EVM PCBs.

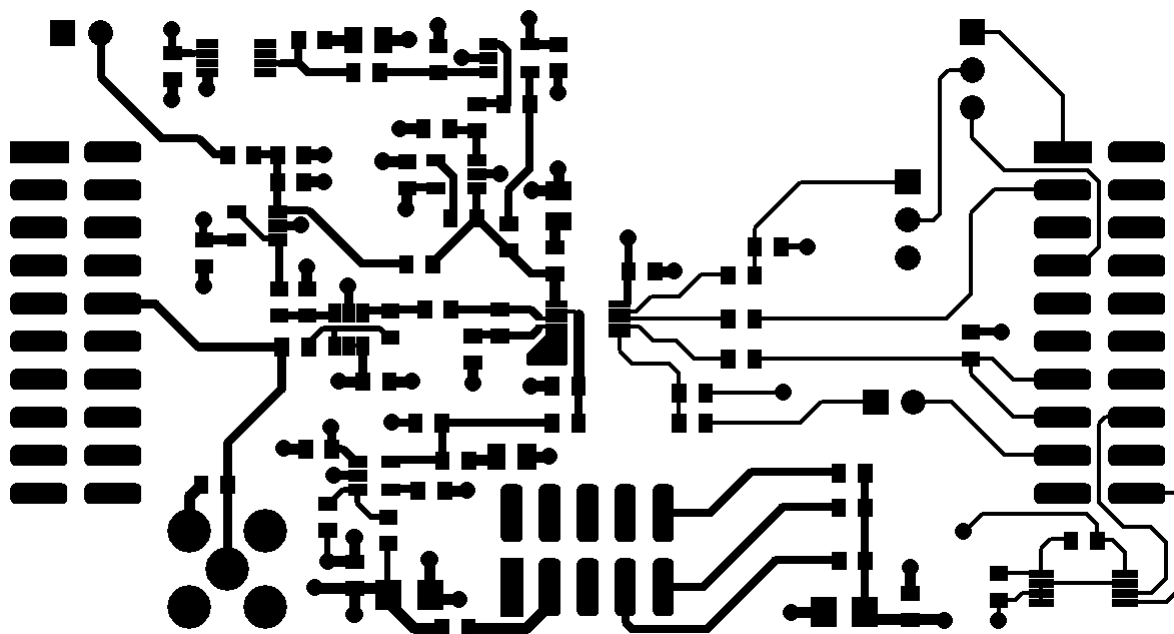


Figure 13. ADS8339EVM PCB: Top Layer

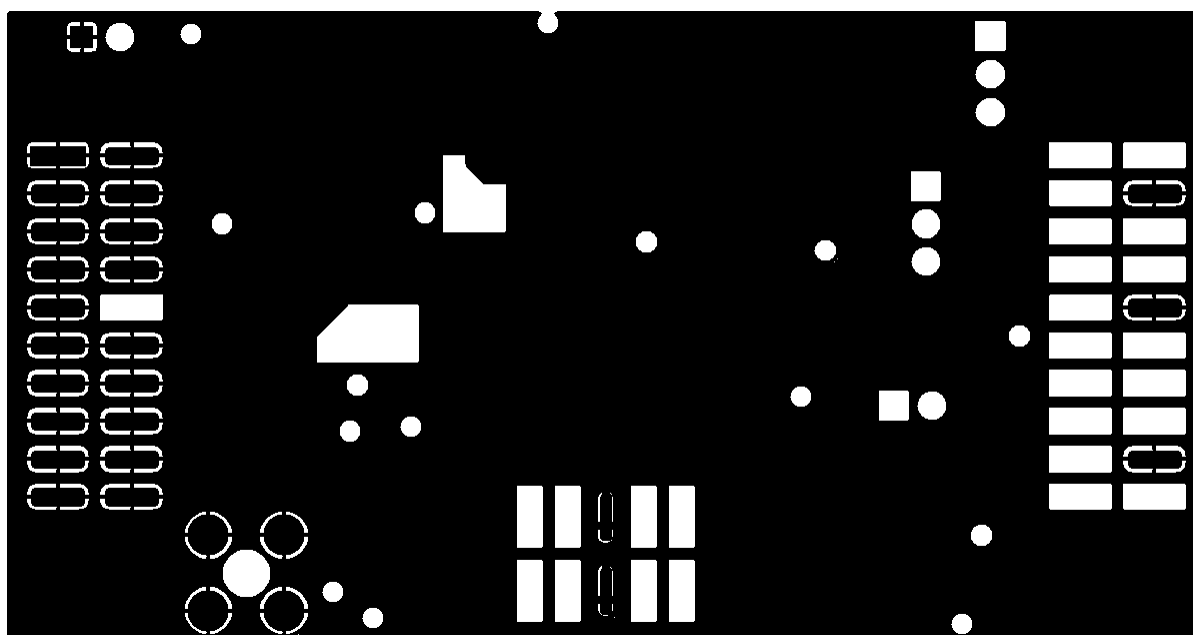


Figure 14. ADS8339EVM PCB: Ground Layer

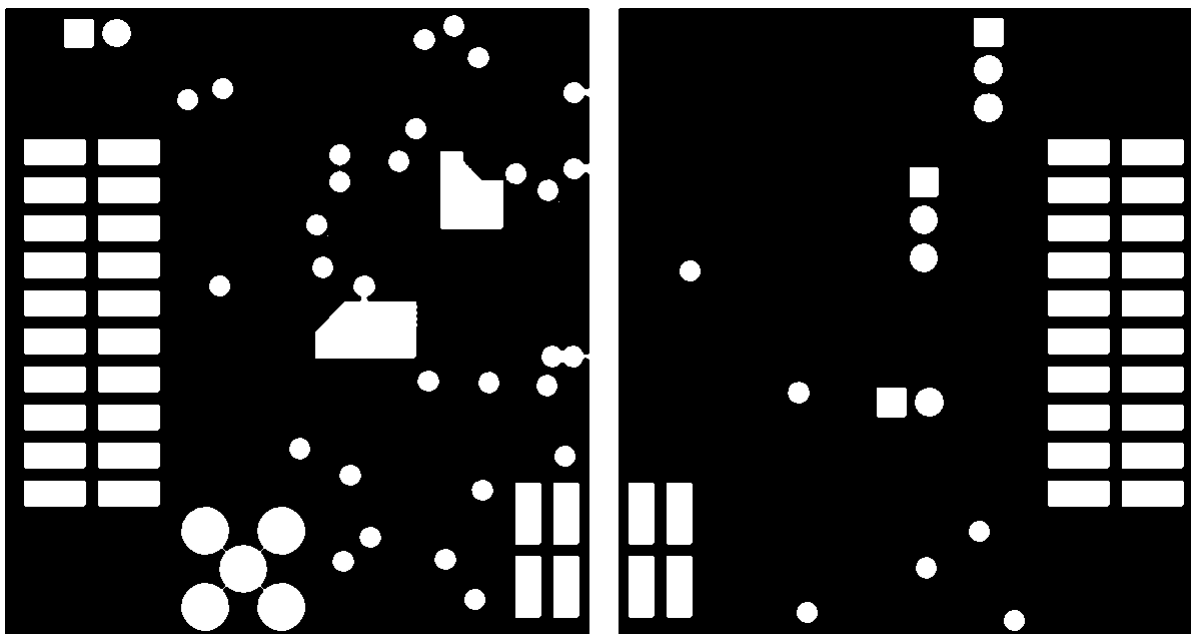


Figure 15. ADS8339EVM PCB: Power Layer

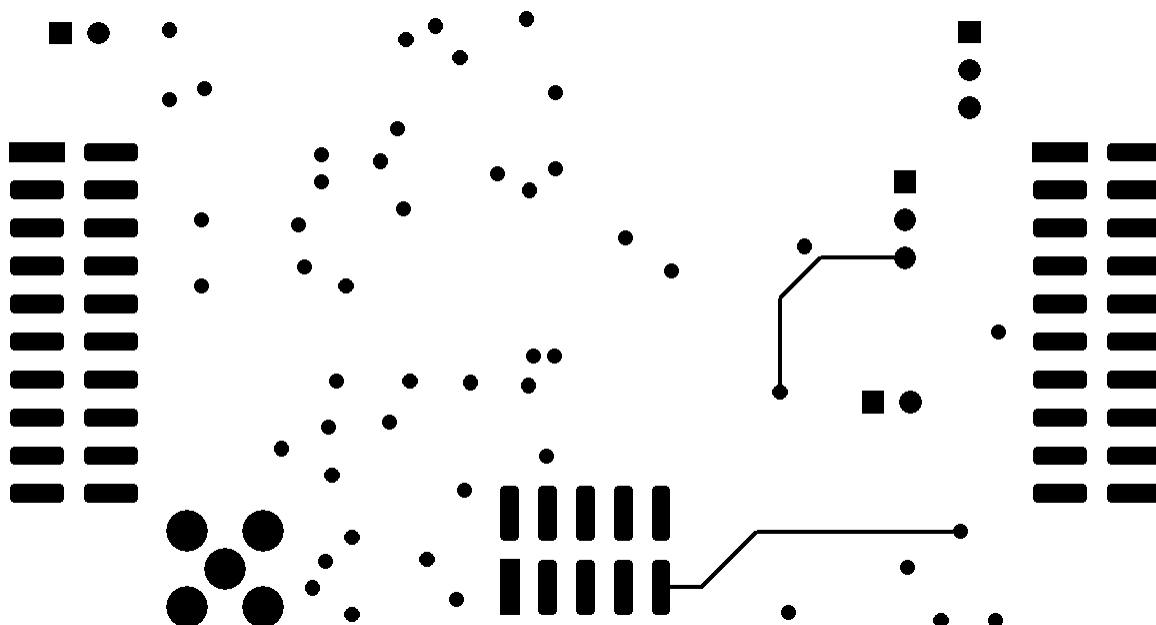


Figure 16. ADS8339EVM PCB: Bottom Layer

8.3 Schematic

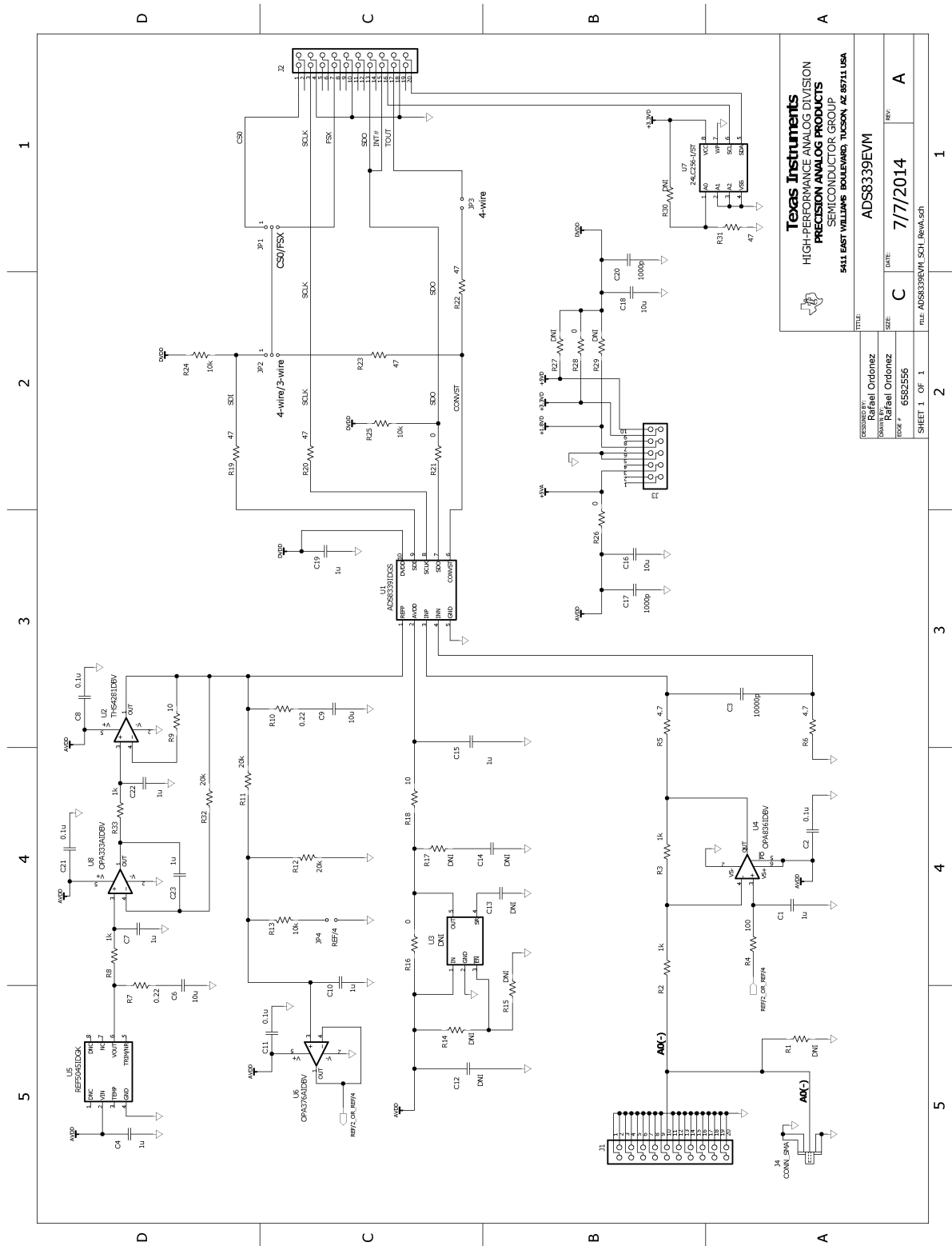


Figure 17. Schematic

Revision History

Changes from Original (October 2014) to A Revision

Page

- Changed list of items included in the ADS8339EVM-PDK in first paragraph [1](#)
- Changed first paragraph of *Power Up ADS8339EVM-PDK* section [12](#)

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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