TEXAS INSTRUMENTS

ADS8320

SBAS108E – MAY 2000 – REVISED DECEMBER 2016

ADS8320 16-Bit, High-Speed, 2.7-V to 5-V microPower Sampling Analog-to-Digital Converter

1 Features

- 100-kHz Sampling Rate
- *micro*Power:
  - 1.8 mW at 100 kHz and 2.7 V
  - 0.3 mW at 10 kHz and 2.7 V
- Power Down: 3 µA (Maximum)
- 8-Pin VSSOP Package
- Pin-Compatible to ADS7816 and ADS7822
- Serial (SPI™/SSI) Interface

2 Applications

- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Simultaneous Sampling, Multichannel Systems
- Industrial Controls
- Robotics
- Vibration Analysis

3 Description

The ADS8320 device is a 16-bit, sampling analog-to-digital (A/D) converter with ensured specifications over a 2.7-V to 5.25-V supply range. It requires very little power even when operating at the full 100-kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode. The average power dissipation is less than 100 mW at 10-kHz data rate.

The ADS8320 also features operation from 2 V to 5.25 V, a synchronous serial (SPI/SSI compatible) interface, and a differential input. The reference voltage can be set to any level within the range of 500 mV to V_{CC}.

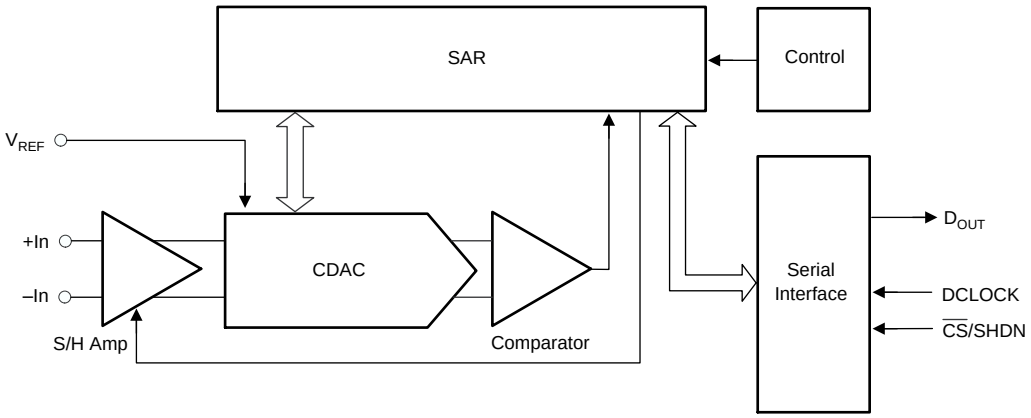
Ultra-low power and small size make the ADS8320 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS8320 is available in an 8-pin VSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8320	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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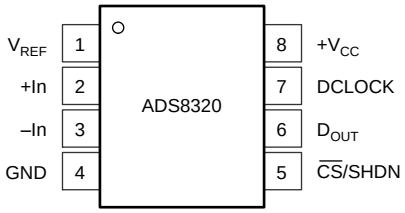
4 Revision History

Changes from Revision D (March 2007) to Revision E **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 4
- Changed *Application Circuits* section To: *Typical Connection Diagram* ... 11

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{REF}	AI	Reference input
2	+In	AI	Noninverting input
3	–In	AI	Inverting input: Connect to ground or to remote ground sense point.
4	GND	GND	Ground
5	$\overline{CS}$/SHDN	DI	Chip select when LOW; Shutdown mode when HIGH.
6	D_{OUT}	DO	The serial output data word is comprised of 16 bits of data. In operation the data is valid on the falling edge of D_{CLOCK}. The second clock pulse after the falling edge of CS enables the serial output. After one null bit the data is valid for the next 16 edges.
7	D_{CLOCK}	DI	Data clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	PWR	Power supply

(1) AI = Analog Input, DI = Digital Input, DO = Digital Output, GND = Ground, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{CC}		6	V
Analog input	–0.3	V_{CC} + 0.3	V
Logic input	–0.3	6	°C
External reference voltage		5.5	V
Input current to any pin except supply		±10	mA
Case temperature		100	°C
Junction temperature		150	°C
Storage temperature, T_{stg}		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} to GND	Low voltage levels	2.7		3.3	V
	5-V logic levels	4.75	5	5.25	
Reference input voltage, V_{REF}		0.5		V_{CC}	V
Analog input voltage	–IN to GND	–0.1	0	0.5	V
	+IN to GND	–0.1		V_{CC} + 0.1	
	+IN to – (–IN)	0		V_{REF}	
Operating temperature, T_A		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS8320 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_{CC} = 5 V

at –40°C to 85°C, V_{REF} = 5 V, –IN = GND, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 × f_{SAMPLE} (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution					16	Bits
ANALOG INPUT						
Full-scale input span	+In – (–In)		0		VREF	V
Absolute input	+In		–0.1		V_{CC} + 0.1	V
	–In		–0.1		1	
Capacitance				45		pF
Leakage current				1		nA
SYSTEM PERFORMANCE						
No missing codes	ADS8320E		14			Bits
	ADS8320EB		15			
Integral linearity error	ADS8320E			±0.008%	±0.018%	FSR
	ADS8320EB			±0.006%	±0.012%	
Offset error	ADS8320E			±1	±2	mV
	ADS8320EB			±0.5	±1	
Offset temperature drift				±3		µV/°C
Gain error	ADS8320E				±0.05%	FSR
	ADS8320EB				±0.024%	
Gain error temperature drift				±0.3		ppm/°C
Noise				20		µVrms
Power-supply rejection ratio	4.7 V < V_{CC} < 5.25 V			3		LSB(1)
SAMPLING DYNAMICS						
Conversion time					16	Clock Cycles
Acquisition time			4.5			Clock Cycles
Throughput rate					100	kHz
Clock frequency			0.024		2.4	MHz
DYNAMIC CHARACTERISTICS						
Total harmonic distortion	V_{IN} = 5 V_{P-P} at 10 kHz	ADS8320E		–84		dB
		ADS8320EB		–86		
SINAD	V_{IN} = 5 V_{P-P} at 10 kHz	ADS8320E		82		dB
		ADS8320EB		84		
Spurious-free dynamic	V_{IN} = 5 V_{P-P} at 10 kHz	ADS8320E		84		dB
		ADS8320EB		86		
SNR	ADS8320E			90		dB
	ADS8320EB			92		
REFERENCE INPUT						
Voltage			0.5		V_{CC}	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0 Hz			5		GΩ
	$\overline{CS}$ = V_{CC}			5		
Current drain				40	80	µA
	f_{SAMPLE} = 0 Hz			0.8		
	$\overline{CS}$ = V_{CC}			0.1	3	

(1) LSB means Least Significant Bit with VREF equal to 2.5 V, one LSB is 0.038 mV.

Electrical Characteristics: V_{CC} = 5 V (continued)

at –40°C to 85°C, V_{REF} = 5 V, –IN = GND, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 × f_{SAMPLE} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
Logic levels	V_{IH}	I_{IH} = 5 µA	3		V_{CC} + 0.3	V
	V_{IL}	I_{IL} = 5 µA	–0.3		0.8	
	V_{OH}	I_{OH} = –250 µA	4			
	V_{OL}	I_{OL} = 250 µA			0.4	
Data format				Straight Binary		
POWER SUPPLY REQUIREMENTS						
V_{CC}		Specified performance	4.75		5.25	V
V_{CC} (2)			2		5.25	V
Quiescent current				900	1700	µA
		f_{SAMPLE} = 10 kHz (3) (4)		200		
Power dissipation				4.5	8.5	mW
Power down		$\overline{CS}$ = V_{CC}		0.3	3	µA

(2) See *Typical Characteristics* for more information.
(3) f_{CLK} = 2.4 MHz, CS = V_{CC} for 216 clock cycles out of every 240.
(4) See *Power Dissipation* for more information regarding lower sample rates.

6.6 Electrical Characteristics: V_{CC} = 2.7 V

at –40°C to 85°C, V_{REF} = 5 V, –IN = GND, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 × f_{SAMPLE} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION					
Resolution				16	Bits
ANALOG INPUT					
Full-scale input span	+In – (–In)	0		VREF	V
Absolute input	+In	–0.1		V_{CC} + 0.1	V
	–In	–0.1		0.5	
Capacitance			45		pF
Leakage current			1		nA
SYSTEM PERFORMANCE					
No missing codes	ADS8320E	14			Bits
	ADS8320EB	15			
Integral linearity error	ADS8320E		±0.008%	±0.018%	FSR
	ADS8320EB		±0.006%	±0.012%	
Offset error	ADS8320E		±1	±2	mV
	ADS8320EB		±0.5	±1	
Offset temperature drift			±3		µV/°C
Gain error	ADS8320E			±0.05%	FSR
	ADS8320EB			±0.024%	
Gain error temperature drift			±0.3		ppm/°C
Noise			20		ppm/°C
Power-supply rejection ratio	2.7 V < V_{CC} < 3.3 V		3		LSB (1)

(1) LSB means Least Significant Bit with VREF equal to 2.5 V, one LSB is 0.038 mV.

Electrical Characteristics: V_{CC} = 2.7 V (continued)

at –40°C to 85°C, V_{REF} = 5 V, –IN = GND, f_{SAMPLE} = 100 kHz, and f_{CLK} = 24 × f_{SAMPLE} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS							
Conversion time						16	Clock Cycles
Acquisition time				4.5			Clock Cycles
Throughput rate						100	kHz
Clock frequency				0.024		2.4	MHz
DYNAMIC CHARACTERISTICS							
Total harmonic distortion		V_{IN} = 2.7 V_{P-P} at 1 kHz	ADS8320E		–86		dB
			ADS8320EB		–88		
SINAD		V_{IN} = 2.7 V_{P-P} at 1 kHz	ADS8320E		84		dB
			ADS8320EB		86		
Spurious-free dynamic		V_{IN} = 2.7 V_{P-P} at 1 kHz	ADS8320E		86		dB
			ADS8320EB		88		
SNR		ADS8320E			88		dB
		ADS8320EB			90		
REFERENCE INPUT							
Voltage				0.5		V_{CC}	V
Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0 Hz			5		GΩ
		$\overline{CS}$ = V_{CC}			5		
Current drain					20	50	µA
		$\overline{CS}$ = V_{CC}			0.1	3	
DIGITAL INPUT/OUTPUT							
Logic Family					CMOS		
Logic levels	V_{IH}	I_{IH} = 5 µA		2		V_{CC} + 0.3	V
	V_{IL}	I_{IL} = 5 µA		–0.3		0.8	
	V_{OH}	I_{OH} = –250 µA		2.1			
	V_{OL}	I_{OL} = 250 µA				0.4	
Data format					Straight Binary		
POWER SUPPLY REQUIREMENTS							
V_{CC}		Specified performance		2.7		3.3	V
V_{CC} (2)				2		5.25	V
		See (3)		2		2.7	
Quiescent current					650	1300	µA
		f_{SAMPLE} = 10 kHz (4)(5)			100		
Power dissipation					1.8	3.8	mW
Power down		$\overline{CS}$ = V_{CC}			0.3	3	µA

(2) See *Typical Characteristics* for more information.
(3) The maximum clock rate of the ADS8320 is less than 2.4 MHz in this power supply range.
(4) f_{CLK} = 2.4 MHz, CS = V_{CC} for 216 clock cycles out of every 240.
(5) See *Power Dissipation* for more information regarding lower sample rates.

6.7 Typical Characteristics

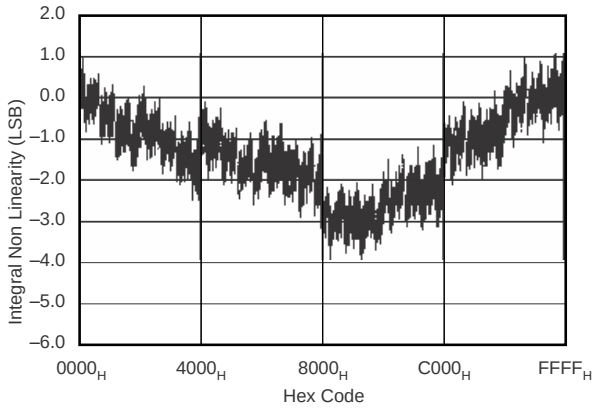


Figure 1. Integral Non-Linearity (INL) vs Code (25°C)

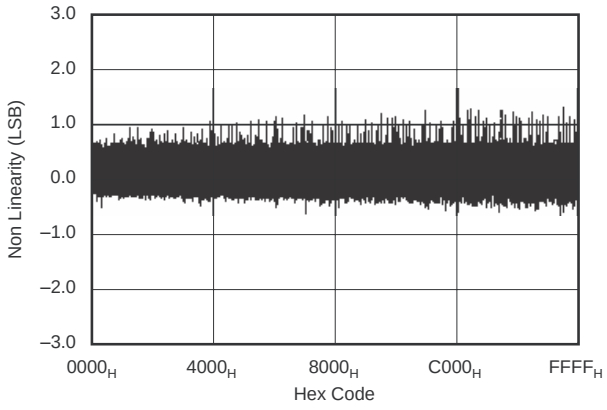


Figure 2. Differential Non-Linearity Error vs Code (25°C)

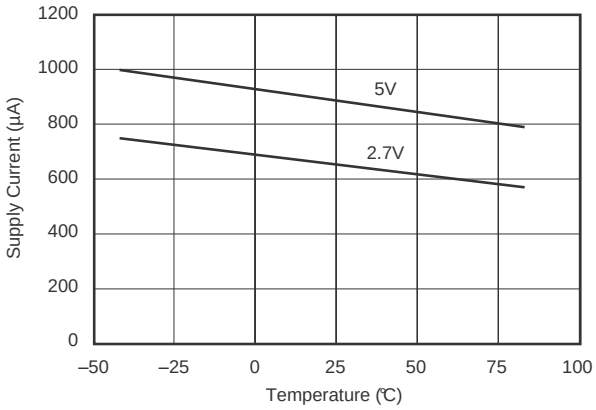


Figure 3. Supply Current vs Temperature

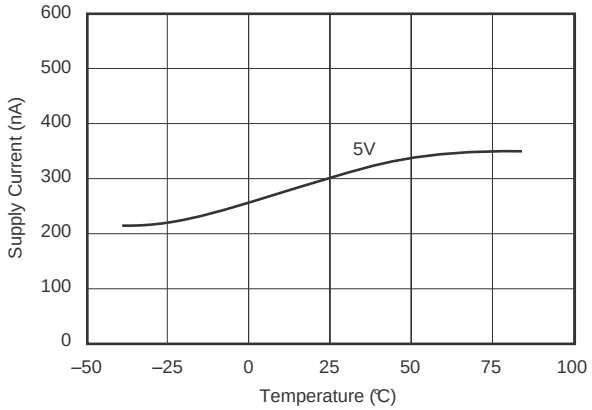


Figure 4. Power-Down Supply Current Code (25°C)

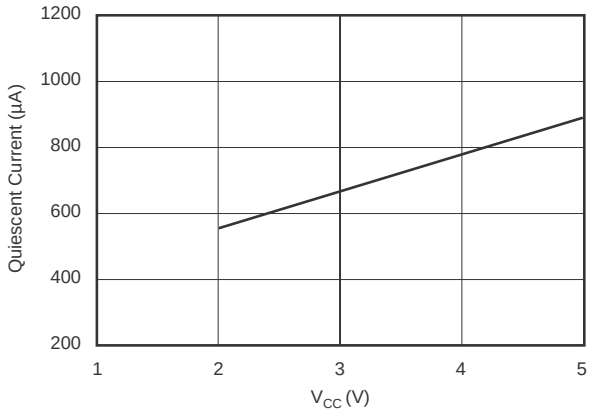


Figure 5. Quiescent Current vs V_{CC}

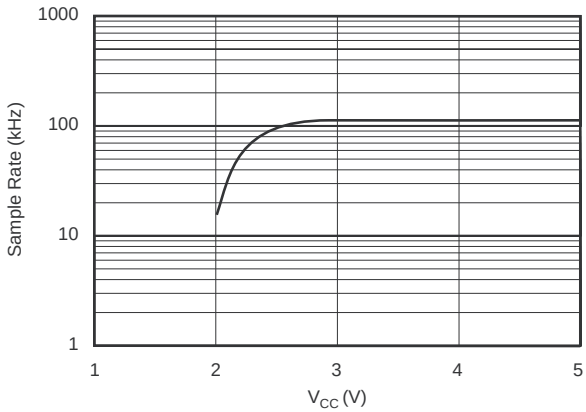


Figure 6. Maximum Sample Rate vs V_{CC}

Typical Characteristics (continued)

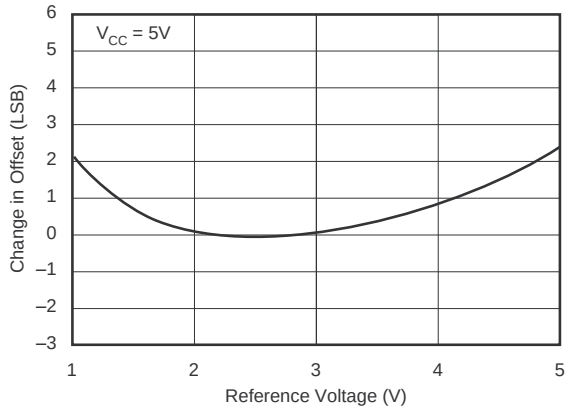


Figure 7. Change In Offset vs Reference Voltage

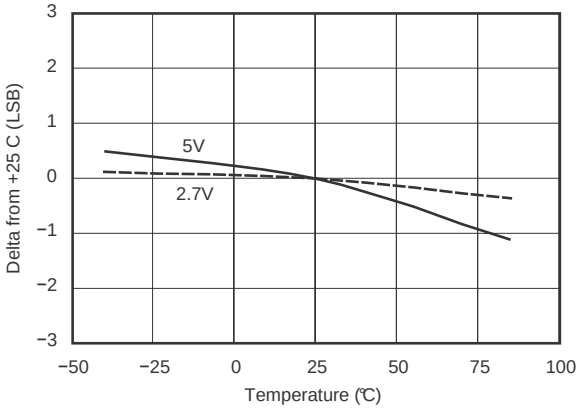


Figure 8. Change In Offset vs Temperature

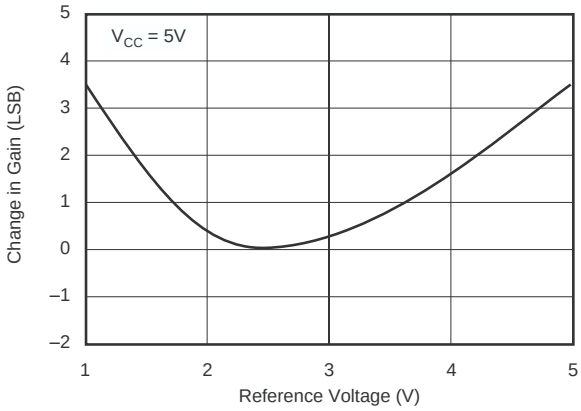


Figure 9. Change In Gain Error vs Reference Voltage

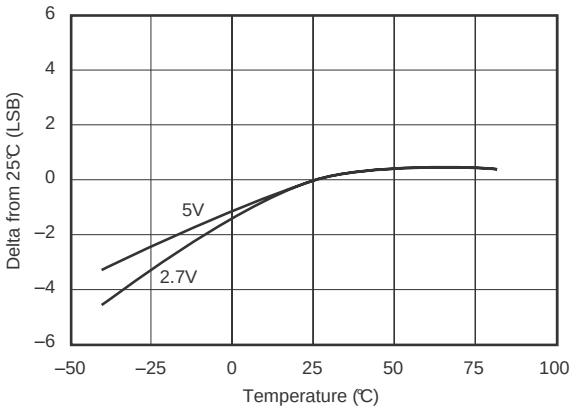


Figure 10. Change In Gain Error vs Temperature

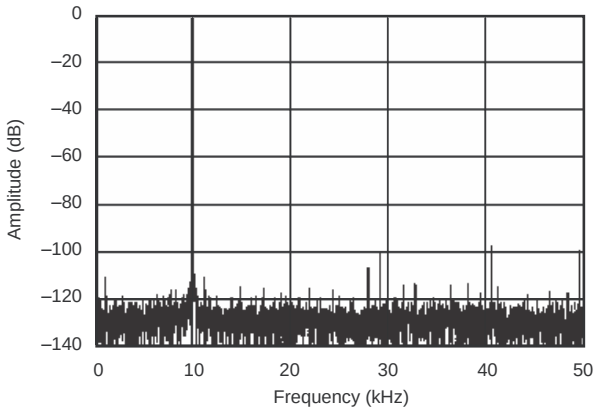


Figure 11. Frequency Spectrum (8192 Point FFT, FIN = 10.120 kHz, –0.3 dB)

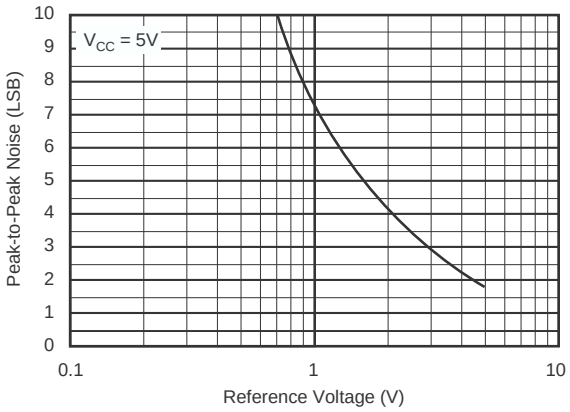


Figure 12. Peak-to-Peak Noise vs Reference Voltage

Typical Characteristics (continued)

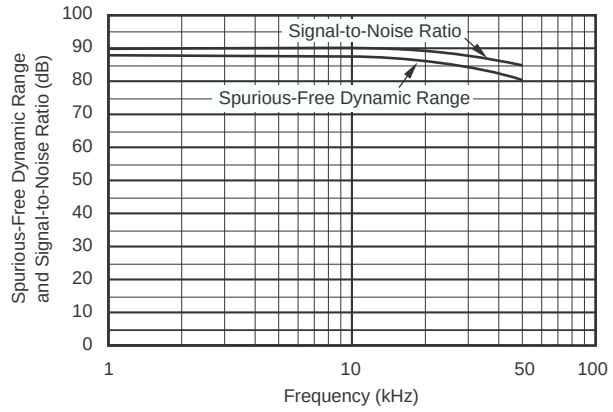


Figure 13. Spurious-Free Dynamic Range and Signal-to-Noise Ratio vs Frequency

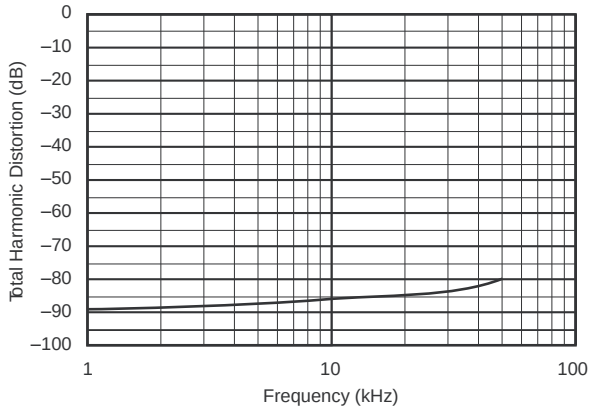


Figure 14. Total Harmonic Distortion vs Frequency

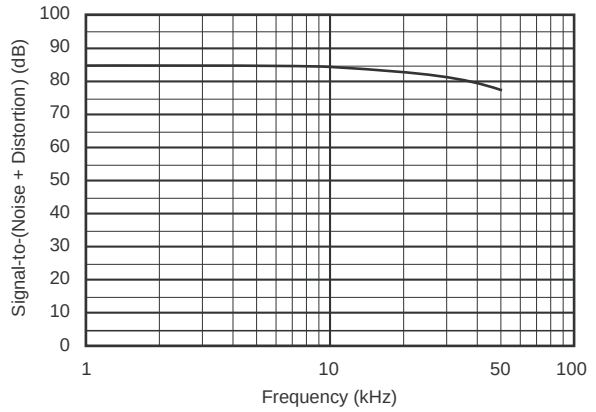


Figure 15. Signal-to-(Noise + Distortion) vs Frequency

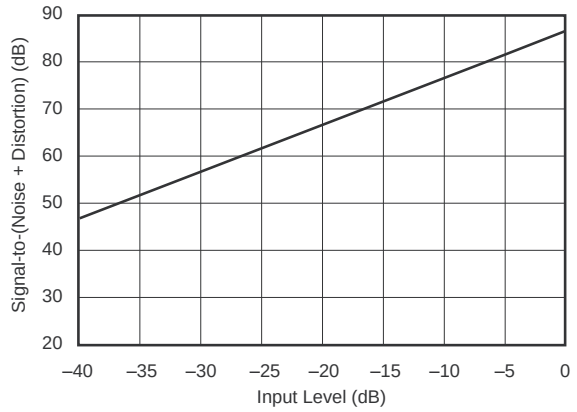


Figure 16. Signal-to-(Noise + Distortion) vs Input Level

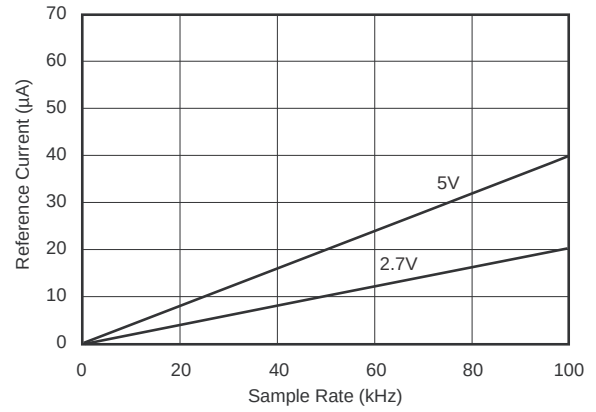


Figure 17. Reference Current vs Sample Rate

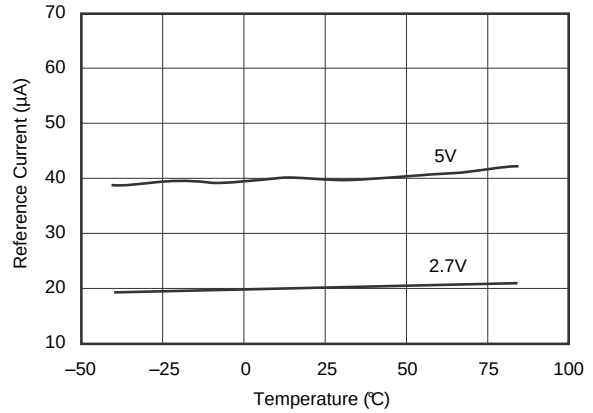


Figure 18. Reference Current vs Temperature

7 Detailed Description

7.1 Overview

The ADS8320 device is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution, which inherently includes a sample and hold function. The converter is fabricated on a 0.6µm CMOS process. The architecture and process allow the ADS8320 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 4.5 mW from $+V_{CC}$.

The ADS8320 requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 500 mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8320.

The external clock can vary between 24 kHz (1-kHz throughput) and 2.4 MHz (100-kHz throughput). The duty cycle of the clock is essentially unimportant, as long as the minimum high and low times are at least 200 ns (V_{CC} = 2.7 V or greater). The minimum clock frequency is set by the leakage on the capacitors internal to the ADS8320.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the D_{CLOCK} input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8320 after the conversion is complete and to obtain the serial data least significant bit first. See *Device Functional Modes* for more information.

7.1.1 Typical Connection Diagram

Figure 19 shows a basic data acquisition system. The ADS8320 input range is 0 V to V_{CC}, as the reference input is connected directly to the power supply. The 5-Ω resistor and 1-µF to 10-µF capacitor filter the microcontroller *noise* on the supply, as well as any high-frequency noise from the supply itself. The exact values must be picked such that the filter provides adequate rejection of the noise.

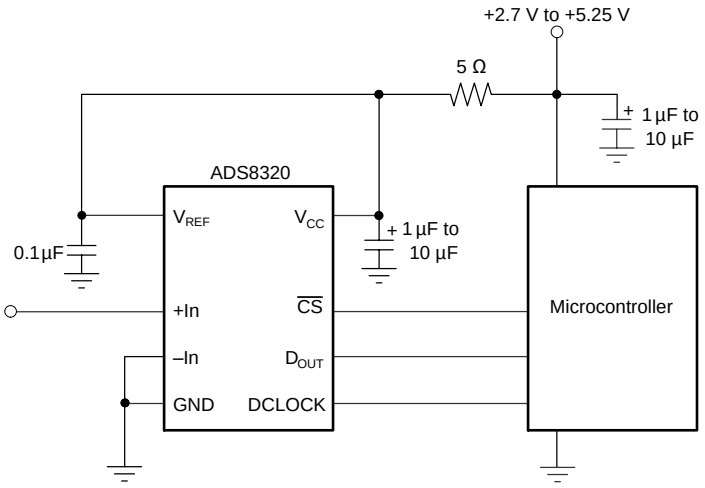
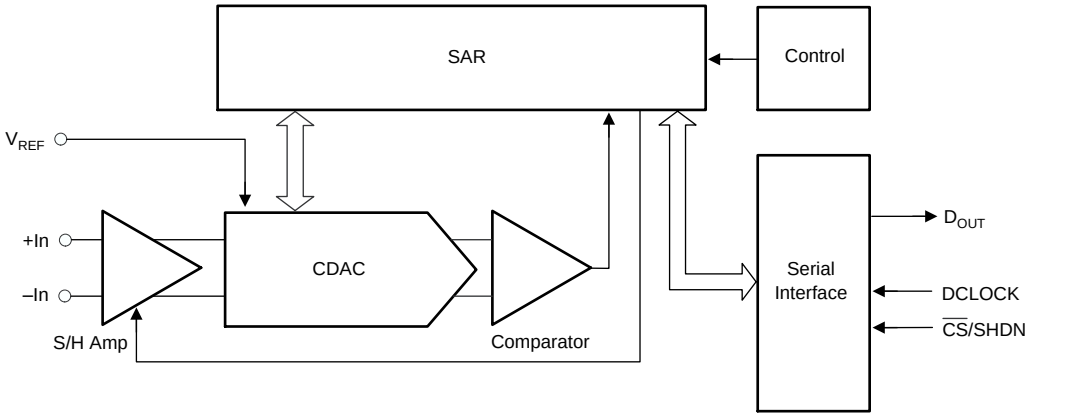


Figure 19. Typical Connection Diagram With ADS8320

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The +In and –In input pins allow for a differential input signal. Unlike some converters of this type, the –In input is not resampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and –In is captured on the internal capacitor array.

The range of the –In input is limited to –0.1 V to 1 V (–0.1 V to 0.5 V when using a 2.7-V supply). Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS8320 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to a 16-bit settling level within 4.5 clock cycles. When the converter goes into the hold mode or while it is in the power down mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –In input must not drop below GND – 100 mV or exceed GND + 1 V. The +In input must always remain within the range of GND – 100 mV to V_{CC} + 100 mV. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with lowpass filters must be used.

7.3.2 Reference Input

The external reference sets the analog input range. The ADS8320 operates with a reference in the range of 500 mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter appears to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter also appears to increase with lower LSB size. With a 5-V reference, the internal noise of the converter typically contributes only 1.5-LSB peak-to-peak of potential error to the output code. When the external reference is 500 mV, the potential error contribution from the internal noise is 10 times larger (15 LSBs). The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, see Figure 12. Note that the Effective Number of Bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1-kHz, 0-dB input signal. SINAD is related to ENOB as shown in Equation 1.

Feature Description (continued)

$$SINAD = 6.02 \times ENOB + 1.76 \quad (1)$$

With lower reference voltages, extra care must be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is also more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

7.3.3 Noise

The noise floor of the ADS8320 itself is extremely low, as can be seen from Figure 20 and Figure 21, and is much lower than competing A/D converters. It was tested by applying a low-noise DC input and a 5-V reference to the ADS8320 and initiating 5000 conversions. The digital output of the A/D converter varies in output code due to the internal noise of the ADS8320. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution must appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions represents the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this yields the ±3σ distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8320, with < 3 output codes for the ±3σ distribution, yields a <±0.5-LSB transition noise. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50 µV.

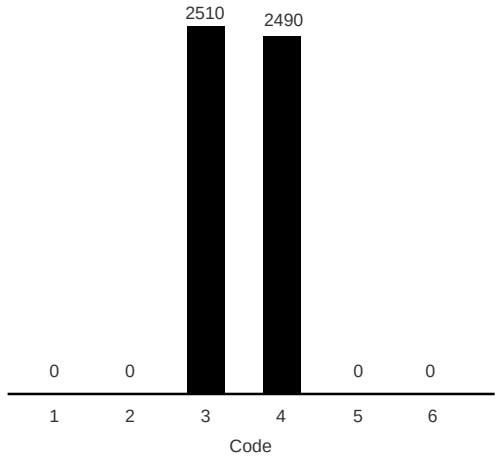


Figure 20. Histogram of 5000 Conversions of a DC Input at the Code Transition

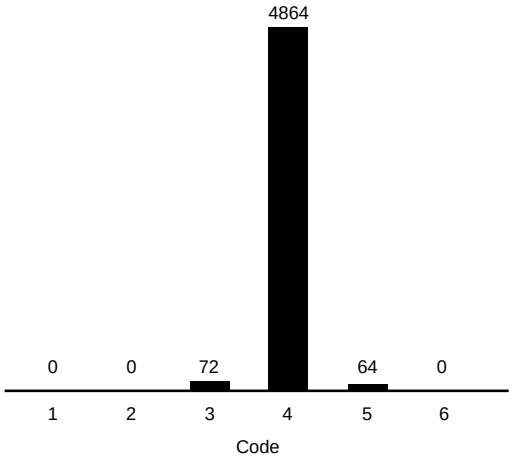


Figure 21. Histogram of 5000 Conversions of a DC Input at the Code Center

7.3.4 Averaging

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging four conversion results reduces the transition noise by 1/2 to ±0.25 LSBs. Averaging must only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio improves 3 dB.

7.4 Device Functional Modes

7.4.1 Signal Levels

The digital inputs of the ADS8320 can accommodate logic levels up to 5.5 V regardless of the value of V_{CC}. Thus, the ADS8320 can be powered at 3 V and still accept inputs from logic powered at 5 V.

The CMOS digital output (D_{OUT}) swings 0 V to V_{CC}. If V_{CC} is 3 V and this output is connected to a 5-V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

Device Functional Modes (continued)

7.4.2 Serial Interface

The ADS8320 communicates with microprocessors and other digital systems through a synchronous 3-wire serial interface, as shown in Figure 3 and Table 1. The D_{CLOCK} signal synchronizes the data transfer with each bit being transmitted on the falling edge of D_{CLOCK}. Most receiving systems capture the bitstream on the rising edge of D_{CLOCK}. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of D_{CLOCK} to capture each bit.

A falling CS signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling D_{CLOCK} edge, D_{OUT} is enabled and outputs a LOW value for one clock period. For the next 16 D_{CLOCK} periods, D_{OUT} outputs the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks repeat the output data but in a least significant bit first format.

After the most significant bit (B15) has been repeated, D_{OUT} tri-states. Subsequent clocks has no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

Table 1. Timing Specifications (V_{CC} = 2.7 V and Above, –40°C to 85°C)

		MIN	TYP	MAX	UNIT
t_{SMPL}	Analog input sample time	4.5		5	Clock Cycles
t_{CONV}	Conversion time		16		Clock Cycles
t_{CYC}	Throughput rate			100	kHz
t_{CSD}	$\overline{CS}$ falling to D_{CLOCK} LOW			0	ns
t_{SUCS}	$\overline{CS}$ falling to D_{CLOCK} rising	20			ns
t_{hDO}	D_{CLOCK} falling to current D_{OUT} not valid	5	15		ns
t_{dDO}	D_{CLOCK} falling to next D_{OUT} not valid		30	50	ns
t_{dis}	CS rising to D_{OUT} Tri-state		70	100	ns
t_{en}	D_{CLOCK} falling to D_{OUT}		20	50	ns
t_f	D_{OUT} fall time		5	25	ns
t_r	D_{OUT} rise time		7	25	ns

7.4.3 Data Format

The output data from the ADS8320 is in straight binary format, as shown in Table 2. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

Table 2. Ideal Input Voltages

DESCRIPTION	ANALOG VALUE
Full-scale range	V_{REF}
Least significant bit (LSB)	$V_{REF}/65,536$
Full-scale	V_{REF} – 1 LSB
Midscale	$V_{REF}/2$
Midscale – 1 LSB	$V_{REF}/2$ – 1 LSB
Zero	0 V

Table 3. Ideal Output Codes

DIGITAL OUTPUT STRAIGHT BINARY	
BINARY CODE	HEX CODE
1111 1111 1111 1111	FFF
1000 0000 0000 0000	8000
0111 1111 1111 1111	7FFF
0000 0000 0000 0000	0000

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To maximize the performance of data acquisition (DAQ) system based on a high-precision, successive approximation register (SAR), and analog-to-digital converter (ADC), the input driver and the reference driver circuits must be designed properly and must be optimized. This section introduces some application circuits designed using the ADS8320, and the detailed information for the some general principles designing these circuits can be referred to the related documentation.

8.2 Typical Applications

8.2.1 Universal Sensor IF SAR Booster Pack

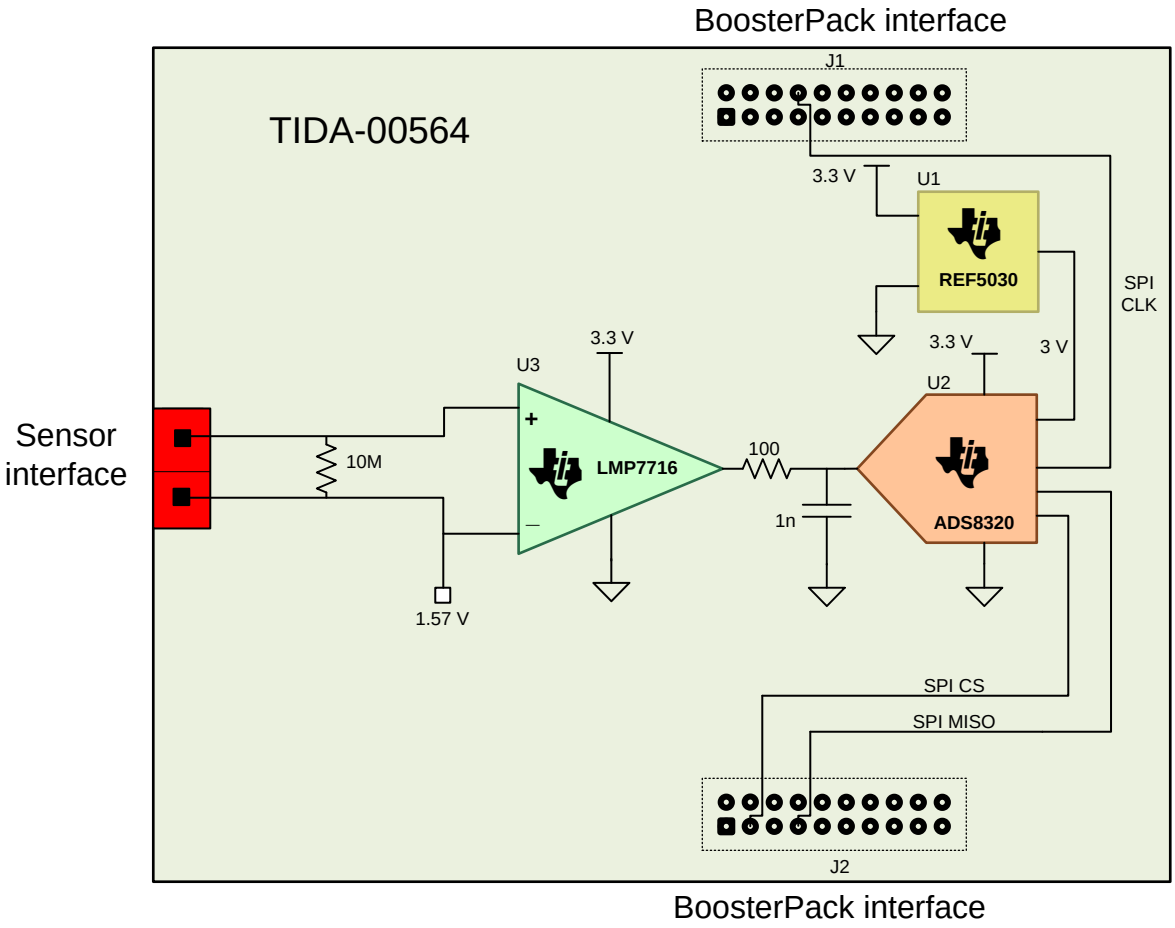


Figure 22. Block Diagram for Universal Sensor IF SAR Booster Pack

Typical Applications (continued)

8.2.1.1 Design Requirements

This TI Design is a universal sensor IF based on a successive approximation register (SAR) ADC built in a Booster Pack form factor to be easily connected to TI LaunchPad for development and testing. The analog front end (AFE) of the board has been designed for sensors with low output voltage range and high output impedance such as thermopiles, infrared (IR) thermometers, thermocouple amplifiers, pH electrode buffers, piezoelectric accelerometers, and many others.

This application circuit for ADS8320 is designed to achieve the key specifications:

- 16-bit 100 KHz
- Low-input referred noise and low-input bias (100 fA)
- Ideal choice for high-impedance output sensors

8.2.1.2 Detailed Design Procedure

The ADS8320 was selected in this design because it best matches the design's input requirements and high performance. The maximum throughput rate of the ADS8320 is 100 ksps, the resolution is equal to 16 bits, and the input range of the ADS8320 is equal to the reference voltage supplied to the converter. In this design, the reference voltage is equal to 3 V. The REF5030 features low noise, very low drift, and high initial accuracy for high-performance data converters. The output of the REF5030 is 3 V, which fixes the voltage range of the ADC and can provide a stable reference voltage to maintain the accuracy.

Because the system is targeted for high-impedance output sensors, CMOS or JFET input amplifiers are preferable. The LMP7716 is a CMOS amplifier with low-input referred noise and low-input bias current, which make it an ideal choice for sensor interfaces such as thermopiles, IR thermometers, thermocouple amplifiers, and pH electrode buffers. To ensure the amplifier settles in enough time for the ADC to complete the signal acquisition. The gain bandwidth product of the amplifier is high enough to make sure that the input signal bandwidth is accounted for, and the amplifier is stable with the filter load. The amplifier has a fast slew rate to charge the filter changes and to quickly react to changes of the input.

A low-pass filter must be placed between the input of the ADC and input amplifier. Choosing the capacitor and resistor values play an important role to have a good AFE design. CFLT serves two purposes. Firstly, this capacitor stores energy to charge the ADC internal sampling capacitor. Secondly, CFLT provides a place for the internal capacitor's charge to go. Due to the storage capabilities of CFLT, this design guide sometimes refers to this capacitor as the *flywheel* capacitor. CFLT has this alternative name because, like a flywheel, it stores energy for the acquisition time of the ADC. Another name used to describe CFLT is *charge reservoir*. This TI design has a CFLT equal to 1 nF. This capacitor must be a high-quality capacitor with low voltage and frequency coefficients. The recommended capacitor type is C0G. As a check, make sure the filter capacitor value chosen is at least 20 times the internal capacitor value of ADC. In this case, the value is more than 20 times the size.

The external R_{FLT} | C_{FLT} in the low-pass filter must settle within the ADC acquisition time. As a rule of thumb, set the external R_{FLT} | C_{FLT} settling time constant a bit faster than ideal (for example, 60%) to allow a margin for error of the op-amp load transient and the small signal settling time. TI design has an RFLT equal to 100 Ω. The detailed discussion and calculation can be found in *Universal Sensor IF SAR BoosterPack* (TIDUAI7).

Typical Applications (continued)

8.2.1.3 Application Curves

8.2.1.3.1 Static Test (DC)

Figure 23 shows the error, which is the measured output voltage minus the ideal output voltage.

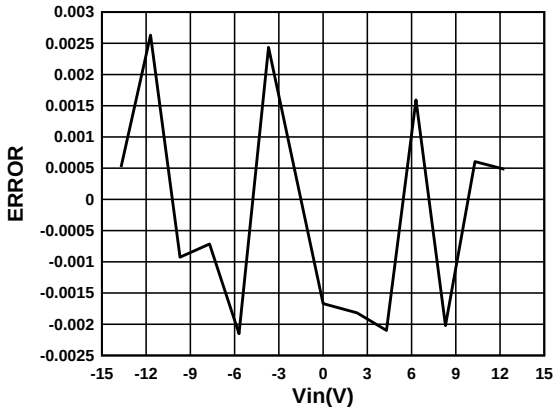


Figure 23. Error (Measured V_{OUT} Minus Ideal V_{OUT}) vs Input Voltage

8.2.1.3.2 Dynamic Test (AC)

For the dynamic test, sine wave is applied at the input of the board with fixed amplitude equal to –1 dBFS and a varying frequency of 0.5 kHz, 1 kHz, 5 kHz, and 10 kHz. Figure 24 shows the test result for 0.5 kHz.

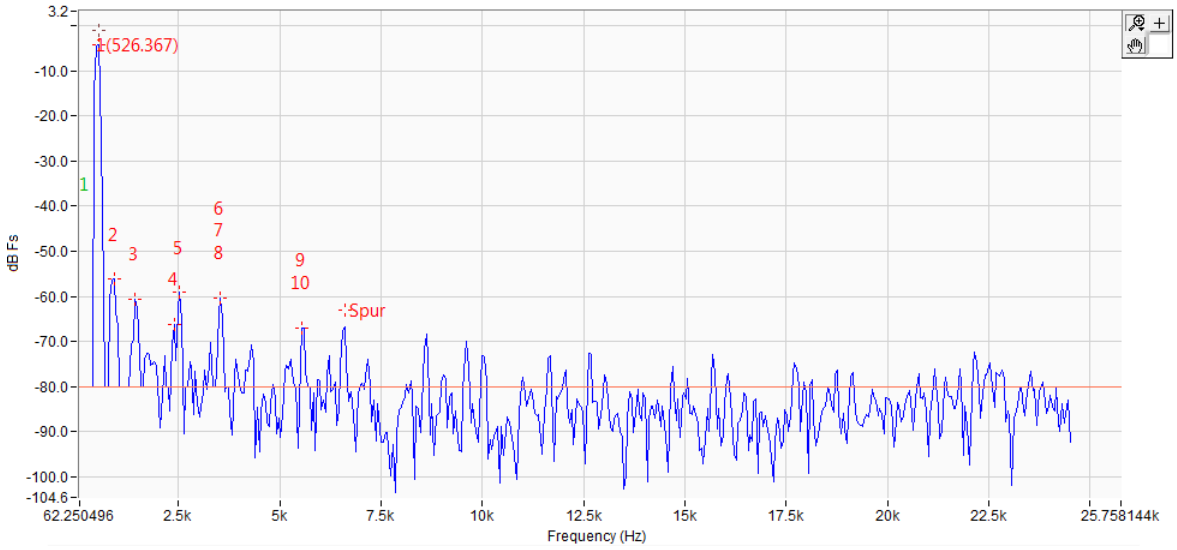


Figure 24. FFT at 500 Hz (Input Signal –1 dBFS)

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDA-00564, *Universal Sensor IF SAR Booster Pack Reference Design*.

8.2.2 Wireless Motor Monitor (WMM)

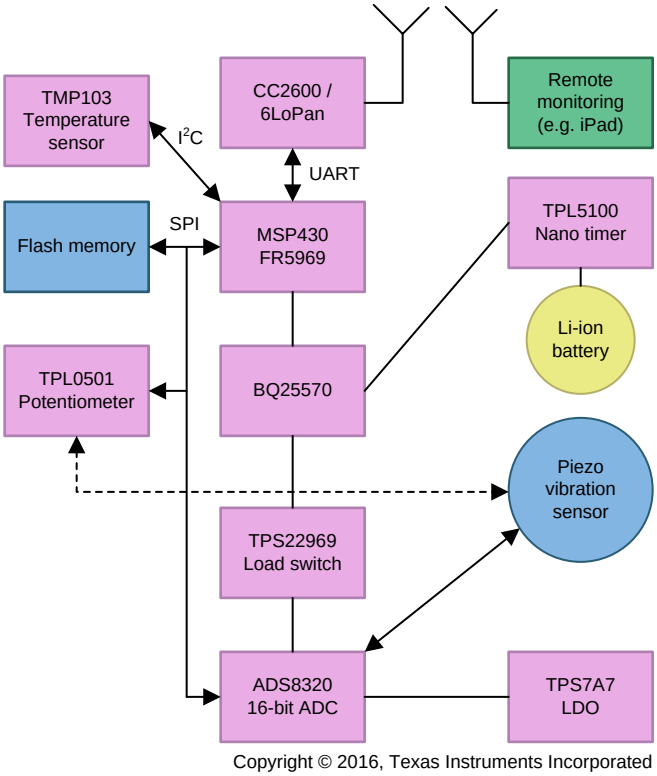


Figure 25. System Block Diagram for Wireless Motor Monitor (WMM)

8.2.2.1 Design Requirements

This application circuit for ADS8320 is designed to achieve the key specifications:

- 16-bit 100 KHz
- 4-K FFT for vibration spectral
- Optimized for ultra-low sleep-mode current: I_Q < 45-nA (typical; BQ-harvester in smart mode)

8.2.2.2 Detailed Design Procedure

This TI Design is inspired by the need to monitor the health of motors and machines to accurately predict and schedule maintenance (or replacement) while minimizing cost and down time during industrial production.

This design uses a Piezo vibration sensor to monitor machine vibrations, and a 16-bit precision SAR ADC, ADS8320, is connected to the Piezo shock sensor signal chain for signal acquisition. Because Piezo sensors have high-impedance output nodes, so it's important to carefully design the analog front-end (AFE) circuitry to reduce the noise and increase the sensitivity of the system, also drive ADS8320 and settle the signal properly during the acquisition time.

8.2.2.3 Application Curves

When testing the system with a portable speaker, the test result graph with 4-K FFT is shown in Figure 26.

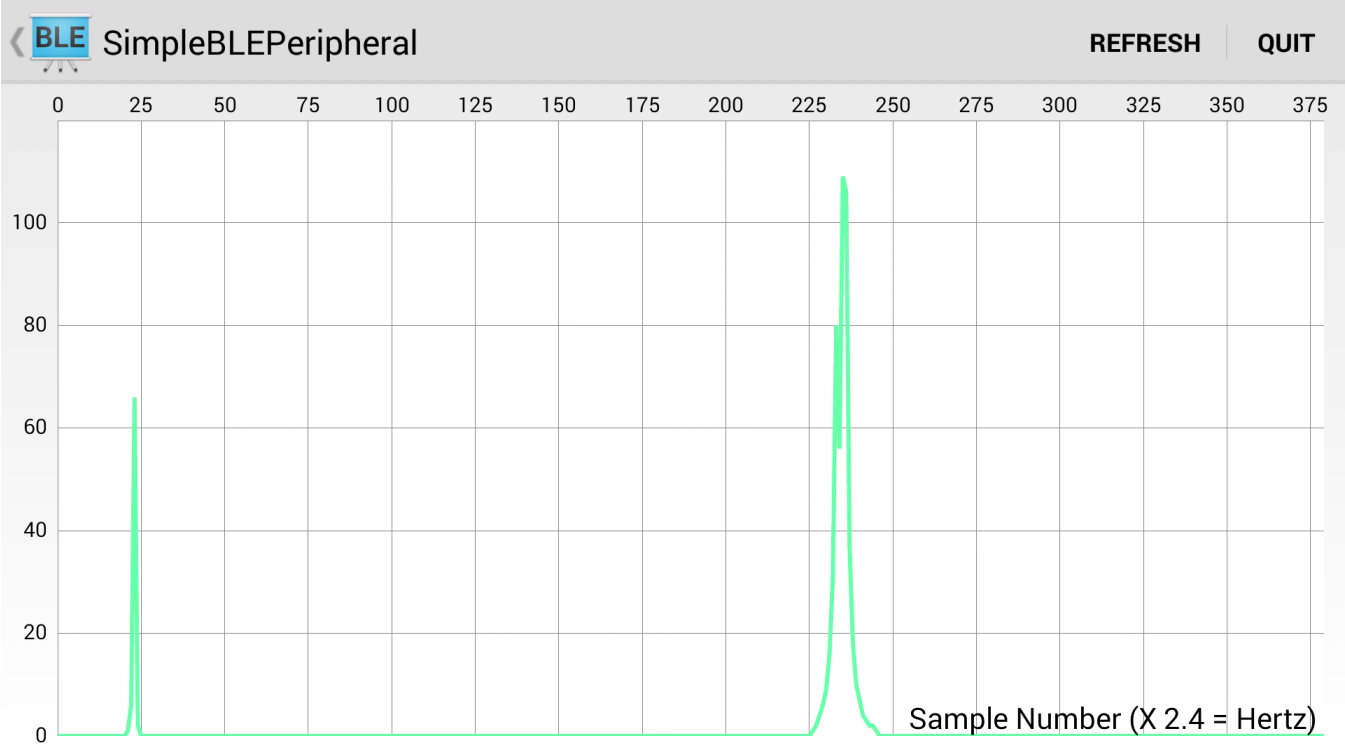


Figure 26. Android Screen Shot of FFT at 600-Hz Excitation With Portable Speaker

When testing the system with a shaker calibrated with a accelerometer, the ADC is used and the AFE gain is set to 11, then configure the software to output 0.1-g of vibration at 500 KHz (or 1.5 KHz, and 2.5 KHz) as depicted in Figure 27.

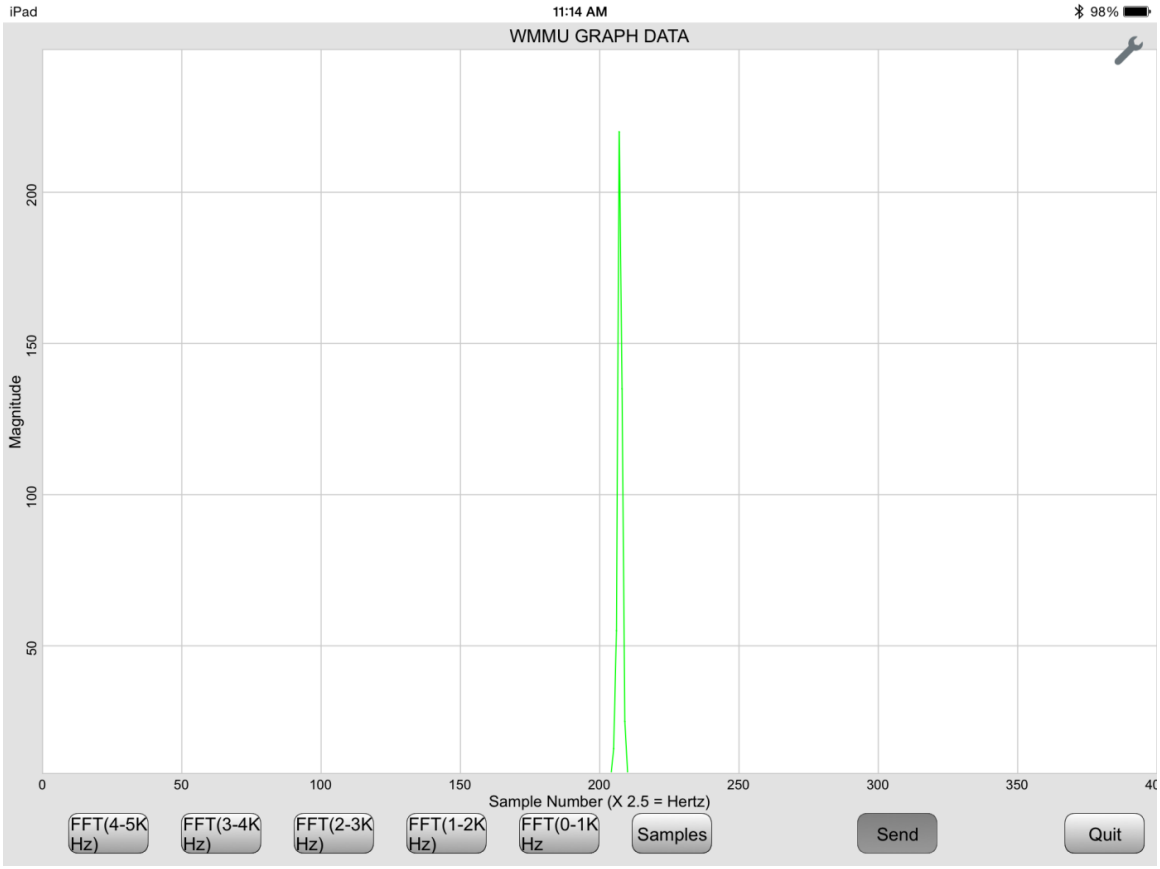


Figure 27. BLE Received FFT at 500-Hz 0.1-g Excitation (X 2.4 = Hertz)

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDM-WLMOTORMONITOR, *Wireless Motor Monitor Reference Design*.

9 Power Supply Recommendations

The ADS8320 is designed to operate using a simple power supply voltage from 2.0 V to 5.25 V, but the specifications are ensured over a 2.7-V to 5.25-V supply range. This supply must be well regulated and bypassed. A ceramic decoupling capacitor must be placed on the supply pin as close as possible to the ADS8320 package. In addition, a 1-µF to 10-µF capacitor and a 5-Ω or 10-Ω series resistor may be used to low-pass filter a noisy supply.

10 Layout

10.1 Layout Guidelines

For optimum performance, care must be taken with the physical layout of the ADS8320 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At a 100-kHz conversion rate, the ADS8320 makes a bit decision every 416 ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.

TI recommends following these layout guidelines:

- A printed-circuit board (PCB) with at least four layers to keep all critical components on the top layer.
- Analog input signals and the reference input signals must be kept away from noise sources. Crossing digital lines with the analog signal path must be avoided. The analog input and the reference signals are routed on to the left side of the board and the digital connections are routed on the right side of the device.
- Due to the dynamic currents that occur during conversion and data transfer, the supply pin ($+V_{CC}$) must have a decoupling capacitor that keeps the supply voltage stable. A 1-µF ceramic decoupling capacitor is recommended for the supply pin.
- A layout that interconnects the converter and accompanying capacitors with the low inductance path is critical for achieving optimal performance. Using 15-mil vias to interconnect components to a solid analog ground plane at the subsequent inner layer minimizes stray inductance. Avoid placing vias between the supply pin and the decoupling capacitor. Any inductance between the supply capacitor and the supply pin of the converter must be kept to less than 5 nH by placing the capacitor within 0.2 inches from the supply or input pins of the ADS8320 and by using 20-mil traces.
- Dynamic currents are also present at the REF pin during the conversion phase. Therefore, good decoupling is critical to achieve optimal performance. The inductance between the reference capacitor and the REF pin must be kept to less than 2 nH by placing the capacitor within 0.1 inches from the REFIN pin and by using 20-mil traces.
- A single 10-µF, X7R-grade, 0805-size ceramic capacitor with at least a 10-V rating for good performance over temperature range.
- A small, 0.1-Ω to 0.47-Ω, 0603-size resistor placed in series with the reference capacitor keeps the overall impedance low and constant, especially at very high frequencies.
- Avoid using additional lower value capacitors because the interactions between multiple capacitors can affect the ADC performance at higher sampling rates.
- Place the RC filters immediately next to the input pins. Among surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
- The GND pin on the ADS8320 must be placed on a clean ground plane. In many cases, this is the *analog* ground.

10.2 Layout Example

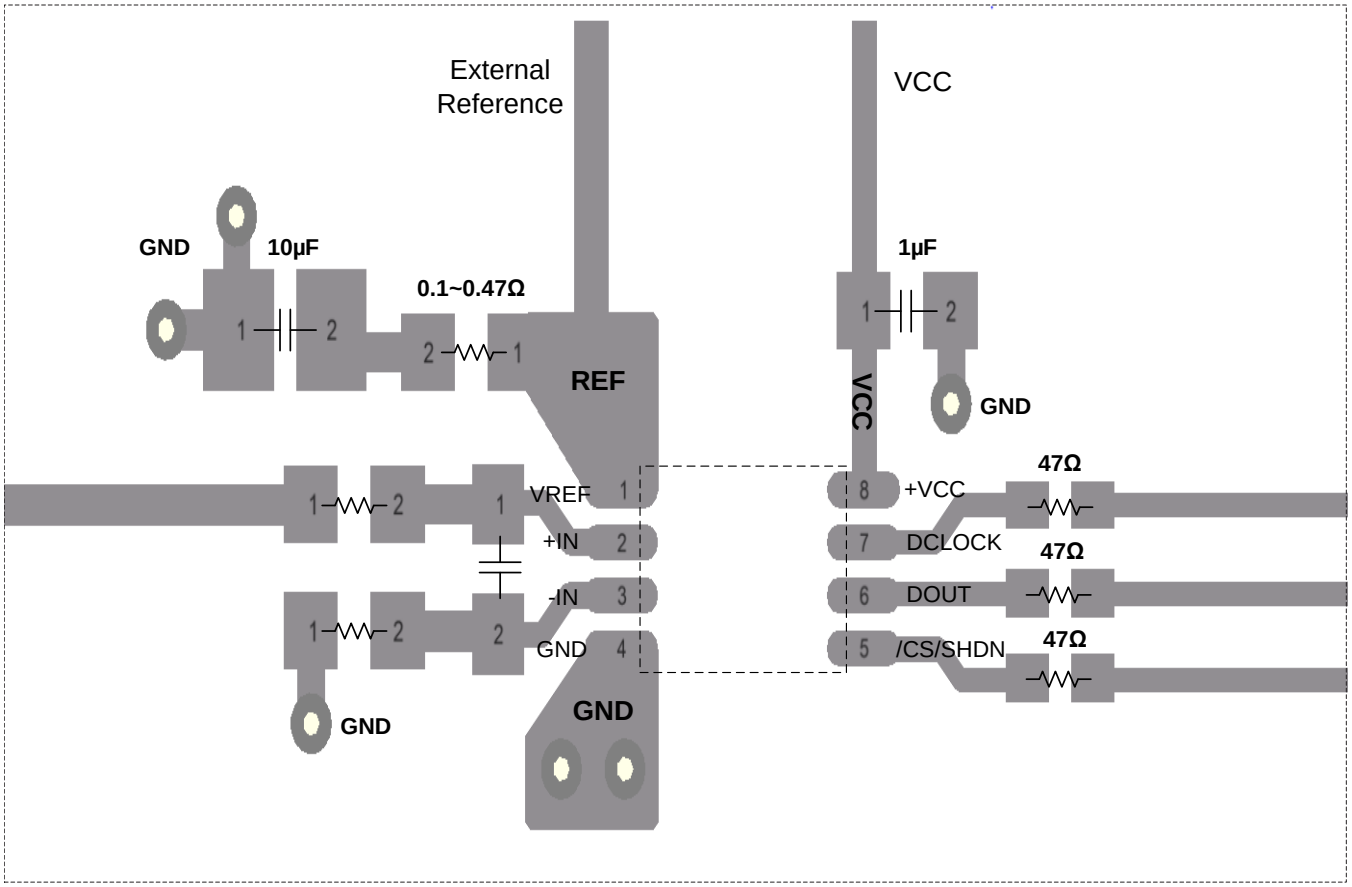


Figure 28. Layout Example

10.3 Power Dissipation

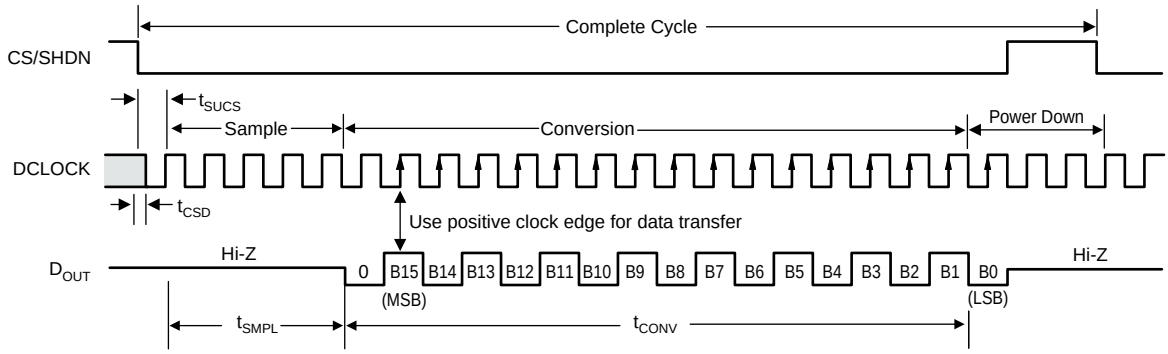
The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS8320 to convert at up to a 100kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8320 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that satisfies the requirements of the system.

In addition, the ADS8320 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (as shown in Figure 29). Ideally, each conversion must occur as quickly as possible, preferably at a 2.4-MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each D_{CLOCK} transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.

The following timing diagrams and test circuits pertain to the parameters in Table 1.

Power Dissipation (continued)



Minimum 22 clock cycles required for 16-bit conversion. Shown are 24 clock cycles.

If $\overline{CS}$ remains LOW at the end of conversion, a new datastream with LSB-first is shifted out again.

Figure 29. ADS8320 Basic Timing Diagrams

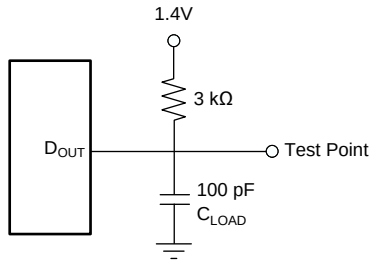


Figure 30. Load Circuit for t_{dDO}, t_r, and t_f

Figure 31. Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

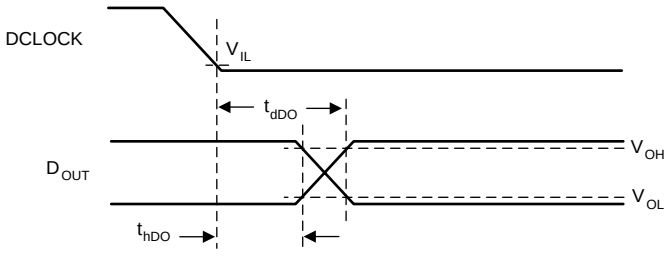
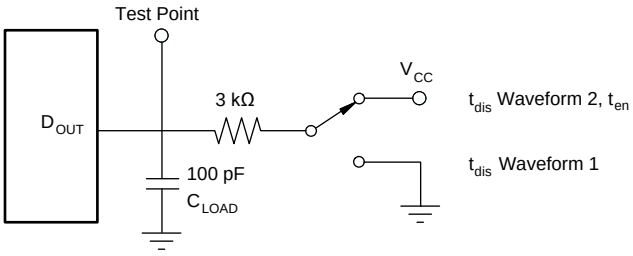


Figure 32. Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}

Power Dissipation (continued)



Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control. (2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

Figure 33. Load Circuit for t_{dDO}, t_r, and t_f Table 1

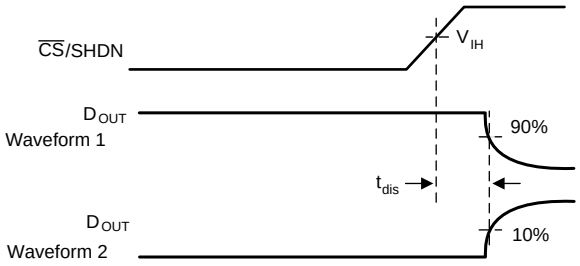


Figure 34. Voltage Waveforms for t_{dis}

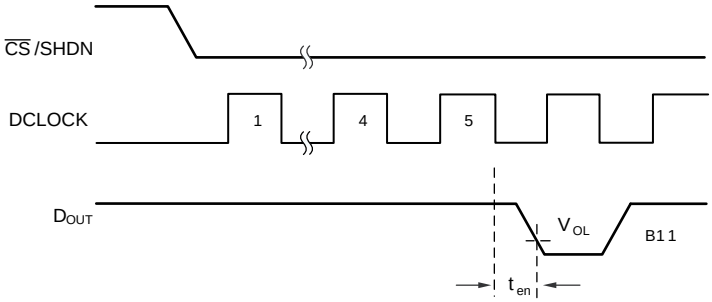


Figure 35. Voltage Waveforms for t_{en}

Figure 36 shows the current consumption of the ADS8320 versus sample rate. For this graph, the converter is clocked at 2.4 MHz regardless of the sample rate; $\overline{CS}$ is HIGH for the remaining sample period. Figure 37 also shows current consumption versus sample rate. However, in this case, the D_{CLOCK} period is 1/24th of the sample period—$\overline{CS}$ is HIGH for one D_{CLOCK} cycle out of every 16.

Power Dissipation (continued)

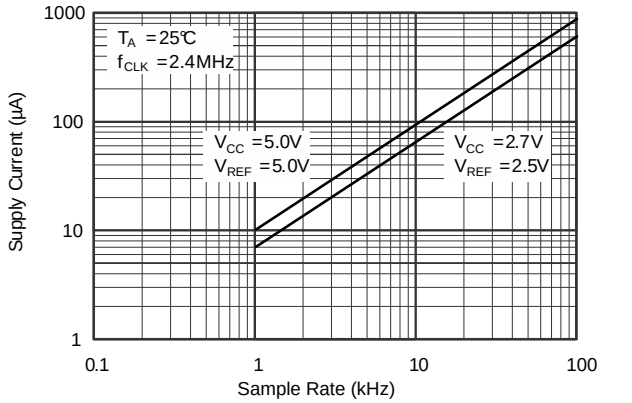


Figure 36. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Linearly With Sample Rate

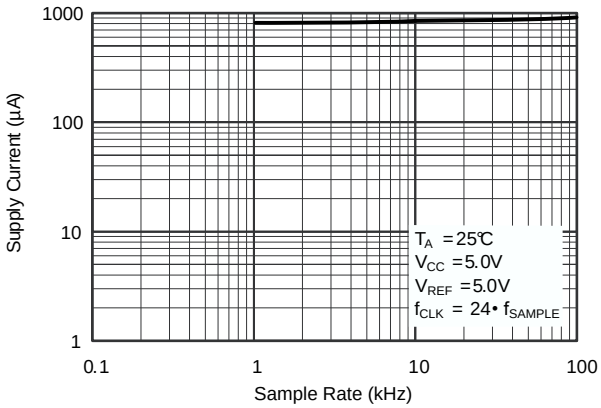
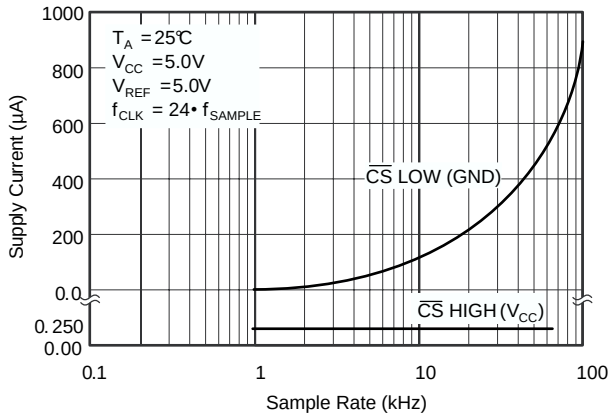


Figure 37. Scaling f_{CLK} Reduces Supply Current Only Slightly With Sample Rate

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode which is enabled when CS is HIGH. CS LOW shuts down only the analog section. The digital section is completely shut down only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption is not as low as when CS is HIGH. Figure 38 shows more information.

Power dissipation can also be reduced by lowering the power-supply voltage and the reference voltage. The ADS8320 operates over a V_{CC} range of 2 V to 5.25 V. However, at voltages below 2.7 V, the converter does not run at a 100-kHz sample rate. See *Typical Characteristics* for more information regarding power supply voltage and maximum sample rate.



Shutdown current with $\overline{CS}$ LOW varies with sample rate

Figure 38. Shutdown Current With $\overline{CS}$ HIGH is 50 nA (Typically, Regardless of the Clock)

10.3.1 Short Cycling

Another way of saving power is to use the CS signal to short cycle the conversion. Because the ADS8320 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are required, then the conversion can be terminated (by pulling CS HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be required. If so, the conversion can be terminated after the first n bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power-down mode.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Universal Sensor IF SAR BoosterPack* (TIDUAI7)
- TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* (TIDU032)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SPI, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8320E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320EB/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320EB/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples
ADS8320EB/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A20	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

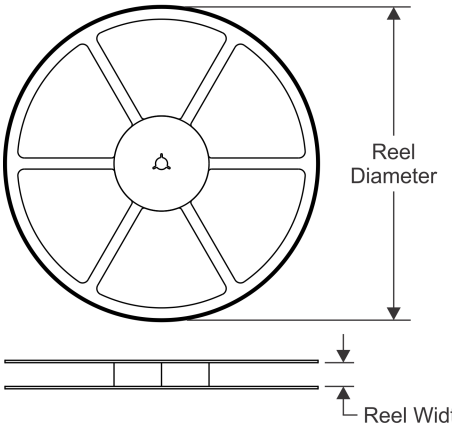
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS8320 :

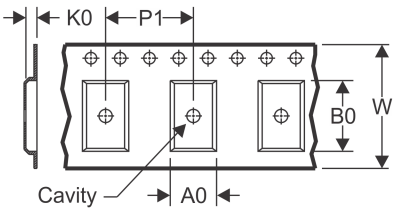
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

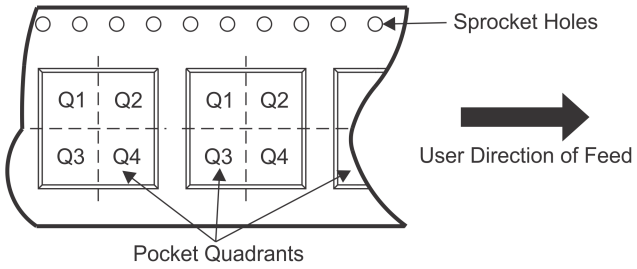


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

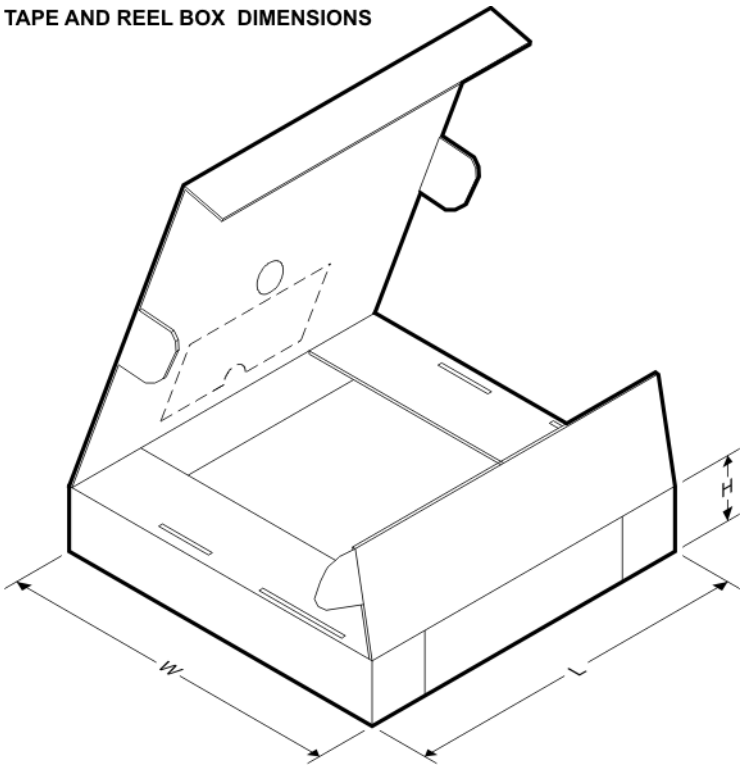
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8320E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8320E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8320EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8320EB/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

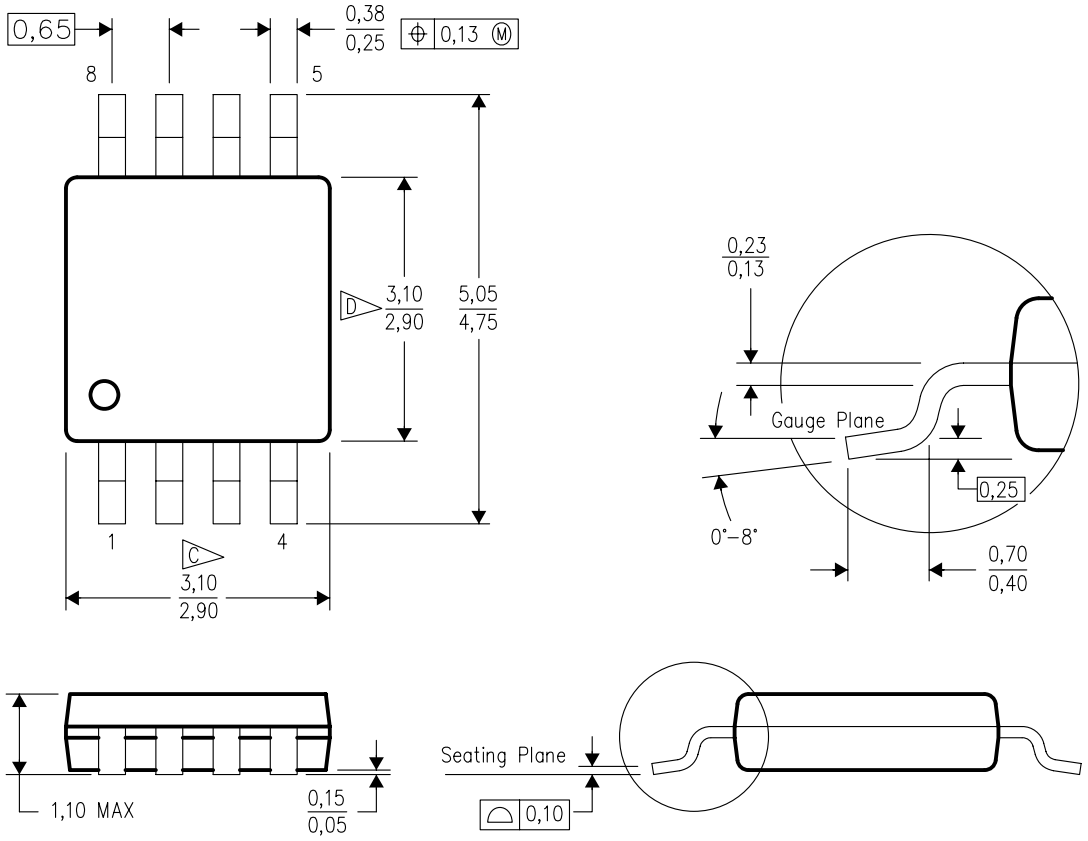
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8320E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8320E/2K5	VSSOP	DGK	8	2500	350.0	350.0	43.0
ADS8320EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8320EB/2K5	VSSOP	DGK	8	2500	350.0	350.0	43.0

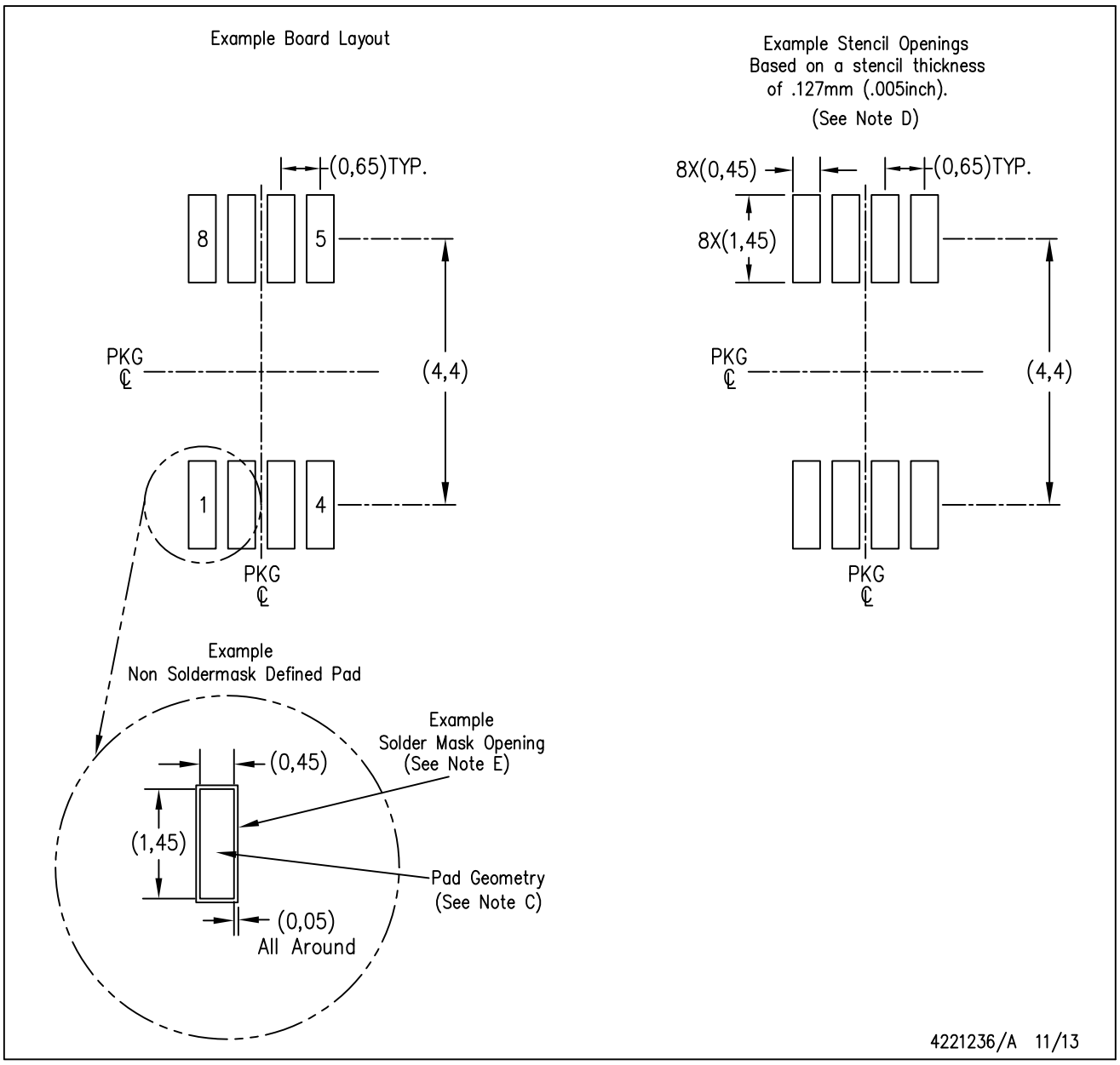
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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