ADS830



SBAS086A – APRIL 2001

SpeedPLUS™ 8-Bit, 60MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SNR: 49.5dB
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE: 1Vp-p/2Vp-p
- LOW POWER: 170mW
- LOW DNL: 0.2LSB
- SINGLE +5V SUPPLY OPERATION
- SSOP-20 PACKAGE

APPLICATIONS

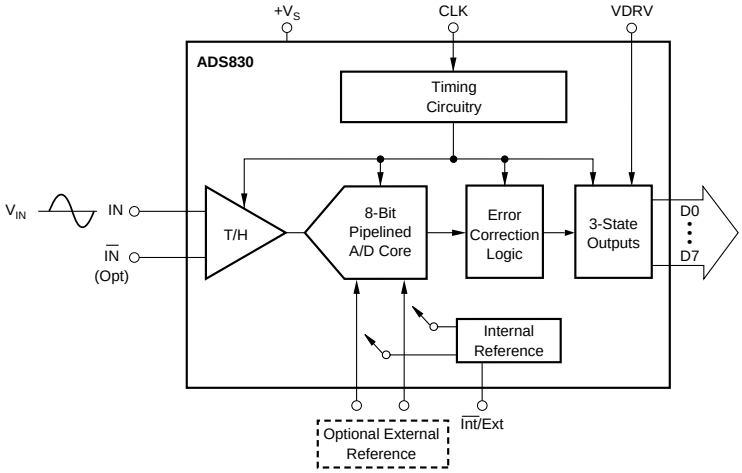
- MEDICAL IMAGING
- VIDEO DIGITIZING
- COMMUNICATIONS
- DISK-DRIVE CONTROL

DESCRIPTION

The ADS830 is a pipeline, CMOS Analog-to-Digital (A/D) converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where DC full scale range adjustment is required.

The ADS830 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation.

The ADS830 is specified at a maximum sampling frequency of 60MHz and a single-ended input range of 1.5V to 3.5V. The ADS830 is available in a SSOP-20 package and is pin-for-pin compatible with the 8-bit, 80MHz ADS831.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	–0.3V to ($+V_S$ + 0.3V)
Logic Input	–0.3V to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

DEMO BOARD ORDERING INFORMATION

PRODUCT	DEMO BOARD
ADS830	DEM-ADS830E

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS830E	SSOP-20 (QSOP)	349	–40°C to +85°C	ADS830E	ADS830E	Rails
"	"	"	"	"	ADS830E/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS830E/1K" will get a single 1000-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS830E MIN	ADS830E TYP	ADS830E MAX	UNITS
RESOLUTION			8 Guaranteed		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Single-Ended Input Range	2Vp-p	1.5		3.5	V
Optional Single-Ended Input Range	1Vp-p	2		3	V
Common-Mode Voltage			2.5		V
Optional Differential Input Range	2Vp-p	2		3	V
Analog Input Bias Current			1		µA
Input Impedance			1.25 || 5		MΩ || pF
Track-Mode Input Bandwidth	–3dBFS		300		MHz
CONVERSION CHARACTERISTICS					
Sample Rate		10k		60M	Samples/s
Data Latency			4		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (Largest Code Error)					
f = 1MHz			±0.1	±1.0	LSB
f = 10MHz			±0.2		LSB
No Missing Codes			Guaranteed		
Integral Nonlinearity Error, f = 1MHz			±0.3	±1.5	LSBs
Spurious Free Dynamic Range(1)					
f = 1MHz (–1dB input)			67		dBFS(2)
f = 10MHz (–1dB input)		54	65		dBFS
Two-Tone Intermodulation Distortion(3)					
f = 9.5MHz and 9.9MHz (–7dB each tone)			–60		dBc
Signal-to-Noise Ratio (SNR)	Referred to Full Scale				
f = 1MHz			49.5		dB
f = 10MHz		47	49.5		dB
Signal-to-(Noise + Distortion) (SINAD)	Referred to Full Scale				
f = 1MHz			48		dB
f = 10MHz		45	48		dB
Effective Number of Bits(4), f = 1MHz			7.7		Bits
Differential Gain Error	NTSC, PAL		0.2		%
Differential Phase Error	NTSC, PAL		0.2		degrees
Output Noise	Input Tied to Common-Mode		0.2		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			1.2		ps rms
Overvoltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			2.5		ns

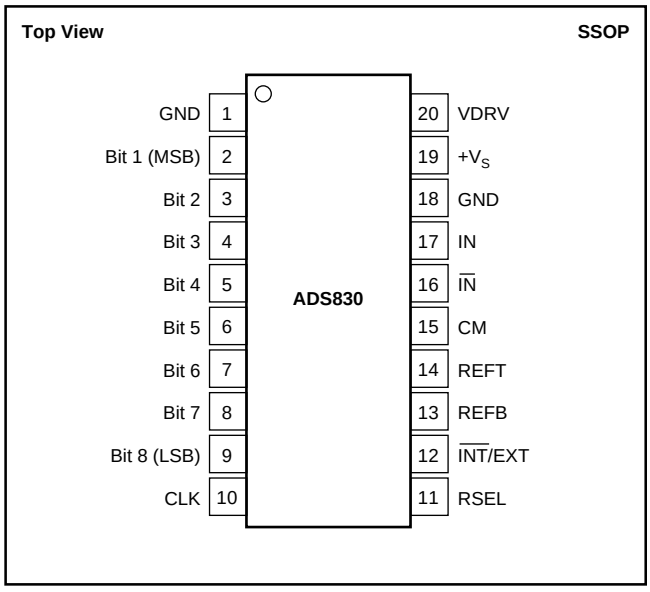
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 60MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS830E MIN	ADS830E TYP	ADS830E MAX	UNITS
DIGITAL INPUTS					
Logic Family			CMOS/TTL Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = 5V)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+2.4			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS/TTL Compatible		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA)	VDRV = 5V			+0.1	V
Low Output Voltage, (I_{OL} = 1.6mA)				+0.2	V
High Output Voltage, (I_{OH} = 50µA)		+4.9			V
High Output Voltage, (I_{OH} = 0.5mA)		+4.8			V
Low Output Voltage, (I_{OL} = 50µA)	VDRV = 3V			+0.1	V
High Output Voltage, (I_{OH} = 50µA)		+2.8			V
Output Capacitance			5		pF
ACCURACY (External Reference, 2Vp-p, Unless Otherwise Noted)	f_S = 2.5MHz				
Zero Error (Referred to –FS)	at 25°C	–2.5	±0.25	+2.5	%FS
Zero Error Drift (Referred to –FS)			±53		ppm/°C
Gain Error[6]	at 25°C	–2.5	±0.3	+2.5	%FS
Gain Error Drift[6]			±75		ppm/°C
Power Supply Rejection of Gain	ΔV_S = ±5%		58		dB
Internal REFT Tolerance	Deviation from Ideal 3.0V		±10	±100	mV
Internal REFB Tolerance	Deviation from Ideal 2.0V		±10	±100	mV
External REFT Voltage Range		REFB + 0.8	3.0	V_S – 1.25	V
External REFB Voltage Range		1.25	2.0	REFT – 0.8	V
Reference Input Resistance	REFT to REFB		800		kΩ
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		37	45	mA
Power Dissipation: VDRV = 5V	External Reference		185	225	mW
VDRV = 3V	External Reference		170		mW
VDRV = 5V	Internal Reference		215		mW
VDRV = 3V	Internal Reference		200		mW
Thermal Resistance, θ_{JA}					
SSOP-20			115		°C/W

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76) /6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Excludes internal reference.

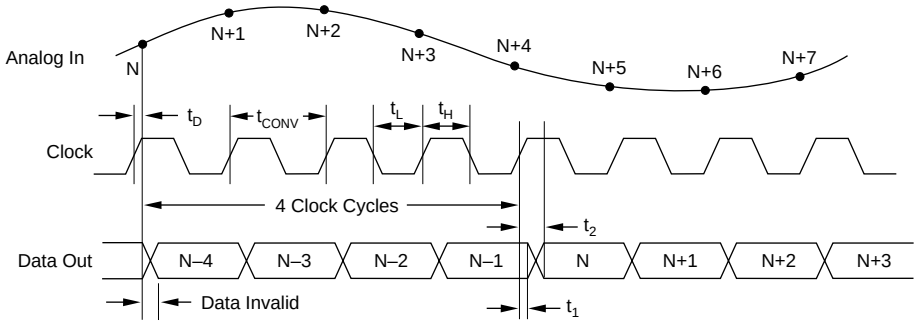
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	Bit 1	Data Bit 1 (D7) (MSB)
3	Bit 2	Data Bit 2 (D6)
4	Bit 3	Data Bit 3 (D5)
5	Bit 4	Data Bit 4 (D4)
6	Bit 5	Data Bit 5 (D3)
7	Bit 6	Data Bit 6 (D2)
8	Bit 7	Data Bit 7 (D1)
9	Bit 8	Data Bit 8 (D0) (LSB)
10	CLK	Convert Clock
11	RSEL	Input Range Select: HI = 2V; LO = 1V
12	INT/EXT	Reference Select: HI = External; LO = Internal
13	REFB	Bottom Reference
14	REFT	Top Reference
15	CM	Common-Mode Voltage Output
16	IN	Complementary Input
17	IN	Analog Input
18	GND	Ground
19	+VS	+5V Supply
20	VDRV	Output Logic Drive Supply Voltage

TIMING DIAGRAM

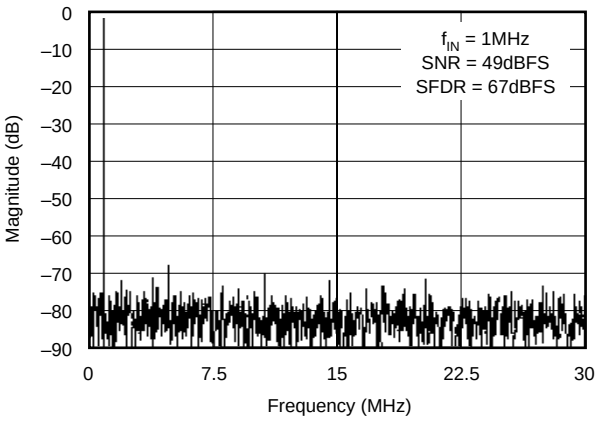


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	16.6		100µs	ns
t_L	Clock Pulse Low	7.3	8.3		ns
t_H	Clock Pulse High	7.3	8.3		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max		5.9	12	ns

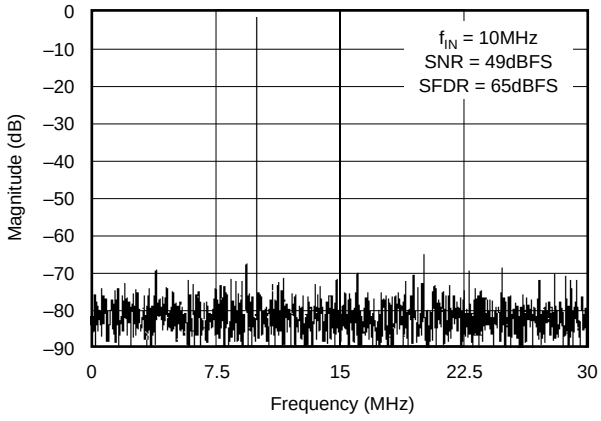
TYPICAL CHARACTERISTICS

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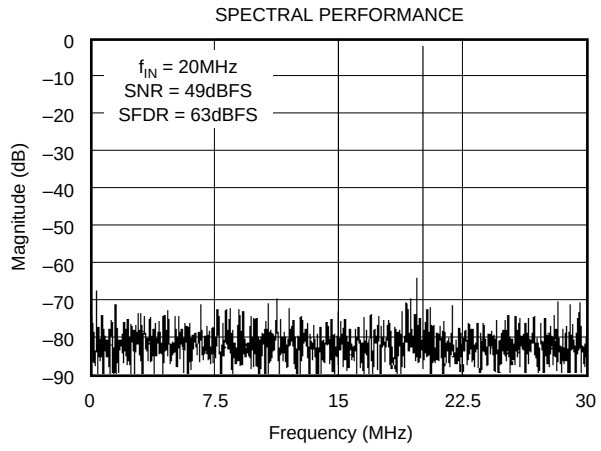
SPECTRAL PERFORMANCE



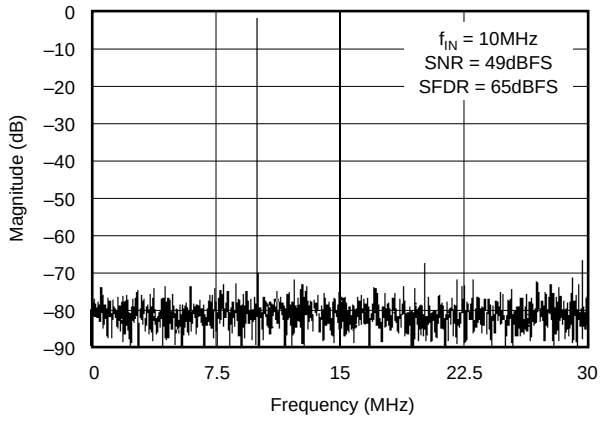
SPECTRAL PERFORMANCE



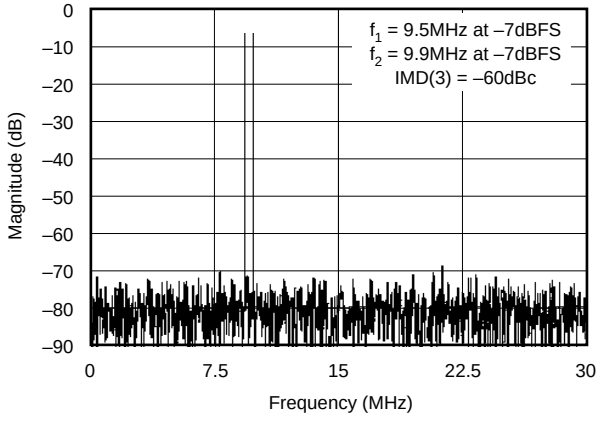
SPECTRAL PERFORMANCE



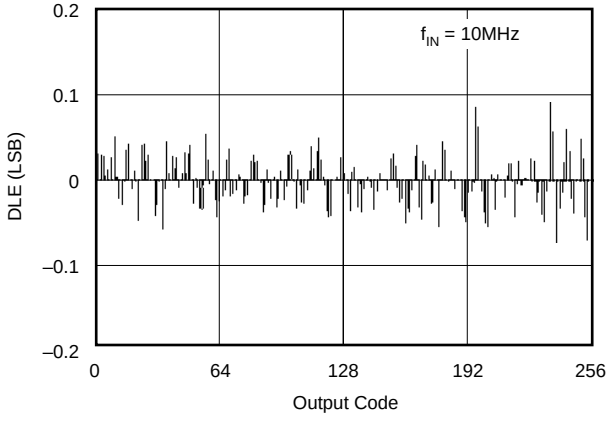
SPECTRAL PERFORMANCE
(Single-Ended, 1Vp-p)



TWO-TONE INTERMODULATION DISTORTION



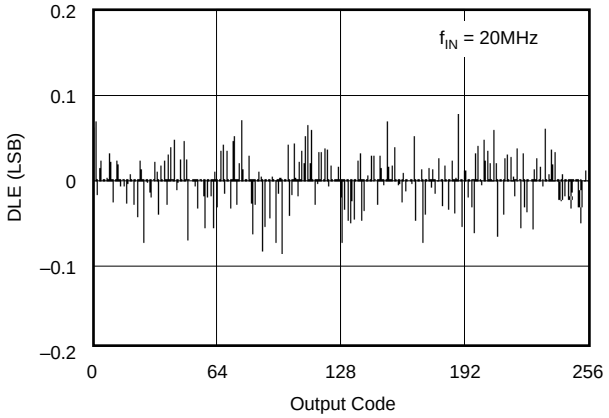
DIFFERENTIAL LINEARITY ERROR



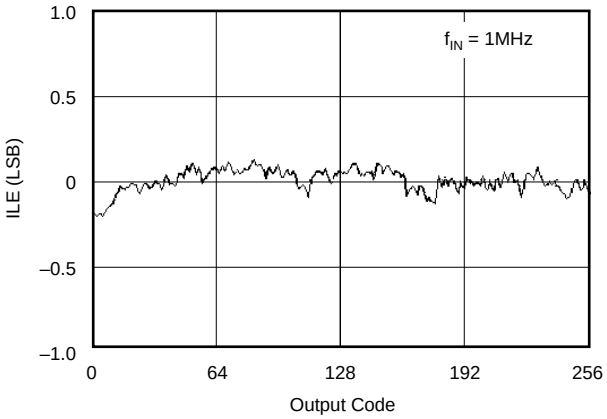
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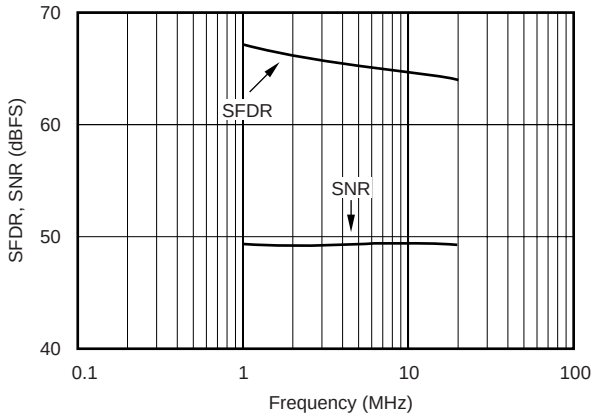
DIFFERENTIAL LINEARITY ERROR



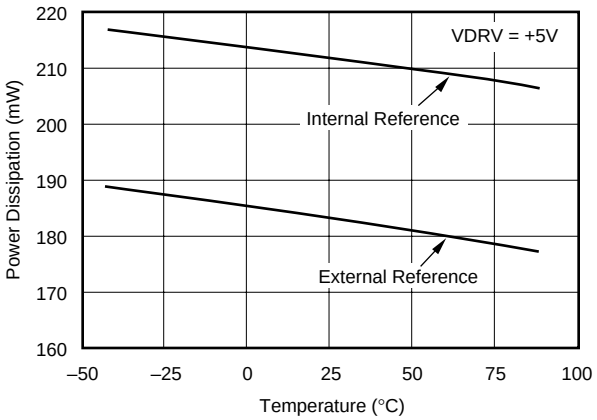
INTEGRAL LINEARITY ERROR



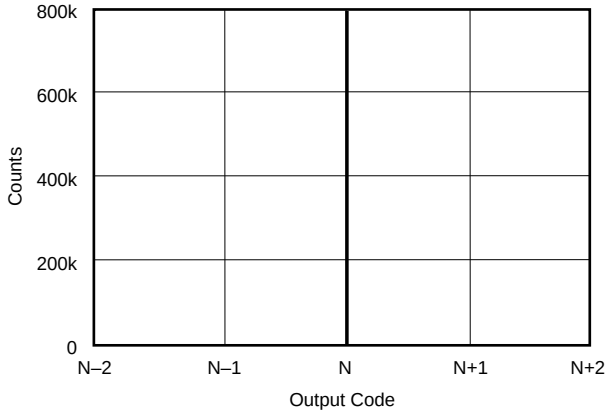
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



POWER DISSIPATION vs TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC Input)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS830 is a high-speed CMOS A/D converter which employs a pipelined converter architecture consisting of 6 internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 8-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 4 clock cycles.

The analog input of the ADS830 is a differential track and hold, see Figure 1. The differential topology along with tightly matched capacitors produce a high level of ac performance while sampling at very high rates.

The ADS830 allows its analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS830 is for the single-ended mode in which the input track and hold performs a single-ended to differential conversion of the analog input signal.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS830 are characterized using the single-ended mode of operation.

DRIVING THE ANALOG INPUT

The ADS830 achieves excellent ac performance either in the single-ended or differential mode of operation. The selection for the optimum interface configuration will depend on the individual application requirements and system structure. For example, communications applications often process a band of frequencies that does not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the A/D converter. Features on the ADS830 like the input range select (RSEL pin) or the option for an external reference provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS830 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

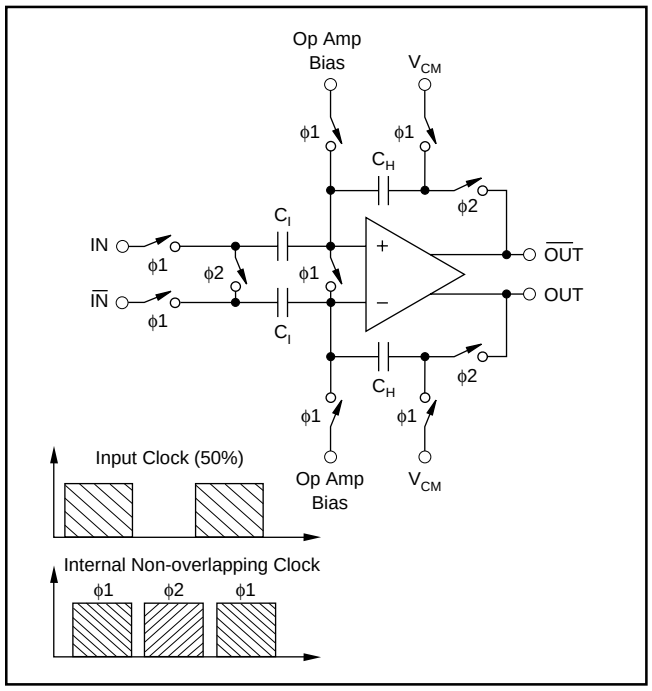


FIGURE 1. Simplified Circuit of Input Track and Hold with Timing Diagram.

INPUT CONFIGURATIONS

AC-Coupled, Single-Supply Interface

Figure 2 shows the typical circuit for an ac-coupled analog input configuration of the ADS830 where all components are powered from a single +5V supply.

With the RSEL pin connected HIGH, the full-scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.0V and +2.0V, respectively. Two resistors (2 x 1kΩ) are used to create a common-mode voltage (V_{CM}) of approximately +2.5V to bias the inputs of the driving amplifier. Using the OPA681 on a single +5V supply, its ideal common-mode point is at +2.5V. This coincides with the recommended common-mode input level for the ADS830 thus, obviating the need for a coupling capacitor between the amplifier and the converter. Even though the OPA681 has an ac gain of +2, the dc gain is only +1 due to the blocking capacitor at resistor R_G.

The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS830 will be beneficial in almost all interface configurations. This will de-couple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 75Ω. The series resistor in combination with the 47pF capacitor establishes a passive low-pass filter, limiting the bandwidth for the wideband noise thus help improving the SNR performance.

AC-Coupled, Dual Supply Interface

The circuit provided in Figure 3 shows typical connections for the analog input in case the selected amplifier operates on dual supplies. This might be necessary to take full advantage of very low distortion operational amplifiers, such as the OPA642. The advantage is that the driving amplifier can be operated with a ground referenced bipolar signal swing. This will keep the distortion performance at its lowest since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. By capacitively coupling the single-ended signal to the input of the ADS830, its common-mode requirements can easily be satisfied with two resistors connected between the top and bottom reference.

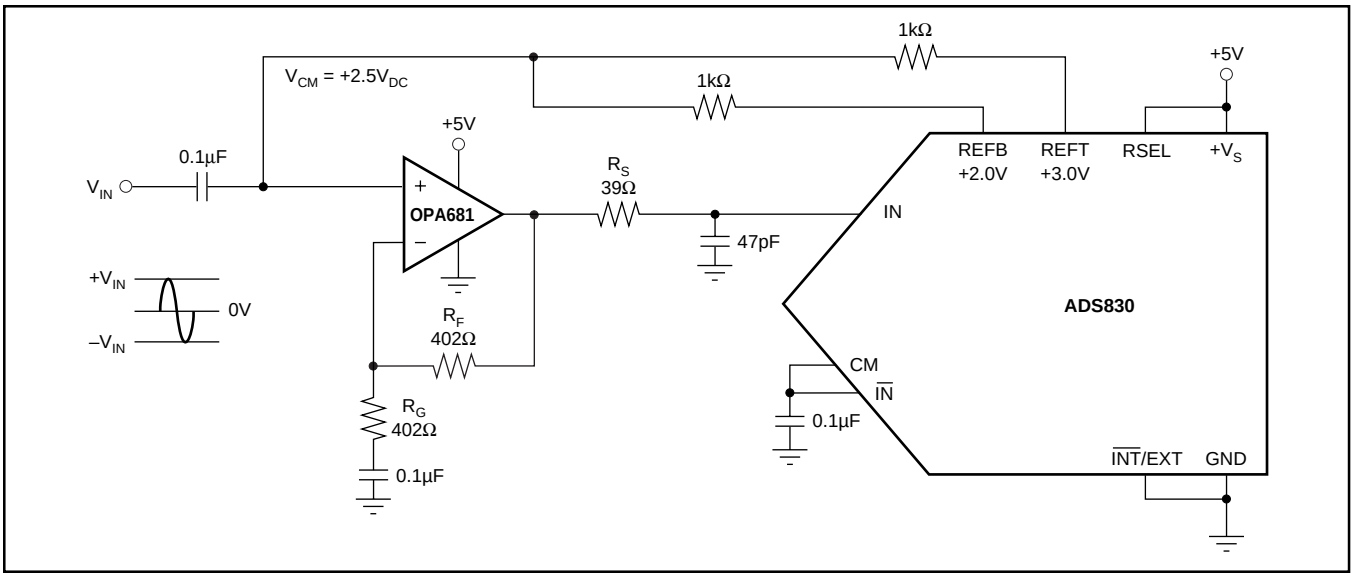


FIGURE 2. AC-Coupled Input Configuration for a 2Vp-p Full-Scale Range and a Common-Mode Voltage, V_{CM}, at +2.5V Derived from the Internal Top (REFT) and Bottom Reference (REFB). The OPA680 can be used in place of the OPA681 if a voltage feedback amplifier is preferred.

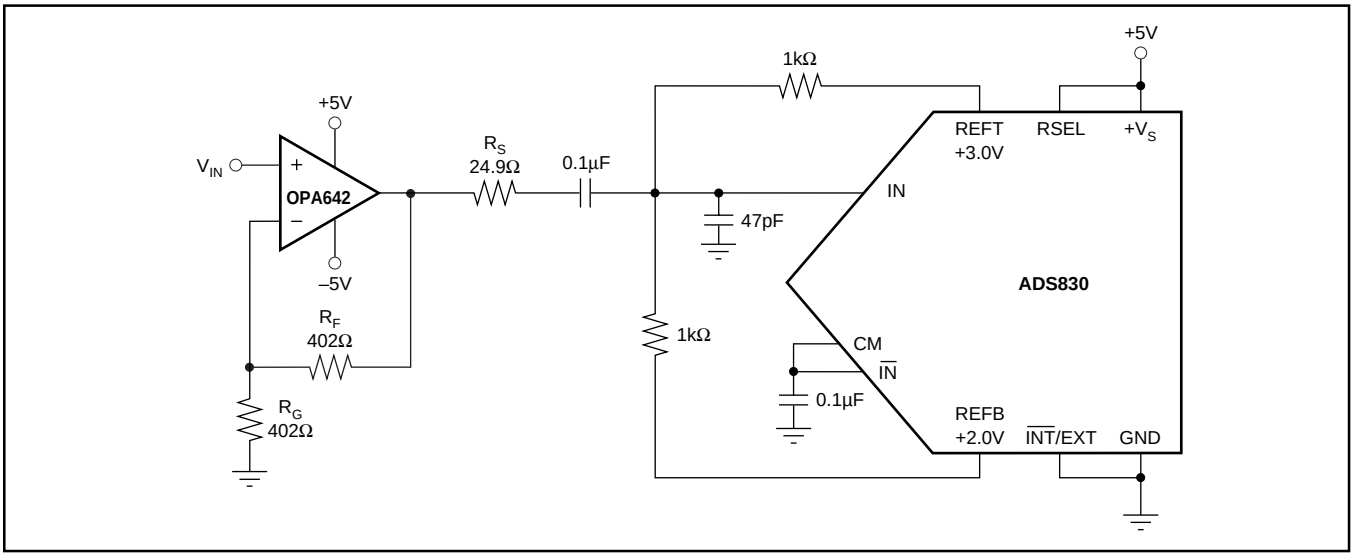


FIGURE 3. AC-Coupling the Dual Supply Amplifier OPA642 to the ADS830 for a 2Vp-p Full Scale Input Range.

For applications requiring the driving amplifier to provide a signal amplification, with a gain ≥ 5, consider using decompensated voltage feedback op amps, such as the OPA643, or current feedback op amps OPA681 and OPA658.

DC-Coupled with Level Shift

Several applications may require that the bandwidth of the signal path includes DC, in which case the signal has to be DC-coupled to the A/D converter. In order to accomplish this, the interface circuit has to provide a DC level shift to the analog input signal. The circuit shown in Figure 4 employs a dual op amp, A1, to drive the input of the ADS830 and level shift the signal to be compatible with the selected input range. With the RSEL pin tied to the supply and the $\overline{INT}$/EXT pin to ground, the ADS830 is configured for a 2Vp-p input range and uses the internal references. The complementary input ($\overline{IN}$) may be appropriately biased using the +2.5V common-mode voltage available at the CM pin. One-half of the amplifier (OPA2681) buffers the REFB pin and drives the voltage divider R_1, R_2. Because of the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the common-mode voltage (V_{CM}) has to be re-scaled to +1.25V, resulting in the correct DC level of +2.5V for the signal input (IN). Any DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS830 effectively produce an offset, which can be corrected for by adjusting the resistor values of the divider, R_1 and R_2. The selection criteria for a suitable op amp should include the supply voltage, input bias current, output voltage swing, distortion and noise specification. Note that in this example the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the IN and $\overline{IN}$ connections.

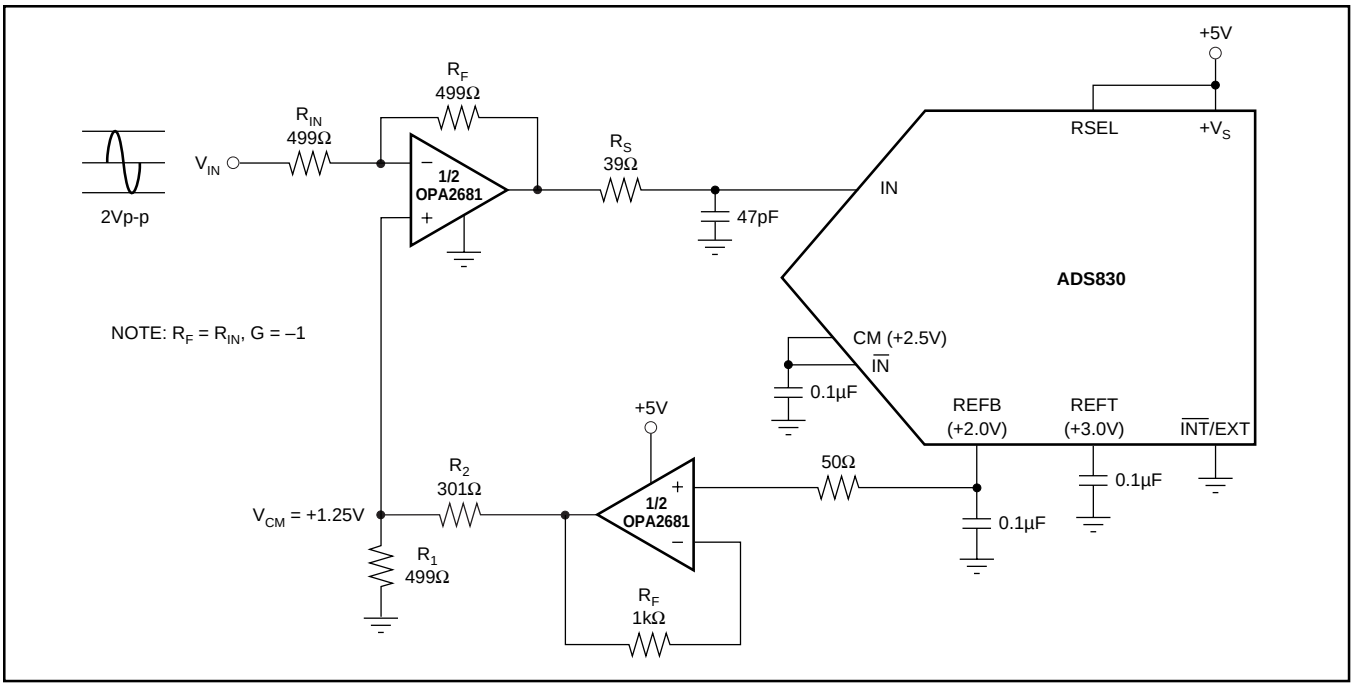


FIGURE 4. DC-Coupled Interface Circuit with Dual Current-Feedback Amplifier OPA2681. The OPA2680 can be used in place of the OPA2681 if a voltage feedback amplifier is preferred.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS830 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode both inputs of the ADS830 see closely matched impedances, and the differential signal swing is reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer coupled interface circuit. The component values of the R-C lowpass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \times R_G$ to match the source impedance (R_G) for good power transfer and VSWR.

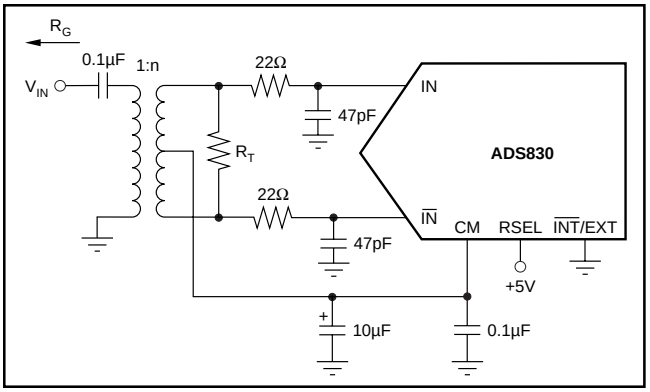


FIGURE 5. Transformer Coupled Input.

REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom reference, and

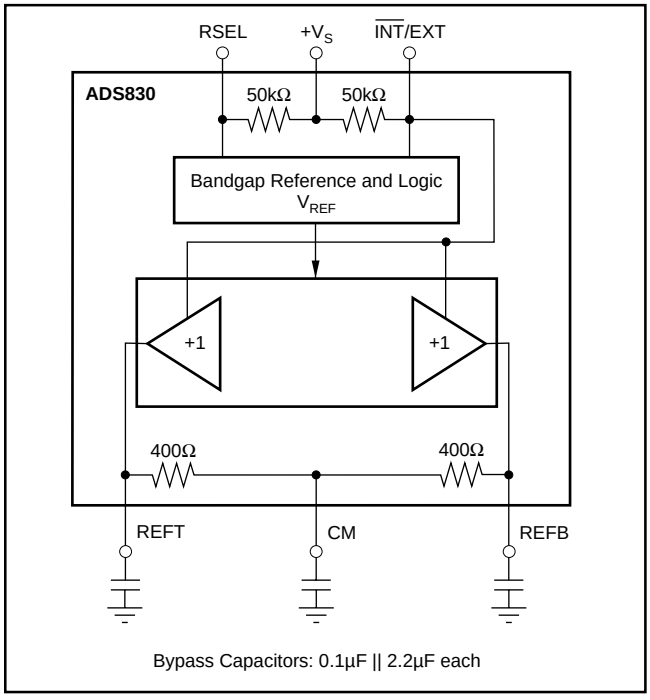


FIGURE 6. Equivalent Reference Circuit with Recommended Reference Bypassing.

the resistive reference ladder. The bandgap reference circuit includes logic functions that allow to set the analog input swing of the ADS830 to either a 1Vp-p or 2Vp-p full-scale range simply by tying the RSEL pin to a LOW or HIGH potential, respectively. While operating the ADS830 in the external reference mode, the buffer amplifiers for REFT and REFB are disconnected from the reference ladder.

As shown, the ADS830 has internal 50kΩ pull-up resistors at the Range Select pin (RSEL) and Reference Select pin ($\overline{INT}$/EXT). Leaving those pins open configures the ADS830 for a 2Vp-p input range and external reference operation. Setting the ADS830 up for internal reference mode requires to bring the $\overline{INT}$/EXT pin LOW.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at the reference pins in order to keep the clock feedthrough to a minimum (Figure 6). All bypassing capacitors should be located as close to their respective pins as possible.

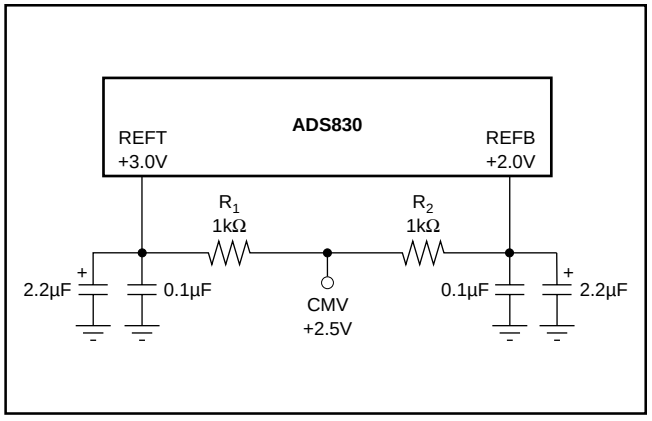


FIGURE 7. Alternative Circuit to Generate Common-Mode Voltage.

The common-mode voltage available at the CM pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (1% tolerance or better) are located between the top and bottom reference pins. The common-mode voltage, CMV, will appear at the midpoint.

EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference $REFT_{EXT}$ stays within the range of (V_S – 1.25V) and (REFB + 0.8V), and the external bottom reference $REFB_{EXT}$ stays within 1.25V and (REFT – 0.8V), see Figure 8.

The full-scale input signal range (FSR) of the ADS830 is determined by the voltage difference across the reference pins REFT and REFB (FSR = REFT – REFB), while the common-mode voltage is defined by CMV = (REFT + REFB)/2. In order to maintain good ac performance, it is recommended that the typical common-mode voltage be kept at +2.5V while setting the external reference voltages. It is possible, however, to deviate from this common-mode level without significantly impacting the performance. In particular, DC-coupled applications may benefit from a

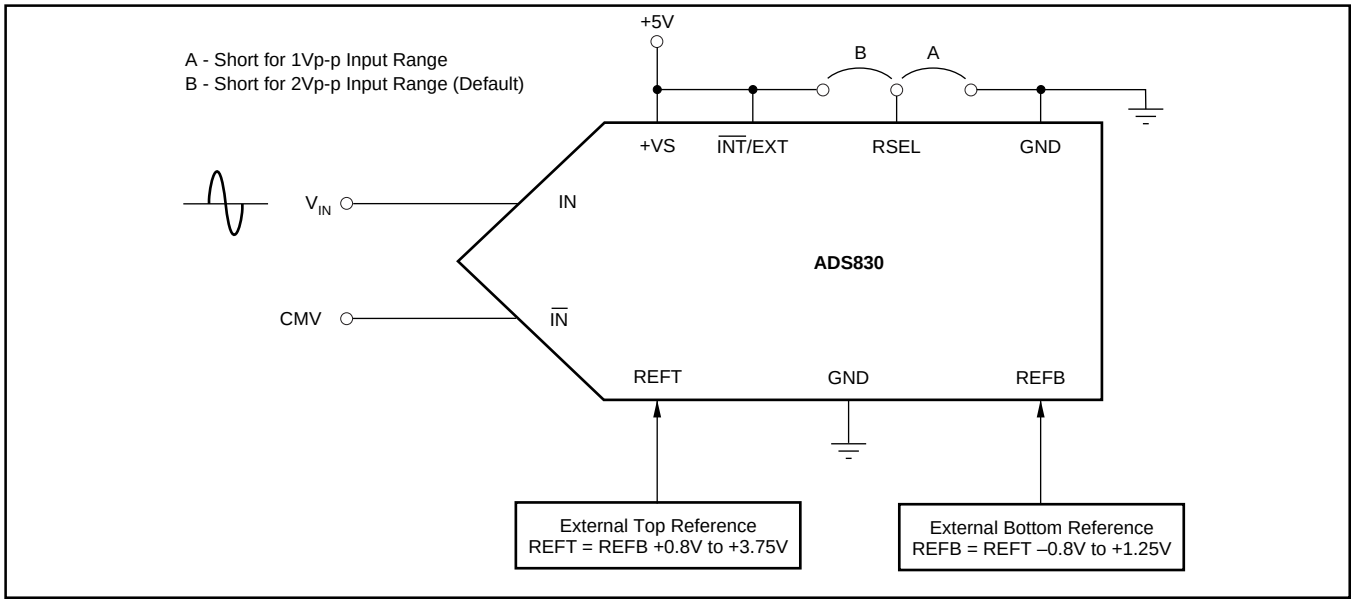


FIGURE 8. Configuration Example for External Reference Operation.

lower CMV as it increases the signal headroom of the driving amplifier. The internal reference ladder has a nominal impedance of 800Ω. Depending on the selected reference voltages, the required drive current will vary accordingly and the external reference circuitry should be designed to supply the maximum required current.

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Clock jitter is critical to the SNR performance of high speed, high resolution Analog to Digital Converters. It leads to aperture jitter (t_A) which adds noise to the signal being converted. The ADS830 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20 \log \frac{1}{2\pi f_{IN} t_A} \quad \text{rms signal to rms noise}$$

Where: f_{IN} is Input Signal Frequency
t_A is rms Clock Jitter

Particularly in udersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have a 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less.

Digital Outputs

The output data format of the ADS830 is in positive Straight Offset Binary code, see Table I. This format can easily converted into the Two's Binary Complement code by inverting the MSB.

SINGLE-ENDED INPUT (2Vp-p) ($\overline{IN}$ = CMV)	STRAIGHT OFFSET BINARY (SOB)
+FS (IN = +3.5V)	1111 1111
+1/2 FS	1100 0000
+1LSB	1000 0001
Bipolar Zero (IN = 2.5V)	1000 0000
–1LSB	0111 1111
–1/2 FS	0100 0000
–FS (IN = +1.5V)	0000 0000

TABLE I. Coding Table for the ADS830.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS830 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS830 from any digital noise activities on the bus coupling back high frequency noise.

Digital Output Driver (VDRV)

The ADS830 features a dedicated supply pin for the output logic drivers, VDRV, which is not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS830 produces corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS830 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the ac performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS830 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS830 are internally joined together, obviating the design of split ground planes. The ground pins (1, 18) should directly connect to an analog ground plane which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Because of its high sampling rate, the ADS830 generates high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the ADS830. In most cases 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.

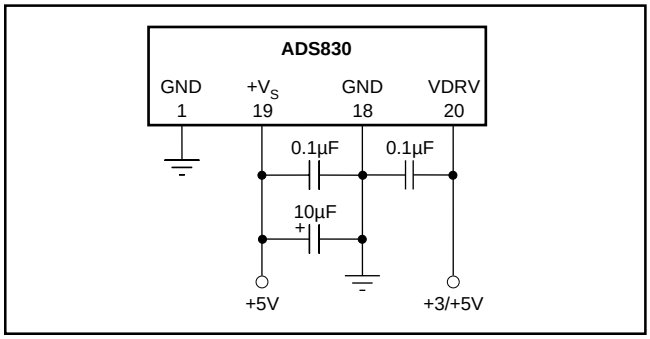


FIGURE 9. Recommended Bypassing for the Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS830E	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS830E	Samples
ADS830E/2K5	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS830E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

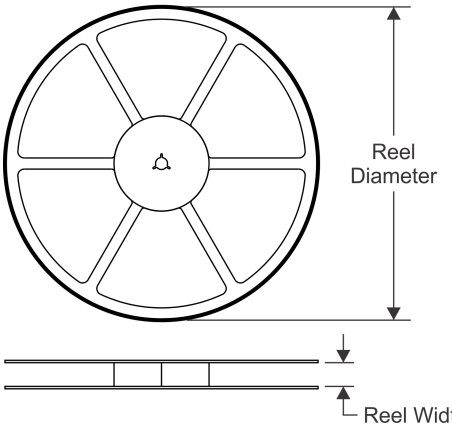
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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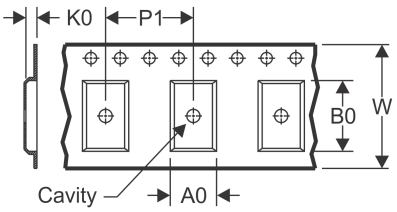
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

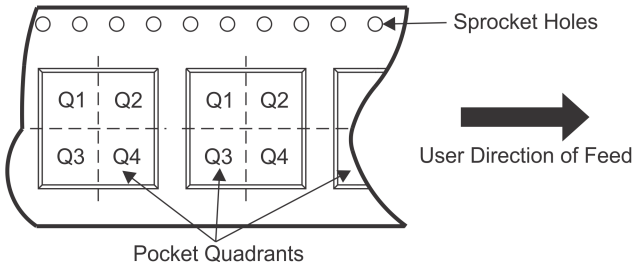


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

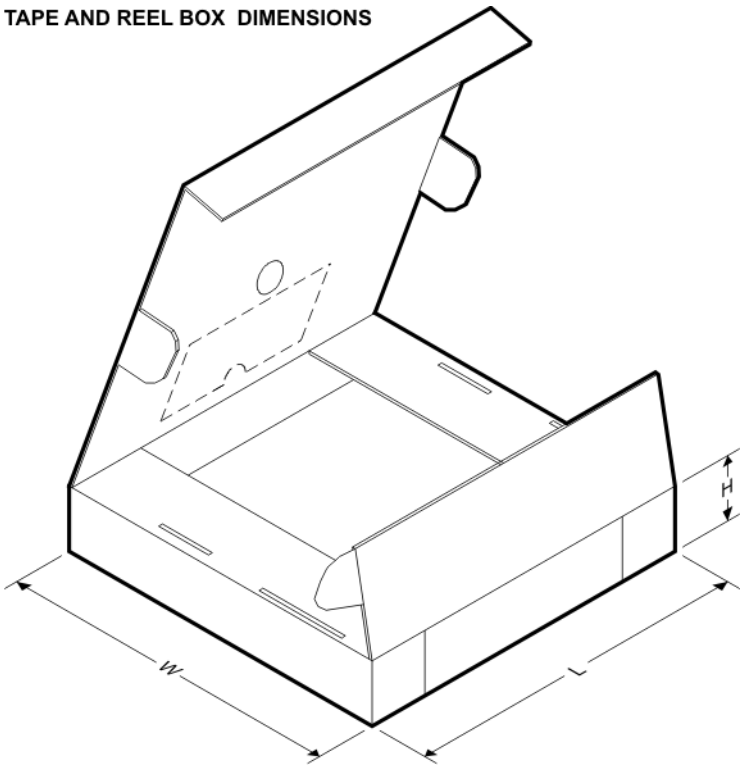
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS830E/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS830E/2K5	SSOP	DBQ	20	2500	350.0	350.0	43.0

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