

SBAS073B – JANUARY 1997 – REVISED NOVEMBER 2002

12-Bit, 20MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH SFDR: 74dB at 9.8MHz f_{IN}**
- **HIGH SNR: 68dB**
- **LOW POWER: 300mW**
- **LOW DLE: 0.25LSB**
- **FLEXIBLE INPUT RANGE**
- **OVER-RANGE INDICATOR**

APPLICATIONS

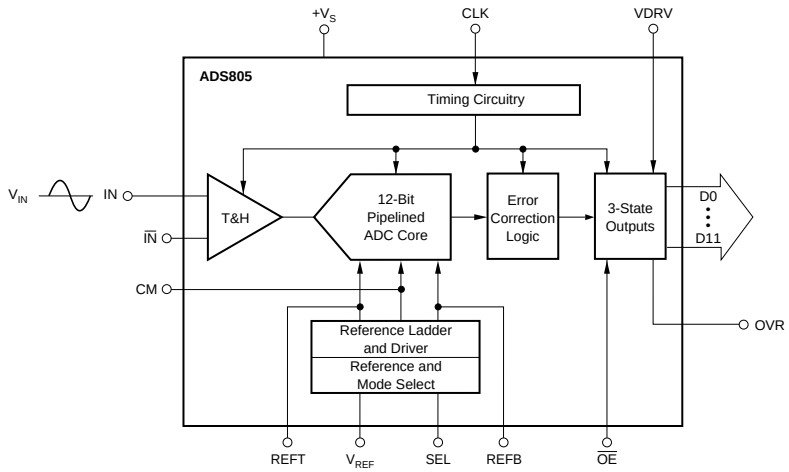
- **STUDIO CAMERAS**
- **IF AND BASEBAND DIGITIZATION**
- **COPIERS**
- **TEST INSTRUMENTATION**

DESCRIPTION

The ADS805 is a 20MHz, high dynamic range, 12-bit, pipelined Analog-to-Digital Converter ADC. This converter includes a high-bandwidth track-and-hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth, linear track-and-hold minimizes harmonics and has low jitter, leading to excellent Signal-to-Noise Ratio (SNR) performance. The ADS805 is also pin-compatible with the 10MHz ADS804 and the 5MHz ADS803.

The ADS805 provides an internal reference or an external reference can be used. The ADS805 can be programmed for a 2Vp-p input range which is the easiest to drive with a single op amp and provides the best spurious performance. Alternatively, the 5Vp-p input range can be used for the lowest input-referred noise of 0.09LSBs rms giving superior imaging performance. There is also the capability to set the input range between 2Vp-p and 5Vp-p, either single-ended or differential. The ADS805 also provides an over-range flag that indicates when the input signal has exceeded the converter's full-scale range. This flag can also be used to reduce the gain of the front end signal conditioning circuitry.

The ADS805 employs digital error techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for communications, medical imaging, video, and test instrumentation applications. The ADS805 is available in an SSOP-28 package.



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ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	–0.3V to $(+V_S)$ + 0.3V
Logic Input	–0.3V to $(+V_S)$ + 0.3V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA, QUANTITY
ADS805	SSOP-28	DB	–40°C to +85°C	ADS805E	ADS805E	Rails, 48
"	"	"	"	"	ADS805E/1K	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, and single-ended input and sampling rate = 20MHz, unless otherwise specified.

		ADS805E			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESOLUTION			12 Bits Tested		
SPECIFIED TEMPERATURE RANGE			–40 to +85		°C
CONVERSION CHARACTERISTICS					
Sample Rate		10k		20M	Samples/s
Data Latency			6		Clk Cycles
ANALOG INPUT					
Standard Single-Ended Input Range		1.5		3.5	V
Optional Single-Ended Input Range		0		5	V
Standard Common-Mode Voltage			2.5		V
Standard Optional Common-Mode Voltage			1		V
Input Capacitance			20		pF
Analog Input Bandwidth	–3dBFS Input		270		MHz
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (Largest Code Error)					
f = 500kHz			±0.25	±0.75	LSB
No Missing Codes			Tested		
Spurious-Free Dynamic Range[1]					
f = 9.8MHz		65	74		dBFS[2]
2-Tone Intermodulation Distortion[3]					
f = 7.7MHz and 7.9MHz (–7dB each tone)			–70		dBc
Signal-to-Noise Ratio (SNR)					
f = 9.8MHz		63	68		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 9.8MHz		62	66		dBFS
Effective Number of Bits at 9.8MHz[4]			10.7		Bits
Input Referred Noise	0V to 5V Input		0.09		LSBs rms
	1.5V to 3.5V Input		0.23		LSBs rms
Integral Nonlinearity Error					
f = 500kHz			±1	±2	LSB
Aperture Delay Time			3		ns
Aperture Jitter			4		ps rms
Over-Voltage Recovery Time	1.5x FS Input		2		ns
Full-Scale Step Acquisition Time			20		ns

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full-scale. (3) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) Internal 50kΩ pull-down resistor. (6) Includes internal reference. (7) Excludes internal reference.

ELECTRICAL CHARACTERISTICS (Cont.)

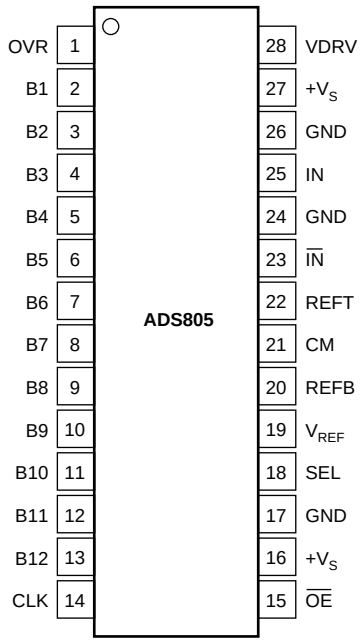
At T_A = full specified temperature range, V_S = +5V, specified input range = 1.5V to 3.5V, and single-ended input and sampling rate = 20MHz, unless otherwise specified.

PARAMETER	CONDITIONS	ADS805E MIN	ADS805E TYP	ADS805E MAX	UNITS
DIGITAL INPUTS					
Logic Family			CMOS Compatible		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current (V_{IN} = 5V)[5]				±100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+3.5			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS/TTL Compatible		
Logic Coding			Straight Offset Binary		
Low Output Voltage	(I_{OL} = 50µA)			0.1	V
Low Output Voltage	(I_{OL} = 1.6mA)			0.4	V
High Output Voltage	(I_{OH} = 50µA)	+4.5			V
High Output Voltage	(I_{OH} = 0.5mA)	+2.4			V
3-State Enable Time	$\overline{OE}$ = L		20	40	ns
3-State Disable Time	$\overline{OE}$ = H		2	10	ns
Output Capacitance			5		pF
ACCURACY (5Vp-p Input Range)	f_S = 2.5MHz				
Zero-Error (Referred to –FS)	At 25°C		0.3	±1.5	%FS
Zero-Error Drift (Referred to –FS)			±5		ppm/°C
Gain Error[6]	At 25°C		0.7	±2.0	%FS
Gain Error Drift[6]			±18		ppm/°C
Gain Error[7]	At 25°C		0.2	±1.5	%FS
Gain Error Drift[7]			±10		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%	60	70		dB
Reference Input Resistance			1.6		kΩ
Internal Voltage Reference Tolerance (V_{REF} = 2.5V)	At 25°C			±35	mV
Internal Voltage Reference Tolerance (V_{REF} = 1.0V)	At 25°C			±14	mV
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		60	69	mA
Power Dissipation	Operating		300	345	mW
Thermal Resistance, θ_{JA}					
SSOP-28		50		°C/W	

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full-scale. (3) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) Internal 50kΩ pull-down resistor. (6) Includes internal reference. (7) Excludes internal reference.

PIN CONFIGURATION

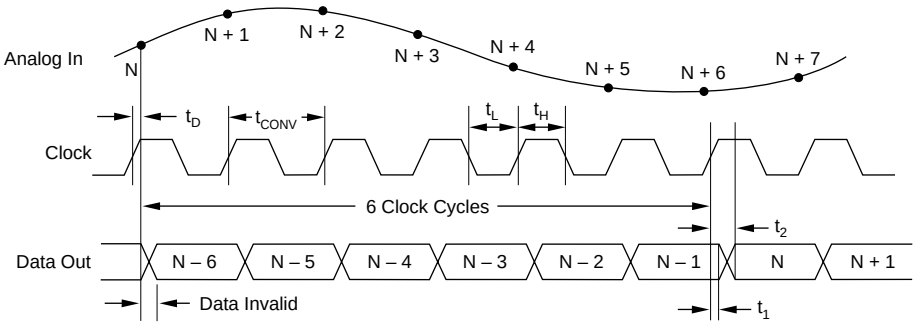
Top View **SSOP**



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	OVR	Over-Range Indicator
2	B1	Data Bit 1 (D11) (MSB)
3	B2	Data Bit 2 (D10)
4	B3	Data Bit 3 (D9)
5	B4	Data Bit 4 (D8)
6	B5	Data Bit 5 (D7)
7	B6	Data Bit 6 (D6)
8	B7	Data Bit 7 (D5)
9	B8	Data Bit 8 (D4)
10	B9	Data Bit 9 (D3)
11	B10	Data Bit 10 (D2)
12	B11	Data Bit 11 (D1)
13	B12	Data Bit 12 (D0) (LSB)
14	CLK	Convert Clock Input
15	$\overline{OE}$	Output Enable. H = High Impedance State. L = LOW or floating, normal operation (internal pull-down resistor).
16	$+V_S$	+5V Supply
17	GND	Ground
18	SEL	Input Range Select
19	V_{REF}	Reference Voltage Select
20	REFB	Bottom Reference
21	CM	Common-Mode Voltage
22	REFT	Top Reference
23	$\overline{IN}$	Complementary Analog Input
24	GND	Ground
25	IN	Analog Input (+)
26	GND	Ground
27	$+V_S$	+5V Supply
28	VDRV	Output Driver Voltage

TIMING DIAGRAM

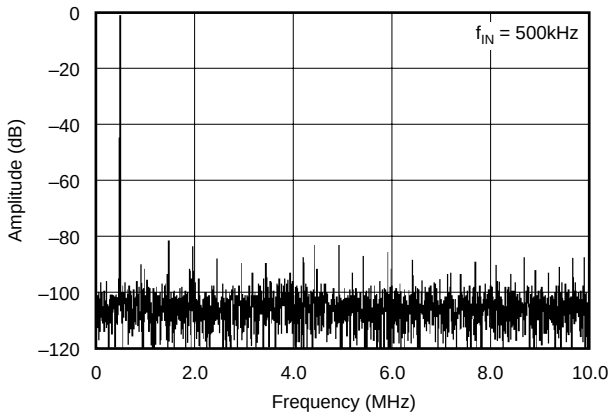


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	50		100µs	ns
t_L	Clock Pulse LOW	24	25		ns
t_H	Clock Pulse HIGH	24	25		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

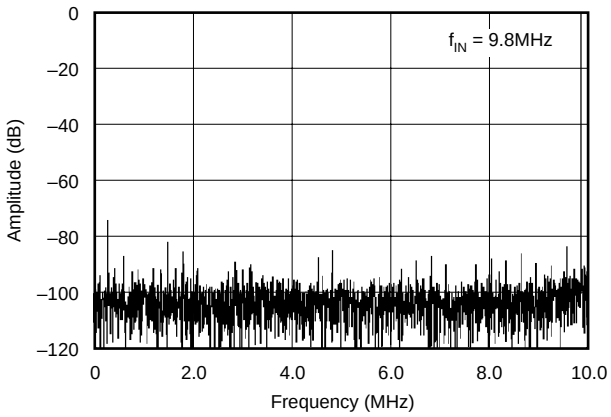
TYPICAL CHARACTERISITCS

At T_A = full specified temperature range, V_S = +5V, specified single-ended input range = 1.5V to 3.5V, and sampling rate = 20MHz, unless otherwise specified.

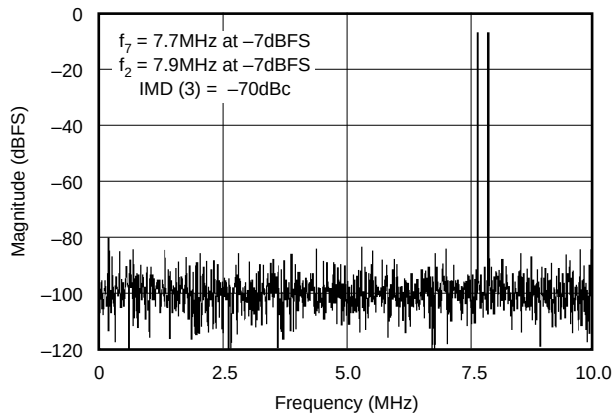
SPECTRAL PERFORMANCE



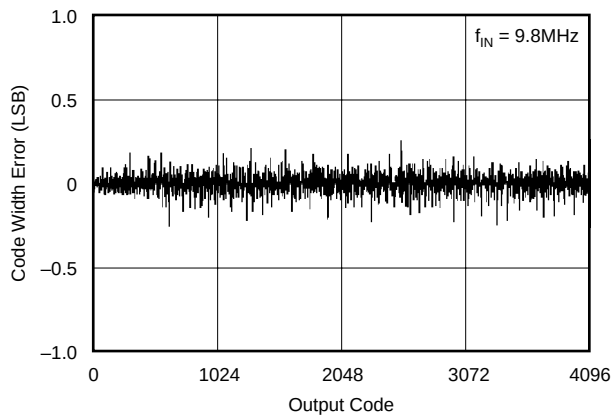
SPECTRAL PERFORMANCE



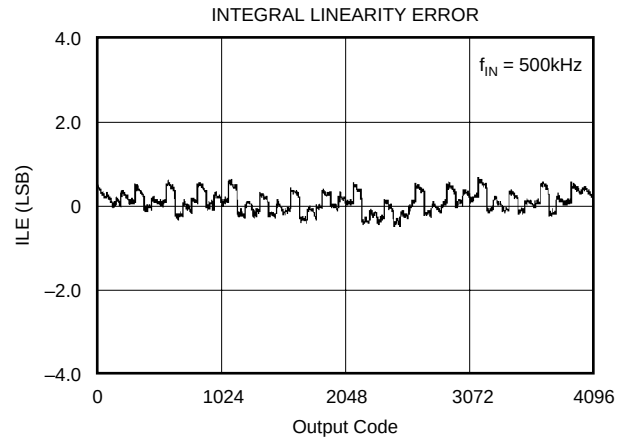
2-TONE INTERMODULATION DISTORTION



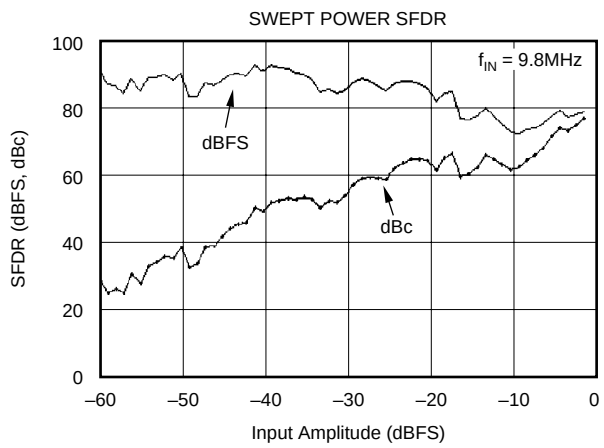
DIFFERENTIAL LINEARITY ERROR



INTEGRAL LINEARITY ERROR



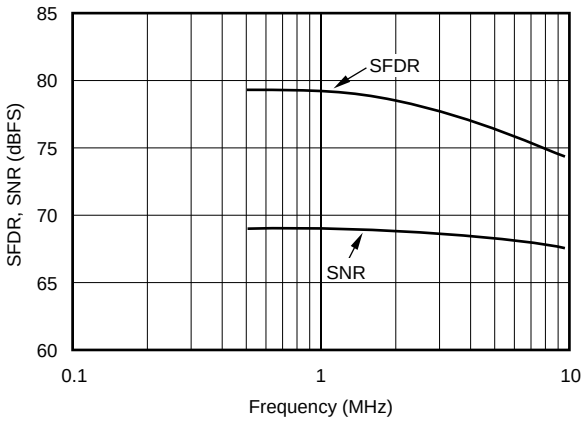
SWEPT POWER SFDR



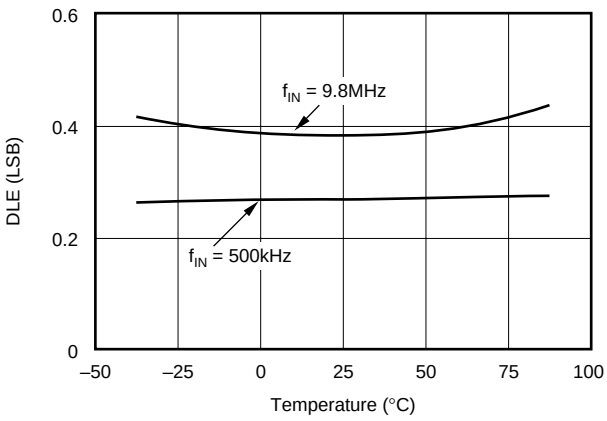
TYPICAL CHARACTERISITCS (Cont.)

At T_A = full specified temperature range, V_S = +5V, specified single-ended input range = 1.5V to 3.5V, and sampling rate = 20MHz, unless otherwise specified.

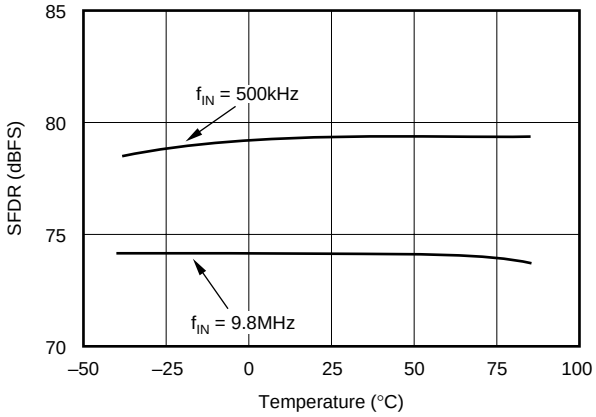
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



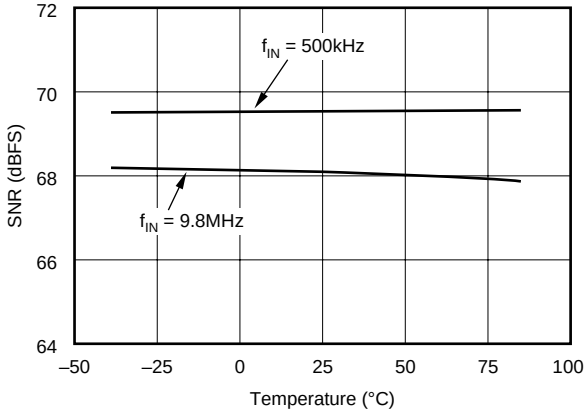
DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



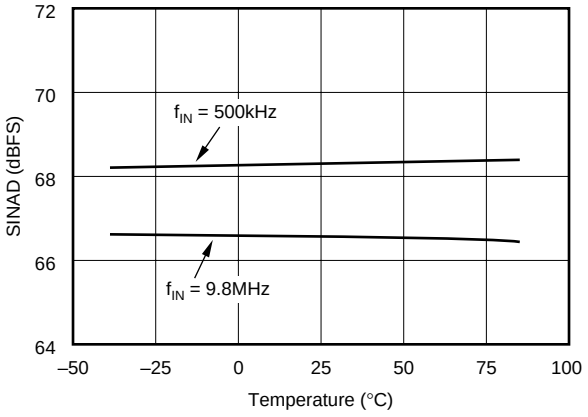
SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE



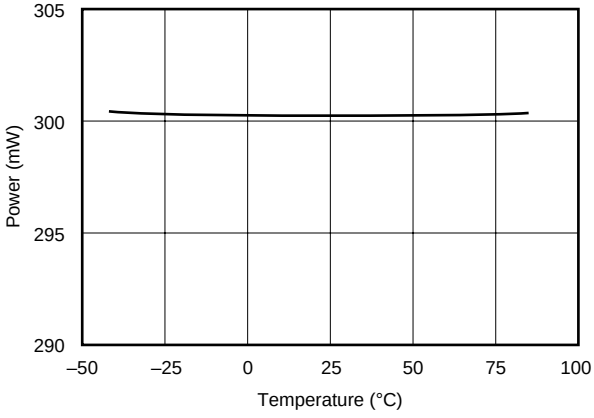
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE



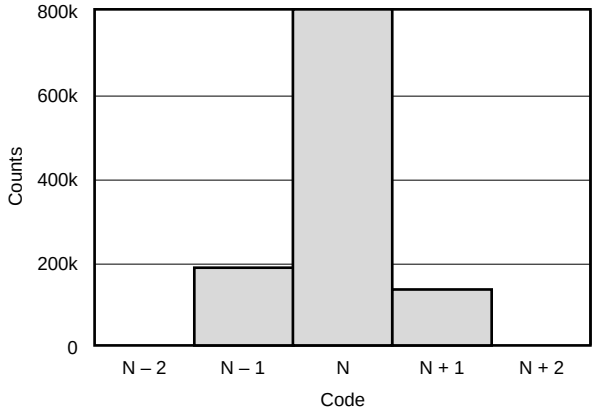
POWER DISSIPATION vs TEMPERATURE



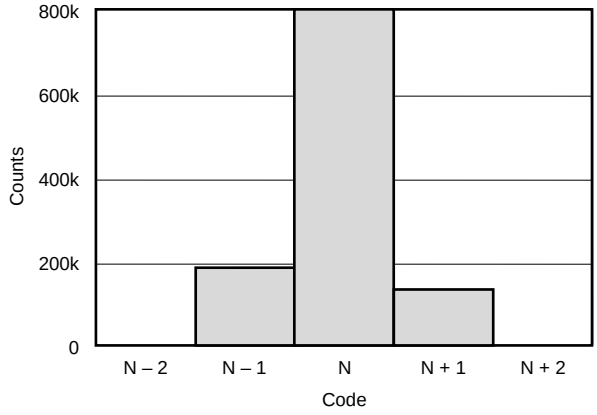
TYPICAL CHARACTERISITCS (Cont.)

At T_A = full specified temperature range, V_S = +5V, specified single-ended input range = 1.5V to 3.5V, and sampling rate = 20MHz, unless otherwise specified.

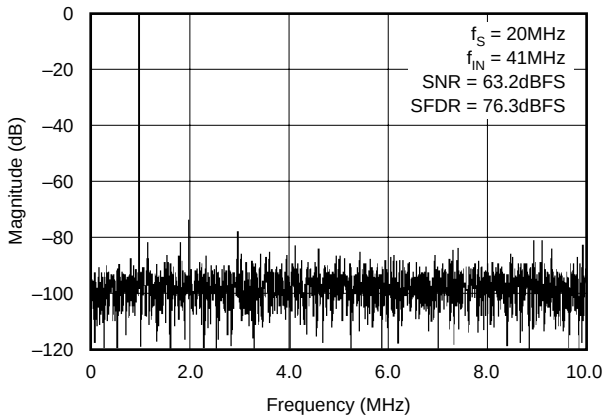
OUTPUT NOISE HISTOGRAM
(DC Input)



OUTPUT NOISE HISTOGRAM
(DC Input, V_{IN} = 5Vp-p Range)



UNDERSAMPLING
(Differential Input, 2Vp-p)



APPLICATION INFORMATION

DRIVING THE ANALOG INPUT

The ADS805 allows its analog inputs to be driven either single-ended or differentially. The focus of the following discussion is on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS805 are characterized using the single-ended mode of operation.

AC-COUPLED INPUT CONFIGURATION

Given in Figure 1 is the circuit example of the most common interface configuration for the ADS805. With the V_{REF} pin connected to the SEL pin, the full-scale input range is defined to be 2Vp-p. This signal is ac-coupled in single-ended form to the ADS805 using the low distortion voltage-feedback amplifier OPA642. As is generally necessary for single-supply components, operating the ADS805 with a full-scale input signal swing requires a level-shift of the amplifier's zero centered analog signal to comply with the ADC's input range requirements. Using a DC-blocking capacitor between the output of the driving amplifier and the converter's input, a simple level-shifting scheme can be implemented. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3V and +2V, respectively. Here, two resistor pairs (2 • 2kΩ) are used to create a common-mode voltage of approximately +2.5V to bias the inputs of the ADS805 (IN, $\overline{IN}$) to the required DC voltage.

An advantage of ac-coupling is that the driving amplifier still operates with a ground-based signal swing. This will keep the distortion performance at its optimum since the signal swing stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. Consider using the inverting gain configuration to eliminate CMR induced errors of the amplifier. The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS805 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor, together with the 100pF capacitor, establish a passive low-pass filter, limiting the bandwidth for the wideband noise, thus helping improve the signal-to-noise performance.

DC-COUPLED WITHOUT LEVEL SHIFT

In some applications the analog input signal may already be biased at a level which complies with the selected input range and reference level of the ADS805. In this case, it is only necessary to provide an adequately low source impedance to the selected input, IN or $\overline{IN}$. Always consider wideband op amps since their output impedance will stay low over a wide range of frequencies.

DC-COUPLED WITH LEVEL SHIFT

Several applications may require that the bandwidth of the signal path include DC, in which case the signal has to be DC-coupled to the ADC. In order to accomplish this, the interface circuit has to provide a DC-level shift. The circuit presented in Figure 2 utilizes the single-supply, current-feedback op amp OPA681 (A1), to sum the ground-centered input signal with a required DC offset. The ADS805 typically operates with a +2.5V common-mode voltage, which is established with resistors R_3 and R_4 and connected to the $\overline{IN}$ input of the converter. Amplifier A1 operates in inverting configuration. Here, resistors R_1 and R_2 set the DC-bias level for A1. Because of the op amp's noise gain of +2V/V, assuming $R_F = R_{IN}$, the DC offset voltage applied to its noninverting input has to be divided down to +1.25V, resulting in a DC output voltage of +2.5V. DC voltage differences between the IN and $\overline{IN}$ inputs of the ADS805 effectively will produce an offset, which can be corrected for by adjusting the values of resistors R_1 and R_2. The bias current of the op amp may also result in an undesired

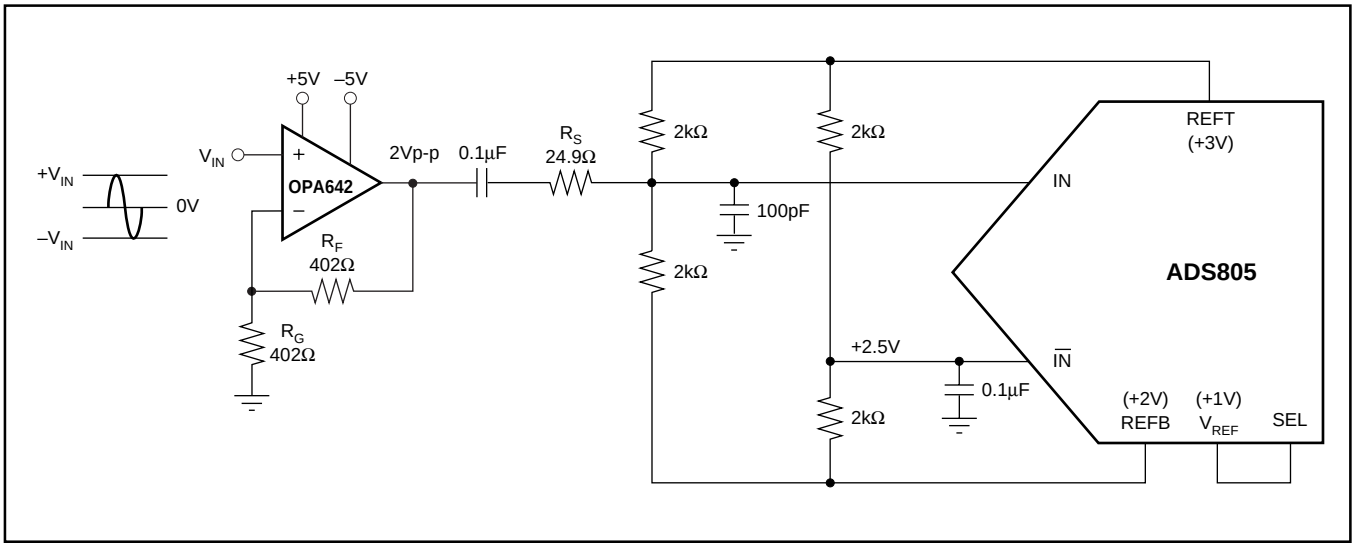


FIGURE 1. AC-Coupled Input Configuration for 2Vp-p Input Swing and Common-Mode Voltage at +2.5V Derived from Internal Top and Bottom Reference.

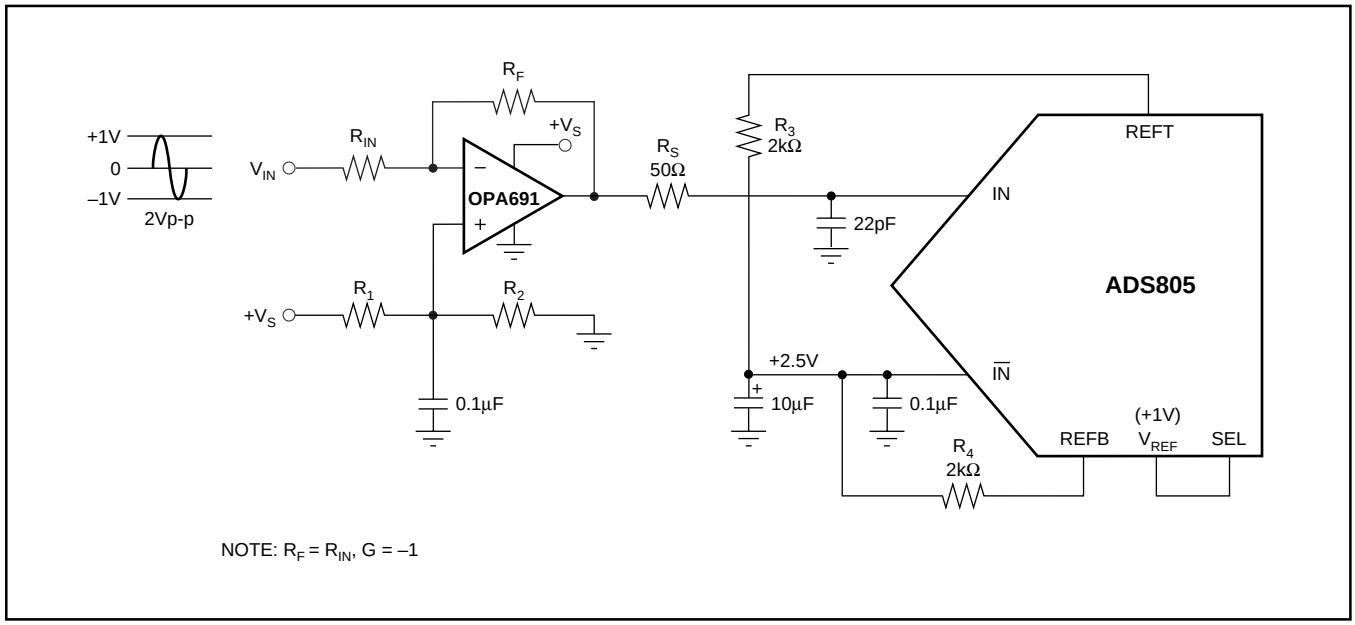


FIGURE 2. DC-Coupled, Single-Ended Input Configuration with DC-level Shift.

offset. The selection criteria for an appropriate op amp should include the input bias current, output voltage swing, distortion, and noise specification. Note that in this example the overall signal phase is inverted. To reestablish the original signal polarity, it is always possible to interchange the IN and $\overline{IN}$ connections.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (TRANSFORMER-COUPLED)

In order to select the best suited interface circuit for the ADS805, the performance requirements must be known. If an ac-coupled input is needed for a particular application, the next step is to determine the method of applying the signal; either single-ended or differentially. The differential input configuration may provide a noticeable advantage of achieving good SFDR performance based on the fact that, in the differential mode, the signal swing can be reduced to half of the swing required for single-ended drive. Secondly, by driving the ADS805 differentially, the even-order harmonics will be reduced. Figure 3 shows the schematic for the suggested transformer-coupled interface circuit. The resistor across the secondary side (R_T) should be set to get an input impedance match (e.g., $R_T = n^2 \bullet R_G$).

One application example that will benefit from the differential input configuration is the digitization of IF signals. The wide track-and-hold input bandwidth makes the ADS805 well suited for IF down conversion in both narrow and wideband applications. The ADS805 maintains excellent dynamic performance in multiple Nyquist regions covering a variety of IF frequencies (see the Typical Characteristics). Using the ADS805 for direct IF conversion eliminates the need of an analog mixer along with subsequent functions like amplifiers and filters, thus reducing system cost and complexity.

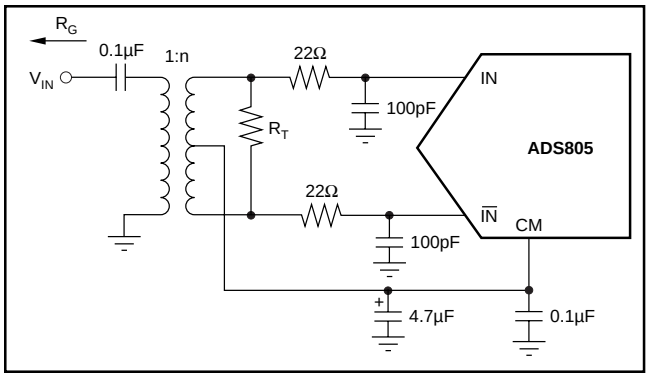


FIGURE 3. Transformer-Coupled Input.

REFERENCE OPERATION

Integrated into the ADS805 is a bandgap reference circuit including logic that provides either a +1V or +2.5V reference output, by simply selecting the corresponding pin-strap configuration. Different reference voltages can be generated by the use of two external resistors, which will set a different gain for the internal reference buffer. For more design flexibility, the internal reference can be shut off and an external reference voltage used. Table I provides an overview of the possible reference options and pin configurations.

MODE	INPUT FULL-SCALE RANGE	REQUIRED V_{REF}	CONNECT	TO
Internal	2Vp-p	+1V	SEL	V_{REF}
Internal	5Vp-p	+2.5V	SEL	GND
Internal	2V ≤ FSR < 5V FSR = 2 • V_{REF}	1V < V_{REF} < 2.5V $V_{REF} = 1 + (R_1/R_2)$	R_1 R_2	V_{REF} and SEL SEL and Gnd
External	1V < FSR < 5V	0.5V < V_{REF} < 2.5V	SEL V_{REF}	+V_S Ext. V_{REF}

TABLE I. Selected Reference Configuration Examples.

A simple model of the internal reference circuit is shown in Figure 4. The internal blocks are a 1V-bandgap voltage reference, buffer, the resistive reference ladder and the drivers for the top and bottom reference which supply the necessary current to the internal nodes. As shown, the output of the buffer appears at the V_{REF} pin. The full-scale input span of the ADS805 is determined by the voltage at V_{REF}, according to Equation 1:

$$\text{Full-Scale Input Span} = 2 \bullet V_{REF} \quad (1)$$

Note that the current drive capability of this amplifier is limited to approximately 1mA and should not be used to drive low loads. The programmable reference circuit is controlled by the voltage applied to the select pin (SEL). Refer to Table I for an overview.

The top reference (REFT) and the bottom reference (REFB) are brought out mainly for external bypassing. For proper operation with all reference configurations, it is necessary to provide solid bypassing to the reference pins in order to keep the clock feedthrough to a minimum. Figure 5 shows the recommended decoupling network.

In addition, the Common-Mode Voltage (CMV) may be used as a reference level to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternate method of generating a common-mode voltage is given in Figure 6. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode level will appear at the midpoint. The output buffers of the top and bottom reference are designed to supply approximately 2mA of output current.

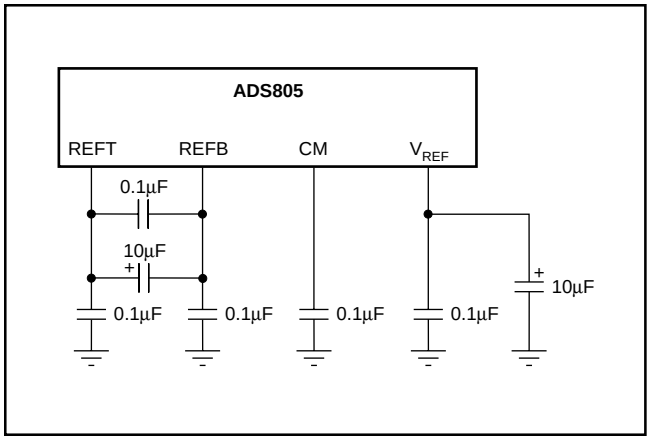


FIGURE 5. Recommended Reference Bypassing Scheme.

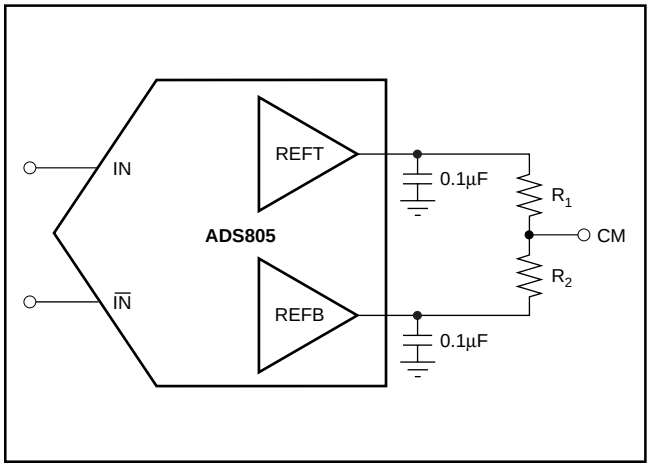


FIGURE 6. Alternative Circuit to Generate Common-Mode Voltage.

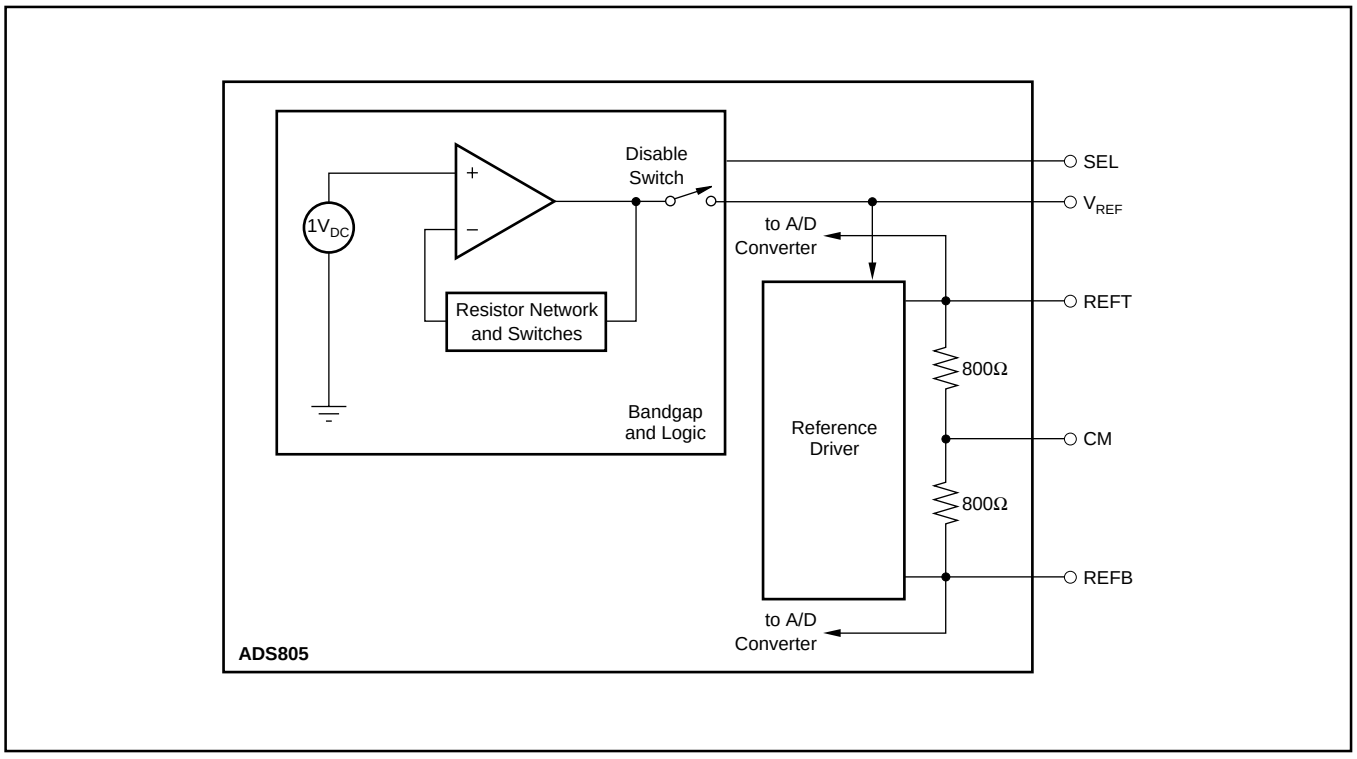


FIGURE 4. Equivalent Reference Circuit.

SELECTING THE INPUT RANGE AND REFERENCE

Figures 7 through 9 show a selection of circuits for the most common input ranges when using the internal reference of the ADS805. All examples are for single-ended input and operate with a nominal common-mode voltage of +2.5V.

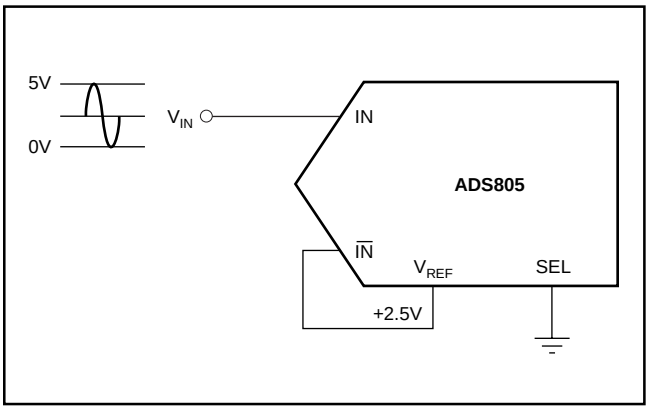


FIGURE 7. Internal Reference with 0V to 5V Input Range.

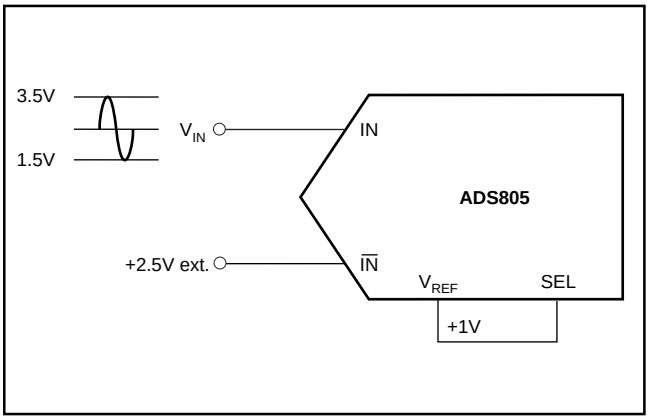


FIGURE 8. Internal Reference with 1.5V to 3.5V Input Range.

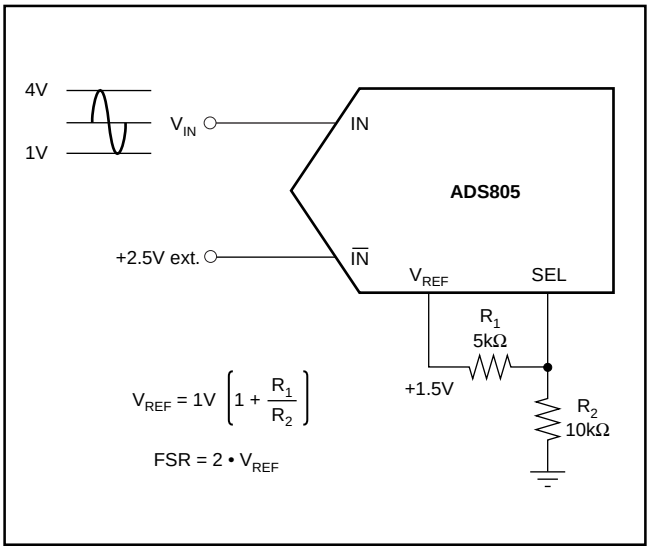


FIGURE 9. Internal Reference with 1V to 4V Input Range.

EXTERNAL REFERENCE OPERATION

Depending on the application requirements, it might be advantageous to operate the ADS805 with an external reference. This may improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy. To use the ADS805 with an external reference, the user must disable the internal reference, as shown in Figure 10. By connecting the SEL pin to $+V_S$, the internal logic will shut down the internal reference. At the same time, the output of the internal reference buffer is disconnected from the V_{REF} pin, which now must be driven with the external reference. Note that a similar bypassing scheme should be maintained as described for the internal reference operation.

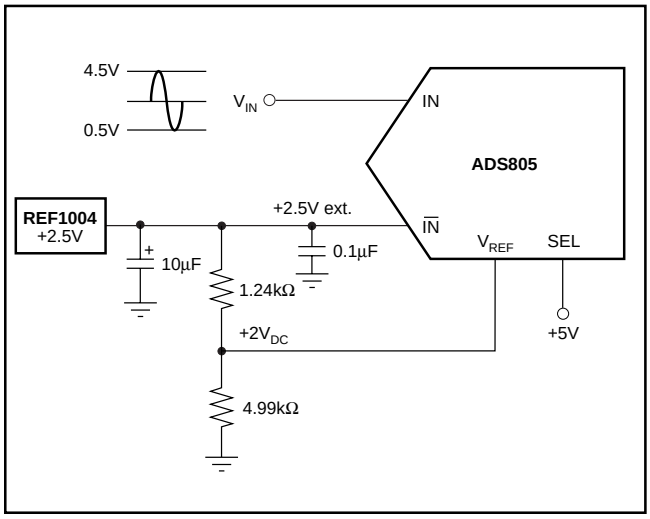


FIGURE 10. External Reference, Input Range 0.5V to 4.5V (4Vp-p), with +2.5V Common-Mode Voltage.

DIGITAL INPUTS AND OUTPUTS

Over-Range (OVR)

One feature of the ADS805 is its 'Over-Range' (OVR) digital output. This pin can be used to monitor any out-of-range condition, which occurs every time the applied analog input voltage exceeds the input range (set by V_{REF}). The OVR output is LOW when the input voltage is within the defined input range. It becomes HIGH when the input voltage is beyond the input range. This is the case when the input voltage is either below the bottom reference voltage or above the top reference voltage. OVR will remain active until the analog input returns to its normal signal range and another conversion is completed. Using the MSB and its complement in conjunction with OVR, a simple decode logic can be built that detects the over-range and under-range conditions, (see Figure 11). It should be noted that OVR is a digital output which is updated along with the bit information corresponding to the particular sampling incidence of the analog signal. Therefore, the OVR data is subject to the same pipeline delay (latency) as the digital data.

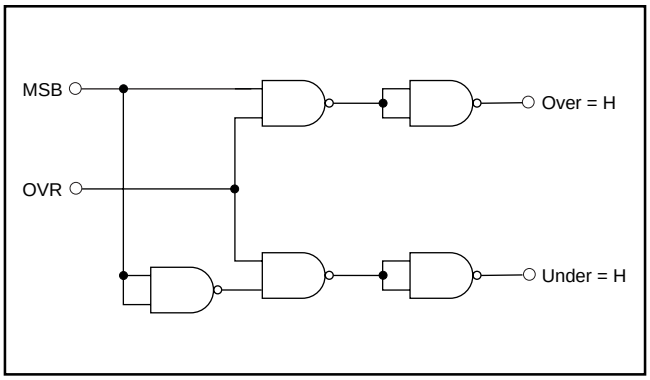


FIGURE 11. External Logic for Decoding Under-Range and Over-Range Conditions.

CLOCK INPUT REQUIREMENTS

Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. It leads to aperture jitter (t_A) which adds noise to the signal being converted. The ADS805 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by Equation 2. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20\log\frac{1}{2\pi f_{IN} t_A}\ \text{rms signal to rms noise} \quad (2)$$

Where: f_{IN} is Input Signal Frequency,

t_A is rms Clock Jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have a 50% duty cycle ($t_H = t_L$), along with fast rise-and-fall times of 2ns or less.

DIGITAL OUTPUTS

The digital outputs of the ADS805 are designed to be compatible with both high-speed TTL and CMOS logic families. The driver stage for the digital outputs is supplied through a separate supply pin, VDRV, which is not connected to the analog supply pins. By adjusting the voltage on VDRV, the digital output levels will vary respectively. Therefore, it is possible to operate the ADS805 on a +5V analog supply while interfacing the digital outputs to 3V-logic with the VDRV pin tied to the +3V digital supply.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Larger capacitive loads demand higher charging currents as the outputs are changing. Those high-current surges can feed back to the analog portion of the ADS805 and influence the performance. If necessary, external buffers or latches may be used which provide the added benefit of isolating the ADS805 from any digital noise activities on the bus coupling back high-frequency noise. In addition, resistors in series with each data line may help maintain the ac performance of the ADS805. Their use depends on the capacitive loading seen by the converter. Values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances, as the output levels change from LOW to HIGH or HIGH to LOW.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. It is recommended that the analog and digital ground pins of the ADS805 be joined together at the IC and be connected only to the analog ground of the system.

The ADS805 has analog and digital supply pins, however the converter should be treated as an analog component and all supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise that would otherwise be coupled into the converter and degrade the achievable performance.

Because of the pipeline architecture, the converter also generates high-frequency current transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 12 shows the recommended decoupling scheme for the analog supplies. In most cases, 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger size bipolar capacitor (1µF to 22µF) should be placed on the PC board in close proximity to the converter circuit.

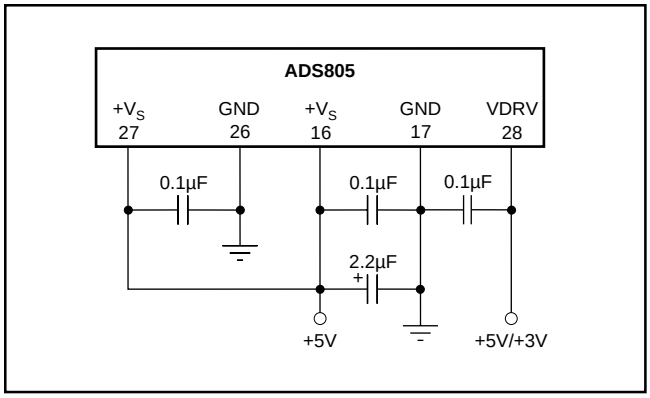


FIGURE 12. Recommended Bypassing for Analog Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS805E	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS805E	Samples
ADS805E/1K	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS805E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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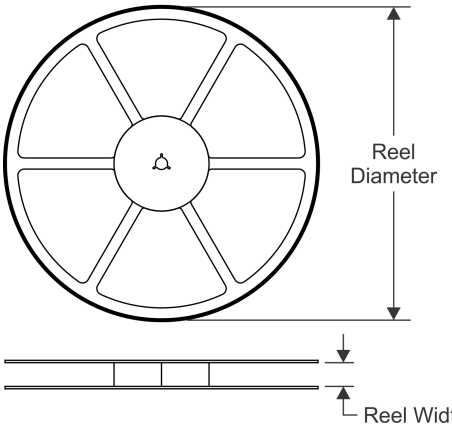
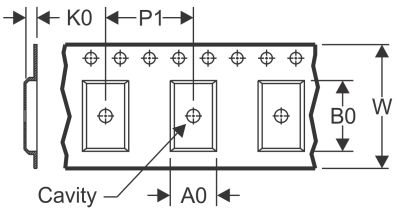
TAPE AND REEL INFORMATION

REEL DIMENSIONS

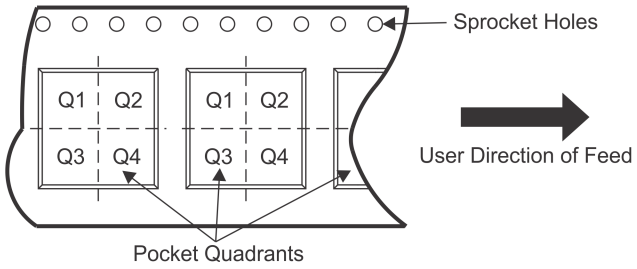


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

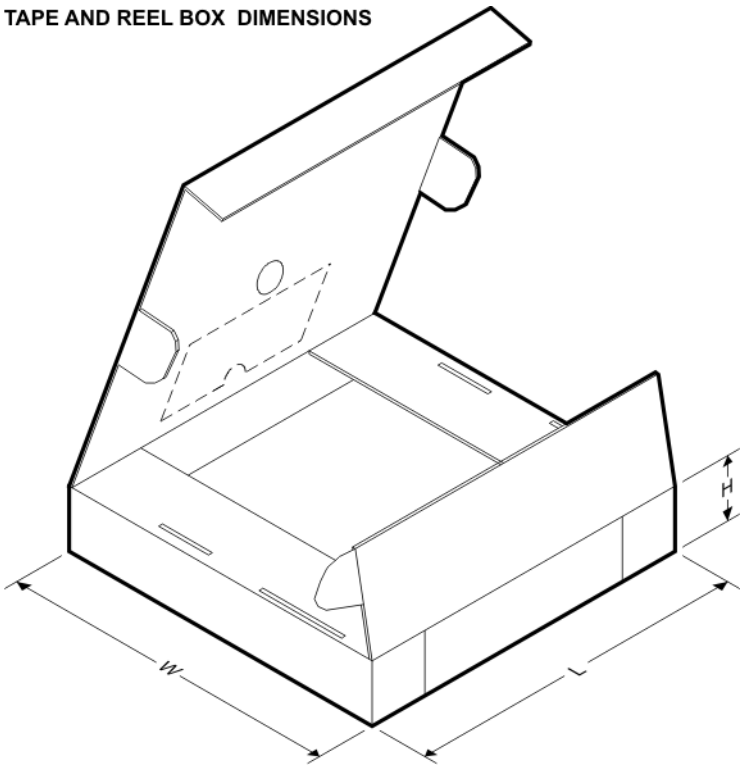
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS805E/1K	SSOP	DB	28	1000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

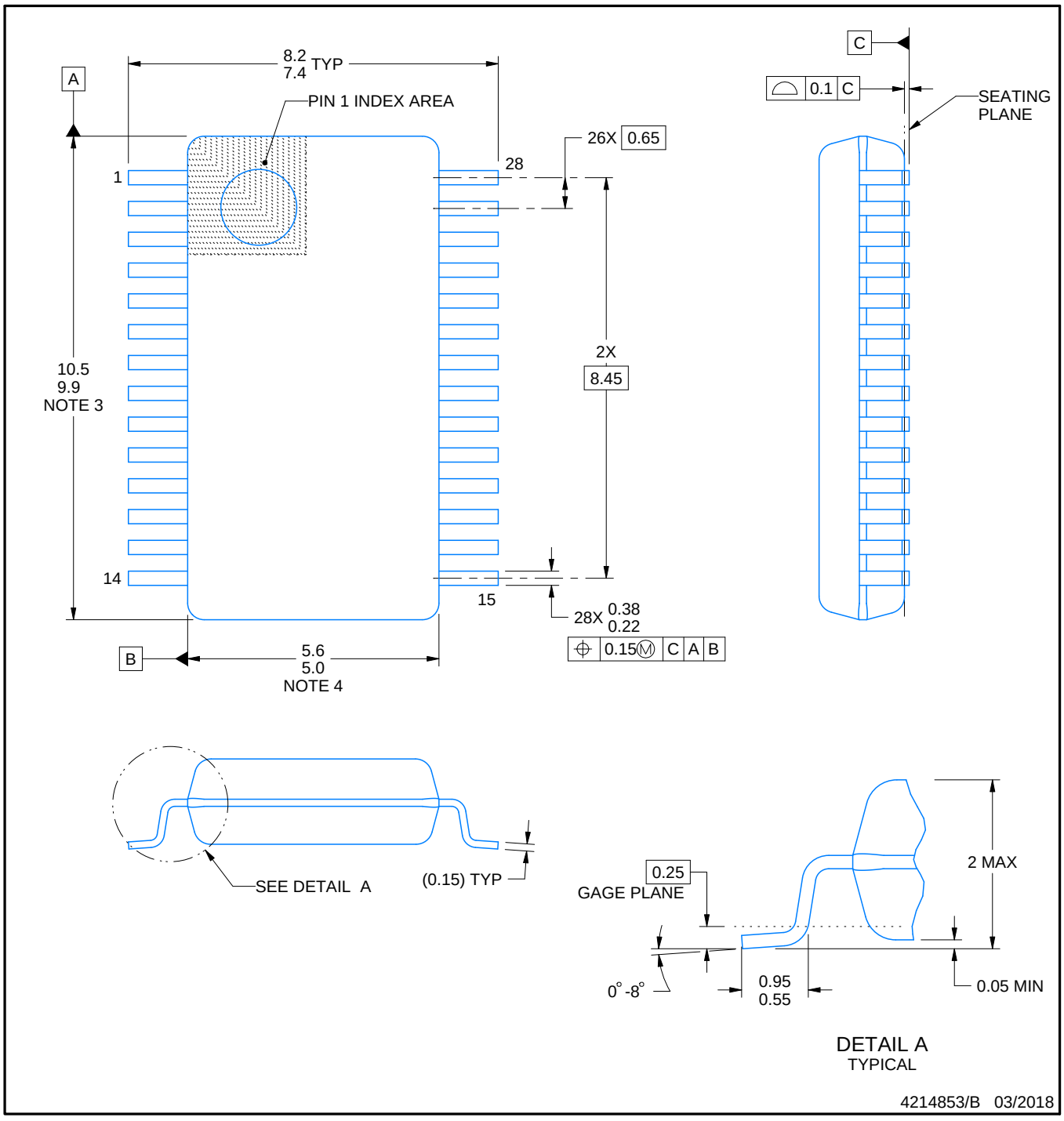
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS805E/1K	SSOP	DB	28	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DB0028A

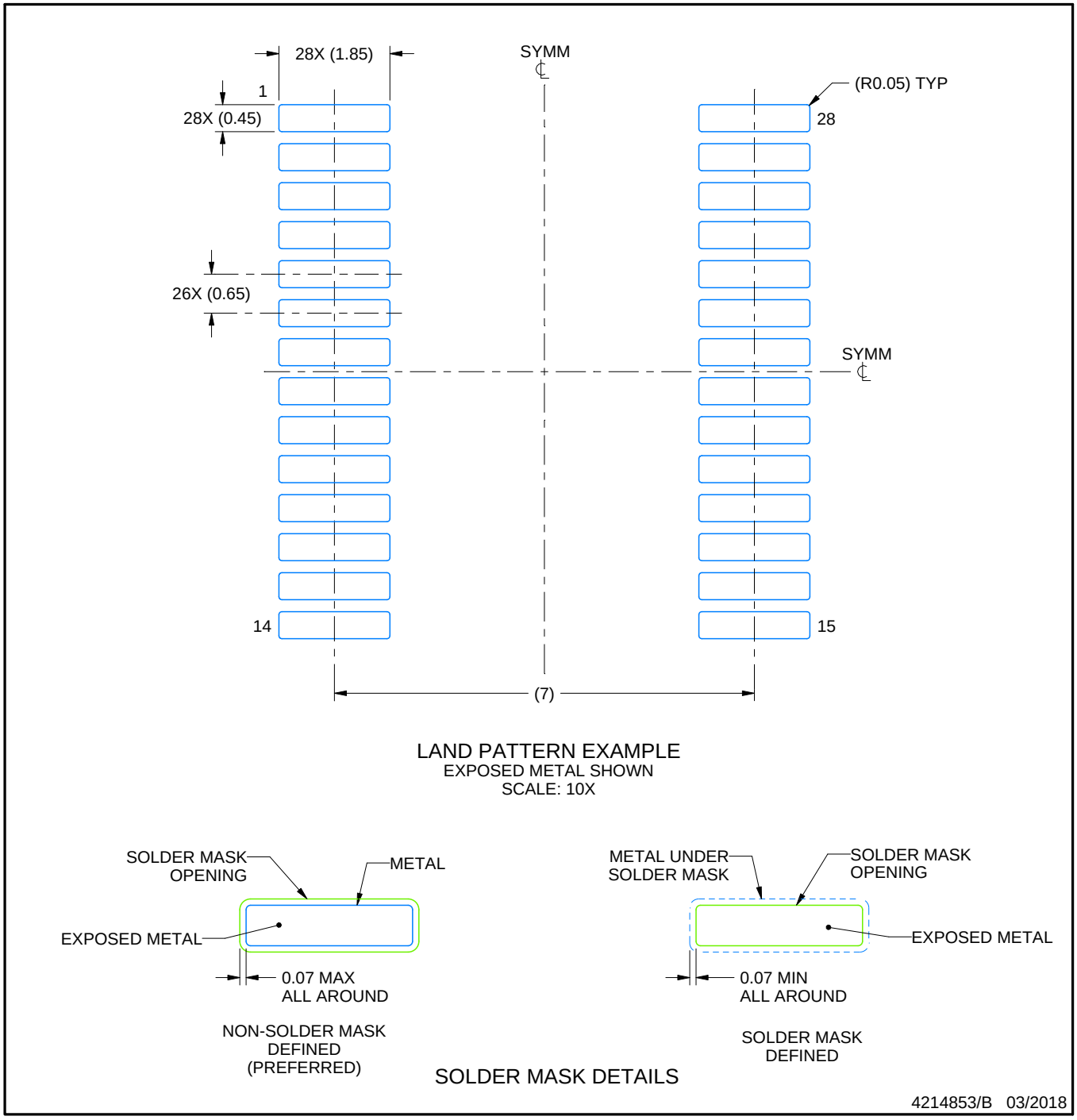
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



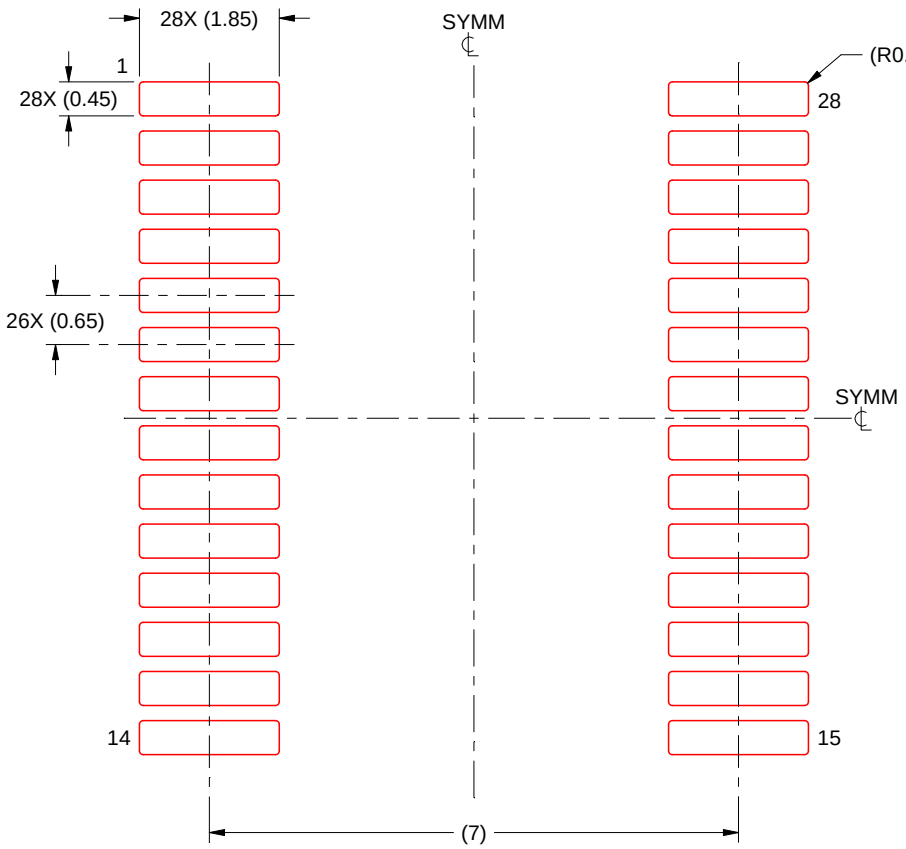
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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