

SBAS101B – JANUARY 1998 – REVISED AUGUST 2005

Dual 500kHz, 12-Bit, 2 + 2 Channel Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 4 INPUT CHANNELS
- FULLY DIFFERENTIAL INPUTS
- 2μs TOTAL THROUGHPUT PER CHANNEL
- GUARANTEED NO MISSING CODES
- PARALLEL INTERFACE
- 1MHz EFFECTIVE SAMPLING RATE
- LOW POWER: 40mW

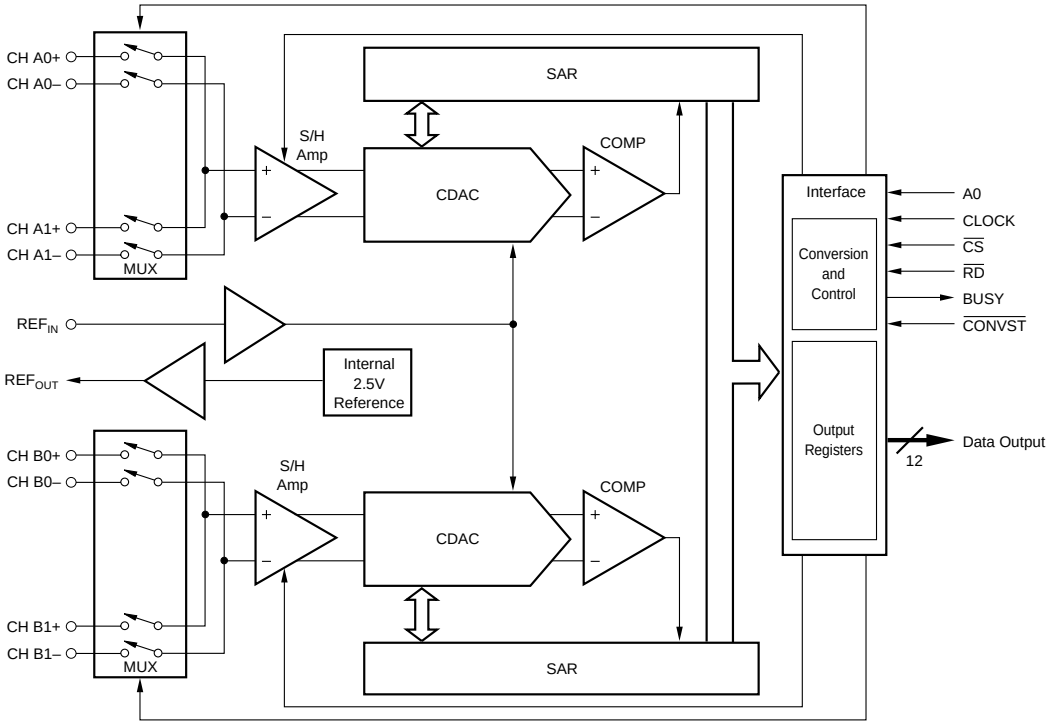
APPLICATIONS

- MOTOR CONTROL
- MULTI-AXIS POSITIONING SYSTEMS
- 3-PHASE POWER CONTROL

DESCRIPTION

The ADS7862 is a dual 12-bit, 500kHz analog-to-digital converter (A/D) with 4 fully differential input channels grouped into two pairs for high speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the A/D converter. This provides excellent common-mode rejection of 80dB at 50kHz, which is important in high noise environments.

The ADS7862 offers parallel interface and control inputs to minimize software overhead. The output data for each channel is available as a 12-bit word. The ADS7862 is offered in an TQFP-32 package and is fully specified over the –40°C to +85°C operating range.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION[1]

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (%)	PACKAGE	PACKAGE DESIGNATOR	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7862Y	±2	±0.75	TQFP-32	PBS	–40°C to +85°C	ADS7862Y/250	Tape and Reel, 250
ADS7862Y	"	"	"	"	"	ADS7862Y/2K5	Tape and Reel, 2500
ADS7862YB	±1	±0.5	TQFP-32	PBS	–40°C to +85°C	ADS7862YB/250	Tape and Reel, 250
ADS7862YB	"	"	"	"	"	ADS7862YB/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs to AGND: Any Channel Input ..... –0.3V to ($+V_D$ + 0.3V)
REF_{IN} ..... –0.3V to ($+V_D$ + 0.3V)
Digital Inputs to DGND ..... –0.3V to ($+V_D$ + 0.3V)
Ground Voltage Differences: AGND, DGND ..... ±0.3V
$+V_D$ to AGND ..... –0.3V to +6V
Power Dissipation 325mW
Maximum Junction Temperature ..... +150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

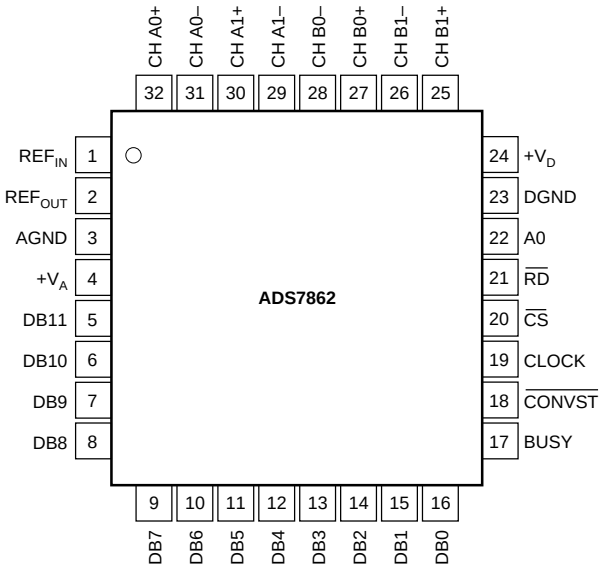
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	REF_{IN}	Reference Input
2	REF_{OUT}	+2.5V Reference Output. Connect directly to REF_{IN} (pin 1) when using internal reference.
3	AGND	Analog Ground
4	$+V_A$	Analog Power Supply, +5VDC. Connect directly to digital power supply (pin 24). Decouple to analog ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.
5	DB11	Data Bit 11, MSB
6	DB10	Data Bit 10
7	DB9	Data Bit 9
8	DB8	Data Bit 8
9	DB7	Data Bit 7
10	DB6	Data Bit 6
11	DB5	Data Bit 5
12	DB4	Data Bit 4
13	DB3	Data Bit 3
14	DB2	Data Bit 2
15	DB1	Data Bit 1
16	DB0	Data Bit 0, LSB
17	BUSY	HIGH when a conversion is in progress.
18	$\overline{CONVST}$	Convert Start
19	CLOCK	An external CMOS-compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source. The CLOCK pin controls the sampling rate by the equation: CLOCK 16 • f_{SAMPLE}.
20	$\overline{CS}$	Chip Select
21	$\overline{RD}$	Synchronization pulse for the parallel output. During a Read operation, the first falling edge selects the A register and the second edge selects the B register, A0, then controls whether input 0 or input 1 is read.
22	A0	On the falling edge of Convert Start, when A0 is LOW Channel A0 and Channel B0 are converted and when it is HIGH, Channel A1 and Channel B1 are converted. During a Read operation, the first falling edge selects the A register and the second edge selects the B of $\overline{RD}$ register, A0, then controls whether input 0 or input 1 is read.
23	DGND	Digital Ground. Connect directly to analog ground (pin 3).
24	$+V_D$	Digital Power Supply, +5VDC
25	CH B1+	Non-Inverting Input Channel B1
26	CH B1–	Inverting Input Channel B1
27	CH B0+	Non-Inverting Input Channel B0
28	CH B0–	Inverting Input Channel B0
29	CH A1–	Inverting Input Channel A1
30	CH A1+	Non-Inverting Input Channel A1
31	CH A0–	Inverting Input Channel A0
32	CH A0+	Non-Inverting Input Channel A0

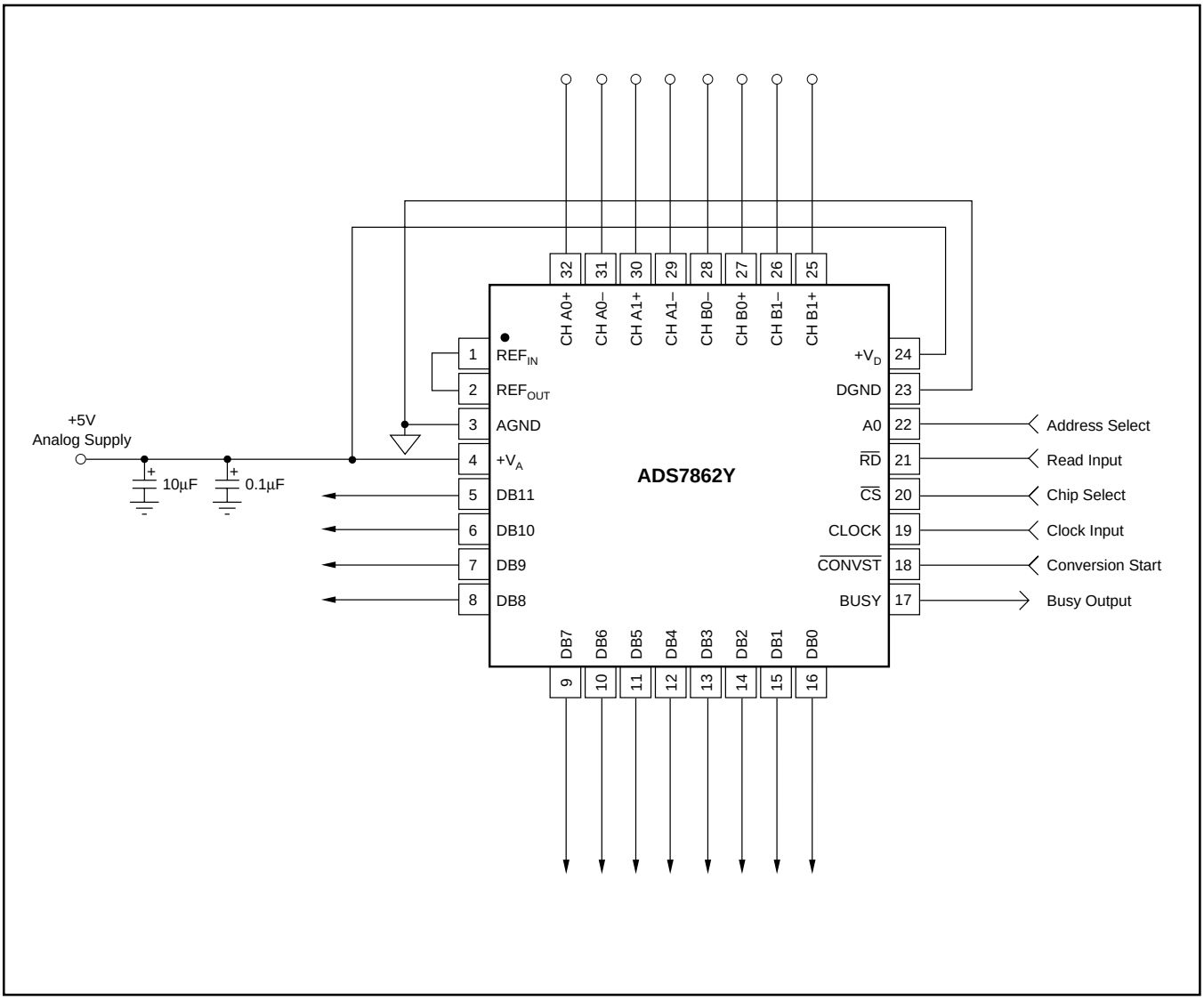
ELECTRICAL CHARACTERISTICS

All specifications T_{MIN} to T_{MAX}, $+V_A = +V_D = +5V$, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7862Y			ADS7862YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Input Voltage Range-Bipolar	V_{CENTER} = Internal V_{REF} at 2.5V	$-V_{REF}$		$+V_{REF}$	*		*	V
Absolute Input Range	+IN	–0.3		V_{CC} + 0.3				V
	–IN	–0.3		V_{CC} + 0.3				V
Input Capacitance			15			*		pF
Input Leakage Current	CLK = GND		±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity			±0.75	±2		±0.5	±1	LSB
Integral Linearity Match			0.5	1		*	*	LSB
Differential Linearity			±0.75			±0.5	±1	LSB
Bipolar Offset Error	Referenced to REF_{IN}		±0.75	±3		±0.5	±2	LSB
Bipolar Offset Error Match				3			2	LSB
Positive Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.1	±0.5	% of FSR
Positive Gain Error Match				2			1	LSB
Negative Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.1	±0.5	% of FSR
Negative Gain Error Match				2			1	LSB
Common-Mode Rejection Ratio	At DC		80			*		dB
	V_{IN} = ±1.25V_{PP} at 50kHz		80			*		dB
Noise			120			*		μV_{RMS}
Power Supply Rejection Ratio			±0.5	±2		*	*	LSB
SAMPLING DYNAMICS								
Conversion Time per A/D			1.75			*		µs
Acquisition Time			0.25			*		µs
Throughput Rate		500			*			kHz
Aperture Delay			3.5			*		ns
Aperture Delay Matching			100			*		ps
Aperture Jitter			50			*		ps
Small-Signal Bandwidth			40			*		MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion	V_{IN} = ±2.5V_{PP} at 100kHz		75			*		dB
SINAD	V_{IN} = ±2.5V_{PP} at 100kHz		71			*		dB
Spurious Free Dynamic Range	V_{IN} = ±2.5V_{PP} at 100kHz		–78			*		dB
Channel-to-Channel Isolation	V_{IN} = ±2.5V_{PP} at 100kHz			–80			*	dB
VOLTAGE REFERENCE								
Internal		2.475	2.5	2.525	*	*	*	V
Internal Drift			±25			*		ppm/°C
Internal Noise			50			*		μV_{PP}
Internal Source Current			2			*		mA
Internal Load Rejection			0.005			*		mV/µA
Internal PSRR			65			*		dB
External Voltage Range		1.2	2.5	2.6	*	*	*	V
Input Current			0.05	1		*	*	µA
Input Capacitance			5			*		pF
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels: V_{IH}	I_{IH} = +5µA	3.0		$+V_{DD}$ + 0.3	*		*	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –500µA	3.5			*			V
V_{OL}	I_{OL} = 500µA			0.4			*	V
External Clock		0.2		8	*		*	MHz
Data Format			Binary Two's Complement			*		
POWER SUPPLY REQUIREMENTS								
Power Supply Voltage, +V		4.75	5	5.25	*	*	*	V
Quiescent Current, $+V_A$			5	8		*	*	mA
Power Dissipation			25	40		*	*	mW

* Specifications same as ADS7862Y.

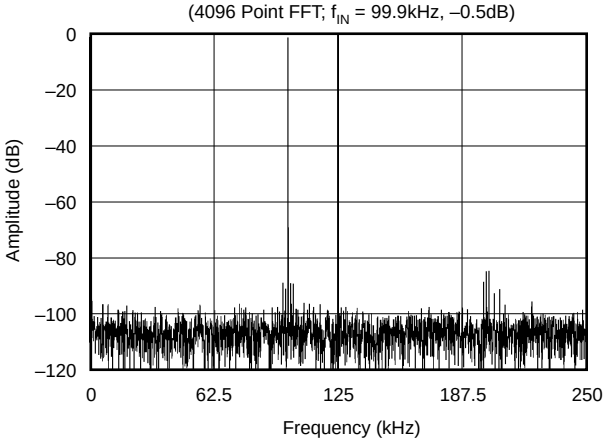
BASIC OPERATION



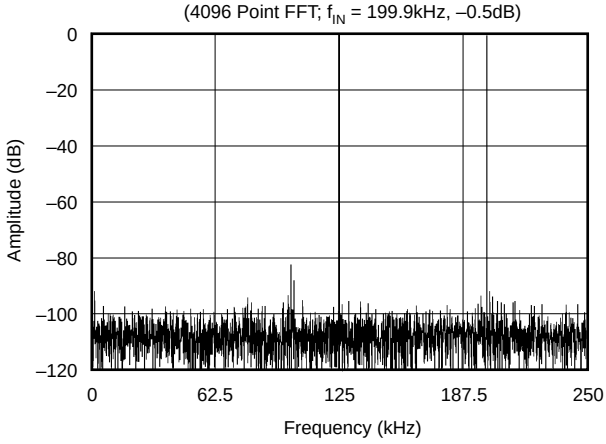
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz, unless otherwise noted.

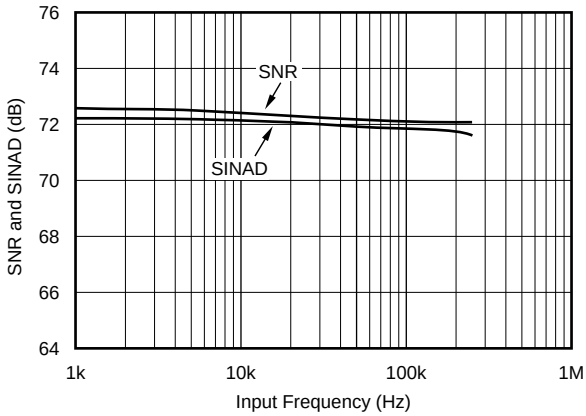
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 99.9kHz, –0.5dB)



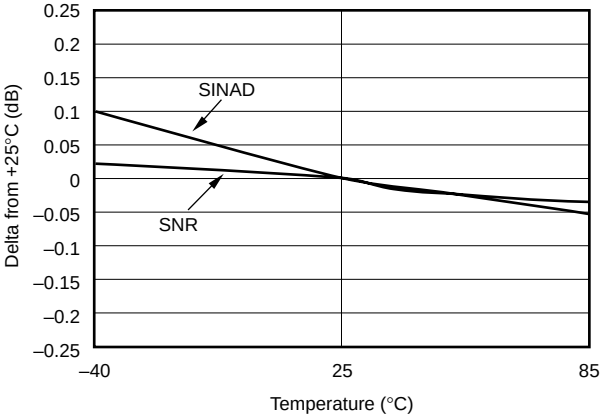
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 199.9kHz, –0.5dB)



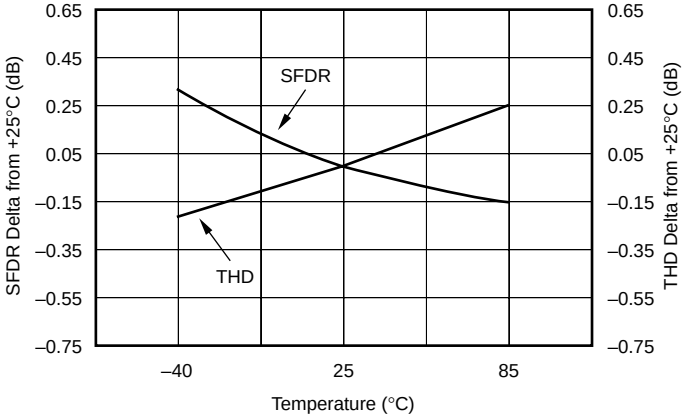
SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



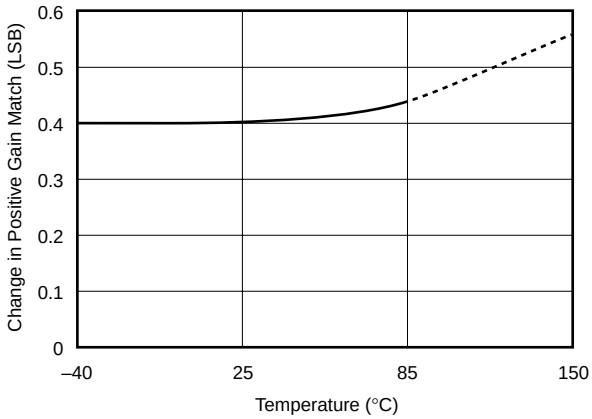
CHANGE IN SIGNAL-TO-NOISE RATIO
AND SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



CHANGE IN SPURIOUS FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE



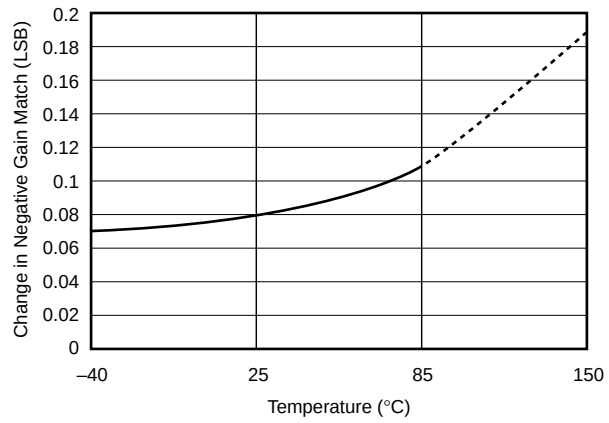
CHANGE IN POSITIVE GAIN MATCH
vs TEMPERATURE
(Maximum Deviation for All Four Channels)



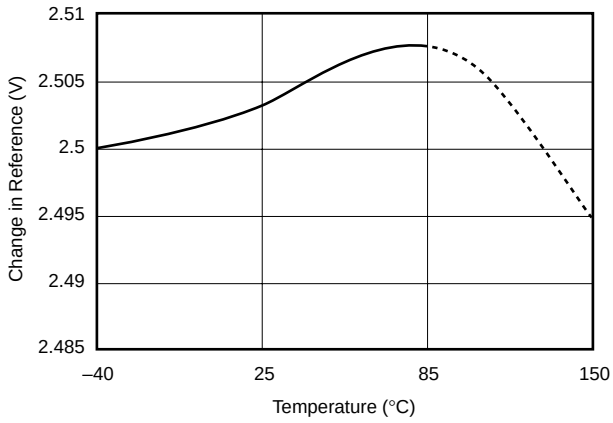
TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz, unless otherwise noted.

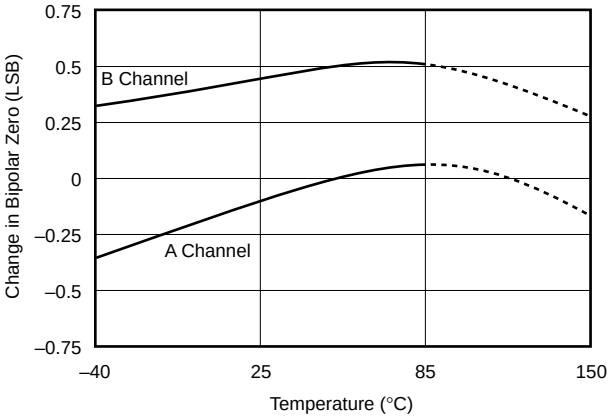
CHANGE IN NEGATIVE GAIN MATCH
vs TEMPERATURE
(Maximum Deviation for All Four Channels)



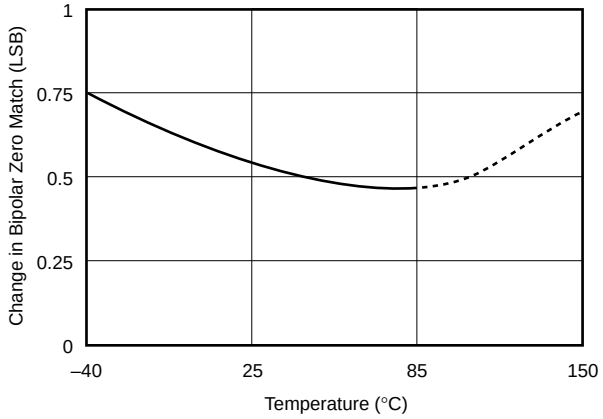
CHANGE IN REFERENCE VOLTAGE
vs TEMPERATURE



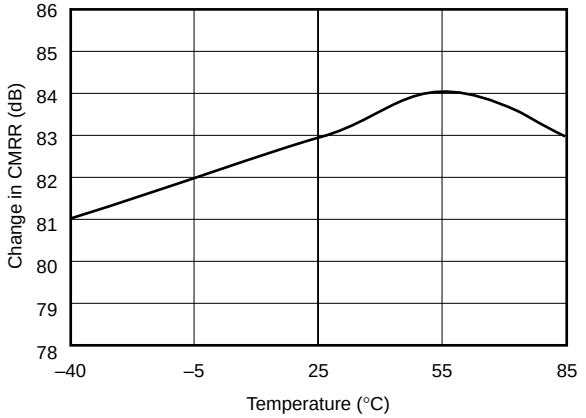
CHANGE IN BIPOLAR ZERO
vs TEMPERATURE



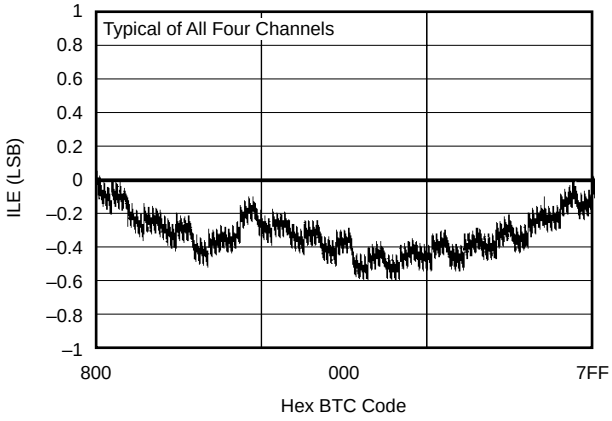
CHANGE IN BPZ MATCH vs TEMPERATURE



CHANGE IN CMRR vs TEMPERATURE



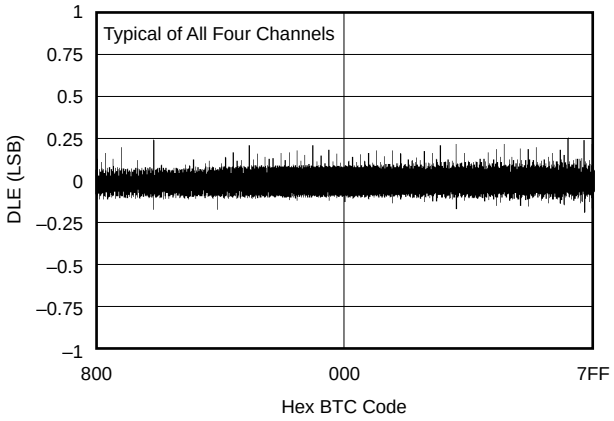
INTEGRAL LINEARITY ERROR vs CODE



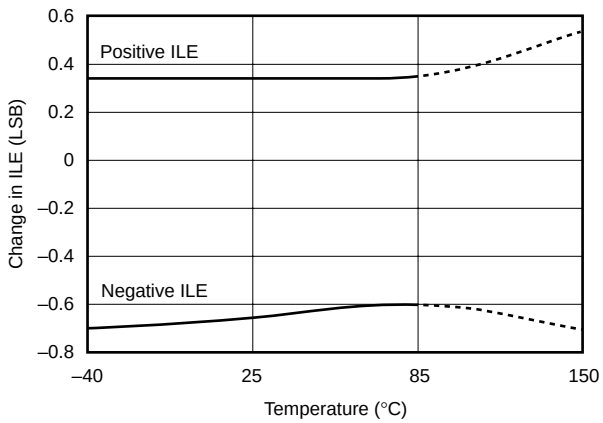
TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz, unless otherwise noted.

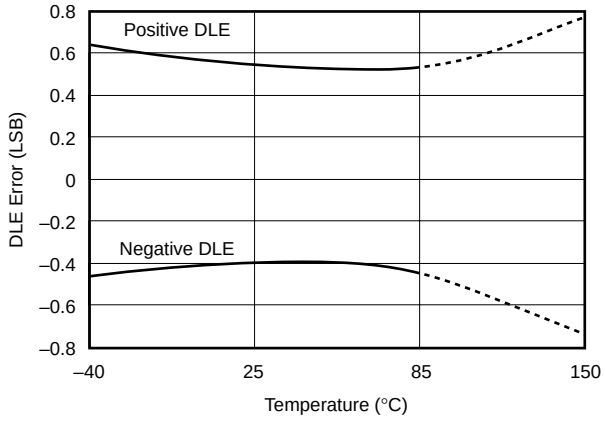
DIFFERENTIAL LINEARITY ERROR vs CODE



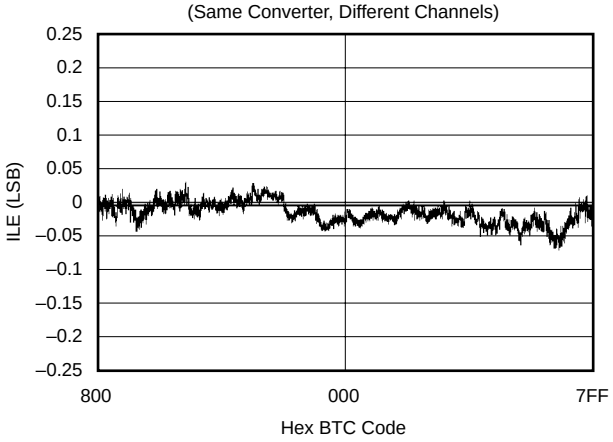
INTEGRAL LINEARITY ERROR vs TEMPERATURE



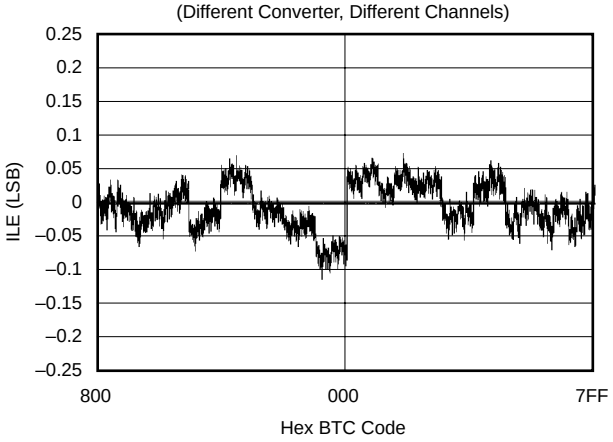
DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



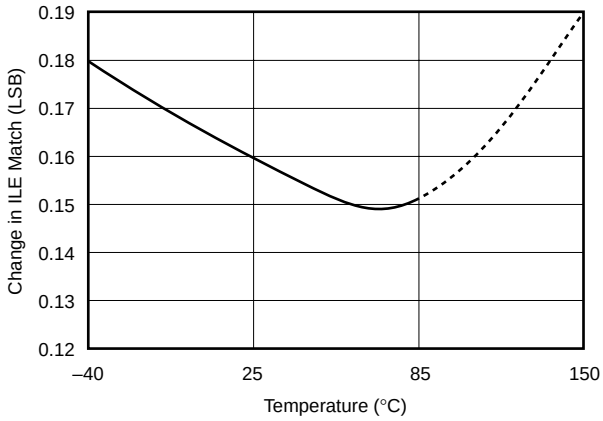
INTEGRAL LINEARITY ERROR MATCH
vs CODE CHANNEL A0/CHANNEL A1
(Same Converter, Different Channels)



INTEGRAL LINEARITY ERROR MATCH
vs CODE CHANNEL A0/CHANNEL B1
(Different Converter, Different Channels)



INTEGRAL LINEARITY ERROR MATCH
vs TEMPERATURE
CHANNEL A0/CHANNEL B0
(Different Converter, Different Channels)



INTRODUCTION

The ADS7862 is a high speed, low power, dual 12-bit A/D converter that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains dual 2µs successive approximation A/Ds, two differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins and a high speed parallel interface. There are four analog inputs that are grouped into two channels (A and B) selected by the A0 input (A0 LOW selects Channels A0 and B0, while A0 HIGH selects Channels A1 and B1). Each A/D converter has two inputs (A0 and A1 and B0 and B1) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered around the internal +2.5V reference. The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 7).

A conversion is initiated on the ADS7862 by bringing the $\overline{CONVST}$ pin LOW for a minimum of 15ns. $\overline{CONVST}$ LOW places both sample-and-hold amplifiers in the hold state simultaneously and the conversion process is started on both channels. The BUSY output will then go HIGH and remain HIGH for the duration of the conversion cycle. Depending on the status of the A0 pin, the data will either reflect a conversion of Channel 0 (A0 LOW) or Channel 1 (A0 HIGH). The data can be read from the parallel output bus following the conversion by bringing both $\overline{RD}$ and $\overline{CS}$ LOW.

Conversion time for the ADS7862 is 1.75µs when an 8MHz external clock is used. The corresponding acquisition time is 0.25µs. To achieve maximum output rate (500kHz), the read function can be performed immediately at the start of the next conversion.

NOTE: This mode of operation is described in more detail in the Timing and Control section of this data sheet.

SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS7862 allow the A/Ds to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the A/D even when the A/D is operated at its maximum throughput rate of 500kHz. The typical small-signal bandwidth of the sample-and-hold amplifiers is 40MHz.

Typical aperture delay time or the time it takes for the ADS7862 to switch from the sample to the hold mode following the $\overline{CONVST}$ pulse is 3.5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS7862 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, the REF_{OUT} pin (pin 2) should be directly connected to the REF_{IN} pin (pin 1) to provide an internal +2.5V reference to the ADS7862. The ADS7862 can operate, however, with an external reference in the range of 1.2V to 2.6V for a corresponding full-scale range of 2.4V to 5.2V.

The internal reference of the ADS7862 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 2 (the internal reference can typically source 2mA of current—load capacitance should not exceed 100pF). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of both CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS7862: single-ended or differential (see Figures 1 and 2). When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode $+V_{REF}$) and the (common-mode $-V_{REF}$). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 3).

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or: (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out of phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 4).

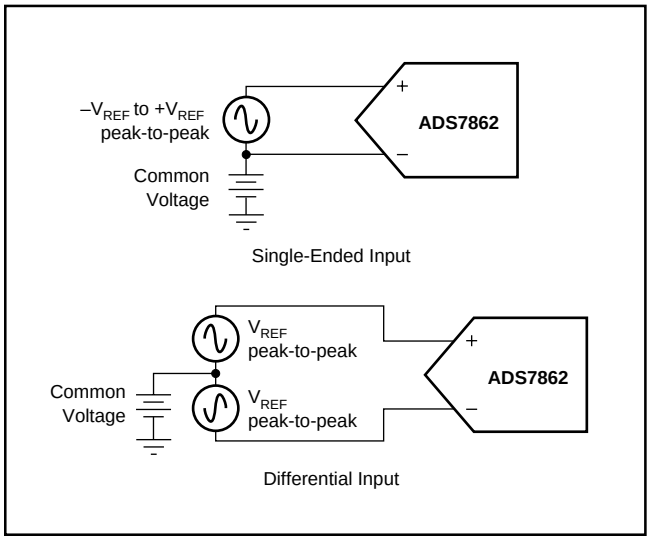
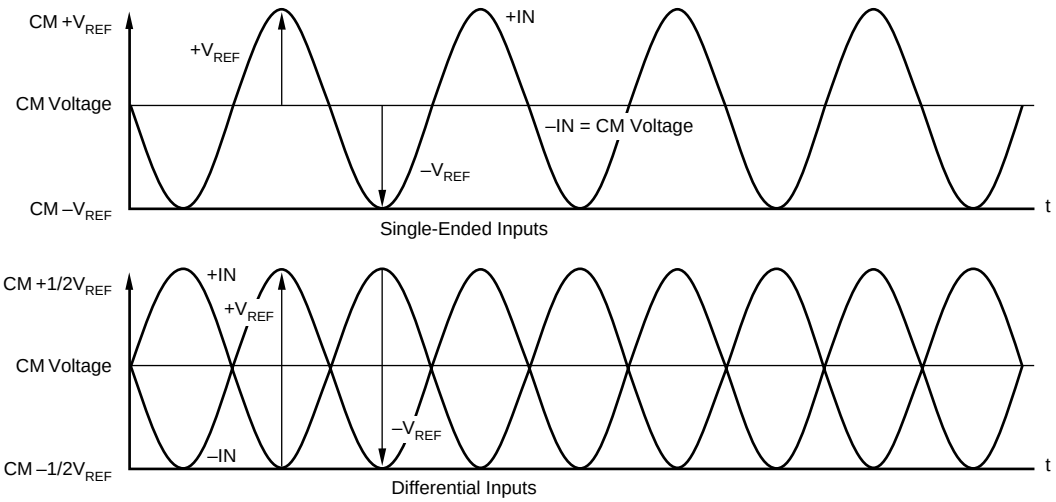


FIGURE 1. Methods of Driving the ADS7862 Single-Ended or Differential.



NOTES: Common-Mode Voltage (Differential Mode) = $\frac{(IN+) + (IN-)}{2}$ Common-Mode Voltage (Single-Ended Mode) = IN–.

The maximum differential voltage between +IN and –IN of the ADS7862 is V_{REF}. See Figures 3 and 4 for a further explanation of the common voltage range for single-ended and differential inputs.

FIGURE 2. Using the ADS7862 in the Single-Ended and Differential Input Modes.

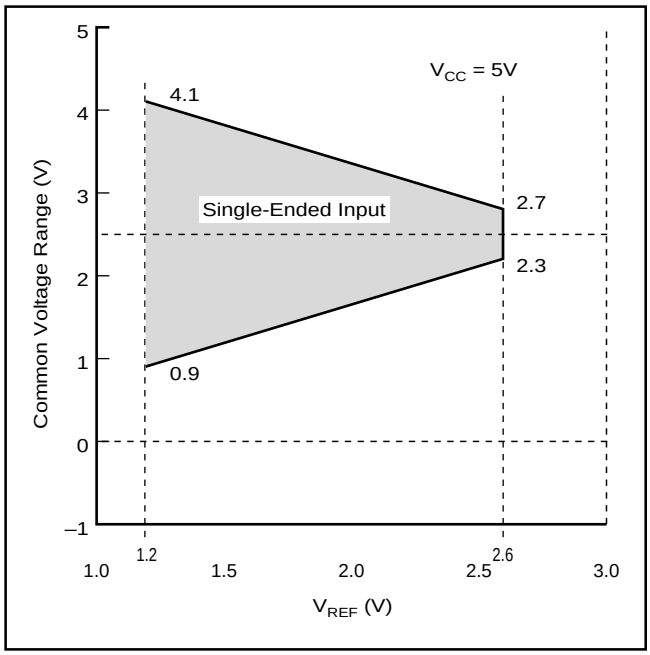


FIGURE 3. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}.

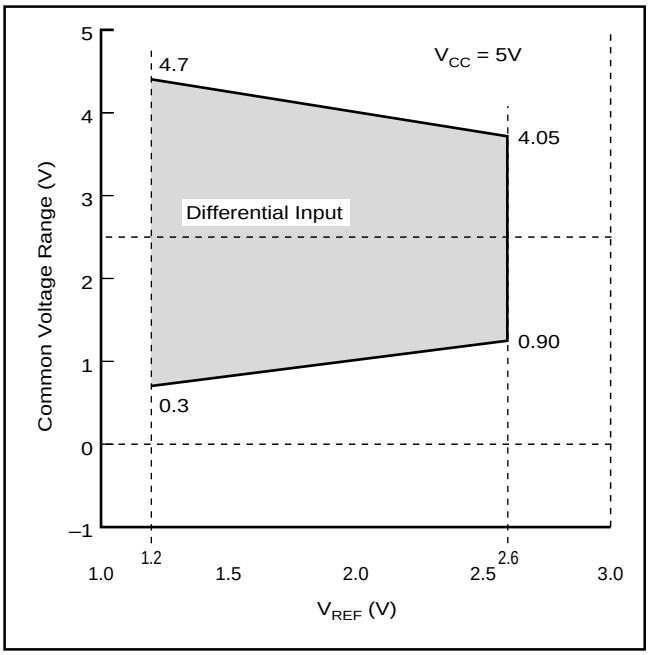


FIGURE 4. Differential Input: Common-Mode Voltage Range vs V_{REF}.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Otherwise, this may result in offset error, which will change with both temperature and input voltage.

The input current on the analog inputs depend on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS7862 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (15pF) to a 12-bit settling level within 2 clock cycles. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN input should always remain within the range of GND – 300mV to V_{DD} + 0.3V.

TRANSITION NOISE

Figure 5 shows a histogram plot for the ADS7862 following 8,000 conversions of a DC input. The DC input was set at output code 2046. All but one of the conversions had an output code result of 2046 (one of the conversions resulted in an output of 2047). The histogram reveals the excellent noise performance of the ADS7862.

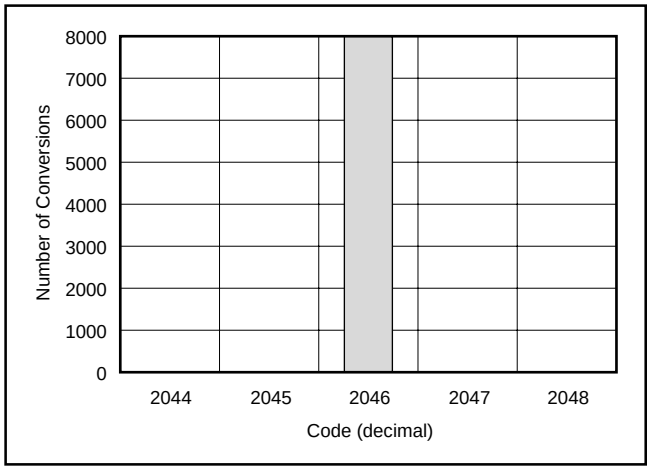


FIGURE 5. Histogram of 8,000 Conversions of a DC Input.

BIPOLAR INPUTS

The differential inputs of the ADS7862 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the internal reference voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring a single amplifier and four external resistors, the ADS7862 can be configured to except bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS7862 using the resistor values shown in Figure 7.

TIMING AND CONTROL

The ADS7862 uses an external clock (CLOCK, pin 19) which controls the conversion rate of the CDAC. With an 8MHz external clock, the A/D sampling rate is 500kHz which corresponds to a 2µs maximum throughput time.

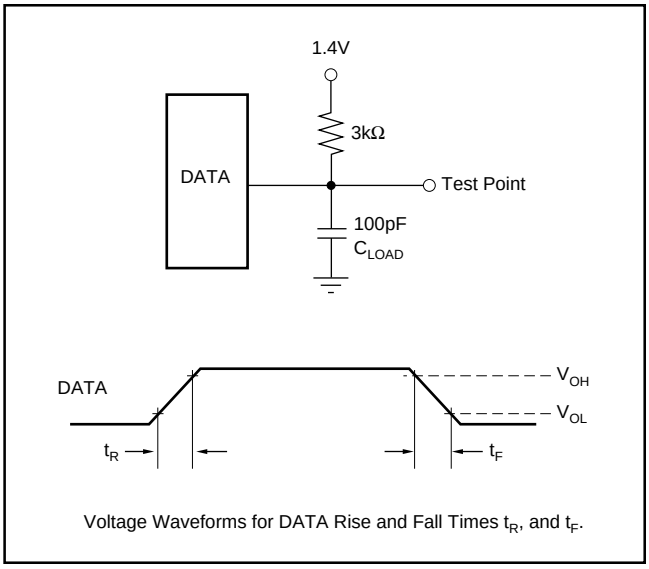
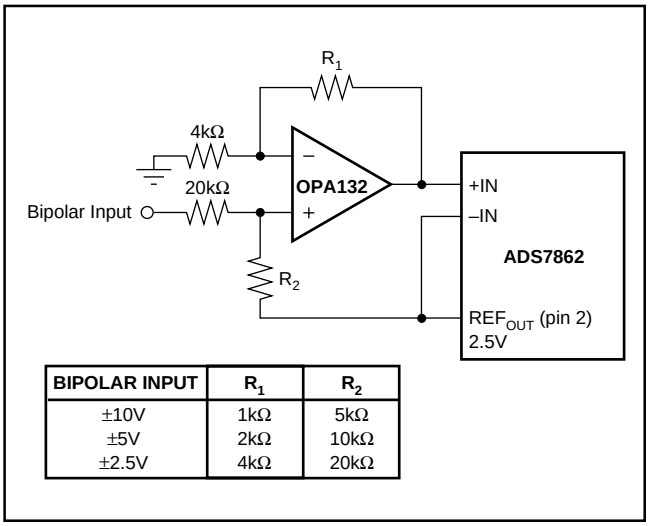


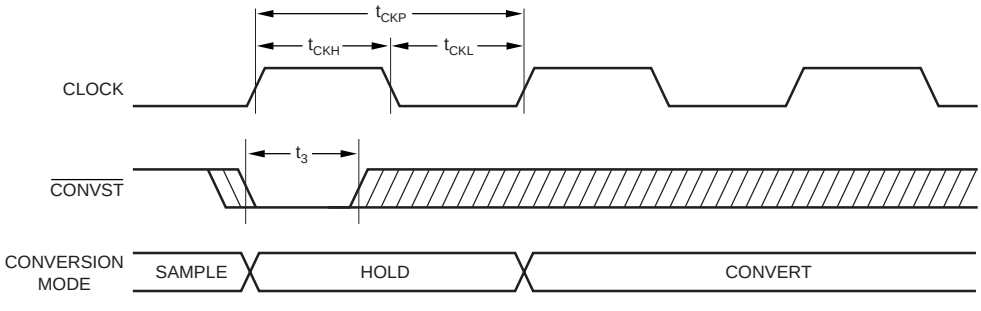
FIGURE 6. Test Circuits for Timing Specifications.



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

FIGURE 7. Level Shift Circuit for Bipolar Input Ranges.

Three timing diagrams are used to explain the operation of the ADS7862. Figure 8 shows the timing relationship between the CLOCK, $\overline{CONVST}$ (pin 18) and the conversion



NOTE: The ADS7862 will switch from the sample to the hold mode the instant $\overline{CONVST}$ goes LOW regardless of the state of the external clock. The conversion process is initiated with the first rising edge of the external clock following $\overline{CONVST}$ going LOW.

FIGURE 8. Conversion Mode.

mode. Figure 9, in conjunction with Table I, shows the basic read/write functions of the ADS7862 and highlights all of the timing specifications. Figure 10 shows a more detailed description of initiating a conversion using $\overline{\text{CONVST}}$. Figure 11 illustrates three consecutive conversions and, with the accompanying text, describes all of the read and write capabilities of the ADS7862.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
Full-Scale Input Span	$-V_{REF}$ to $+V_{REF}$ (1)		
Least Significant Bit (LSB)	$(-V_{REF}$ to $+V_{REF})/4096$ (2)	BINARY CODE	HEX CODE
+Full Scale	4.99878V	0111 1111 1111	7FF
Midscale	2.5V	0000 0000 0000	000
Midscale – 1 LSB	2.49878V	1111 1111 1111	FFF
–Full Scale	0V	1000 0000 0000	800

NOTES: (1) $-V_{REF}$ to $+V_{REF}$ around V_{REF}. With a 2.5V reference, this corresponds to a 0V to 5V input span. (2) 1.22mV with a 2.5V reference.

TABLE I. Ideal Input Voltages and Output Codes.

The Figure 11 timing diagram can be divided into three sections: (a) initiating a conversion (n – 2), (b) starting a second conversion (n – 1) while reading the data output from the previous conversion (n – 2), and (c) starting a third conversion (n) while reading both previous conversions (n – 2 and n – 1). In this sequence, Channel 0 is converted first followed by Channel 1. Channel 1 can be converted prior to Channel 0 if the user wishes by simply starting the conversion process with the A0 pin at logic HIGH (Channel 1) followed by logic LOW (Channel 0).

TIMING SPECIFICATIONS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			1.75	µs
t_{ACQ}	Acquisition Time			0.25	µs
t_{CKP}	Clock Period	125		5000	ns
t_{CKL}	Clock LOW	40			ns
t_{CKH}	Clock HIGH	40			ns
t_1	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	0			ns
t_2	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	0			ns
t_3	$\overline{\text{CONVST}}$ LOW	15			ns
t_4	RD Pulse Width	30			ns
t_5	$\overline{\text{RD}}$ to Valid Data (Bus Access)		16	25	ns
t_6	$\overline{\text{RD}}$ to HI-Z Delay (Bus Relinquish)		10	20	ns
t_7	Time Between Conversion Reads	40			ns
t_8	Address Setup Time	250			ns
t_9	$\overline{\text{CONVST}}$ HIGH	20			ns
t_{10}	Address Hold Time	20			ns
t_{11}	$\overline{\text{CONVST}}$ to BUSY Propagation Delay			30	ns
t_{12}	$\overline{\text{CONVST}}$ LOW Prior to CLOCK Rising Edge	10			ns
t_{13}	$\overline{\text{CONVST}}$ LOW After CLOCK Rising Edge	5			ns
t_F	Data Fall Time		13	25	ns
t_R	Data Rise Time		20	30	ns

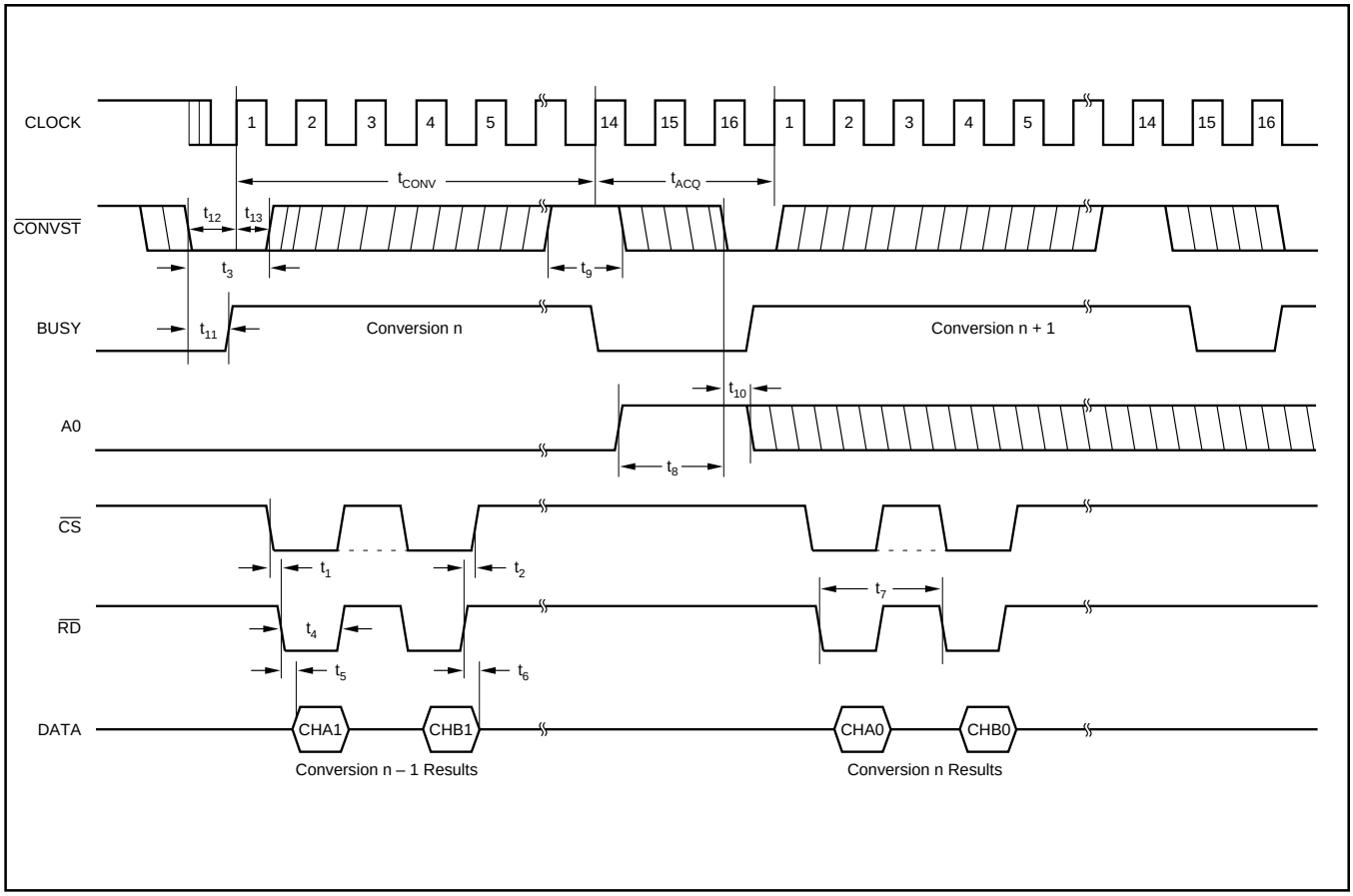
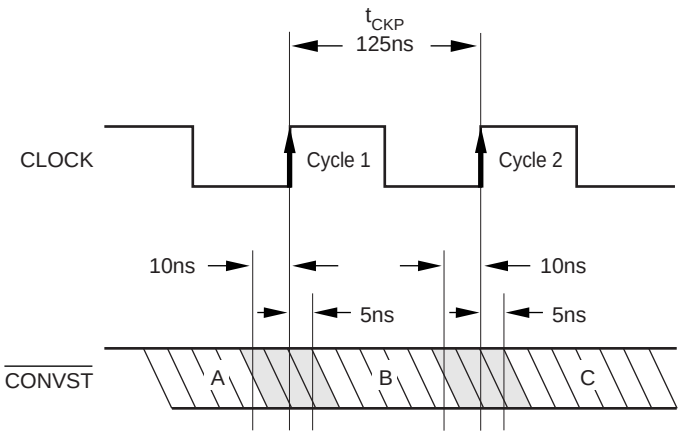


FIGURE 9. Reading and Writing to the ADS7862 During the Same Cycle.



NOTE: All $\overline{\text{CONVST}}$ commands which occur more than 10ns before the rising edge of cycle '1' of the external clock (Region 'A') will initiate a conversion on the rising edge of cycle '1'. All $\overline{\text{CONVST}}$ commands which occur 5ns after the rising edge of cycle '1' or 10ns before the rising edge of cycle 2 (Region 'B') will initiate a conversion on the rising edge of cycle '2'. All $\overline{\text{CONVST}}$ commands which occur 5ns after the rising edge of cycle '2' (Region 'C') will initiate a conversion on the rising edge of the next clock period. The $\overline{\text{CONVST}}$ pin should never be switched from HIGH to LOW in the region 10ns prior to the rising edge of the CLOCK and 5ns after the rising edge (gray areas). If $\overline{\text{CONVST}}$ is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

FIGURE 10. Timing Between CLOCK and $\overline{\text{CONVST}}$ to Start a Conversion.

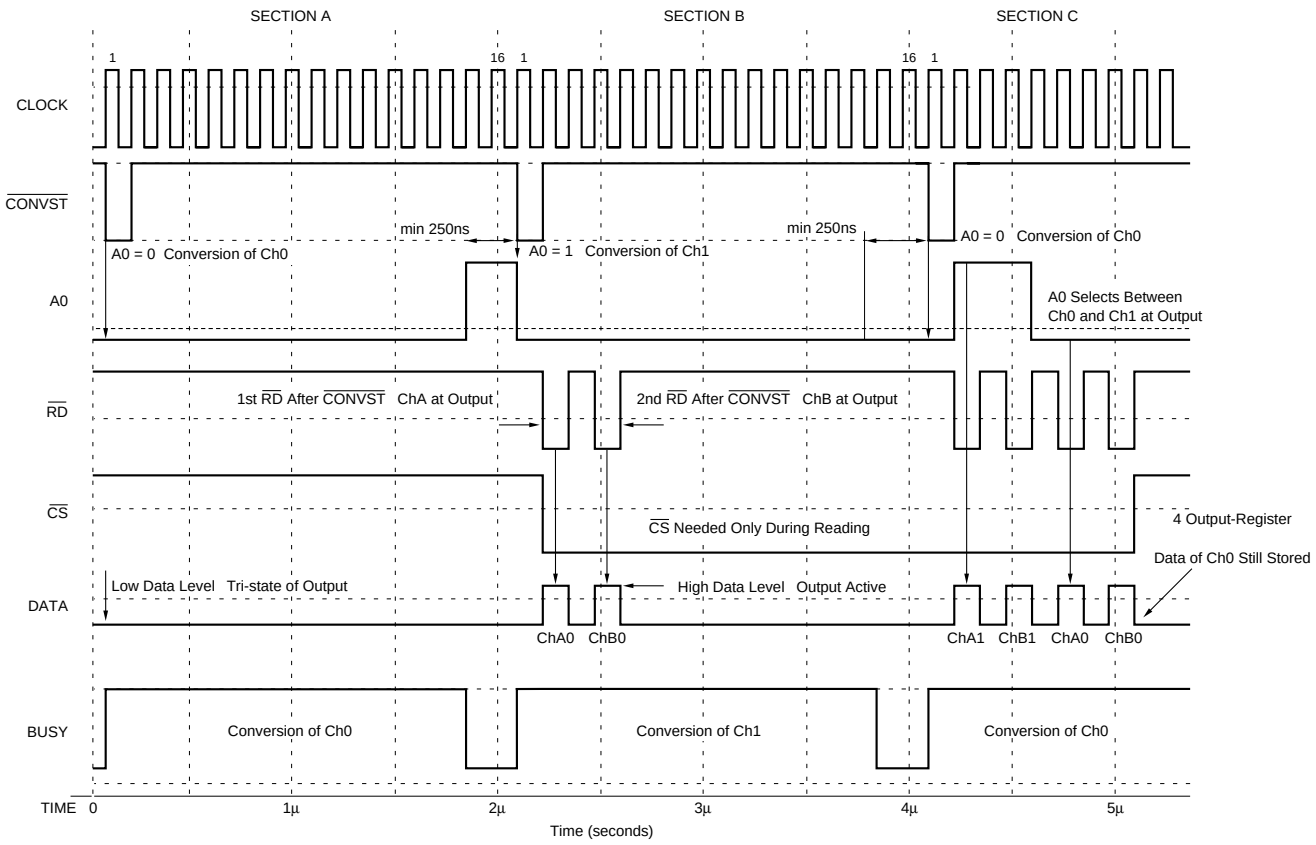


FIGURE 11. ADS7862 Timing Diagram Showing Complete Functionality.

SECTION A

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin (pin 18) LOW for a minimum of 5ns (after the 5ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought HIGH). The ADS7862 will switch from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. Following the first rising edge of the external clock after a $\overline{\text{CONVST}}$ LOW, the ADS7862 will begin conversion (this first rising edge of the external clock represents the start of clock cycle one; the ADS7862 requires sixteen cycles to complete a conversion). The input channel is also latched in at this point in time. The A0 input (pin 22) must be selected 250ns prior to the $\overline{\text{CONVST}}$ pin going LOW so that the correct address will be selected prior to conversion. The BUSY output will go HIGH immediately following $\overline{\text{CONVST}}$ going LOW. BUSY will stay HIGH through the conversion process and return LOW when the conversion has ended. After $\overline{\text{CONVST}}$ has remained LOW for the minimum time, the ADS7862 will switch from the hold mode to the conversion mode synchronous to the next rising edge of the external clock and conversion 'n – 2' will begin. Both $\overline{\text{RD}}$ (pin 21) and $\overline{\text{CS}}$ (pin 20) can be HIGH during and before a conversion. However, they must both be LOW to enable the output bus and read data out.

SECTION B

The $\overline{\text{CONVST}}$ pin is switched from HIGH to LOW a second time to initiate conversion 'n – 1'. Again, the address must be selected 250ns prior to $\overline{\text{CONVST}}$ going LOW to ensure that the new address is selected for conversion. Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought LOW in order to enable the parallel output bus with the 'n – 2' conversion results of Channel A0. While continuing to hold $\overline{\text{CS}}$ LOW, $\overline{\text{RD}}$ is held LOW for a minimum of 30ns which enables the output bus with the Channel A0 results of conversion 'n – 2'. The $\overline{\text{RD}}$ pin is toggled from HIGH to LOW a second time in order to enable the output bus with the Channel B0 results of conversion 'n – 2'.

SECTION C

$\overline{\text{CONVST}}$ is brought LOW for a third time to initiate conversion 'n' (Channel 0). While the conversion is in process, the results for both conversions 'n – 2' and 'n – 1' can be read. The address pin is brought HIGH while $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought LOW which enables the output bus with the Channel A1 results of conversion 'n – 1'. The $\overline{\text{RD}}$ pin is toggled from HIGH to LOW for a second time in Section C and the 'n – 1' conversion results for Channel B1 appear at the output bus. The address pin (A0) is then brought LOW and the read process repeats itself with the most recent conversion results for Channel 0 (n – 2) appearing at the output bus.

READING DATA

The ADS7862 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when $\overline{\text{CS}}$ (pin 20) and $\overline{\text{RD}}$ (pin 21) are both LOW. The output data should not be read 125ns prior to the falling edge of $\overline{\text{CONVST}}$ and 10ns after the falling edge. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ will tri-state the parallel output. Valid conversion data can be read on pins 5 through 16 (MSB–LSB). Refer to Table I for ideal output codes.

In applications where multiple devices are present on the data bus, care should be taken to ensure that the signal applied to $\overline{\text{RD}}$ (pin 21) is toggled only when the target device is properly chip-selected. Toggling the $\overline{\text{RD}}$ pin will advance the internal read pointer regardless of the state of the chip select, causing the output data to appear channel-swapped. If multiple devices share a single read enable from the host processor, the signal may be ORed with an address-decoded chip select to ensure channel data integrity. For more information, refer to Application Report SBAA138, *Reading Data from the ADS7862*, available for download from the TI website at www.ti.com.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7862 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. This error can change if the external event changes in time with respect to the CLOCK input.

With this in mind, power to the ADS7862 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. On average, the ADS7862 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A bypass capacitor is not necessary when using the internal reference (tie pin 1 directly to pin 2).

The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the 'analog' ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7862Y/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	7862Y	Samples
ADS7862Y/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		7862Y	Samples
ADS7862YB/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		7862Y B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

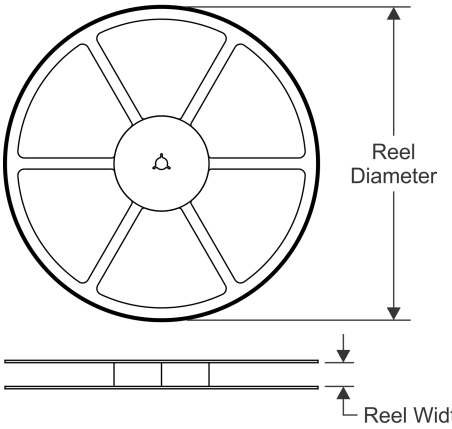
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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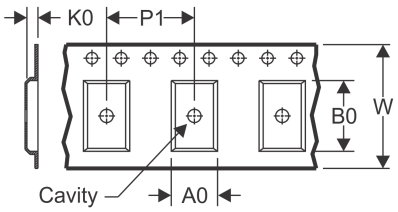
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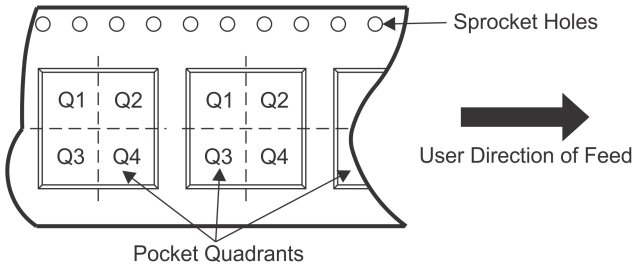


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

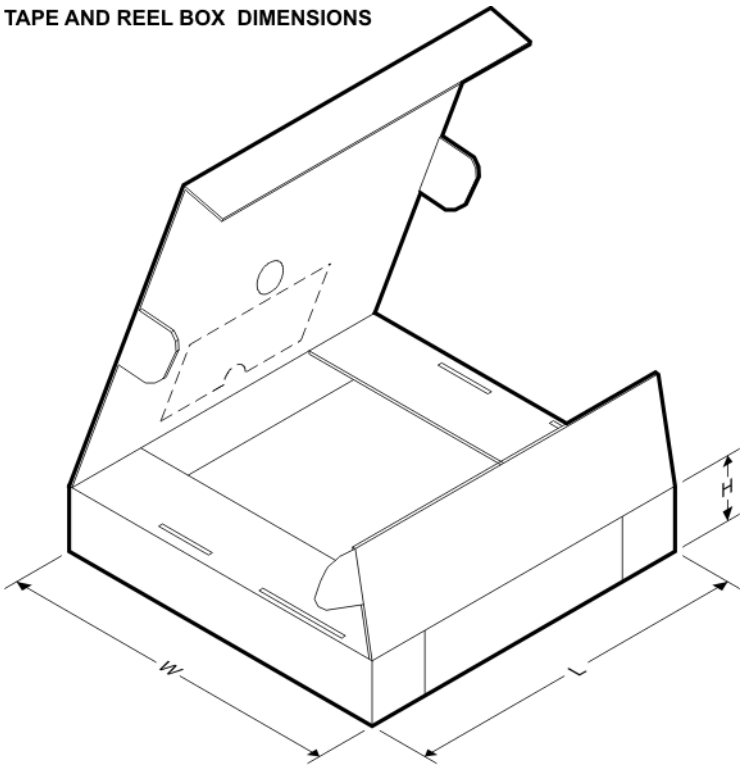
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7862Y/250	TQFP	PBS	32	250	180.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS7862Y/2K	TQFP	PBS	32	2000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS7862YB/250	TQFP	PBS	32	250	180.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

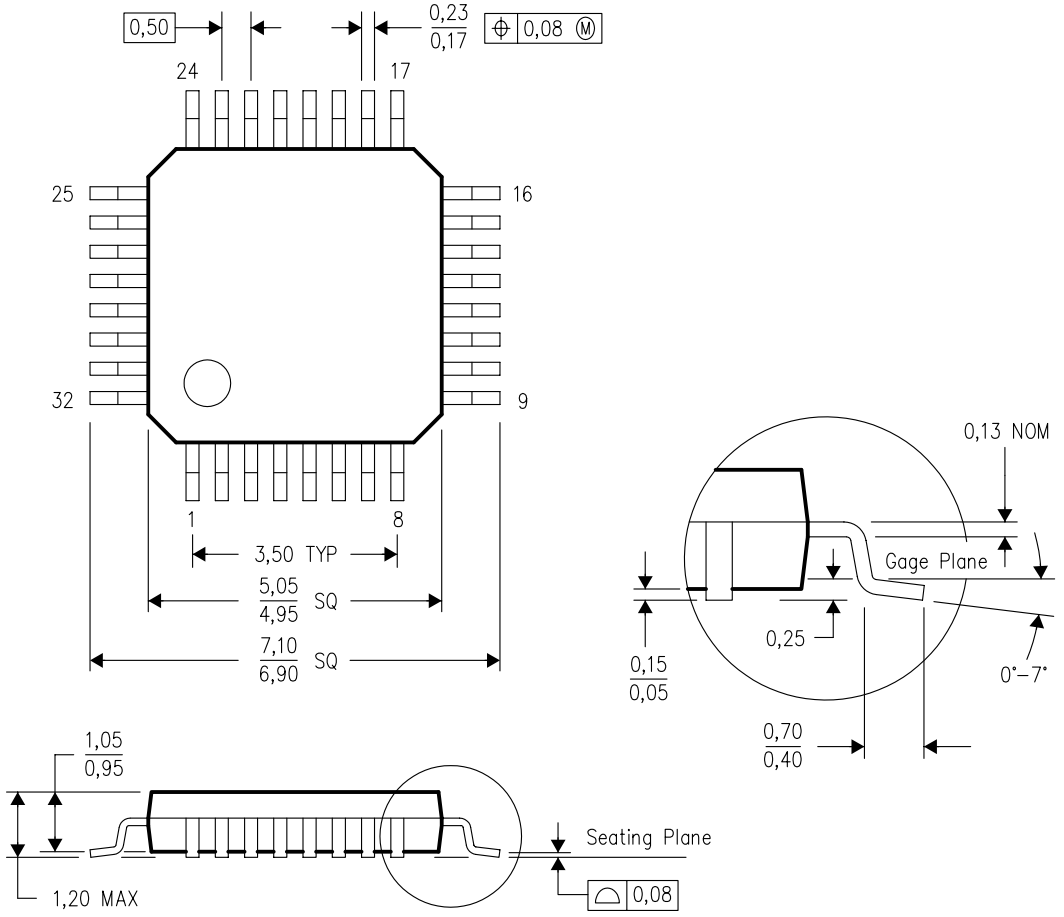
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7862Y/250	TQFP	PBS	32	250	213.0	191.0	55.0
ADS7862Y/2K	TQFP	PBS	32	2000	350.0	350.0	43.0
ADS7862YB/250	TQFP	PBS	32	250	213.0	191.0	55.0

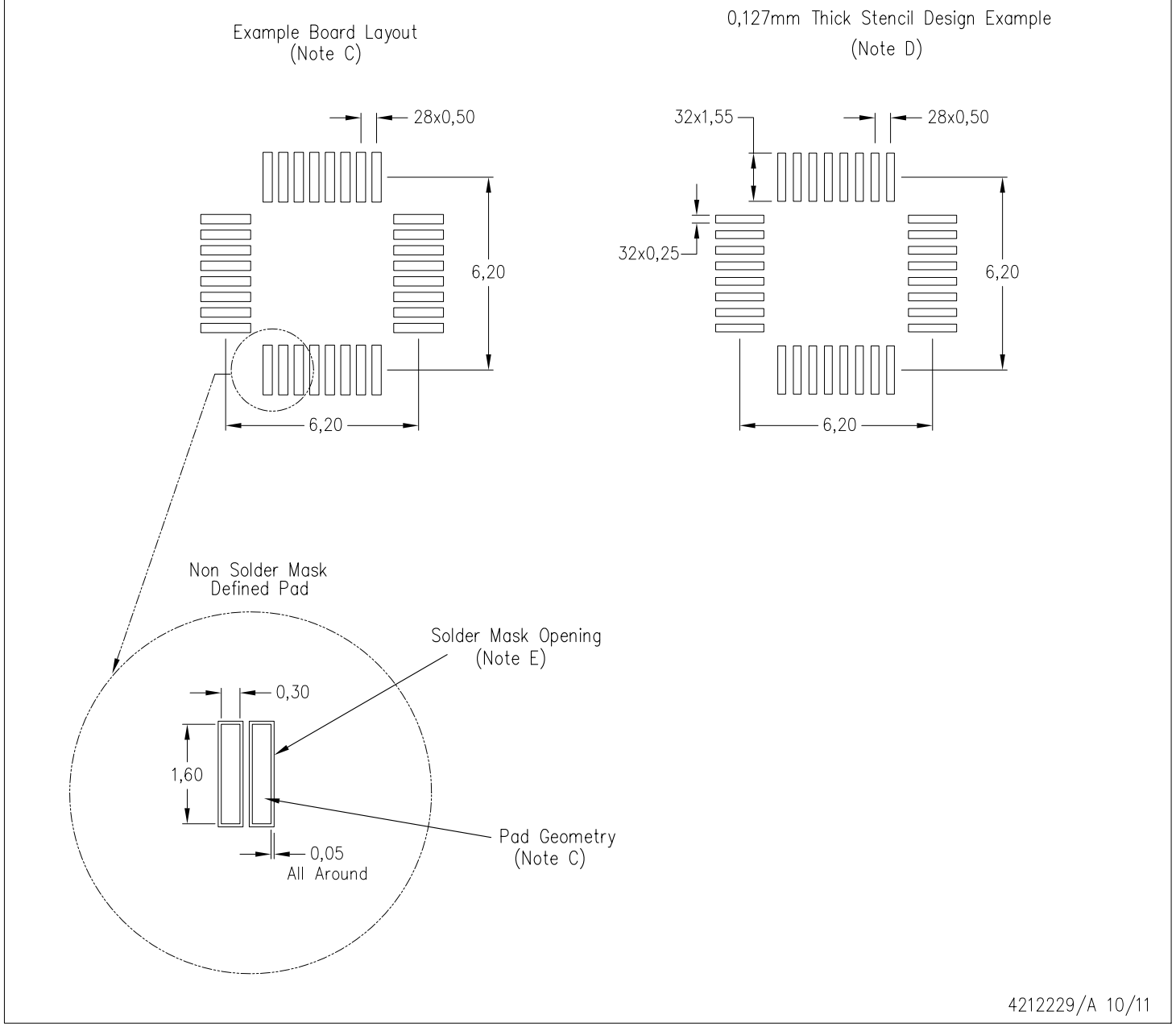
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



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A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
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D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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