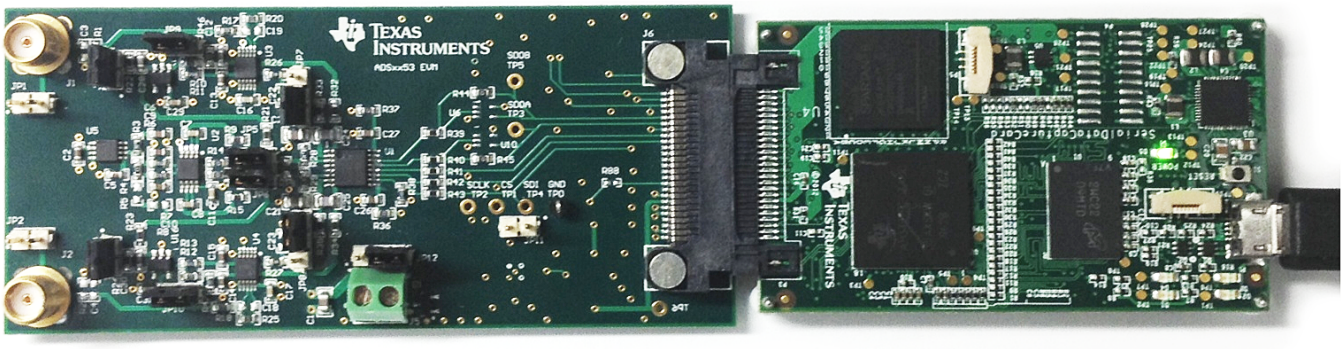
ADS8353EVM-PDK and ADS7853EVM-PDK



ADS8353EVM-PDK and ADS7853EVM-PDK

This user's guide describes the characteristics, operation and use of the ADS8353EVM and ADS7853EVM performance demonstration kits (PDKs). These kits are evaluation platforms for the ADS8353 and ADS7853, dual-channel, 16-bit and 14-bit, simultaneous sampling, successive approximation register (SAR) analog-to-digital converters (ADCs) that support single-ended and pseudo-differential analog inputs. These EVMs ease the evaluation of the ADS8353 and ADS7853 devices with hardware and software for computer connectivity through universal serial bus (USB). This user's guide includes a complete circuit descriptions, schematic diagrams, and bill of materials.

Throughout this document, the terms ADSxx53EVM-PDK, demonstration kit, evaluation board, evaluation module are synonyms with the ADS8353EVM-PDK and ADS7853EVM-PDK.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Related Documentation

Device	Literature Number
ADS8353	SBAS584
ADS7853	SBAS584
REF5025	SBOS410
OPA2350	SBOS099
OPA376	SBOS406
OPA836, OPA2836	SLOS712
TPS3836E18	SLVS292
TPS7A4700	SBVS204
REG71055	SBAS221

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Contents

1 Overview 4
1.1 ADSxx53EVM Features 4
1.2 ADSxx53EVM-PDK Features 4
2 EVM Analog Interface 4
2.1 Analog Input Range Settings 6
2.2 Single-Ended or Pseudo-Differential Input Configuration 6
2.3 Bipolar Input-Signal Configuration 6
2.4 Unipolar Input-Signal Configuration 7
2.5 ADSxx53EVM Onboard Reference and ADSxx53 Device Internal Reference 7
3 Digital Interface 9
3.1 Serial Interface (SPI) 9
3.2 I^2C Bus for Onboard EEPROM 9
4 Power Supplies 10
5 ADSxx53EVM-PDK Initial Setup 11
5.1 Default Jumper Settings 11
5.2 Software Installation 12
6 ADSxx53EVM-PDK Kit Operation 18
6.1 About the Simple Capture Card Controller Board 18
6.2 Loading the ADSxx53EVM-PDK Software 18
6.3 ADSxx53EVM Settings 19
6.4 Device Registers 22
6.5 Capturing Data with the ADSxx53EVM-PDK 22
6.6 FFT Analysis 25
6.7 Histogram Analysis 27
6.8 Troubleshooting 27
7 Bill of Materials, PCB Layout, and Schematics 29
7.1 Bill of Materials 29
7.2 PCB Layout 31
7.3 Schematics 32

List of Figures

1 ADSxx53EVM Analog Interface Input Connections 5
2 Single-Ended or Pseudo-Differential Input Configuration 6
3 Bipolar Input Signal Configuration with $2 \times V_{ref}$ range 7
4 Unipolar Input Signal Configuration 7
5 REF5025 2.5-V External Reference Source and OPA2350 Reference Driver 8
6 ADSxx53EVM Default Jumper Settings 11
7 Bottom View of Simple Capture Card Board with microSD Card Installed 13
8 Bottom View of ADSxx53EVM Rev C with microSD Card Installed 13
9 Connecting the ADSxx53EVM Board to the Simple Capture Card Controller Board 14
10 LED Indicators on a Simple Capture Card Board 14
11 Welcome Screen and Destination Directory Screens 15
12 License Agreement and Start Installation Screens 15
13 Progress Bar and Installation Complete Screens 16
14 Windows 7 Driver Installation Warning 16
15 Simple Capture Card Device Driver Installation 17
16 Simple Capture Card Device Driver Completion 17
17 GUI Display Prompt 18
18 Open the ADSxx53 EVM Settings Page 19
19 Selecting the External Onboard Reference or the ADSxx53 Internal Dual Reference 19
20 Programming the REFDAC Registers in the ADSxx53EVM 20

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21 Selecting 0 to V_{ref} Range or 0 to 2 × V_{ref} Range 20
22 Single-Ended or Pseudo-Differential Jumper Settings Description on the GUI 21
23 Bipolar or Unipolar Signal Jumper Settings Description on the GUI 21
24 Device Registers Page 22
25 Open the *Data Monitor* Page on the GUI 22
26 *Data Monitor* Page 23
27 Saving Data to a Text File 24
28 FFT Performance Analysis Page 25
29 Histogram Analysis 27
30 Open the *GUI Settings* Page 28
31 Set Capture Mode to *SDCC Interface* While Using the EVM Hardware 28
32 ADSxx53EVM PCB: Top Layer 31
33 ADSxx53EVM PCB: Ground Layer 31
34 ADSxx53EVM PCB: Power Layer 32
35 ADSxx53EVM PCB: Bottom Layer 32

List of Tables

1 JP1 - JP2: Analog Interface Connections 5
2 SMA Analog Interface Connections 5
3 Analog Input Range Jumpers 6
4 Connector J6 Pin Out 9
5 Power-Supply Jumpers 10
6 Default Jumper Configuration 11
7 ADSxx53EVM Bill of Materials 29

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1 Overview

The ADSxx53EVM-PDK is a platform for evaluation of the ADSxx53 analog-to-digital converter (ADC). The evaluation kit combines the ADSxx53EVM board with a simple capture card controller board. The simple capture card controller board consists of a TI Sitara embedded microcontroller (AM3352) and a field programmable gate array (FPGA). The simple capture card board provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the simple capture card controller board platform, and the simple capture card board provides the power and digital signals used to communicate with the ADSxx53EVM board. These demonstration kits include the ADSxx53EVM board, the simple capture card controller board, a microSD memory card, and an A-to-micro-B USB cable.

1.1 ADSxx53EVM Features

- Contains support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI™)
- Onboard 5-V analog Supply
- Onboard REF5025 (2.5-V) reference
- Voltage reference buffering with OPA2350
- Onboard OPA2836 (205-MHz BW, 1-mA quiescent current) ADC operational amplifier input drivers

1.2 ADSxx53EVM-PDK Features

- Jumper-selectable (0 to 1 × V_{ref} range or 0 to 2 × V_{ref} range.
- USB port for computer interfacing
- Easy-to-use evaluation software for Windows XP®, Windows 7®, Windows 8® operating systems
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Complete control of board settings

2 EVM Analog Interface

The ADSxx53 is a dual-channel, simultaneous-sampling ADC that supports single-ended and pseudo-differential analog inputs. Each channel of the ADSxx53 uses a OPA2836 dual operational amplifier to drive the inputs of the ADC. The positive input terminals of each ADC are driven by the OPA836 operational amplifier configured in the inverting configuration. The negative input terminals of each ADC are driven by the OPA836 in the buffer configuration. The ADSxx53EVM is designed for easy interfacing to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, header connectors JP1 and JP2 provide a convenient way to connect input signals. Figure 1 illustrates the ADSxx53EVM analog interface input connections.

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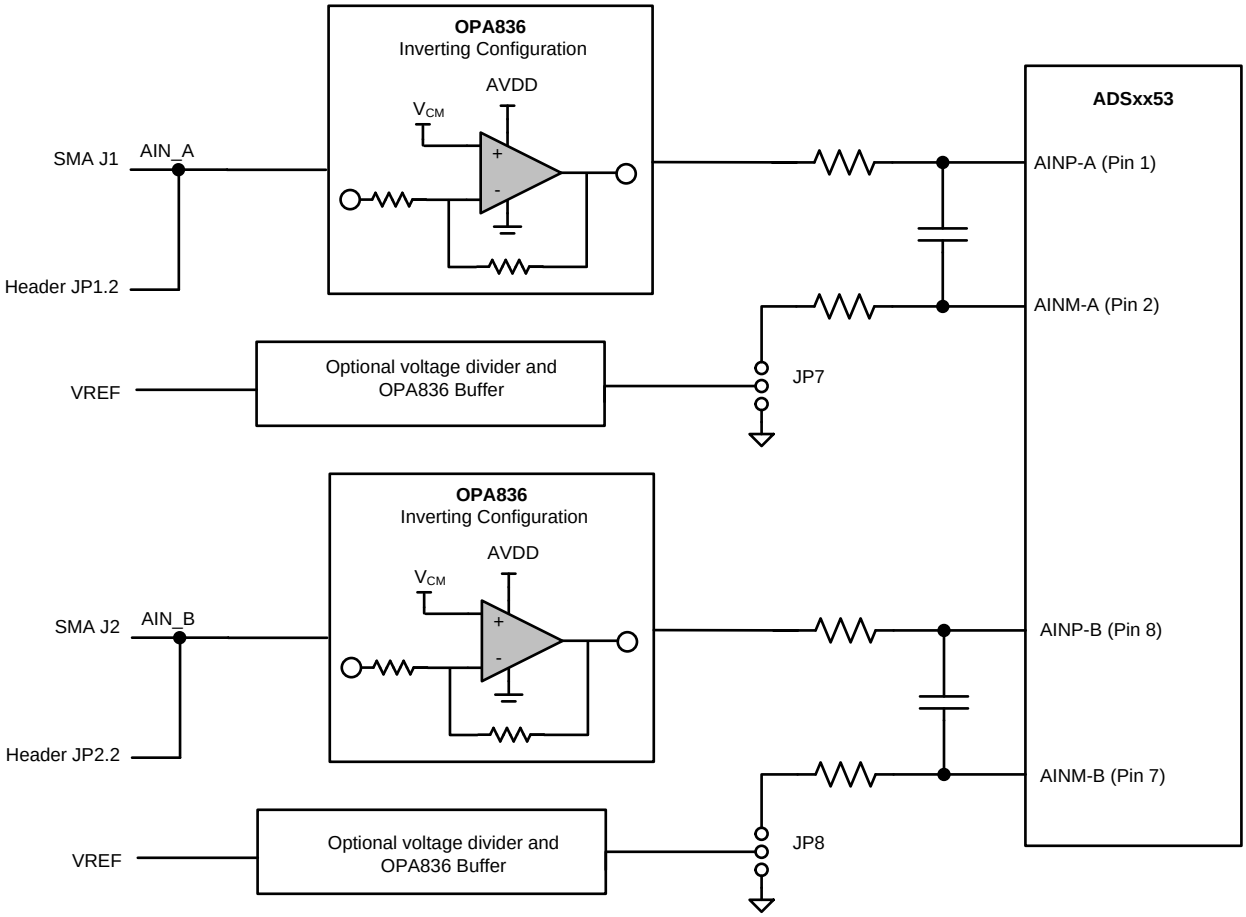


Figure 1. ADSxx53EVM Analog Interface Input Connections

Table 1 summarizes the JP1 and JP2 analog interface connections.

Table 1. JP1 - JP2: Analog Interface Connections

Pin Number	Signal	Description
JP1.2	AIN_A	CHA inverted input. The signal is routed through an OPA836 in the inverting configuration.
JP2.2	AIN_B	CHB inverted input. The signal is routed through an OPA836 in the inverting configuration.

Table 2 lists the SMA analog inputs.

Table 2. SMA Analog Interface Connections

Pin Number	Signal	Description
J1	AIN_A	Channel A inverted input. The signal is routed through an OPA836 in the inverting configuration
J2	AIN_B	Channel B inverted input. The signal is routed through an OPA836 in the inverting configuration.

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2.1 Analog Input Range Settings

The full-scale range (FSR) of the ADSxx53 device can be programmed to either from (0 to 1 × V_{ref}) or (0 to 2 × V_{ref}) range by setting bit B9 of the ADSxx53 configuration register. This register is common to both ADCs in the device (ADC_A and ADC_B). Configure the full-scale range setting in the EVM by navigating to the *ADSxx53EVM Settings* page on the grpahical user interface (GUI); see section Section 6.3 for more information. Install jumpers JP3 and JP4 when supporting the 0 to 1 × V_{ref} range, and remove jumpers JP3 and JP4 when supporting the 0 to 2 x V_{ref} range, as shown in Table 3.

Table 3. Analog Input Range Jumpers

Jumper Number	Default Position	Description
JP3	Installed	Install for FSR = 0 to 1 × V_{ref}; remove for FSR = 0 to 2 × V_{ref}.
JP4	Installed	Install for FSR = 0 to 1 × V_{ref}; remove for FSR = 0 to 2 × V_{ref}.

2.2 Single-Ended or Pseudo-Differential Input Configuration

The ADSxx53 dual, simultaneous ADC supports single-ended or pseudo-differential analog input signals. To support single-ended inputs, set bit B7 in the configuration (CFR) register to 0 (CFR.B7 = 0), and connect ADC inputs AINM_A and AINM_B to GND. These devices can also be programmed to support pseudo-differential inputs by setting bit B7 in the CFR register to 1 (CFR.B7 = 1). In this configuration, AINM_A is connected to FSR_ADC_A / 2, and AINM_B is connected to FSR_ADC_B / 2. Note that bit CFR.B7 is common to both ADCs. By configuring jumpers JP7 and JP8 on the ADSxx53EVM, the negative inputs of the ADC can be connected to GND to support the single-ended configuration, or connected to FSR/2 when programmed to support pseudo-differential inputs, as shown in Figure 2. See Section 6.3 for more information.

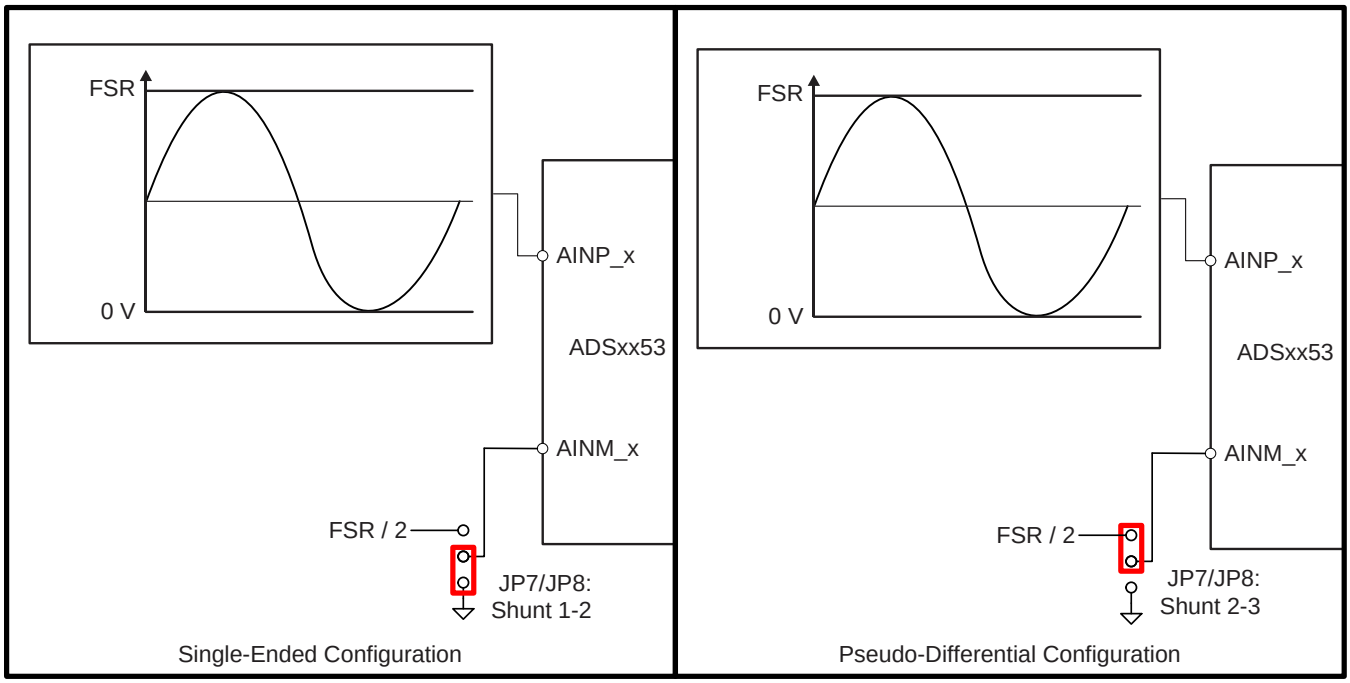


Figure 2. Single-Ended or Pseudo-Differential Input Configuration

2.3 Bipolar Input-Signal Configuration

The ADSxx53EVM-PDK supports both bipolar or unipolar input signals on the J1 (JP1.2) and J2 (JP2.2) analog interface connectors. When jumpers JP9 and JP10 are closed, the inverting amplifier (OPA836) is biased at the appropiate common-mode voltage level to support bipolar signals on the analog interface connectors. In this configuration, apply a bipolar input signal with 0-V common-mode voltage.

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Figure 3 shows an example where the ADSxx53EVM is configured to support a bipolar input signal with 2 × V_{ref} range at the J1 (JP1.2) and J2 (JP2.2) analog interface connectors.

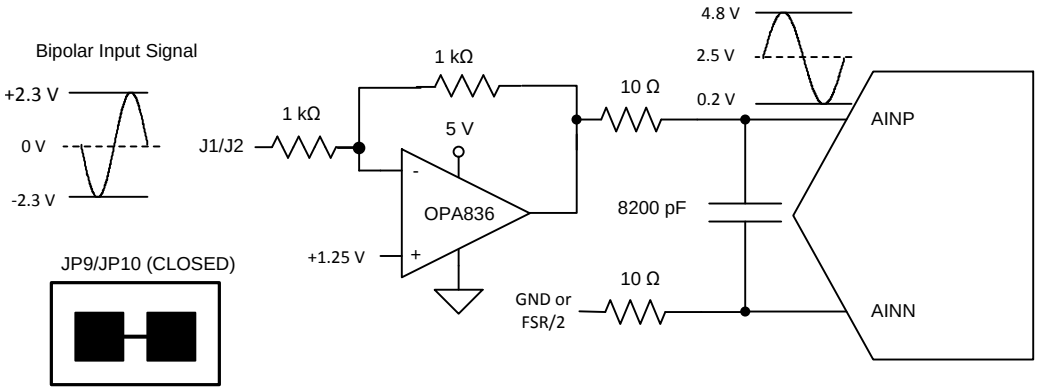


Figure 3. Bipolar Input Signal Configuration with 2 × V_{ref} range

2.4 Unipolar Input-Signal Configuration

When jumpers JP9 and JP10 are open, the inverting amplifier (OPA836) is biased at the appropiate common-mode voltage level to support unipolar signals on the analog interface connectors. In this configuration, apply a unipolar input signal with FSR / 2 common-mode voltage. Figure 4 shows an example where the ADSxx53EVM is configured to support a unipolar input signal with 2 × V_{ref} range at the J1 (JP1.2) and J2 (JP2.2) analog interface connectors.

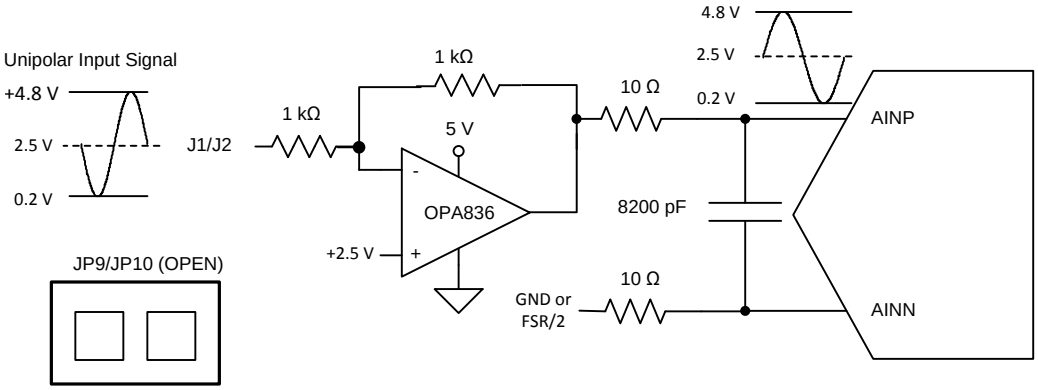


Figure 4. Unipolar Input Signal Configuration

2.5 ADSxx53EVM Onboard Reference and ADSxx53 Device Internal Reference

The ADSxx53 dual, simultaneous ADC operates with reference voltages VREF_A and VREF_B present on pins REFIO_A and REFIO_B, respectively. The ADSxx53 device incorporates two internal individually-programmable 2.5-V reference sources. Alternatively, the onboard 2.5-V reference, REF5025 (U5), can also be selected. The reference voltage source is determined by setting bit B6 of the ADC configuration register. Note that this bit is common to ADC_A and ADC_B. Configure the reference settings on the ADSxx53EVM-PDK by navigating to the *ADSxx53EVM Settings* page on the GUI; see Section 6.3 for more information. By default, the evaluation module is set up with the onboard external reference source, with jumpers JP5 and JP6 installed, as shown in Figure 5. If the ADSxx53 must be configured with the internal reference, make sure to remove jumpers JP5 and JP6 before enabling the internal reference.

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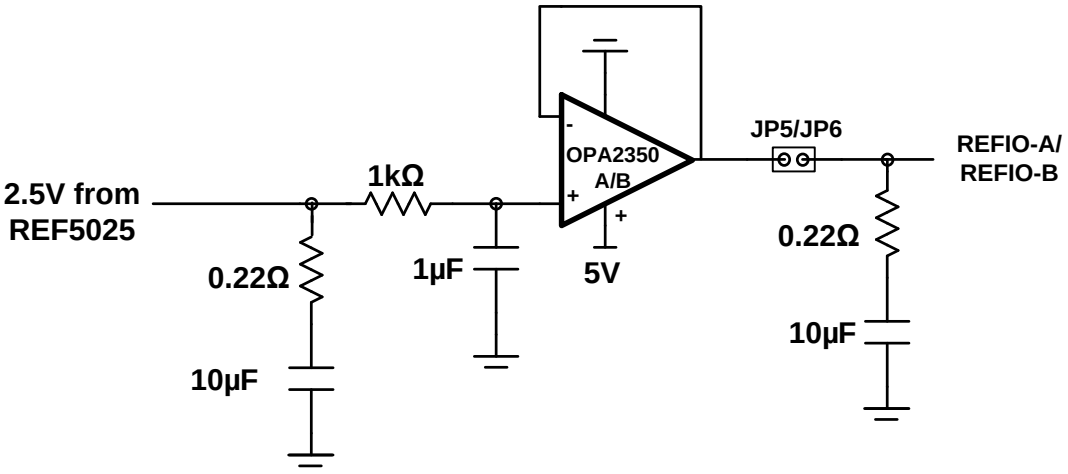


Figure 5. REF5025 2.5-V External Reference Source and OPA2350 Reference Driver

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3 Digital Interface

Socket strip connector J6 provides the digital I/O connections between the ADSxx53EVM board and the simple capture card board.

Table 4 summarizes the pin-outs for connector J6.

Table 4. Connector J6 Pin Out

Pin Number	Signal	Description
J6.2, J6.10, J6.15, J6.16, J6.18	GND	Ground connections
J6.4	$\overline{\text{EVM PRESENT}}$	EVM present signal, active low
J6.11, J6.12	I²C™ bus	I²C bus; used only used to program the U7 EEPROM on the EVM board
J6.13	DVDD	3.3V digital supply from the simple capture card controller board
J6.34	$\overline{\text{CS}}$	Chip select, active low
J6.36	SCLK	Serial interface clock
J6.38	SDI	Serial data input
J6.40	SDO_A	Serial data output for channel A
J6.42	SDO_B	Serial data output for channel B

3.1 Serial Interface (SPI)

The ADSxx53 digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs), and FPGAs easy. The ADSxx53EVM offers 47-Ω resistors between the SPI signals and connector J6 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.2 I²C Bus for Onboard EEPROM

The ADSxx53EVM has an I²C bus to communicate with the onboard EEPROM that records the board name and assembly date. It is not used in any form by the ADSxx53 converter.

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4 Power Supplies

The analog portion of the ADSxx53EVM-PDK requires a 5-V supply. The ADSxx53EVM-PDK is configured at the factory using the onboard regulated analog 5-V supply (+VA); and an onboard 3.3-V digital supply. Alternatively, set the AVDD analog supply voltage by connecting an external power source through two-terminal connector (J5). Table 5 lists the configuration details for P3.

Table 5. Power-Supply Jumpers

Pin Number	Pin Name	Function
JP12	Shunt 2-3 (default)	Onboard 5-V AVDD analog supply selected
	Shunt 1-2	External 5-V AVDD connected through two-terminal block J5
JP11	Open	Onboard regulated AVDD supply set to 5.0 V
	Closed	Onboard regulated AVDD supply set to 5.2 V

CAUTION

The external AVDD supply applied to external two-terminal connector J5 must not exceed 5.5 V or device damage may occur. The external AVDD supply must be in the range of 5.0 V to 5.5 V for proper ADSxx53EVM operation.

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5 ADSxx53EVM-PDK Initial Setup

This section presents the steps required to set up the ADSxx53EVM-PDK kit before operation.

5.1 Default Jumper Settings

Figure 6 shows the silkscreen plot detailing the default jumper settings. Table 6 descibes the configuration for these jumpers.

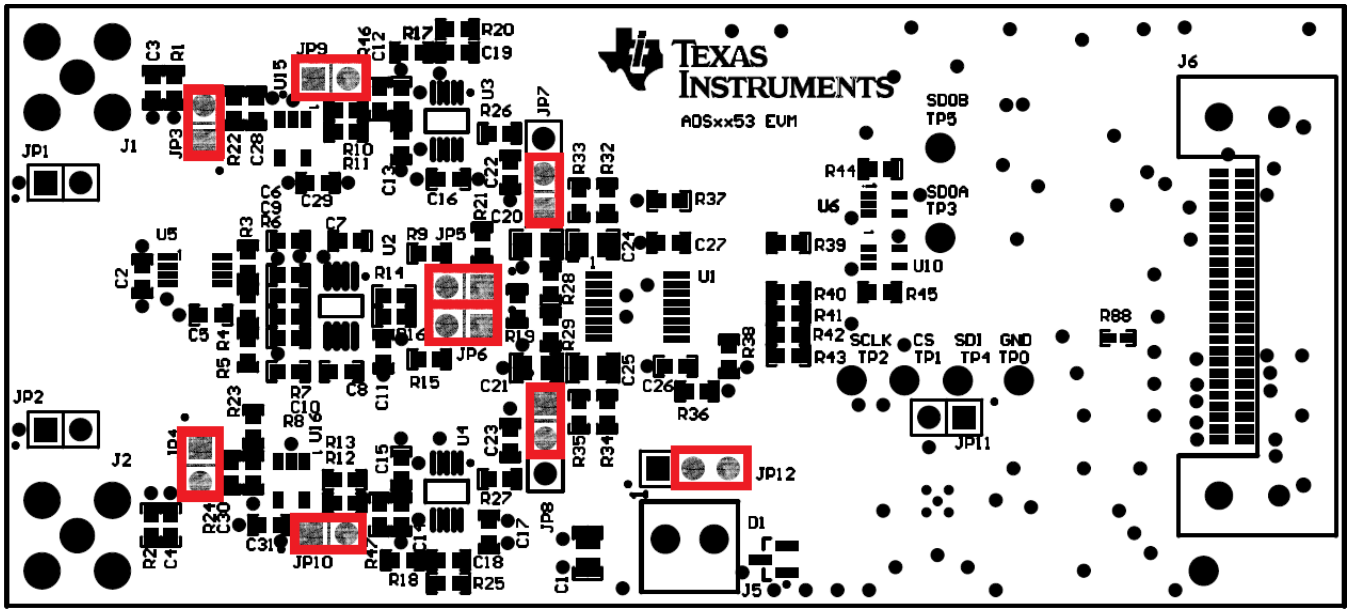


Figure 6. ADSxx53EVM Default Jumper Settings

Table 6. Default Jumper Configuration

Pin Number	Default Position	Switch Description
JP1	Open	JP1.2 Header connector to inverted AINP-A input
JP2	Open	JP2.2 Header connector to inverted AINP-B input
JP3	Closed	Closed when configured in 0 to 1 × V_{ref} range; open to support 0 to 2 × V_{ref} range
JP4	Closed	Closed when configured in 0 to 1 × V_{ref} range; open to support 0 to 2 × V_{ref} range
JP5	Closed	Closed to connect onboard 2.5-V reference to REFIO_A; open when using ADSxx53 internal reference.
JP6	Closed	Closed to connect onboard 2.5-V reference to REFIO_B; open when using ADSxx53 internal reference.
JP7	Shunt 1-2	Shunt 1-2 connects AINM-A(–) to GND; shunt 2-3 connects AINM-A(–) to FSR / 2.
JP8	Shunt 1-2	Shunt 1-2 connects AINM-B(–) to GND; shunt 2-3 connects AINM-B(–) to FSR / 2 .
JP9	Closed	Open for channel A unipolar input signals at SMA connector; installed for channel A bipolar input signals at SMA connector
JP10	Closed	Open for channel B unipolar input signals at SMA connector; installed for channel B bipolar input signals at SMA connector
JP11	Open	Open: onboard AVDD set to +5 V; closed: onboard AVDD set to +5.2 V
JP12	Shunt 2-3	Shunt 2-3 selects onboard regulated AVDD supply; shunt 1-2 selects external AVDD through J5

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5.2 Software Installation

This section presents the steps required to the install the software. Section 6 explains how to operate the software to acquire data.

NOTE: The ADSxx53EVM-PDK with **ADSxx53 PWB Board revision A** includes (1) microSD card. Ensure the microSD memory card included in the kit is installed in the microSD socket on the back of the simple capture card board before connecting the EVM to the PC. Otherwise, as a result of improper boot up, Windows cannot recognize the ADSxx53EVM-PDK as a connected device.

The ADSxx53EVM-PDK with **ADSxx53 PWB Board revision C** includes (2) microSD cards. Ensure both microSD memory cards that contain the software are installed in the microSD sockets on the back of the simple capture card board and on the back of ADSxx53EVM board respectively. Otherwise, as a result of improper boot up, Windows cannot recognize the ADSxx53EVM-PDK as a connected device.

Complete the following steps to install the software:

Step 1. Verify the microSD memory card(s) are installed:
- ADSxx53EVM PWB revision A: This PDK kit version includes (1) microSD Card. Verify the microSD memory card is installed on the simple capture card controller board.
- ADSxx53EVM PWB revision C: This PDK kit version includes (2) microSD Cards. Ensure both microSD memory cards are installed in the microSD sockets on the back of the simple capture card board and ADSxx53EVM board respectively.

Step 2. Verify jumpers are in the factory-default position and connect the hardware

Step 3. Install the ADSxx53EVM-PDK software.

Step 4. Complete the simple capture card device driver installation.

Each task is described in the following subsections.

5.2.1 Verify the microSD Memory Card is Installed on the Simple Capture Card Controller Board

The ADSxx53EVM-PDK includes the micro SD card(s) that contain the EVM software and simple capture card controller board firmware required for the EVM operation.

NOTE: Ensure the microSD memory card is installed in the microSD socket (P6) on the back of the simple capture card board.

Figure 7 illustrates the bottom view of the simple capture card controller board with the microSD card installed.

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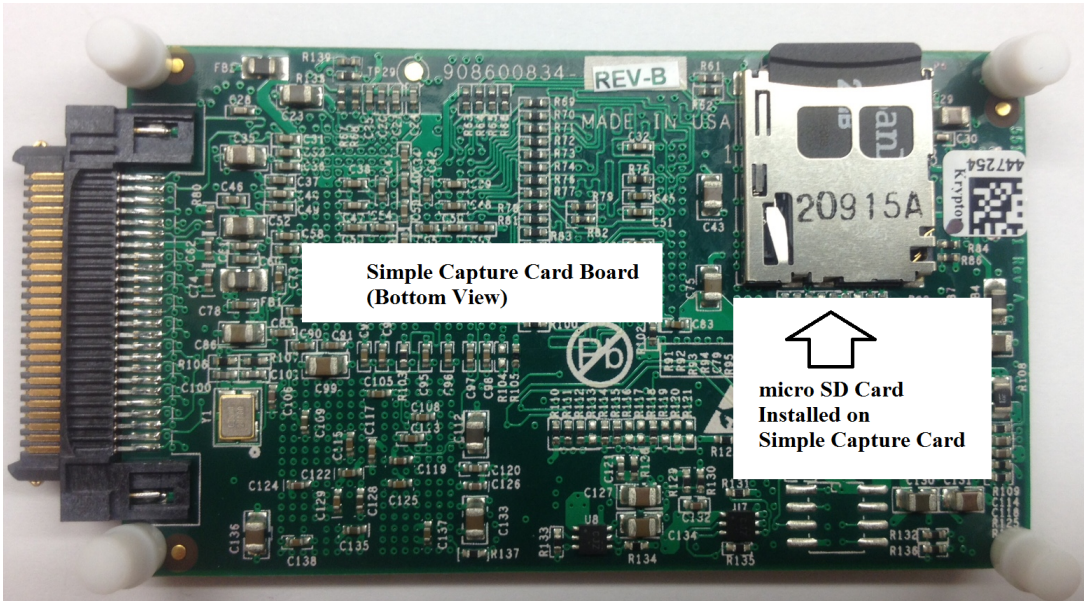


Figure 7. Bottom View of Simple Capture Card Board with microSD Card Installed

NOTE: **ADSxx53EVM-PDK with ADSxx53EVM PWB Board revision C (only):** This ADSxx53EVM PWB version includes (2) microSD cards. Ensure both microSD memory cards are installed in the microSD sockets on the back of the simple capture card board and on the back of ADSxx53EVM, as shown on Figure 7 and Figure 8 respectively.

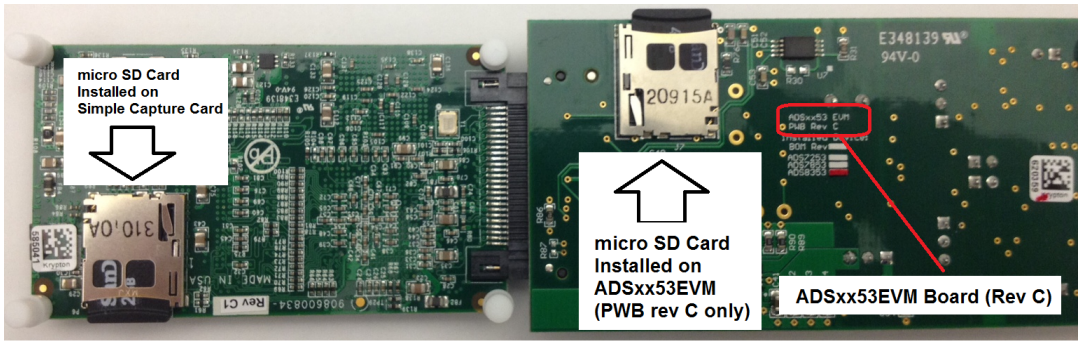


Figure 8. Bottom View of ADSxx53EVM Rev C with microSD Card Installed

The microSD card(s) is formatted from the factory with the necessary firmware files for the simple capture card controller board to boot properly. In addition to the simple capture card firmware files ('app' and 'MLO' files), the microSD card(s) contain the ADSxx53EVM-PDK software installation files inside the *ADS835x EVM V#.#.#* folder. *<V#.#.#>* refers to the installation software version number, and increments with software installer releases.

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5.2.2 Verify Jumpers are in the Factory-Default Position and Connect the Hardware

The ADSxx53EVM-PDK includes both the ADSxx53EVM and the simple capture card controller board; however, the devices are shipped unconnected. Follow these steps to verify that ADSxx53EVM-PDK kit is configured and connected properly.

Step 1. Verify the microSD card is installed on the back of the simple capture card board; see Figure 7.

Step 2. Verify the ADSxx53EVM jumpers are configured; see Figure 6.

Step 3. Connect the ADSxx53EVM board to the simple capture card controller board as Figure 9 shows.

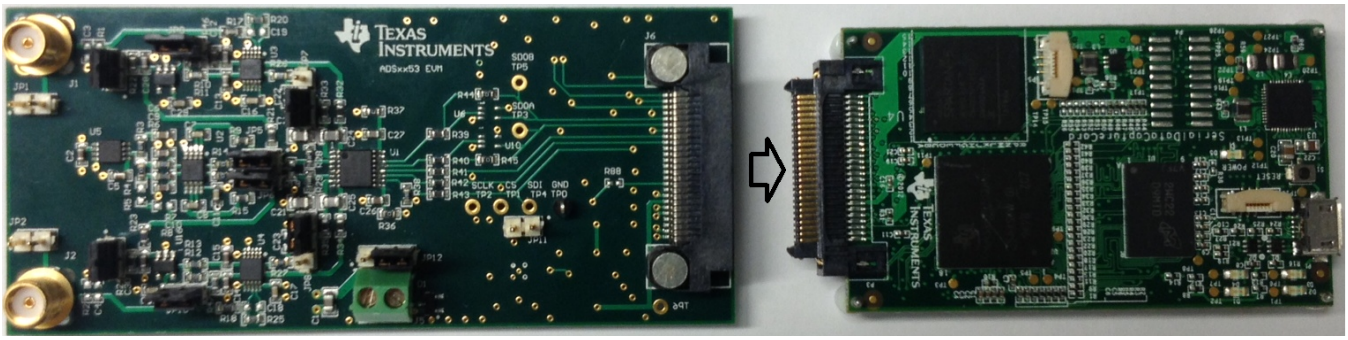


Figure 9. Connecting the ADSxx53EVM Board to the Simple Capture Card Controller Board

Step 4. Connect the simple capture card controller board to the PC through the micro USB cable.

Step 5. Verify that LED D5 *Power Good* indicator is illuminated. Wait approximately ten seconds and verify that diode D2 blinks, indicating that USB communication with the host PC is functioning properly. Figure 10 shows the location of the LED indicators in the simple capture card controller board.

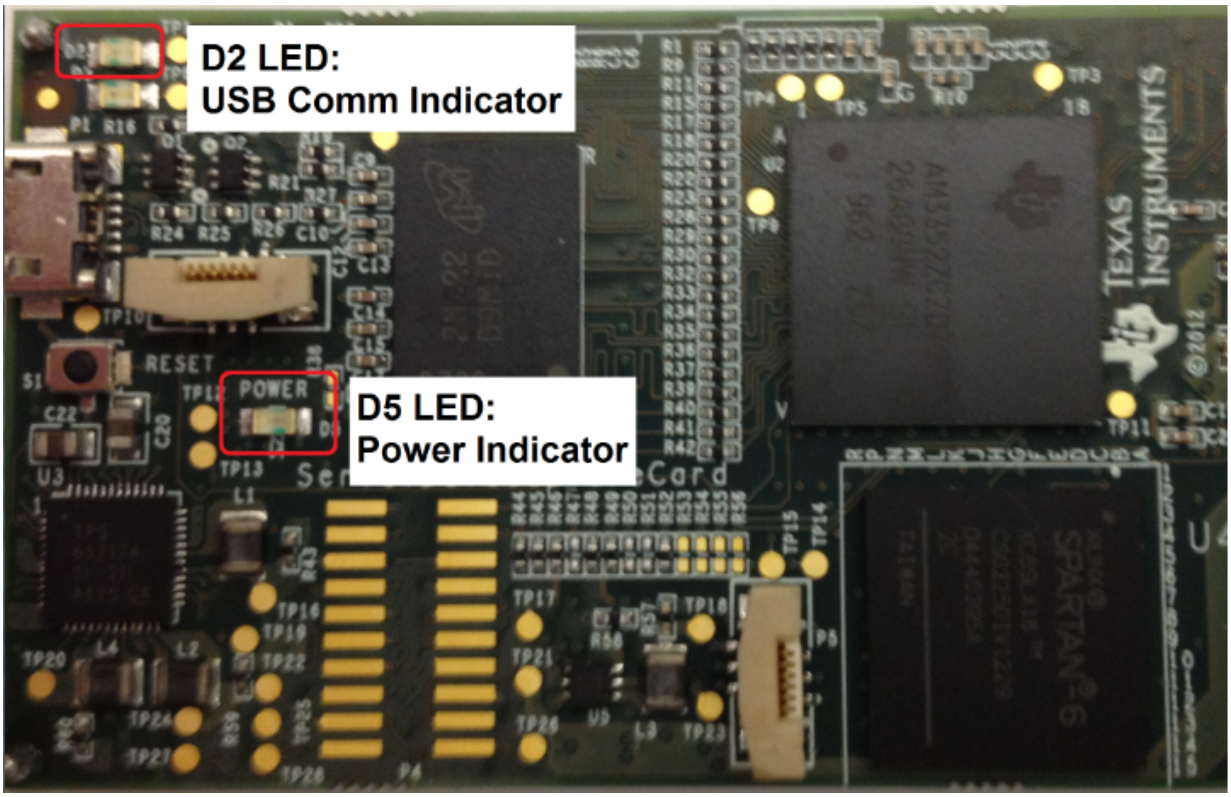


Figure 10. LED Indicators on a Simple Capture Card Board

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5.2.3 Install the ADSxx53EVM-PDK software

The *ADS835x EVM V#.#.#* software needs to be installed on the PC. This software supports the ADSxx53EVM-PDK. The user must have Administrator privileges on the PC to be able to install the EVM software. The following steps list the directions to install the software.

1. Open Windows explorer and find the microSD memory card in the browser as a storage device.
2. Navigate to the *...\ADS835x EVM Vx.x.x\Volume* folder.
3. Run the installer by right-clicking the *setup.exe* and selecting *Run as Administrator*. This action installs the EVM GUI software and the required simple capture card device driver components.
4. After the installer begins, a welcome screen displays. Click *Next* to continue.
5. A prompt appears with the destination directory; select the default directory under: *...\Program Files(x86)\Texas Instruments\ads835xevm*, as shown in Figure 11.

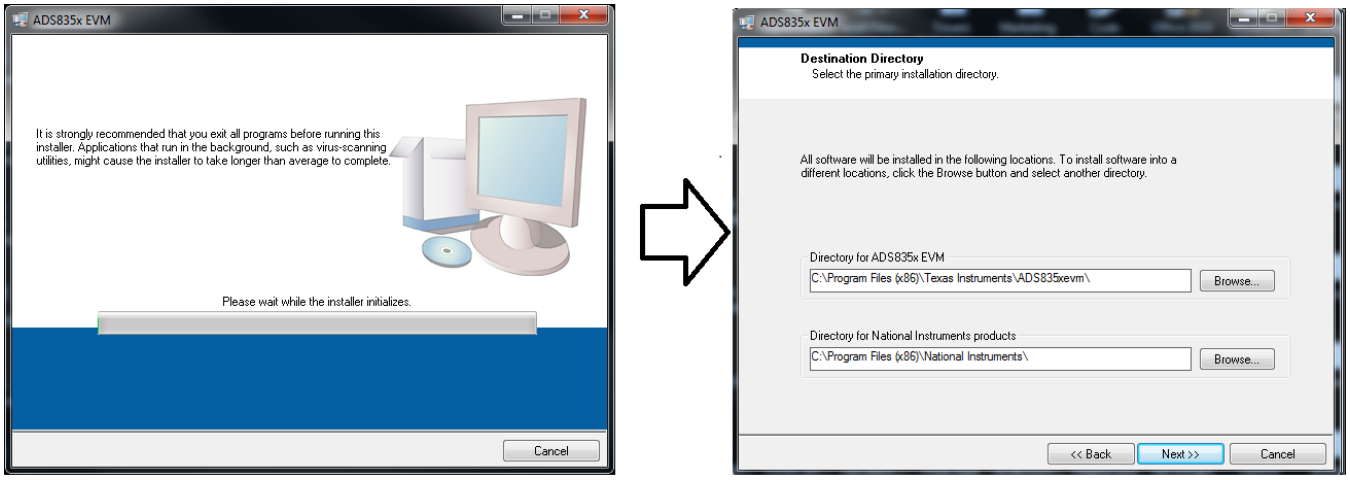


Figure 11. Welcome Screen and Destination Directory Screens

6. One or more software license agreements appear. Select *I Accept the License Agreement* and click *Next*.
7. The *Start Installation* screen appears. Click *Next*, as shown in Figure 12.

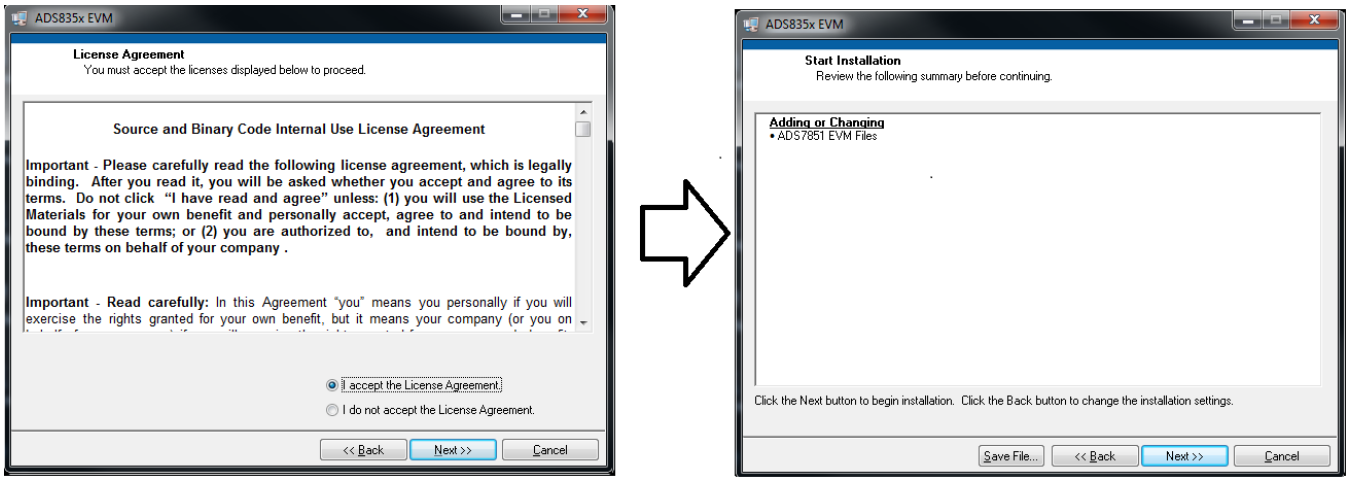


Figure 12. License Agreement and Start Installation Screens

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8. A progress bar appears; this step takes a few minutes.
9. The progress bar is followed by an installation complete notice, as shown in Figure 13.

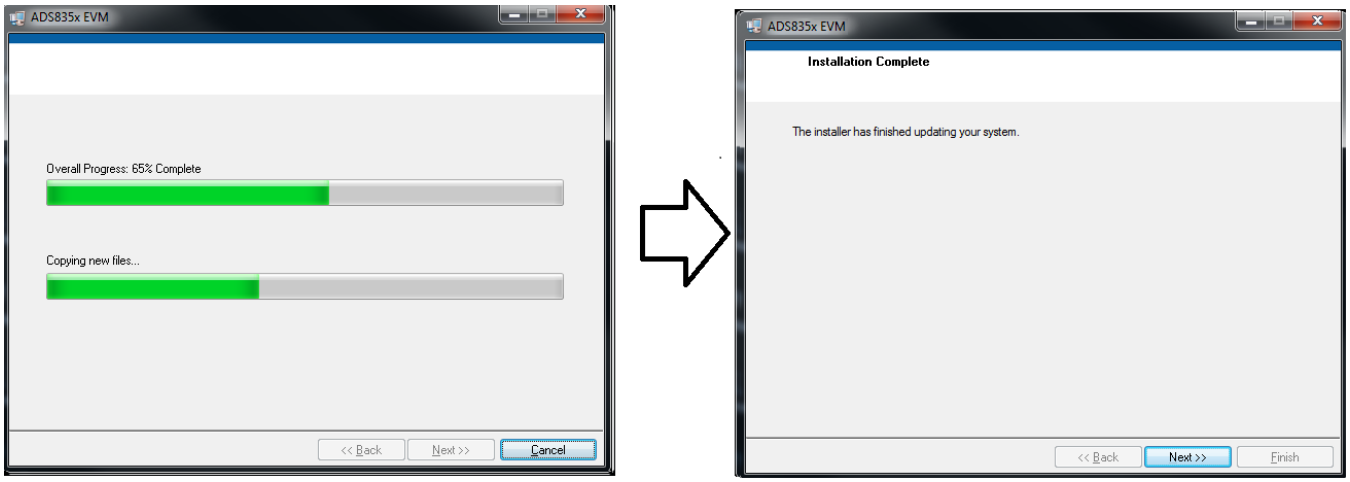


Figure 13. Progress Bar and Installation Complete Screens

5.2.4 Simple Capture Card Device Driver Installation

During installation of the simple capture card device driver, a prompt may appear with the Windows security message shown in Figure 14. Select *Install this driver software anyway* to install the driver required for proper operation of the software. The drivers contained within the installers are safe for installation to your system.

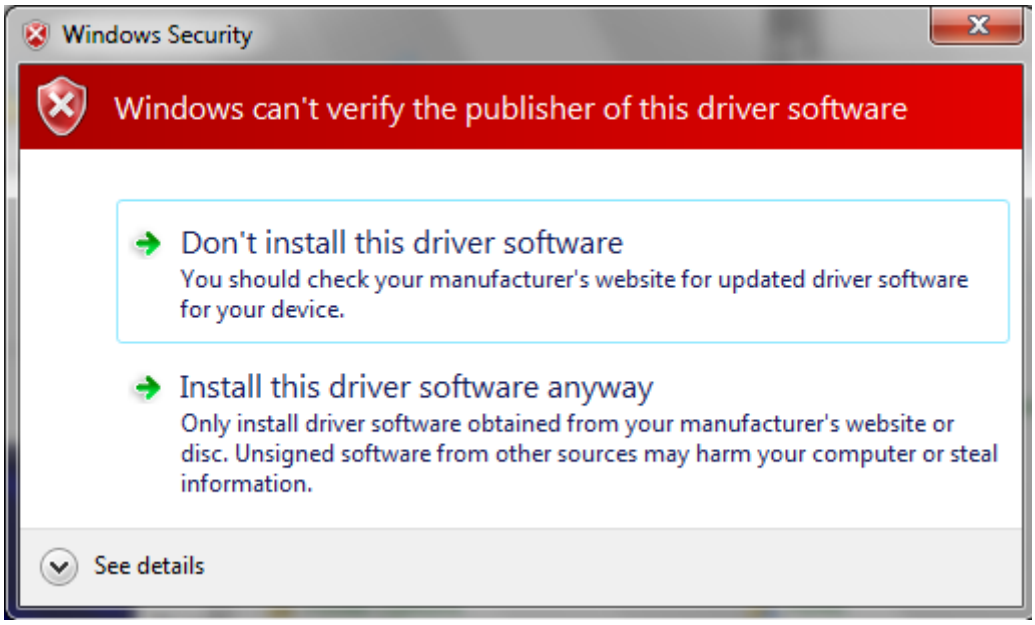


Figure 14. Windows 7 Driver Installation Warning

NOTE: Driver installation prompts do not appear if the simple capture card device driver has been installed on your system previously.

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Follow these procedures to install the simple capture card device driver, if prompted.

Step 1. Immediately after the ADS835x EVM software installation is complete, prompts appear to install the simple capture card device driver, as shown in Figure 15 and Figure 16

Step 2. A computer restart may be required to finish the software installation. If prompted, restart the PC to complete the installation.

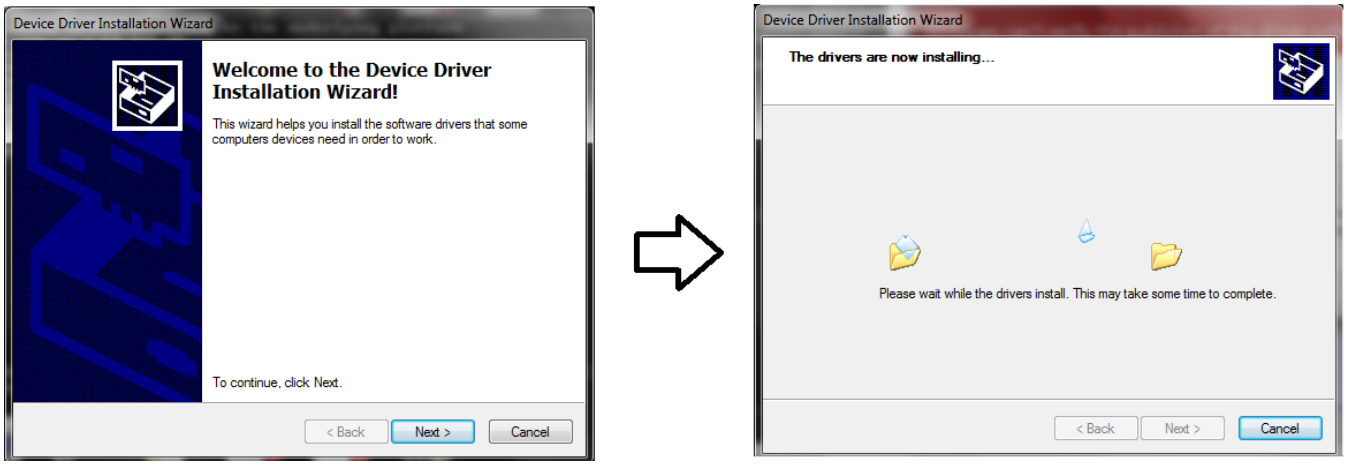


Figure 15. Simple Capture Card Device Driver Installation



Figure 16. Simple Capture Card Device Driver Completion

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6 ADSxx53EVM-PDK Kit Operation

This section describes how to use ADSxx53EVM-PDK and the ADSxx53EVM software to configure the EVM and acquire data.

6.1 About the Simple Capture Card Controller Board

The simple capture card controller board provides the USB interface between the PC and the ADSxx53EVM. The controller board is designed around the AM335x processor, a USB 2.0 high-speed capability, 32-bit ARM core. The simple capture card controller board incorporates an onboard FPGA subsystem and 256 MB of onboard DDR SRAM memory.

The simple capture card controller board is not sold as a development board, and it is not available separately. TI cannot offer support for the simple capture card controller board except as part of this EVM kit.

6.2 Loading the ADSxx53EVM-PDK Software

The ADS835x EVM software (this software also supports the ADSxx53EVM-PDK) provides control over the settings of the ADSxx53. Adjust the ADSxx53EVM settings when the EVM is not acquiring data. During acquisition, all controls are disabled and settings cannot be changed.

Settings on the ADSxx53EVM correspond to settings described in the ADSxx53 product data sheet (available for download at http://www.ti.com); see the product data sheet for details.

To load the *ADS835x EVM* software, follow these steps:

Step 1. Make sure the EVM kit is configured and powered up as explained in Section 5.2.2 and Figure 6.

Step 2. Start the *ADS835x EVM* software. Go to *Start → All Programs →Texas Instruments → ADS835x EVM* and click *ADS835x EVM* to load the software.

Step 3. Verify that the software detects the ADSxx53EVM. The GUI identifies the EVM hardware that is connected to the controller board and displays either *Loading the ADSxx53evm Settings* or *Loading the ADS7854evm Settings*. After the settings are loaded, *ADSxx53EVM GUI* or *ADS7854 EVM GUI* displays at the top of the GUI screen, as shown in Figure 17.

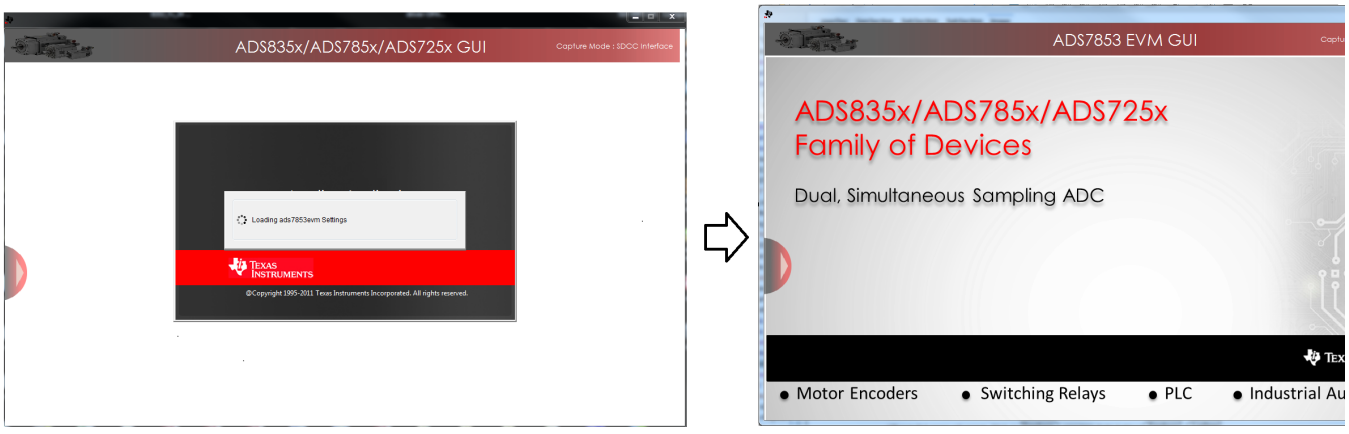


Figure 17. GUI Display Prompt

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6.3 ADSxx53EVM Settings

Configure the ADSxx53EVM with different settings for evaluation. In order to configure the device settings, follow these steps:

1. Load the ADSxx53 EVM settings page in the GUI. Hover the cursor over the red arrow at the left-center side of the GUI screen; a menu with different GUI pages appears. Click on *ADSxx53 EVM Settings*, as shown in Figure 18.

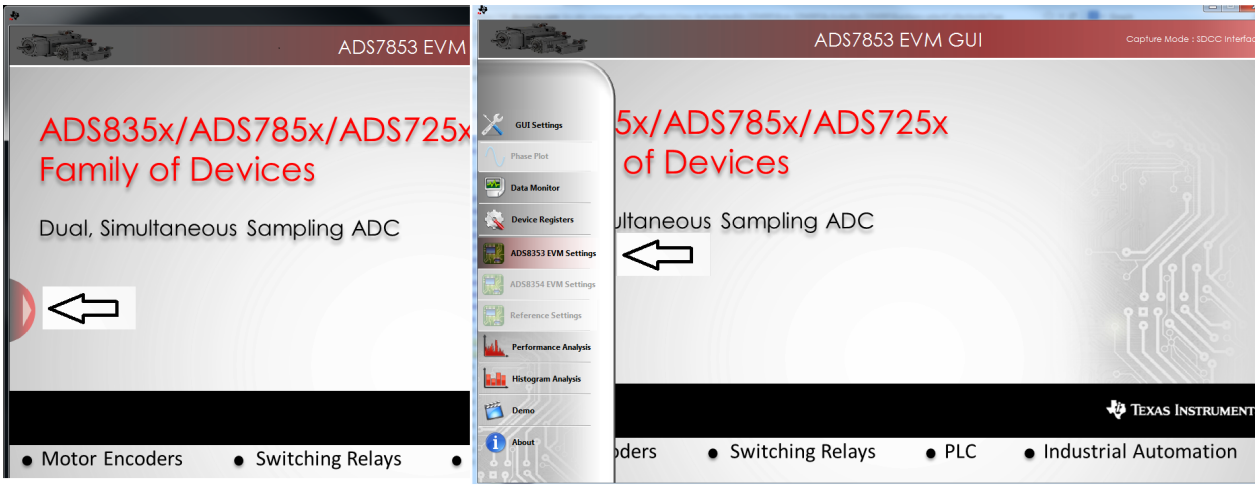


Figure 18. Open the ADSxx53 EVM Settings Page

2. On the *ADSxx53 EVM Settings* page, find the *Internal Reference [CFR, Bit[6]]* button to select the internal or external onboard reference sources. Jumpers JP5 and JP6 must be installed when selecting the external REF5025 (U5) onboard reference. Make sure to uninstall jumpers JP5 and JP6 when selecting the ADSxx53 device internal reference. The GUI displays the appropriate reference jumper settings, as shown in Figure 19.

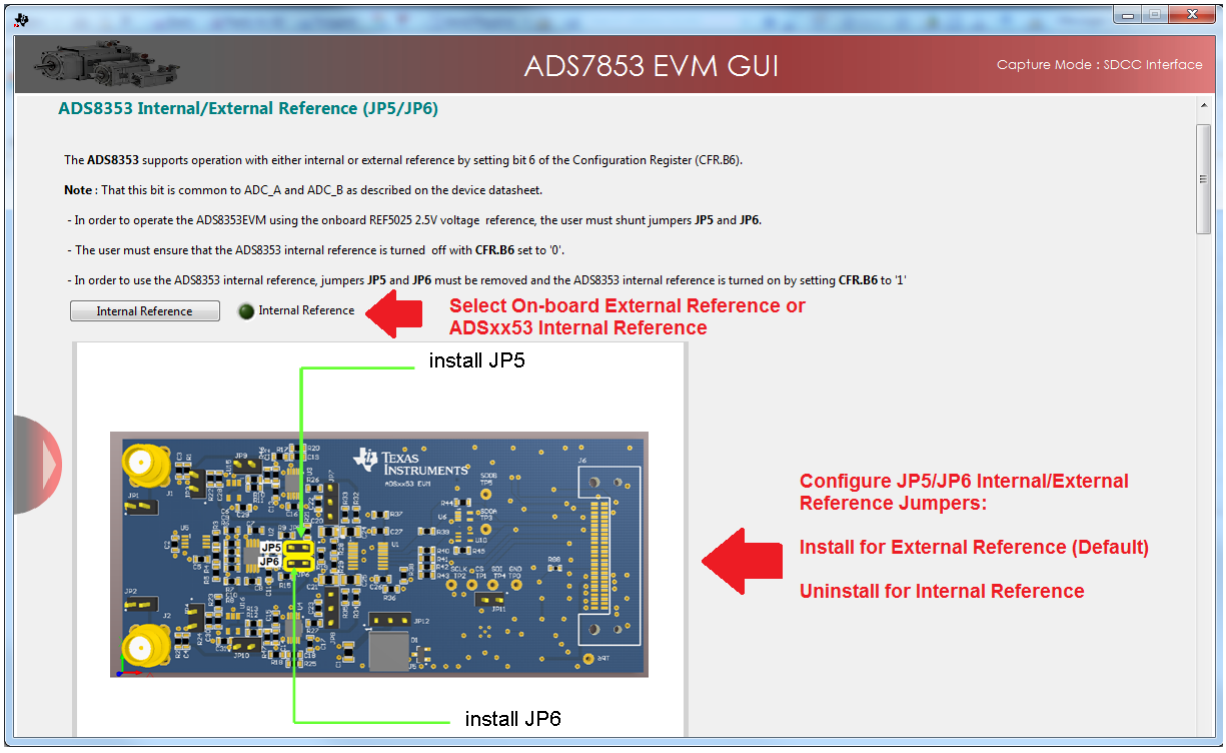


Figure 19. Selecting the External Onboard Reference or the ADSxx53 Internal Dual Reference

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3. The ADSxx53 device incorporates two internal programmable 2.5-V reference sources. When selecting the dual, internal programmable reference, independently change the voltages at VREF_A and VREF_B by writing to user-programmable registers REFDAC_A and REFDAC_B. The *Vref Value-ADC A* and *Vref Value-ADC B* control panels contain the REFDAC_x register settings. The reference voltage can be programmed in the range of 2.5 V to 2.0 V by entering the REFDAC_x register value in the control panel and clicking the *Write REFDAC_x* button. Figure 20 shows the internal reference *Vref Value-ADC x* control panels on the *ADSxx53EVM Settings* page of the GUI.

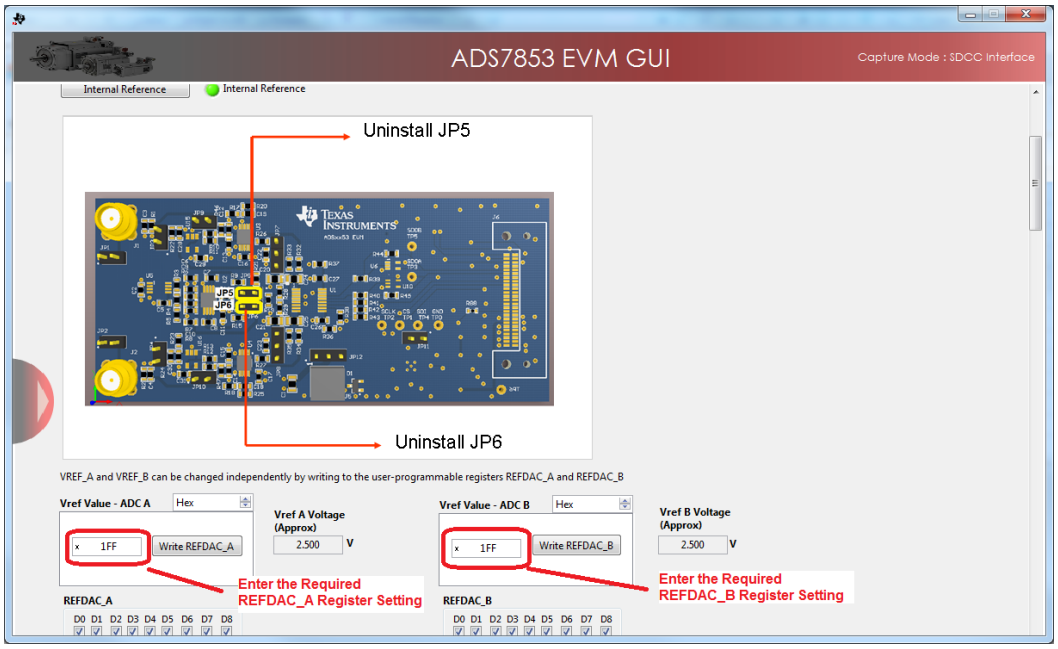


Figure 20. Programming the REFDAC Registers in the ADSxx53EVM

4. Scroll down in the *ADSxx53EVM Settings* page and find the *Input Range Selection [CFR, Bit[9]]* button to select the 0 to V_{ref} range mode or the 0 to 2 × V_{ref} range mode. Install jumpers JP3 and JP4 when selecting the 0 to V_{ref} range. Uninstall jumpers JP3 and JP4 when selecting the 0 to 2 × V_{ref} range . The GUI displays the appropriate JP3 and JP4 jumper settings, as shown in Figure 21.

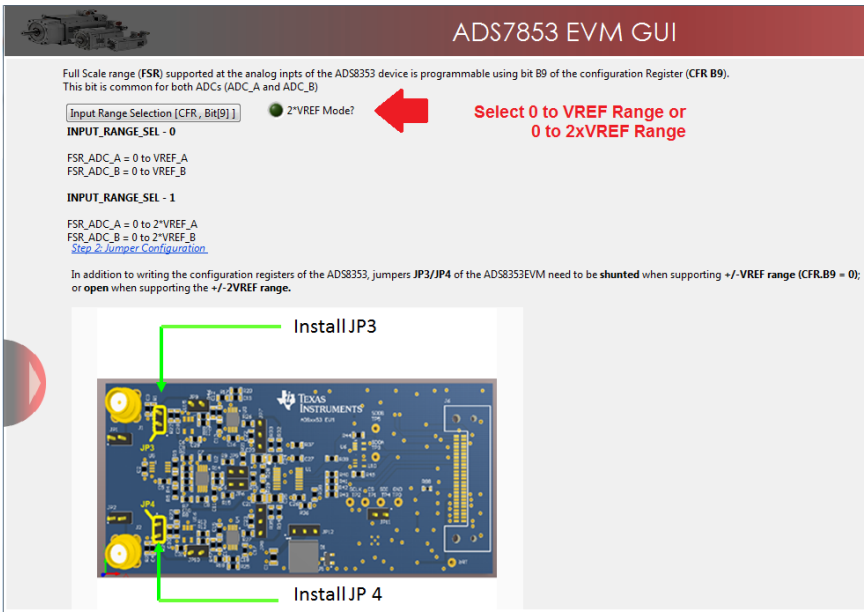


Figure 21. Selecting 0 to V_{ref} Range or 0 to 2 × V_{ref} Range

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5. Scroll down in the *ADSxx53EVM Settings* page and find the *ADSxx53 Analog Inputs* connections descriptions on the GUI. The ADSxx53 device can be programmed to support single-ended inputs or pseudo-differential inputs by setting the *INM_SEL [CFR, Bit[7]]* button. Configure jumpers JP7 and JP8 on the ADSxx53EVM to connect the negative inputs of the ADSxx53 to GND to support single-ended configuration, or to FSR / 2 to support pseudo-diffential inputs. Figure 22 shows jumpers JP7 and JP8 on the *ADSxx53EVM Settings* page of the GUI.

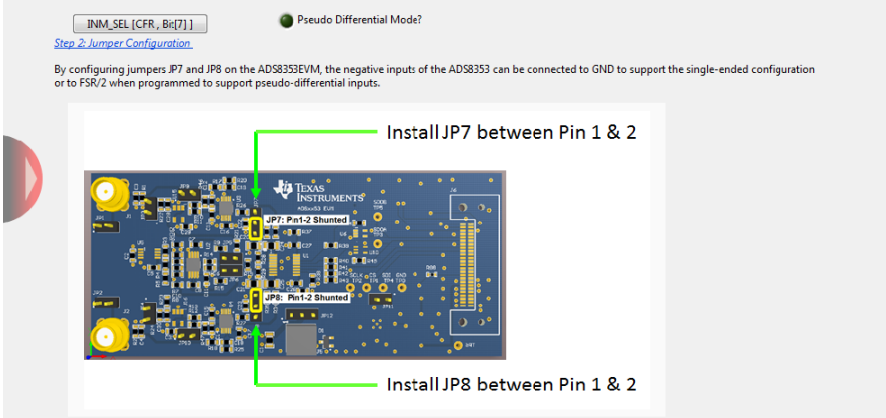


Figure 22. Single-Ended or Pseudo-Differential Jumper Settings Description on the GUI

6. The ADSxx53EVM can be driven with a signal generator producing a bipolar source signal centered on GND, or a unipolar signal centered at +FSR / 2. Install jumpers JP9 and JP10 when supporting a bipolar signal centered at GND. Remove jumpers JP9 and JP10 when supporting a unipolar signal source signal centered at FSR / 2. Figure 23 shows jumpers JP9 and JP10 on the *ADSxx53EVM Settings* page of the GUI.

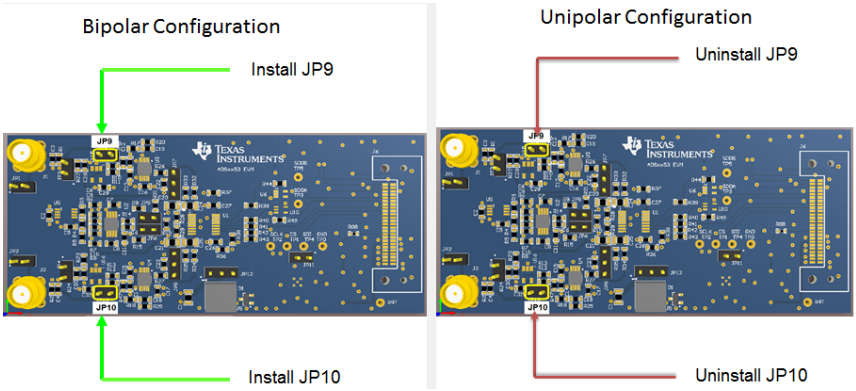


Figure 23. Bipolar or Unipolar Signal Jumper Settings Description on the GUI

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6.4 Device Registers

In addition to the ADSxx53EVM Settings page, the GUI also allows access to the SCLK frequency settings and the ADSxx53 device register settings on the *Device Registers* page of the GUI. Use the EVM software to change the following register settings of the configuration register (CFR):

- INPUT_RANGE (CFR.B9)
- INM_SEL (CFR.B7)
- REF_SEL (CFR.B6)
- STANDBY (CFR.B5)

Use the EVM software to also program the REFDAC register settings. See Section 6.3 or the ADSxx53 device datasheet for more information. Figure 24 shows the *Device Registers* page of the GUI.

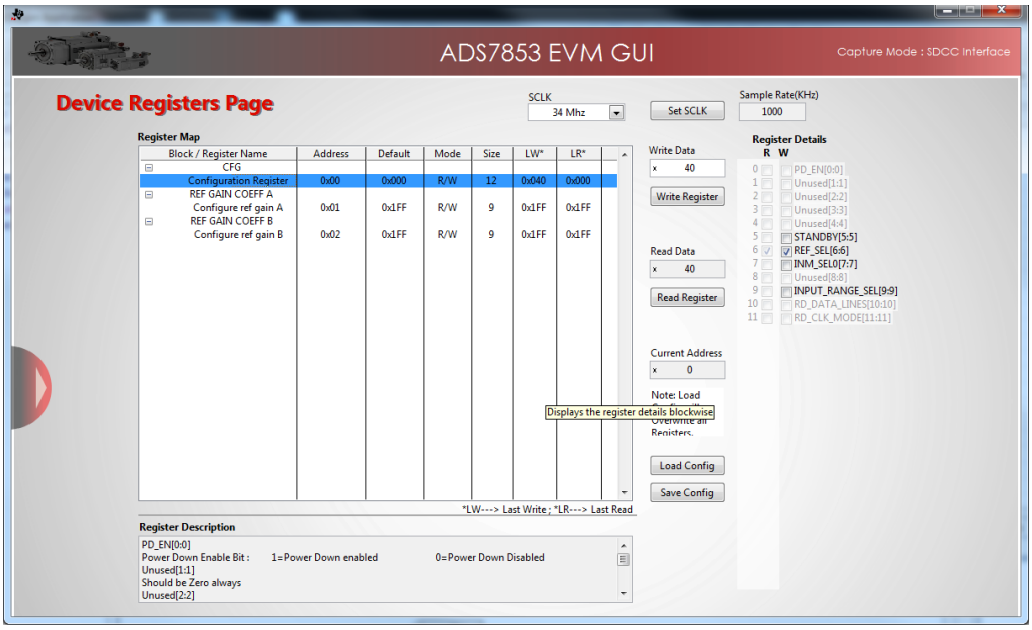


Figure 24. Device Registers Page

6.5 Capturing Data with the ADSxx53EVM-PDK

Access the *Data Monitor* page in the GUI to monitor data acquired by the ADSxx53. This GUI page displays the acquired data versus time. To access the *Data Monitor* page, hover over the red arrow at the left-center side of the GUI screen; a menu with different GUI pages appears. Click on the *Data Monitor* option in the menu, as shown in Figure 25.

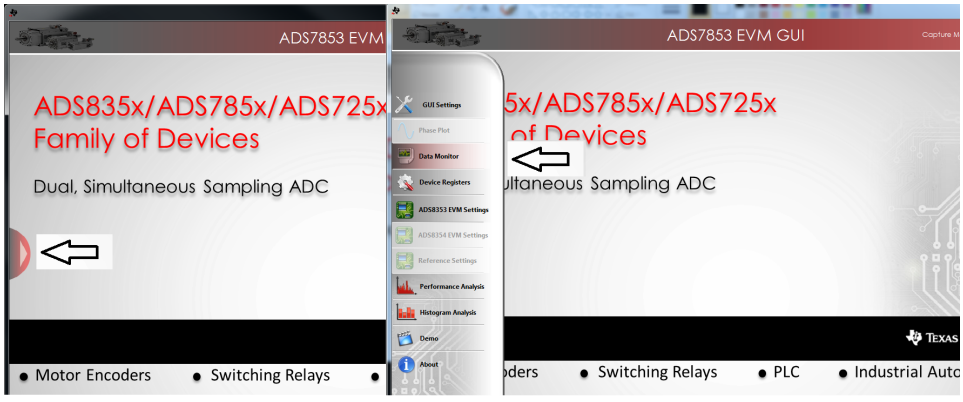


Figure 25. Open the *Data Monitor* Page on the GUI

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Figure 26 shows the *Data Monitor* page of the EVM GUI. Configure the device sampling rate and capture settings by using the *Capture Settings* portion of the *Data Monitor* page. The change in configuration settings are executed immediately after pressing the *Configure Device* button. The following list describes the different options available on the *Data Monitor* page.

# of Samples— This option is used to select the number of samples captured in a block.

The number of samples captured in a block are contiguous. The drop-down menu is used to select a data block in the range of 1024 samples to 1,048,576 samples per channel. This control provides a drop-down list for values restricted to 2^n, where *n* is an integer.

SCLK— This control sets the clock frequency used by the SPI interface to capture data.

By configuring the SCLK frequency, the data rate of the ADS7853 is configured.

The ADS7853EVM-PDK software supports SCLK frequencies of 34 MHz, 24 MHz, 20 MHz, and 16.2 MHz. These SCLK frequencies correspond to data rates of 1 MSPS, 705.8 kSPS, 588 kSPS, and 476.5 kSPS, respectively.

The ADS8353EVM-PDK software supports SCLK frequencies of 20 MHz, 16.2 MHz, and 10MHz . These SCLK frequencies correspond to data rates of 606 kSPS, 490.9 kSPS, and 303.03 kSPS, respectively

Internal Reference?— Use this button to select the ADSxx53 device internal reference, or the onboard REF5025 2.5-V external reference.

Program the internal reference settings by navigating into the *ADSxx53 EVM Settings* GUI page, as described in Section 6.3 of this document.

2*VREF Mode— This option is used to configure the ADSxx53 to the 0 to 1 × V_{ref} range or the 0 to 2 × V_{ref} range.

Make sure to configure jumpers JP3 and JP4 appropriately, depending on the mode of operation.

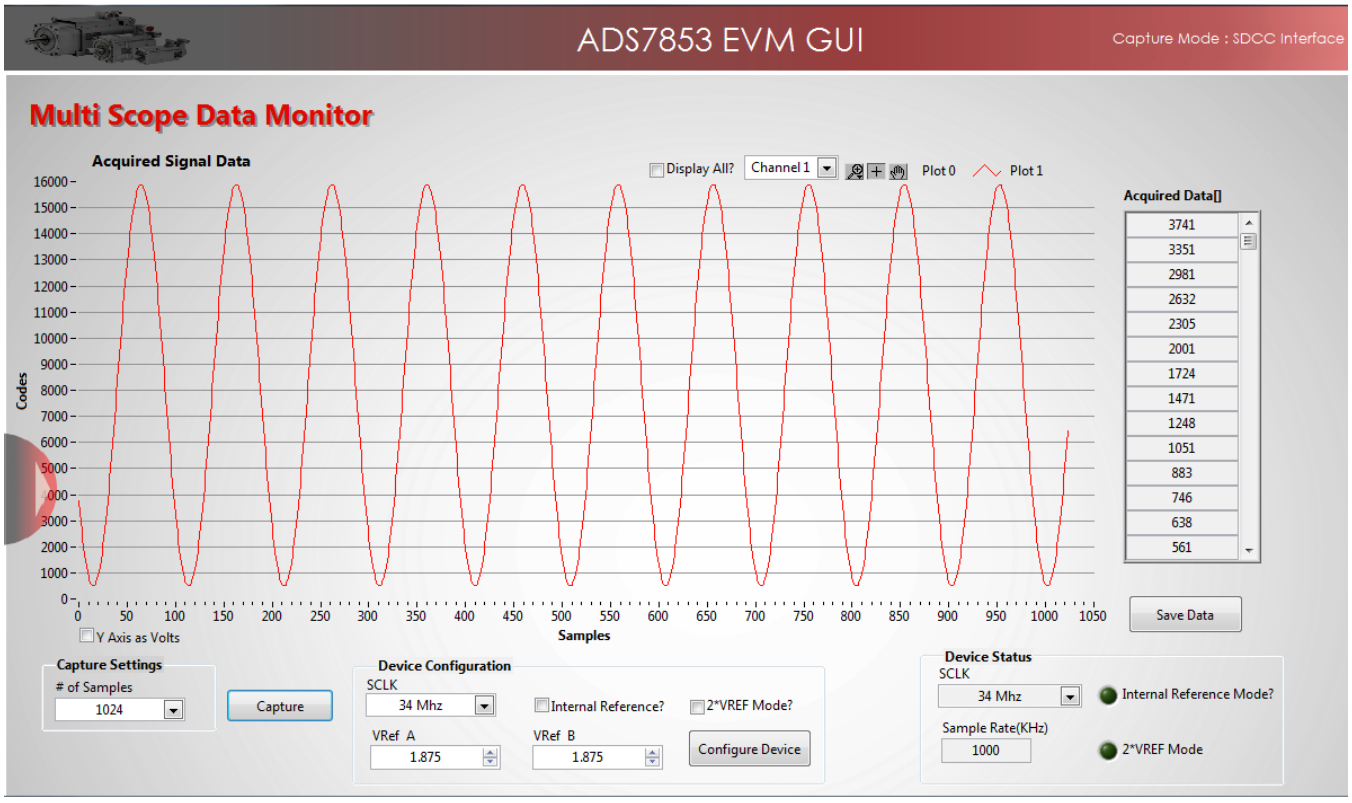


Figure 26. *Data Monitor* **Page**

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6.5.1 Data Collection to Text Files

The *Data Monitor* page of the GUI allows data to be saved in a tab-delimited text file format that can be imported into Excel® or other spreadsheet software tools. The text file contains the raw ADC data of both channel A and channel B in decimal data format. Information such as the device name, date and time, the sampling frequency, and number of samples of the data record are also stored. In order to save any data captured by the EVM, click on the *Save Data* button and specify the file path and file name of the data file, as shown in Figure 27.

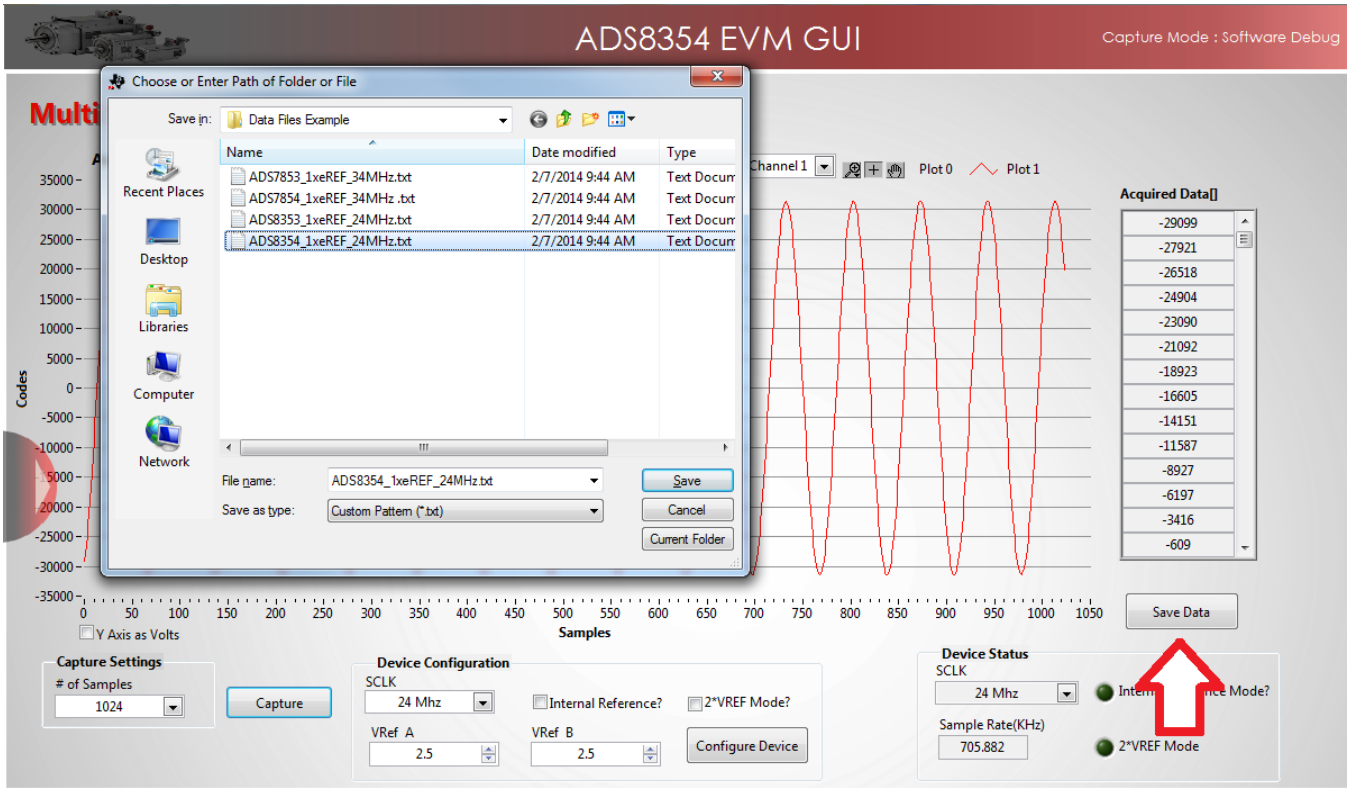


Figure 27. Saving Data to a Text File

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6.6 FFT Analysis

The *Performance Analysis* page in the GUI performs the fast fourier transform (FFT) of the captured data, and displays the resulting frequency domain plots of channel A and channel B of the ADSxx53. This page also calculates key ADC dynamic performance parameters, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD) and spurious-free dynamic range (SFDR).Figure 28 shows the FFT performance analysis display. The FFT calculated parameters are shown on the right side of the display.

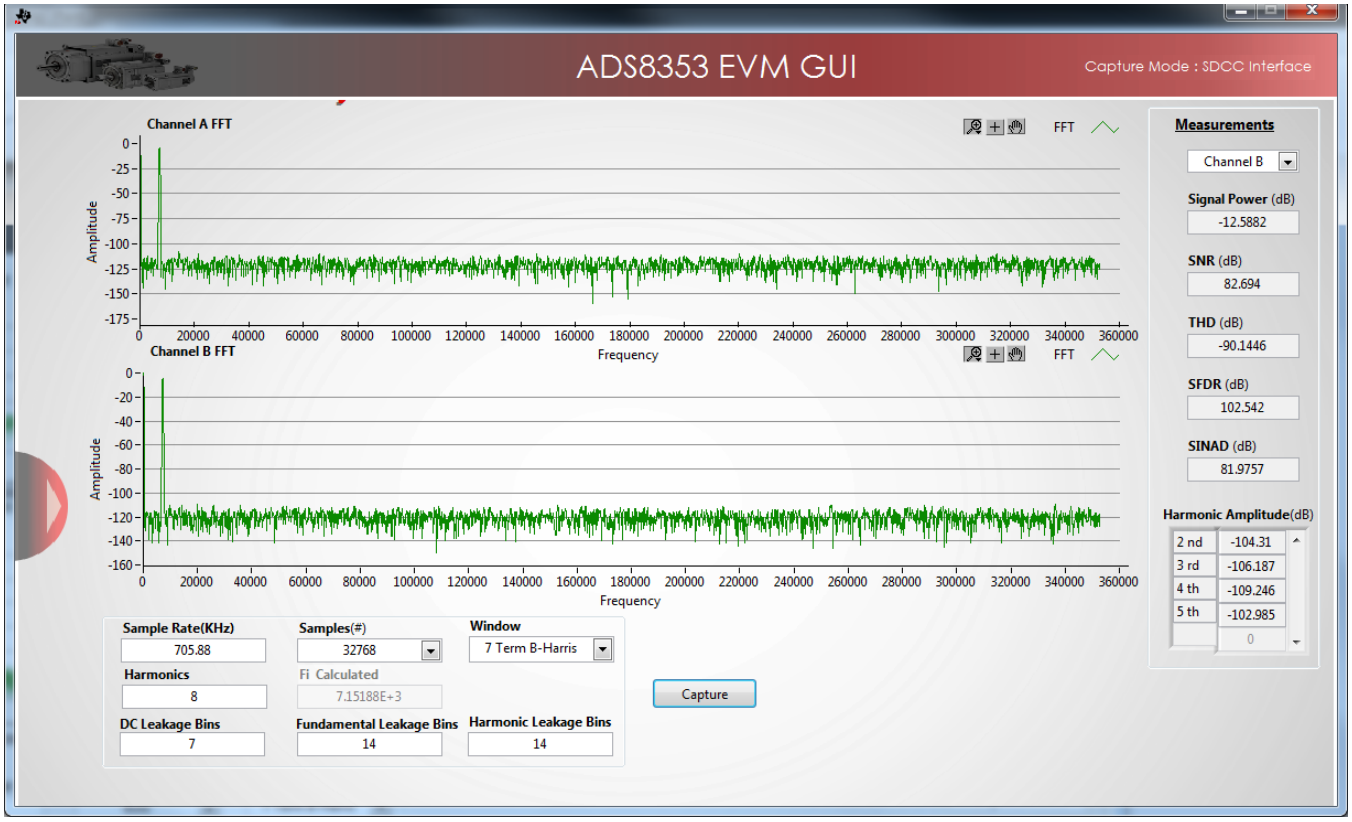


Figure 28. FFT Performance Analysis Page

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6.6.1 FFT Analysis Settings and Controls

Sample Rate (kHz)— This field indicates the sampling frequency of the ADC data (kHz).

Samples (#)— The FFT requires a time domain record with a number of samples that is a power of 2. The Samples (#) drop-down menu provides a list of values that satisfy this requirement.

Fi Calculated— This field displays the frequency of the largest amplitude input signal computed from the FFT data, typically the fundamental frequency.

Window— The window function is a mathematical function that reduces the signal to zero at the end points of the data block.

In applications where coherent sampling cannot be achieved, a window-weighting function can be applied to the data to minimize spectral leakage. The following opions are available:

- None (no window weighting function applied; use for coherent data)
- Hanning
- Hamming
- Blackman-Harris
- Exact Blackman
- Blackman
- Flat Top
- 4-Term Blackman-Harris
- 7-Term Blackman-Harris
- Low Sidelobe

For a more thorough discussion of windowing, refer to IEEE1241-2000.

Harmonics— This field sets the number of harmonics that are included in the FFT performance calculations.

Leakage Bins— These fields provide for the removal of the unwanted frequency bins that may be the result of noncoherent data sampling.

Set the *Fundamental Leakage Bins* and *Harmonic Leakage Bins* fields to the number of adjacent bins on either side of the fundamental or harmonic frequencies to include the main frequency power. The *DC Leakage Bins* field allows the number of frequency bins that are a result of the dc portion of the measurement to be excluded from the calculations.

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6.7 Histogram Analysis

Histogram testing is commonly used when characterizing ADCs. A histogram is merely a count of the number of times a code has occurred in a particular data set. The *Histogram Analysis* page of the GUI creates a histogram of the data of the acquired data set and displays it. Figure 29 shows the *Histogram Analysis* page of the GUI.

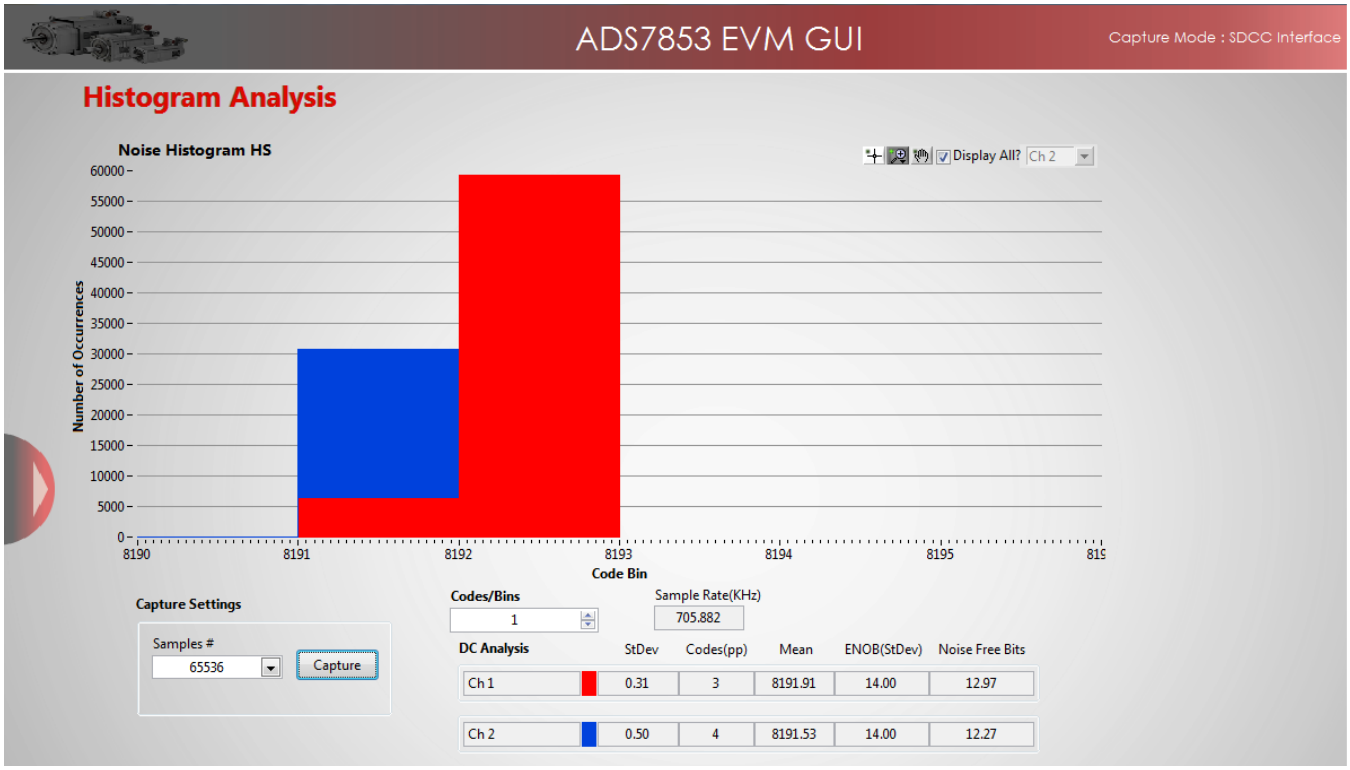


Figure 29. Histogram Analysis

The *DC Analysis* table shown in Figure 29 displays several parameters of the captured data set:

- The *StDev* column displays the standard deviation of the data set. This value is equivalent to the RMS noise of the signal when analyzing a dc data set.
- The *Codes(pp)* column shows the peak-to-peak spread of the codes in the data set; for a dc data set, this range would be the peak-to-peak noise.
- The *Mean* column displays the average value of the data set.
- The *ENOB(StDev)* column displays the effective number of bits of the converter, as calculated from the standard deviation or RMS noise.
- The *Noise Free Bits* column displays the effective bits of the converter when calculated using the peak-to-peak noise.

6.8 Troubleshooting

If the ADSxx53EVM software stops responding while the ADSxx53EVM-PDK is connected, unplug the USB cable from the EVM, unload the ADSxx53EVM-PDK software, reconnect the ADSxx53EVM-PDK to the PC, and reload the ADSxx53EVM software.

When initially setting up the EVM, the software detects the EVM hardware, and loads the appropriate hardware settings. If the EVM hardware is not detected, the GUI defaults to the *Capture Mode: Software Debug* mode of operation using a preloaded captured data file for demonstration purposes.

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While using the EVM-PDK hardware for data acquisition, keep the GUI in the *Capture Mode: SDCC interface* mode of operation. The GUI indicates the selected mode of operation on the top-right corner of the GUI display. In order to select the hardware interface mode of operation, navigate to the *GUI Settings* page and select the *SDCC Interface* option on the *Capture Mode* drop-down menu, as shown in Figure 30 and Figure 31.

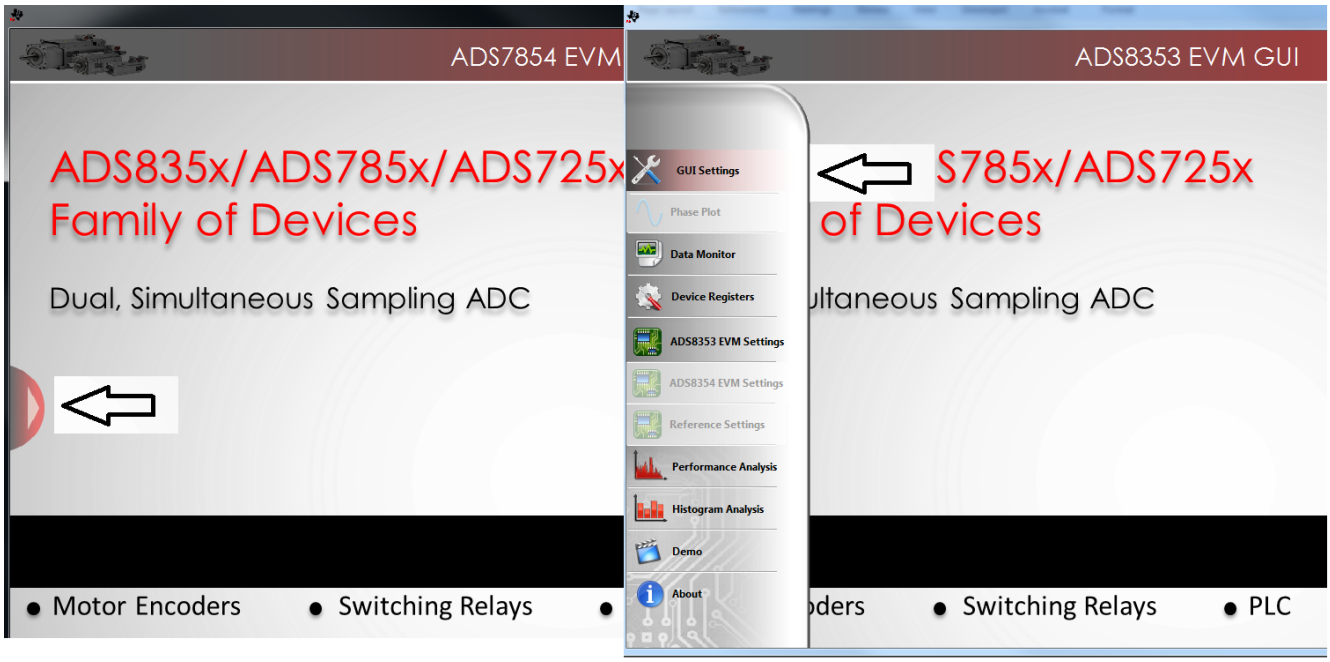


Figure 30. Open the *GUI Settings* Page

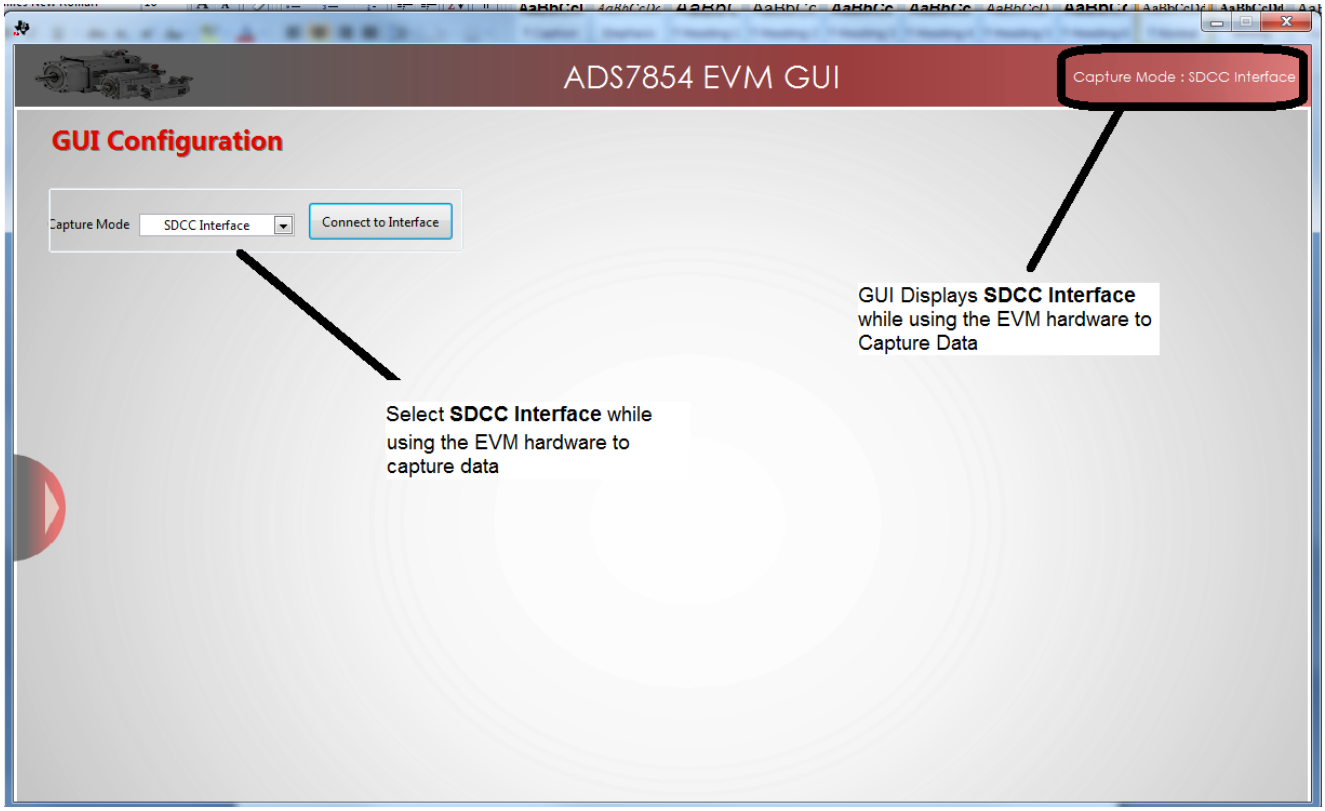


Figure 31. Set Capture Mode to *SDCC Interface* While Using the EVM Hardware

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7 Bill of Materials, PCB Layout, and Schematics

Section 7.1 lists the bill of materials. Section 7.2 shows the printed circuit board (PCB) layout for the ADSxx53EVM. The schematics for the ADSxx53EVM are appended to the end of this user's guide.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the http://www.ti.com.)

Table 7. ADSxx53EVM Bill of Materials

Item No.	Qty	Ref Des	Description	Vendor	Part Number
1	11	C1, C20, C21, C39, C41, C42, C43, C44, C45, C46, C54	CAP, CERM, 10uF, 16V, +/-10%, X5R, 0805	Murata	GRM21BR61C106KE15L
2	11	C2, C5, C9, C10, C12, C13, C14, C15, C28, C30, C40	CAP, CERM, 1uF, 6.3V, +/-10%, X7R, 0603	Murata	GRM188R70J105KA01D
3	0	C3, C4, C18, C19, C22, C23	Not installed	N/A	N/A
4	0	R1, R2, R5, R8, R19, R30	Not installed	N/A	N/A
5	4	C6, C26, C27, C51	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	TDK	C1608X5R0J106M
6	10	C7, C8, C11, C16, C17, C29, C31, C48, C52, C53	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
7	2	C24, C25	CAP CER 8200PF 50V 5% NP0 0805	TDK	C2012C0G1H822J060AA
8	2	C47, C50	CAP, CERM, 2.2uF, 16V, +/-10%, X5R, 0603	Murata	GRM188R61C225KE15D
9	1	C49	CAP, CERM, 0.22uF, 16V, +/-10%, X5R, 0603	TDK	GRM188R61C224KA88D
10	1	D1	DIODE ZENER 5.9V 250MW SOT23	NXP Semiconductors	PLVA659A.215
11	2	J1, J2	Connector, TH, SMA	TE Connectivity	142-0701-201
12	1	J5	2 Terminal Block 3.5MM 2POS PCB	On Shore Technology Inc	ED555/2DS
13	1	J6	SAMTEC, dual-row, right-angle, female, latching	SAMTEC	ERF8-025-01-L-D-RA-L-TR
14	1	J7	Note: Connector Not Installed on PWB Rev. A MOLEX connector for microSD card	Molex Inc	Note: Connector Not Installed on PWB Rev. A MOLEX 502570-0893
15	9	JP1, JP2, JP3, JP4, JP5, JP6, JP9, JP10, JP11	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	SAMTEC	TSW-102-07-G-S
16	3	JP7, JP8, JP12	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	SAMTEC	TSW-103-07-G-S
17	1	R3	RES, 0.22 ohm, 1%, 0.1W, 0603	Panasonic Electronic Components	ERJ-3RQFR22V
18	9	R4, R14, R16, R36, R37, R44, R45, R89, R90	RES, 0 ohm, 5%, 0.1W, 0603	Vishay Dale	CRCW06030000Z0EA
19	2	R6, R7	RES, 100 ohm, 1%, 0.1W, 0603	Yageo	CRCW0603100RFKEA
20	8	R9, R15, R39, R40, R41, R42, R43, R31	RES, 47.0 ohm, 1%, 0.1W, 0603	Yageo	RC0603FR-0747RL
21	8	R10, R12, R17, R18, R20, R25, R46, R47	RES, 1.00k ohm, 0.1%, 0.1W, 0603	Susumu	RG1608P-102-B-T5
22	2	R11, R13	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW06031K00FKEA
23	4	R21, R22, R23, R24	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060320K0FKEA

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Table 7. ADSxx53EVM Bill of Materials (continued)

Item No.	Qty	Ref Des	Description	Vendor	Part Number
24	2	R26, R27	RES, 1.00 ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW06031R00FKEA
25	2	R28, R29	RES, 0.1 ohm, 1%, 0.1W, 0603	Panasonic Electronic Components	ERJ-3RSFR10V
26	4	R38, R86	RES, 100k ohm, 5%, 0.1W, 0603	Vishay Dale	CRCW0603100KJNEA
28	6	R70, R71, R72, R73, R74, R75	RES, 10k ohm, 5%, 0.063W, 0402	Vishay Dale	CRCW040210K0JNED
29	1	R76	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060310K0FKEA
30	2	R80, R84	RES, 0 ohm, 5%, 0.125W, 0805	Vishay Dale	CRCW08050000Z0EA
31	0	R83, R87, R88	Not installed	N/A	N/A
32	1	U1	Dual, 600kSPS or 1-MSPS,16-bit or 14-Bit Simultaneous Sampling ADC	Texas Instruments	ADS8353IPWR or ADS7853IPWR
33	1	U2	High-Speed, Single-Supply, Rail-to-Rail OPA	Texas Instruments	OPA2350EA
34	2	U3, U4	Very Low-Power, Rail-to-Rail Out, Negative Rail In, VFB Op Amp 205MHz	Texas Instruments	OPA2836IDGS
35	1	U5	Low Noise, Low Drift, Precision Voltage Reference	Texas Instruments	REF5025IDGK
36	2	U6, U10	Not installed	N/A	N/A
37	1	U7	Atmel I2C Compatible (2-Wire) Serial EEPROM	Atmel	AT24C02C-XHM
38	1	U8	36-V, 1-A, 4.17uVRMS RF LDO Voltage Regulator	Texas Instruments	TPS7A4700RGW
39	1	U9	60mA, 5.5V, Buck/Boost Charge Pump	Texas Instruments	REG71055DDC
40	1	U14	NanoPower Supervisory Circuit	Texas Instruments	TPS3836E18DBVT
41	2	U15, U16	Low Noise, Low Quiescent Current, Precision OPA	Texas Instruments	OPA376AIDBVT
42	9	N/A	Conn Shunt, Pitch 0.100"; Height 0.240" , Gold Plated	SAMTEC	SNT-100-BK-G
43	1	TP0	TEST POINT PC MINI .040"D BLACK	Keystone Elerctronics	5001
44	4	TP7, TP8, TP9, TP10	Note: These Test Points only available on PWB Rev. C TEST POINT PC MINI .040"D BLACK	Keystone Elerctronics	Note: These Test Points only available on PWB Rev. C 5001
45	0	TP1, TP2, TP3, TP4, TP5, TP6	Not Installed	N/A	N/A
46	2	N/A	BUMPON CYLINDRICAL .375X.135 BLK	3M	SJ61A8

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7.2 PCB Layout

Figure 32 through Figure 35 show the PCB layout for the ADSxx53EVM.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADSxx53EVM PCBs.

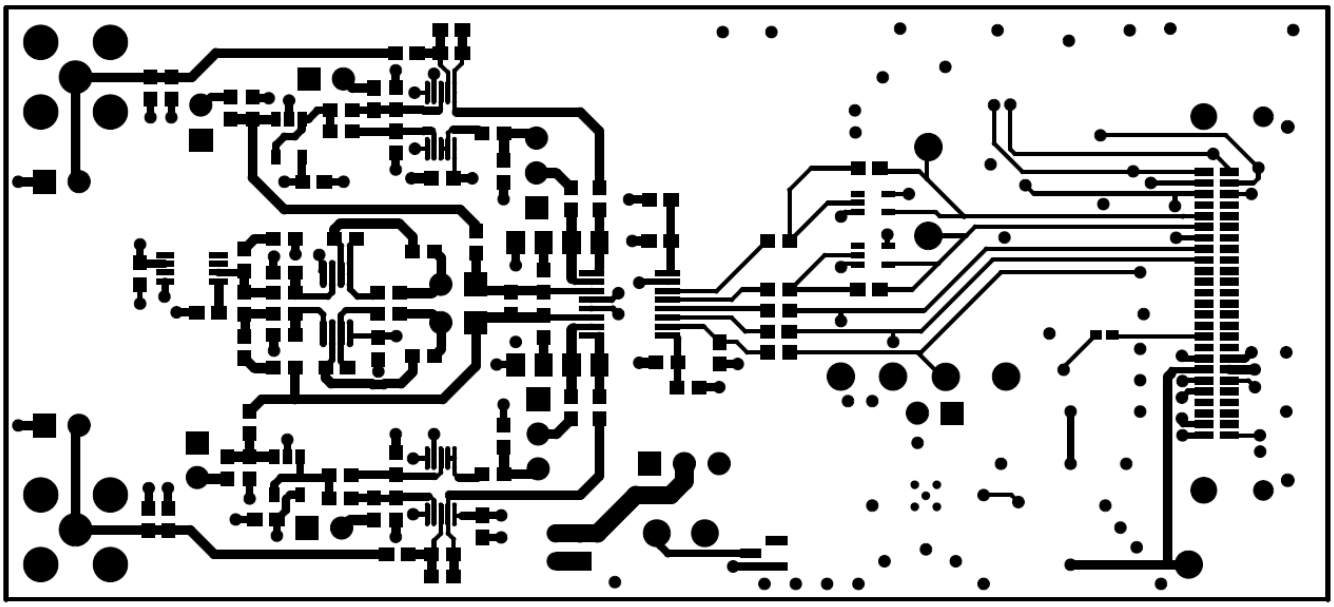


Figure 32. ADSxx53EVM PCB: Top Layer

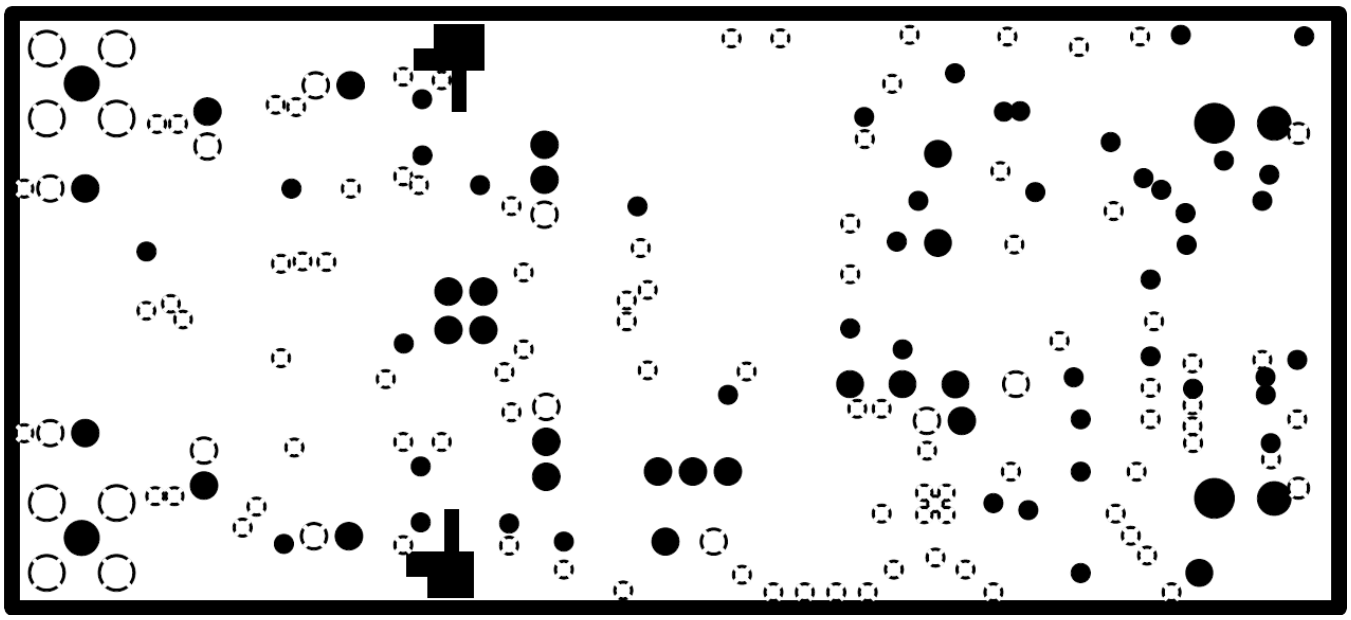


Figure 33. ADSxx53EVM PCB: Ground Layer

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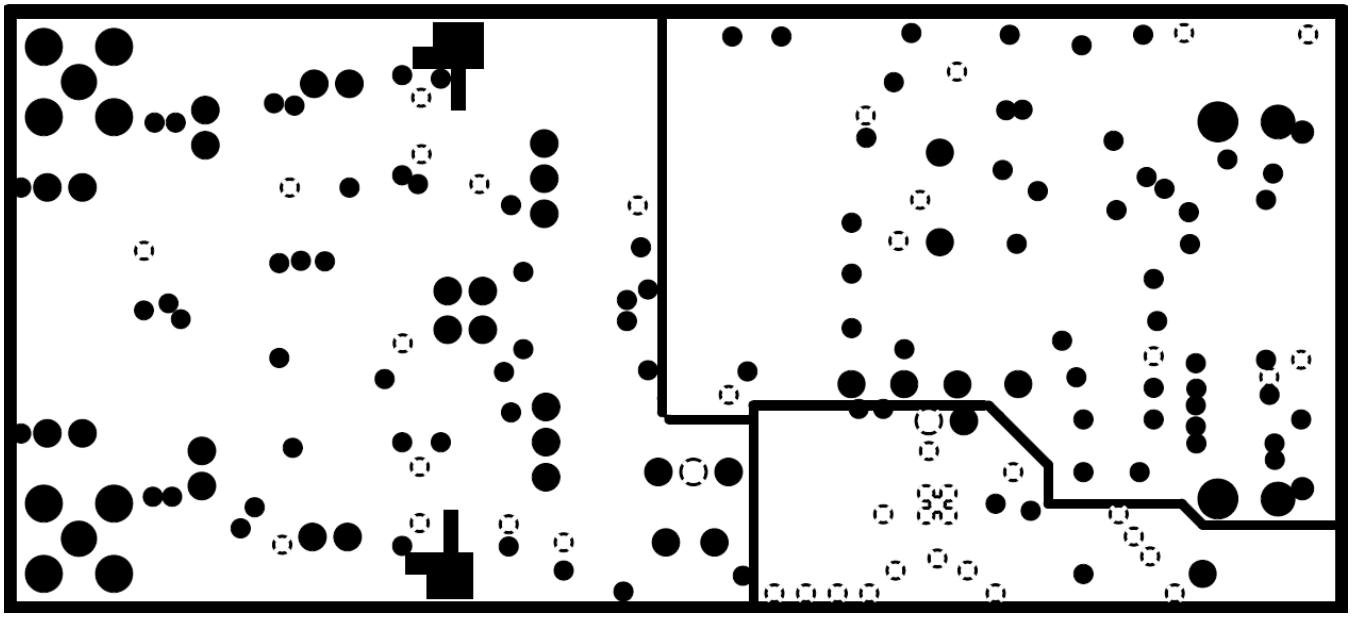


Figure 34. ADSxx53EVM PCB: Power Layer

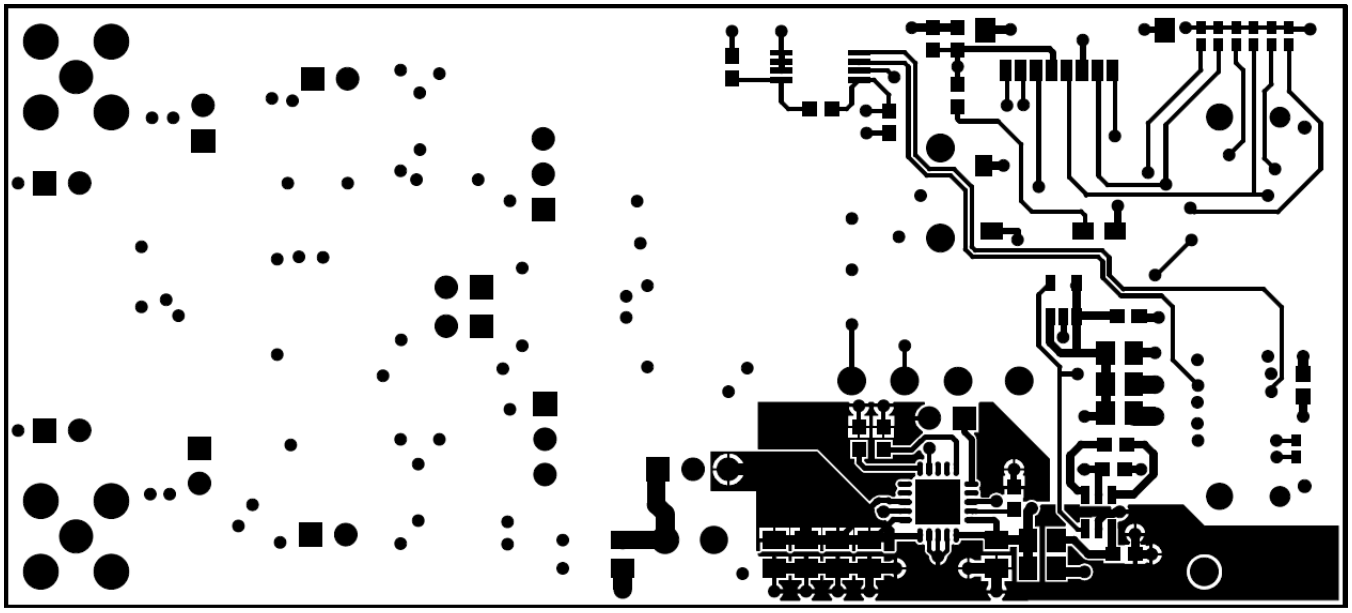


Figure 35. ADSxx53EVM PCB: Bottom Layer

7.3 Schematics

The schematics for the ADSxx53EVM are appended to the end of this user's guide.

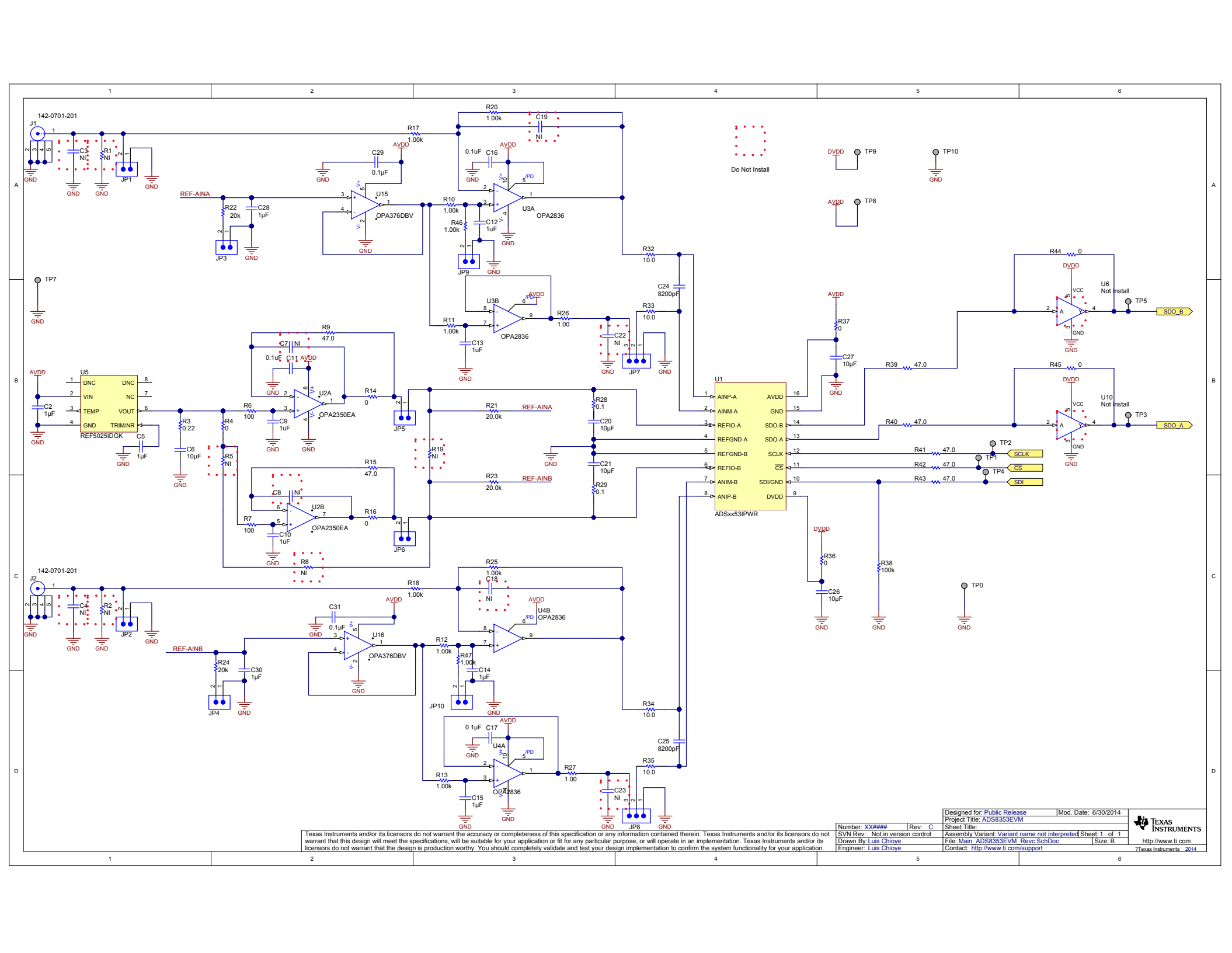
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Revision History

Changes from Original (June 2014) to A Revision	Page
• Added ADS8353EVM-PDK to document	1
• Changed ADS7853 to ADSxx53 where applicable throughout document	1
• Changed *SDCC controller* to *simple capture card controller* throughout document	4
• Changed ADSxx53EVM revision C requirement to two microSD cards in Section 5.2	12
• Added Figure 8	13
• Added SCLK frequencies for the ADS8353EVM in Section 6.5	22
• Changed J7 ,TP7,TP8, TP9, TP10 rows (item no. 14 and 44) in Table 7	29

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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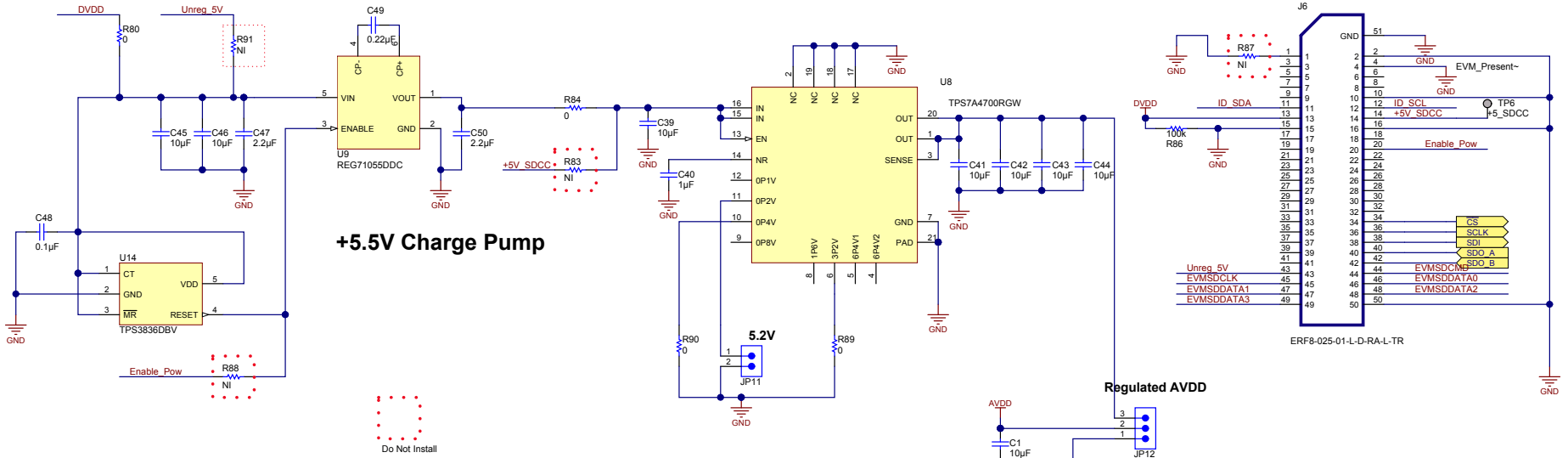
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Number: XX####	Rev: C	Designed for: Public Release	Mod. Date: 6/30/2014
SVN Rev: Not in version control		Project Title: ADS8353EVM	
Drawn By: Luis Chioye		Sheet Title:	
Engineer: Luis Chioye		Assembly Variant: Variant name not interpreted	Sheet: 1 of 1
		File: Main_ADS8353EVM_Revc.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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Number: XX####	Rev: C	Designed for: Public Release	Mod. Date: 6/30/2014
SVN Rev: Not in version control		Project Title: ADS8353EVM	
Drawn By:		Sheet Title:	
Engineer: Luis Chioye		Assembly Variant: Variant name not interpreted	Sheet: 1 of 1
		File: Connector_ADS8353EVM_RevC.SchDoc	Size: B
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- *Reorient or relocate the receiving antenna.*
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- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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