SBAS103C – SEPTEMBER 2000 – REVISED OCTOBER 2006

12-Bit, 4-Channel Parallel Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL INPUT MULTIPLEXER
- UP TO 200kHz SAMPLING RATE
- FULL 12-BIT PARALLEL INTERFACE
- ±1LSB INL AND DNL
- NO MISSING CODES
- 72dB SINAD
- LOW POWER: 2mW
- SSOP-28 PACKAGE

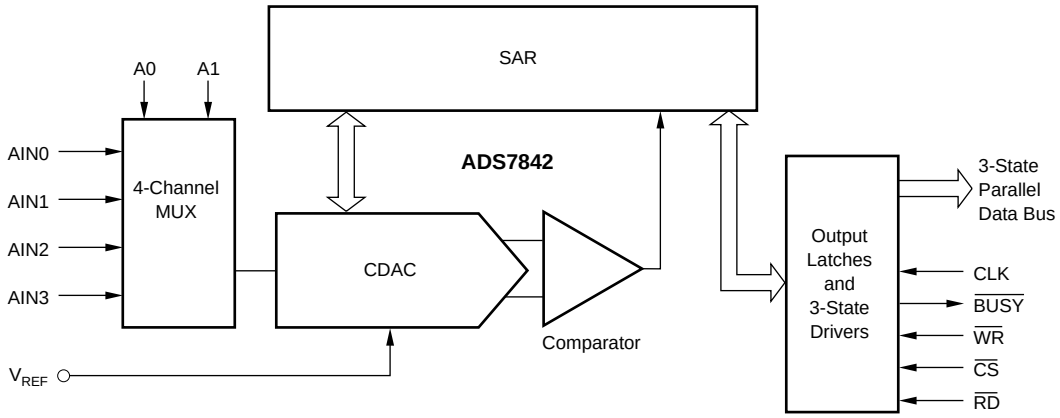
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTS
- LABORATORY EQUIPMENT

DESCRIPTION

The ADS7842 is a complete, 4-channel, 12-bit Analog-to-Digital Converter (ADC). It contains a 12-bit, capacitor-based, Successive Approximation Register (SAR) ADC with a sample-and-hold amplifier, interface for microprocessor use, and parallel, 3-state output drivers. The ADS7842 is specified at a 200kHz sampling rate while dissipating only 2mW of power. The reference voltage can be varied from 100mV to V_{CC} with a corresponding LSB resolution from 24µV to 1.22mV. The ADS7842 is tested down to 2.7V operation.

Low power, high speed, and an onboard multiplexer make the ADS7842 ideal for battery-operated systems such as portable, multi-channel dataloggers and measurement equipment. The ADS7842 is available in an SSOP-28 package and is tested over the –40°C to +85°C temperature range.



PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	SINAD (dB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7842E	±2	68	SSOP-28	DB	–40°C to +85°C	ADS7842E	ADS7842E	Rails, 48
"	"	"	"	"	"	"	ADS7842E/1K	Tape and Reel, 1000
ADS7842EB	±1	70	SSOP-28	DB	–40°C to +85°C	ADS7842EB	ADS7842EB	Rails, 48
"	"	"	"	"	"	"	ADS7842EB/1K	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

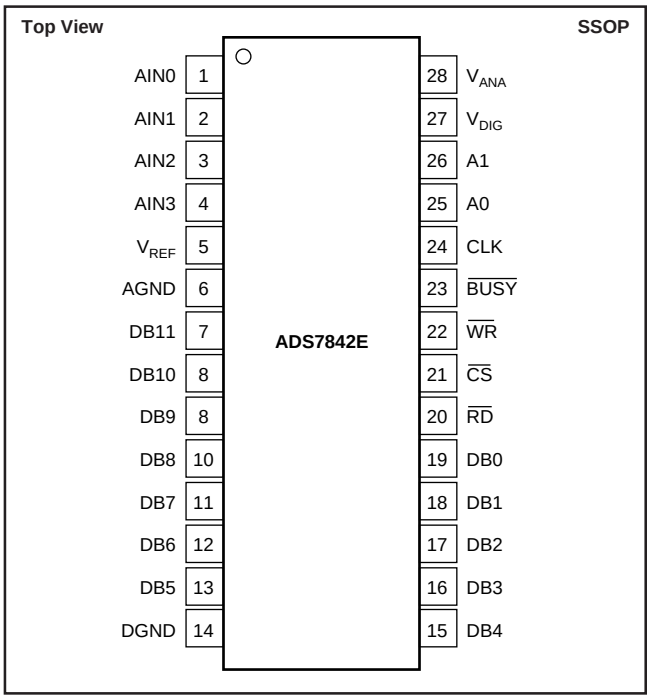
NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	AIN0	Analog Input Channel 0
2	AIN1	Analog Input Channel 1
3	AIN2	Analog Input Channel 2
4	AIN3	Analog Input Channel 3
5	V_{REF}	Voltage Reference Input. See Electrical Characteristics Tables for ranges.
6	AGND	Analog Ground
7	DB11	Data Bit 11 (MSB)
8	DB10	Data Bit 10
9	DB9	Data Bit 9
10	DB8	Data Bit 8
11	DB7	Data Bit 7
12	DB6	Data Bit 6
13	DB5	Data Bit 5
14	DGND	Digital Ground
15	DB4	Data Bit 4
16	DB3	Data Bit 3
17	DB2	Data Bit 2
18	DB1	Data Bit 1
19	DB0	Data Bit 0 (LSB)
20	$\overline{RD}$	Read Input. Active LOW. Reads the data outputs in combination with $\overline{CS}$.
21	$\overline{CS}$	Chip Select Input. Active LOW. The combination of $\overline{CS}$ taken LOW and $\overline{WR}$ taken LOW initiates a new conversion and places the outputs in the tri-state mode.
22	$\overline{WR}$	Write Input. Active LOW. Starts a new conversion and selects an analog channel via address inputs A0 and A1, in combination with $\overline{CS}$.
23	$\overline{BUSY}$	$\overline{BUSY}$ goes LOW and stays LOW during a conversion. $\overline{BUSY}$ rises when a conversion is complete and enables the parallel outputs.
24	CLK	External Clock Input. The clock speed determines the conversion rate by the equation $f_{CLK} = 16 \cdot f_{SAMPLE}$.
25, 26	A0, A1	Address Inputs. Selects one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of either $\overline{RD}$ or $\overline{WR}$.
		A1 / A0 / Channel Selected 0 / 0 / AIN0 0 / 1 / AIN1 1 / 0 / AIN2 1 / 1 / AIN3
27	V_{DIG}	Digital Supply Input. Nominally +5V.
28	V_{ANA}	Analog Supply Input. Nominally +5V.

ELECTRICAL CHARACTERISTICS: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

		ADS7842E			ADS7842EB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Span		0		V_{REF}	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power-Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–80	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz	68	71		70	72		dB
Spurious-Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	79		76	81		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		120			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	| I_{IH} | ≤ +5µA	3.0		5.5	*		*	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
External Clock		0.2		3.2	*		*	MHz
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900		*	*	µA
	f_{SAMPLE} = 12.5kHz		300			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				4.5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7842E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV.
(2) First five harmonics of the test frequency.
(3) Power-down mode at end of conversion when $\overline{WR}$, $\overline{CS}$, and $\overline{BUSY}$ conditions have all been met. Refer to Table III of this data sheet.

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7842E			ADS7842EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Full-Scale Input Span		0		V_{REF}	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±5			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power-Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	3.6V ≥ V_{CC} ≥ 3.0V, V_{IN} = 2.5Vp-p at 10kHz		–77	–70		–79	–74	dB
	3.0V > V_{CC} ≥ 2.7V, V_{IN} = 2.5Vp-p at 10kHz		–77	–70		*	*	dB
Signal-to-(Noise + Distortion)	3.6V ≥ V_{CC} ≥ 3.0V, V_{IN} = 2.5Vp-p at 10kHz	68	71		70	72		dB
	3.0V > V_{CC} ≥ 2.7V, V_{IN} = 2.5Vp-p at 10kHz	68	71		*	*		dB
Spurious-Free Dynamic Range	3.6V ≥ V_{CC} ≥ 3.0V, V_{IN} = 2.5Vp-p at 10kHz	72	78		76	80		dB
	3.0V > V_{CC} ≥ 2.7V, V_{IN} = 2.5Vp-p at 10kHz	72	78		*	*		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	| I_{IH} | ≤ +5µA	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
External Clock		0.2		2	*		*	MHz
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

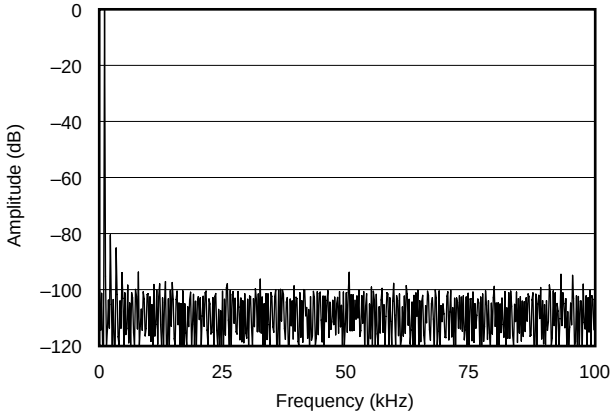
* Same specifications as ADS7842E.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV.
(2) First five harmonics of the test frequency.
(3) Power-down mode at end of conversion when $\overline{WR}$, $\overline{CS}$, and $\overline{BUSY}$ conditions have all been met. Refer to Table III of this data sheet.

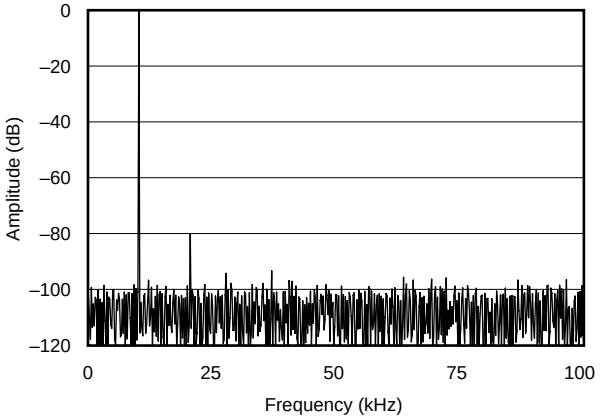
TYPICAL CHARACTERISTICS: +5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

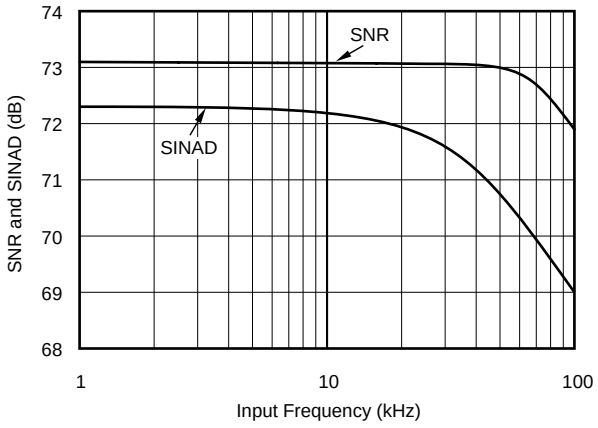
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



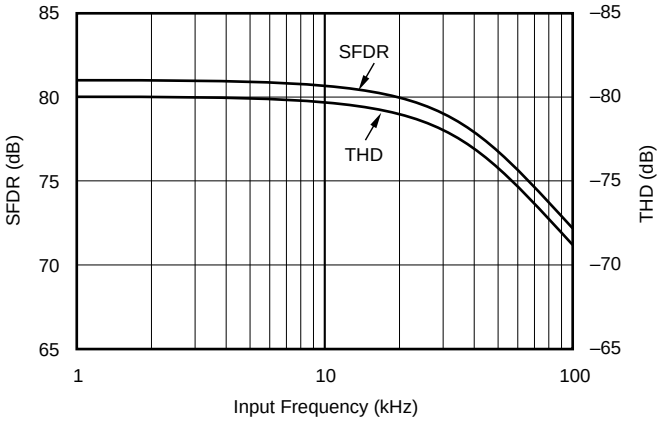
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



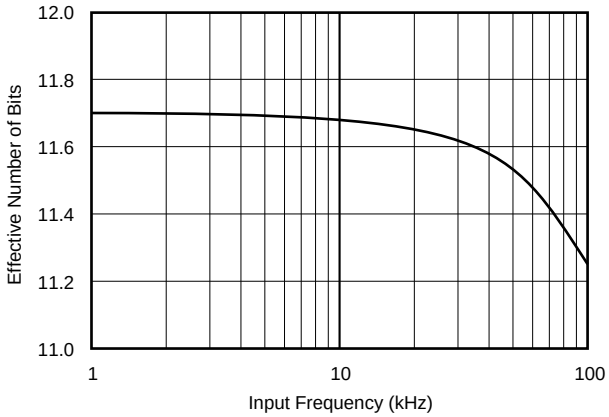
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE + DISTORTION) vs INPUT FREQUENCY



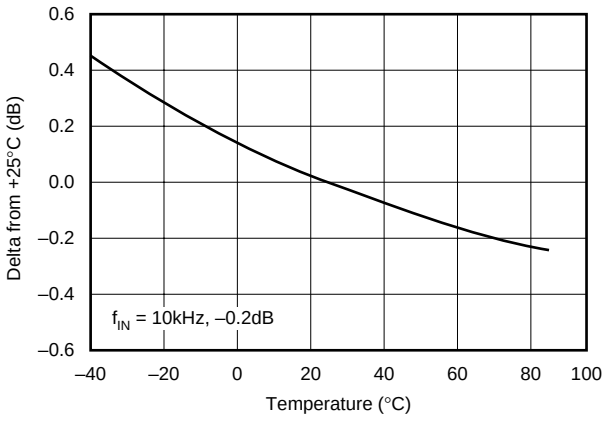
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



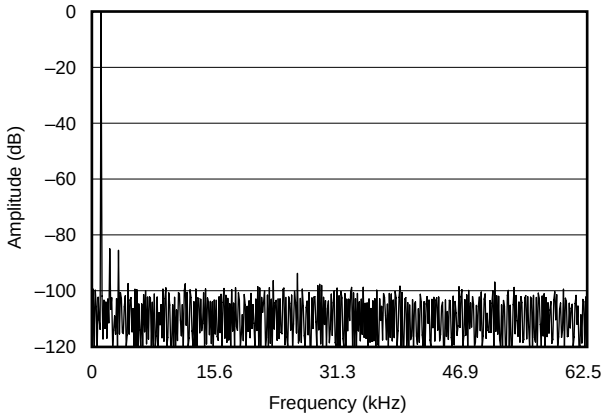
CHANGE IN SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



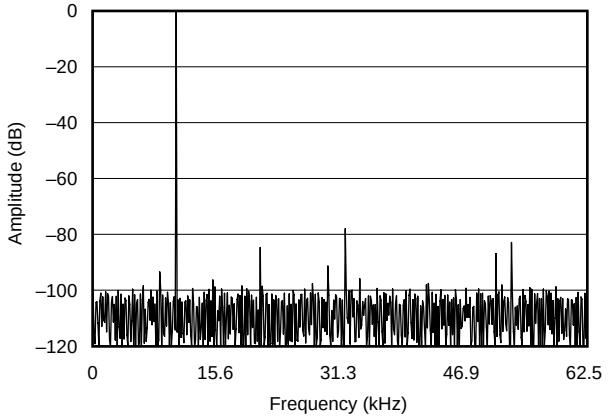
TYPICAL CHARACTERISTICS: +2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

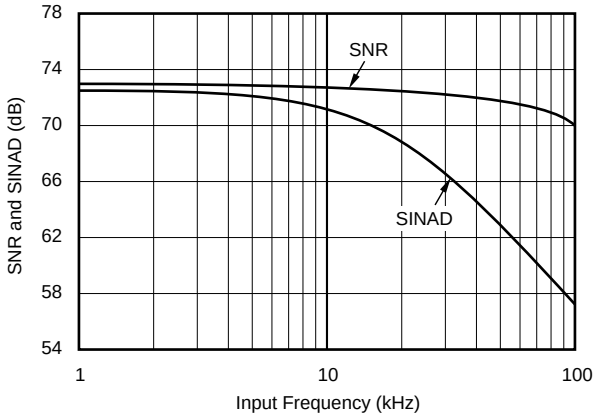
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



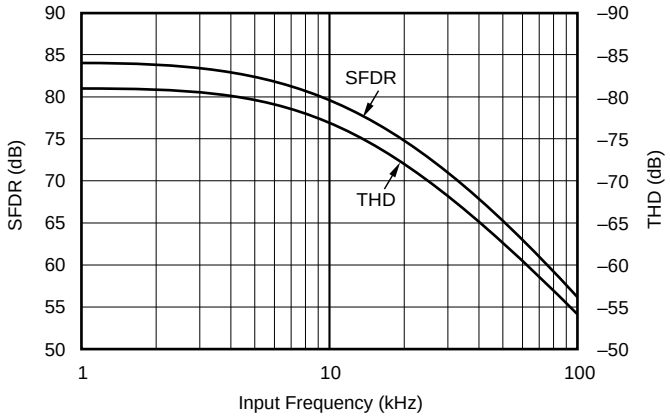
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



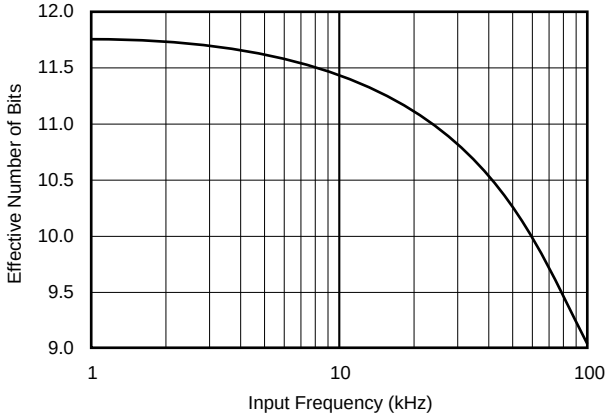
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE + DISTORTION) vs INPUT FREQUENCY



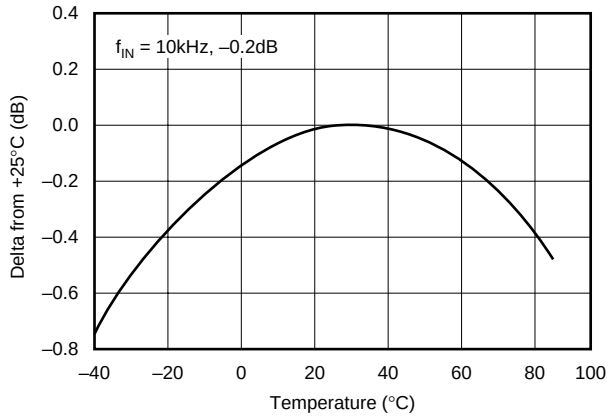
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



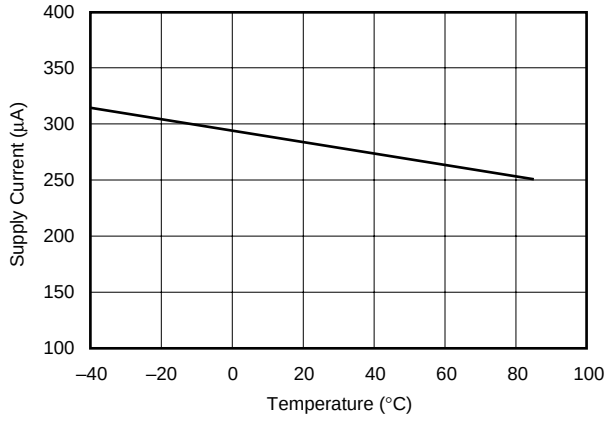
CHANGE IN SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



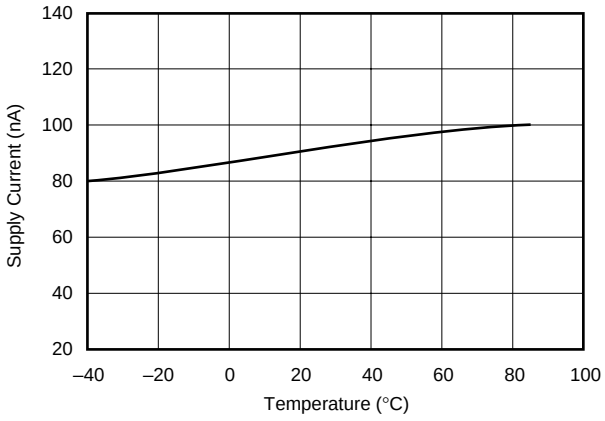
TYPICAL CHARACTERISTICS: +2.7V (Continued)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

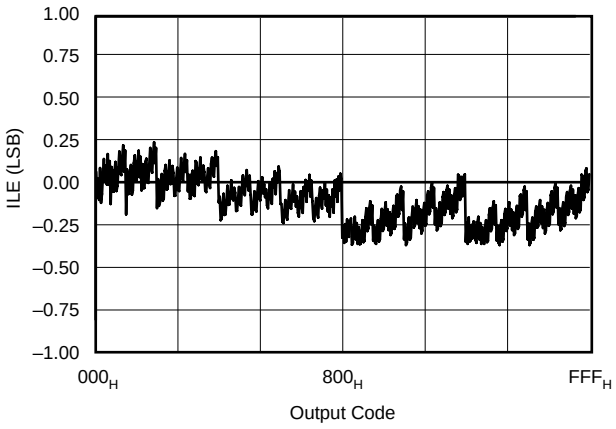
SUPPLY CURRENT vs TEMPERATURE



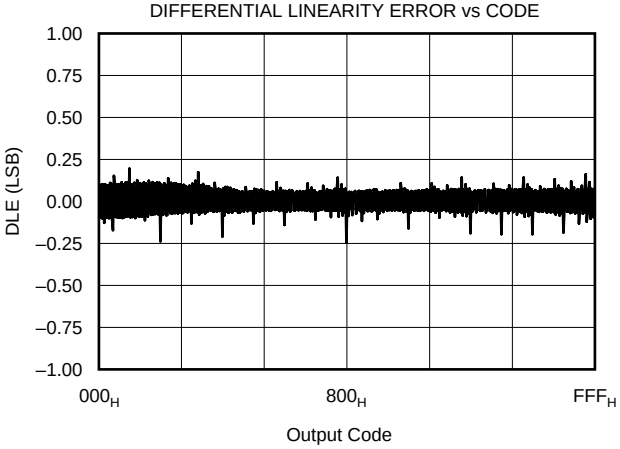
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



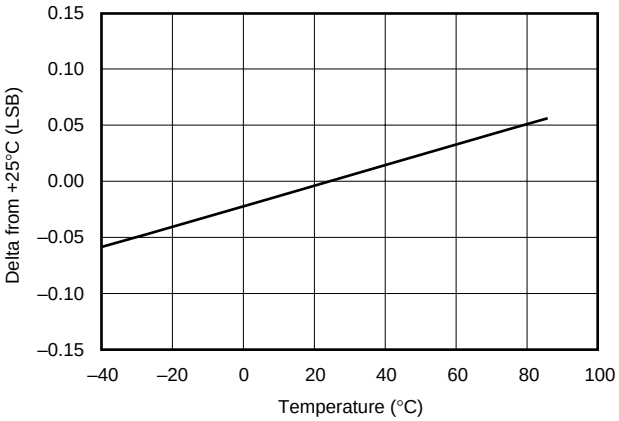
INTEGRAL LINEARITY ERROR vs CODE



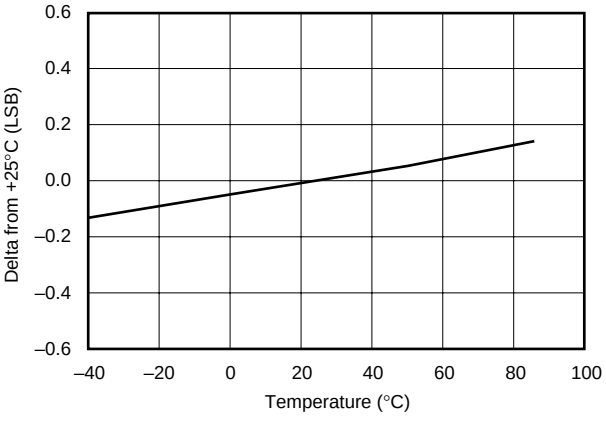
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



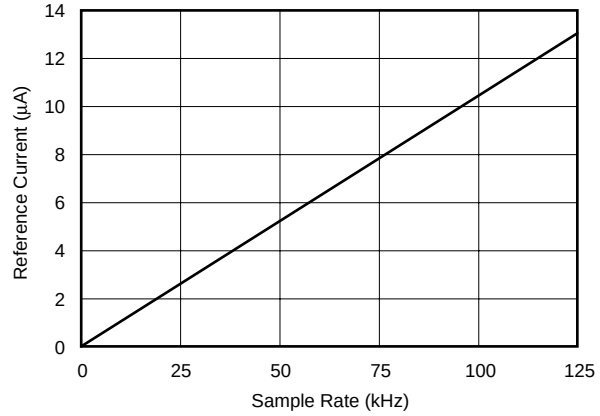
CHANGE IN OFFSET vs TEMPERATURE



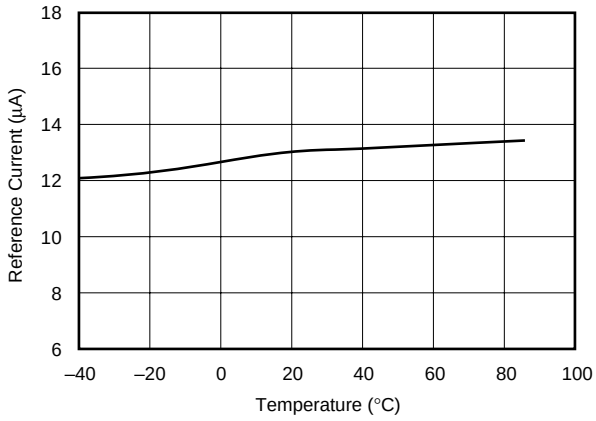
TYPICAL CHARACTERISTICS: +2.7V (Continued)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

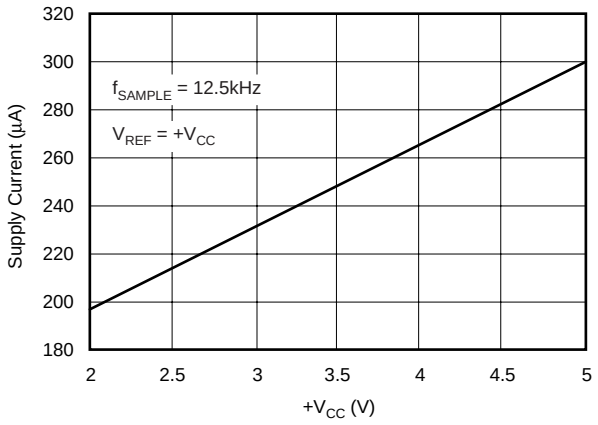
REFERENCE CURRENT vs SAMPLE RATE



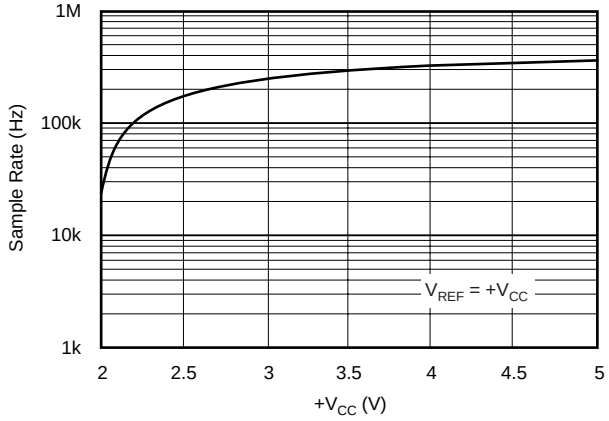
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7842 is a classic SAR ADC. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the ADS7842 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7842.

ANALOG INPUTS

The ADS7842 features four, single-ended inputs. The input current into each analog input depends on input voltage and sampling rate. Essentially, the current into the device must charge the internal hold capacitor during the sample period. After this capacitance has fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the same period, which can be as little as 350ns in some operating modes. While the converter is in the hold mode, or after the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

EXTERNAL CLOCK

The ADS7842 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5kHz throughput) and 3.2MHz (200kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 150ns and the clock period is at least 300ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7842.

BASIC OPERATION

Figure 1 shows the simple circuit required to operate the ADS7842 with Channel 0 selected. A conversion can be initiated by bringing the $\overline{WR}$ pin (pin 22) LOW for a minimum of 25ns. $\overline{BUSY}$ (pin 23) will output a LOW during the conversion process and rises only after the conversion is complete. The 12 bits of output data will be valid on pins 7-13 and 15-19 following the rising edge of $\overline{BUSY}$.

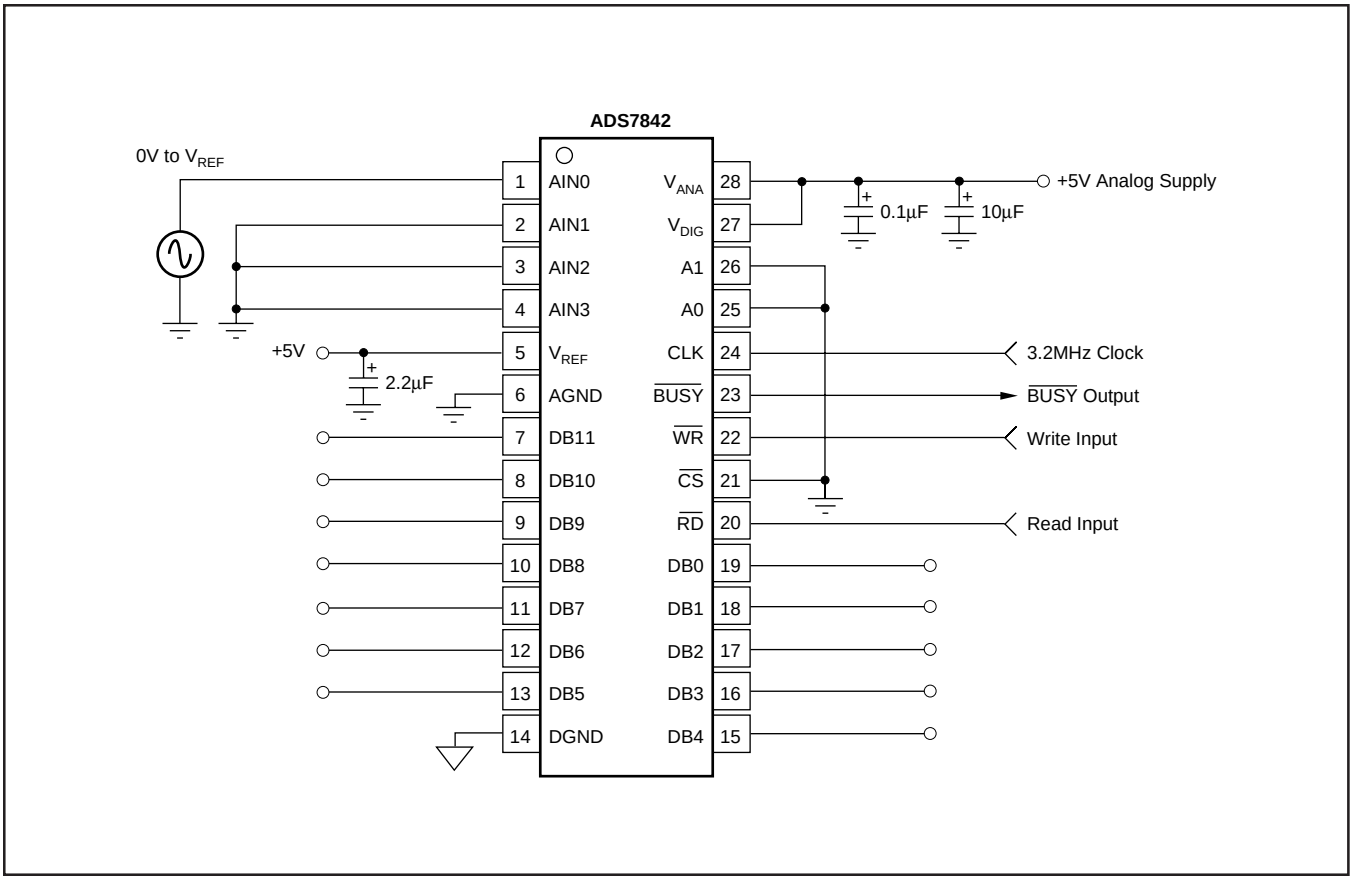


FIGURE 1. Basic Operation of the ADS7842.

STARTING A CONVERSION

A conversion is initiated on the falling edge of the $\overline{WR}$ input, with valid signals on A0, A1, and $\overline{CS}$. The ADS7842 will enter the conversion mode on the first rising edge of the external clock following the $\overline{WR}$ pin going LOW. The ADS7842 will start the conversion on the 1st clock cycle. The MSB will be approximated by the Capacitive Digital-to-Analog Converter (CDAC) on the 1st clock cycle, the 2nd-MSB on the 2nd cycle, and so on until the LSB has been decided on the 12th clock cycle. The $\overline{BUSY}$ output will go LOW 20ns after the falling edge of the $\overline{WR}$ pin. The $\overline{BUSY}$ output will return HIGH just after the ADS7842 has finished a conversion and the data will be valid on pins 7-13, 15-19. The rising edge of $\overline{BUSY}$ can be used to latch the data. It is recommended that the data be read immediately after each conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance. See Figure 2.

READING DATA

Data from the ADS7842 will appear at pins 7-13 and 15-19. The MSB will output on pin 7 while the LSB will output on pin 19. The outputs are coded in Straight Binary (with 0V = 000_H and V_{REF} = FFF_H, see Table IV). Following a conversion, the $\overline{BUSY}$ pin will go HIGH. After $\overline{BUSY}$ goes HIGH, the $\overline{CS}$ and $\overline{RD}$ pins may be brought LOW to enable the 12-bit output bus. $\overline{CS}$ and $\overline{RD}$ must be held LOW for at least 25ns seconds following $\overline{BUSY}$ HIGH. Data will be valid 25ns seconds after the falling edge of both $\overline{CS}$ and $\overline{RD}$. The output data will remain valid for 25ns seconds following the rising edge of both $\overline{CS}$ and $\overline{RD}$. See Figure 4 for the read cycle timing diagram.

POWER-DOWN MODE

The ADS7842 incorporates a unique method of placing the ADC in the power-down mode. Rather than adding an extra pin to the package, the A0 address pin is used in conjunction with the $\overline{RD}$ pin to place the device in power-down mode and also to 'wake-up' the ADC following power-down. In this shutdown mode, all analog and digital circuitry is turned off. The simplest way to place the ADS7842 in power-down mode is immediately following a conversion. After a conversion has been completed and the $\overline{BUSY}$ output has returned HIGH, $\overline{CS}$ and $\overline{RD}$ must be brought LOW for a minimum of 25ns. While keeping $\overline{CS}$ LOW, $\overline{RD}$ is brought HIGH and the ADS7842 enters the power-down mode, provided the A0 pin is HIGH (see Figure 5 and Table III). In order to 'wake-up' the device following power-down, A0 must be LOW when $\overline{RD}$ switches from LOW to HIGH a second time (see Figure 6).

The typical supply current of the ADS7842 with a 5V supply and 200kHz sampling rate is 550µA. In the power-down mode the current is typically reduced to 3µA.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			6.5	µs
t_{ACQ}	Acquisition Time			1.5	µs
t_{CKP}	Clock Period	500			ns
t_{CKL}	Clock LOW	150			ns
t_{CKH}	Clock HIGH	150			ns
t_1	$\overline{CS}$ to $\overline{WR}$/$\overline{RD}$ Setup Time	0			ns
t_2	Address to $\overline{CS}$ Hold Time	0			ns
t_3	$\overline{CS}$ LOW	25			ns
t_4	CLK to $\overline{WR}$ Setup Time	25			ns
t_5	$\overline{CS}$ to $\overline{BUSY}$ LOW			20	ns
t_6	CLK to $\overline{WR}$ LOW	5			ns
t_7	CLK to $\overline{WR}$ HIGH	25			ns
t_8	$\overline{WR}$ to CLK HIGH	25			ns
t_9	Address Hold Time	5			ns
t_{10}	Address Setup Time	5			ns
t_{11}	$\overline{BUSY}$ to $\overline{RD}$ Delay	0			ns
t_{12}	CLK LOW to $\overline{BUSY}$ HIGH	10			ns
t_{13}	BUS Access	25			ns
t_{14}	BUS Relinquish	25			ns
t_{15}	Address to $\overline{RD}$ HIGH	2			ns
t_{16}	Address Hold Time	2			ns
t_{17}	$\overline{RD}$ HIGH to CLK LOW	50			ns

TABLE I. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			3.5	µs
t_{ACQ}	Acquisition Time			1.5	µs
t_{CKP}	Clock Period	300			ns
t_{CKL}	Clock LOW	150			ns
t_{CKH}	Clock HIGH	150			ns
t_1	$\overline{CS}$ to $\overline{WR}$/$\overline{RD}$ Setup Time	0			ns
t_2	Address to $\overline{CS}$ Hold Time	0			ns
t_3	$\overline{CS}$ LOW	25			ns
t_4	CLK to $\overline{WR}$ Setup Time	25			ns
t_5	$\overline{CS}$ to $\overline{BUSY}$ LOW			20	ns
t_6	CLK to $\overline{WR}$ LOW	5			ns
t_7	CLK to $\overline{WR}$ HIGH	25			ns
t_8	$\overline{WR}$ to CLK HIGH	25			ns
t_9	Address Hold Time	5			ns
t_{10}	Address Setup Time	5			ns
t_{11}	$\overline{BUSY}$ to $\overline{RD}$ Delay	0			ns
t_{12}	CLK LOW to $\overline{BUSY}$ HIGH	10			ns
t_{13}	BUS Access	25			ns
t_{14}	BUS Relinquish	25			ns
t_{15}	Address to $\overline{RD}$ HIGH	2			ns
t_{16}	Address Hold Time	2			ns
t_{17}	$\overline{RD}$ HIGH to CLK LOW	50			ns

TABLE II. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	$\overline{BUSY}$	A0	A1	COMMENTS
0	↓	X	1	1	X	Power-Down Mode
0	↓	X	1	0	X	Wake-Up Mode
↓ means rising edge triggered. X = Don't care.						

TABLE III. Truth Table for Power-Down and Wake-Up Modes.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Least Significant Bit (LSB)	1.2207mV		
Full-Scale	4.99878V	1111 1111 1111	FFF
Midscale	2.5V	1000 0000 0000	800
Midscale –1LSB	2.49878V	0111 1111 1111	7FF
Zero Full-Scale	0V	0000 0000 0000	000

TABLE IV. Ideal Input Voltages and Output Codes (V_{REF} = 5V).

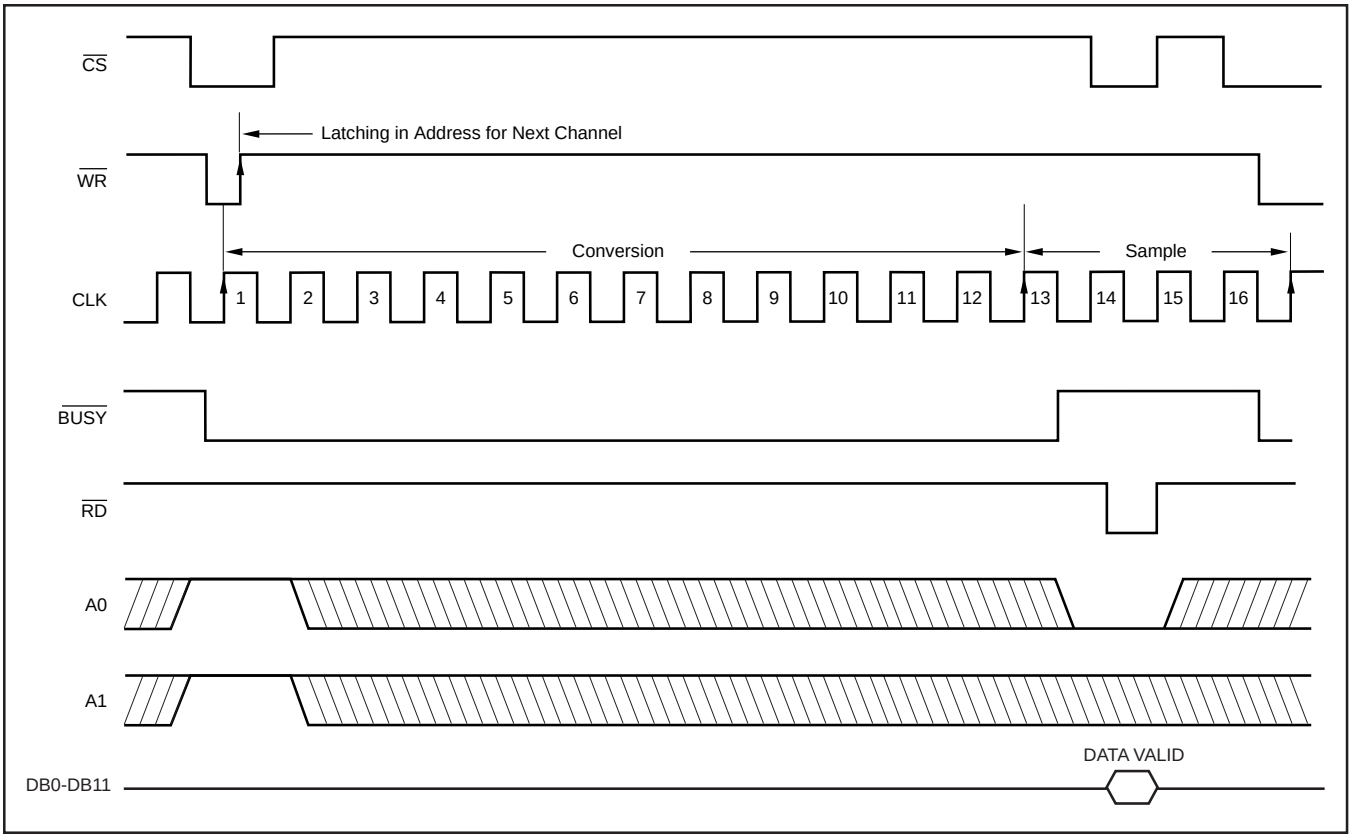
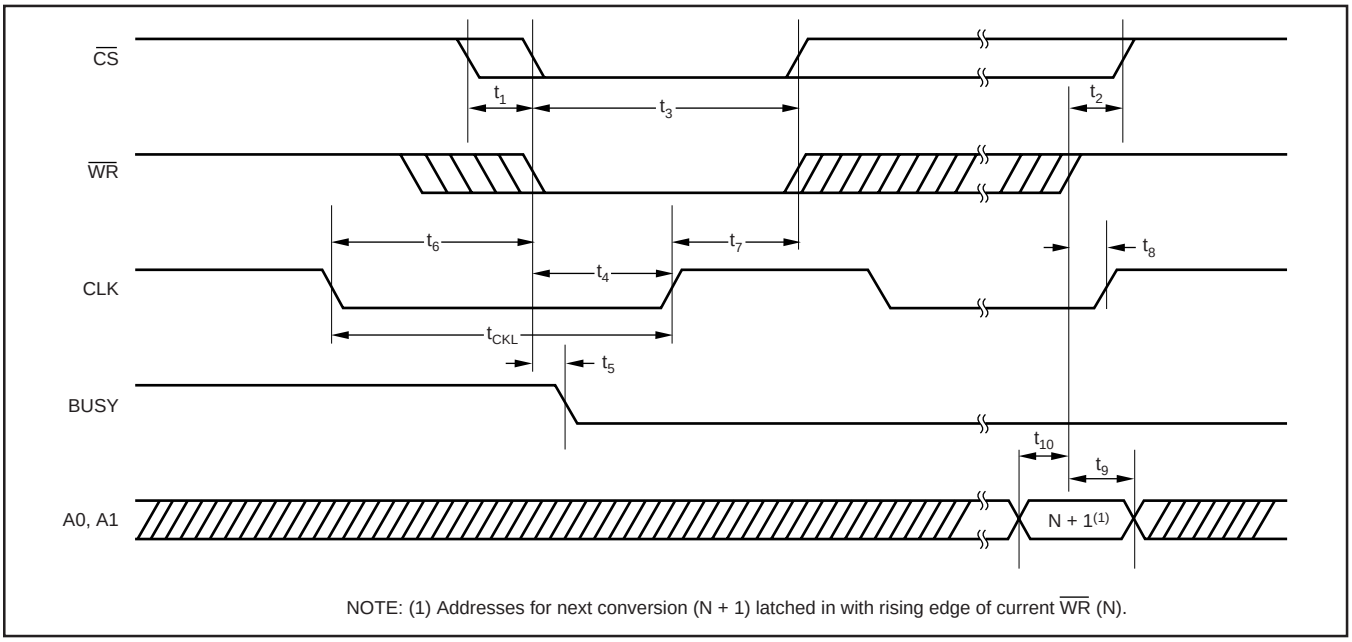
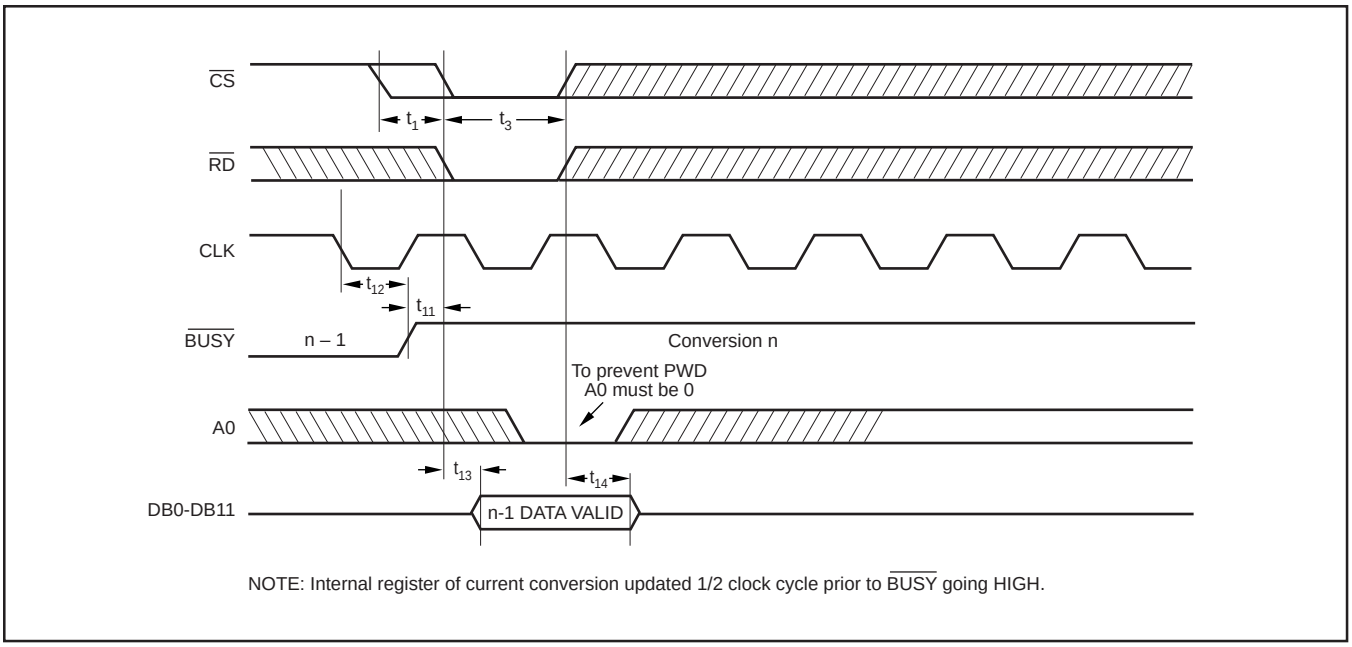


FIGURE 2. Normal Operation, 16 Clocks per Conversion.



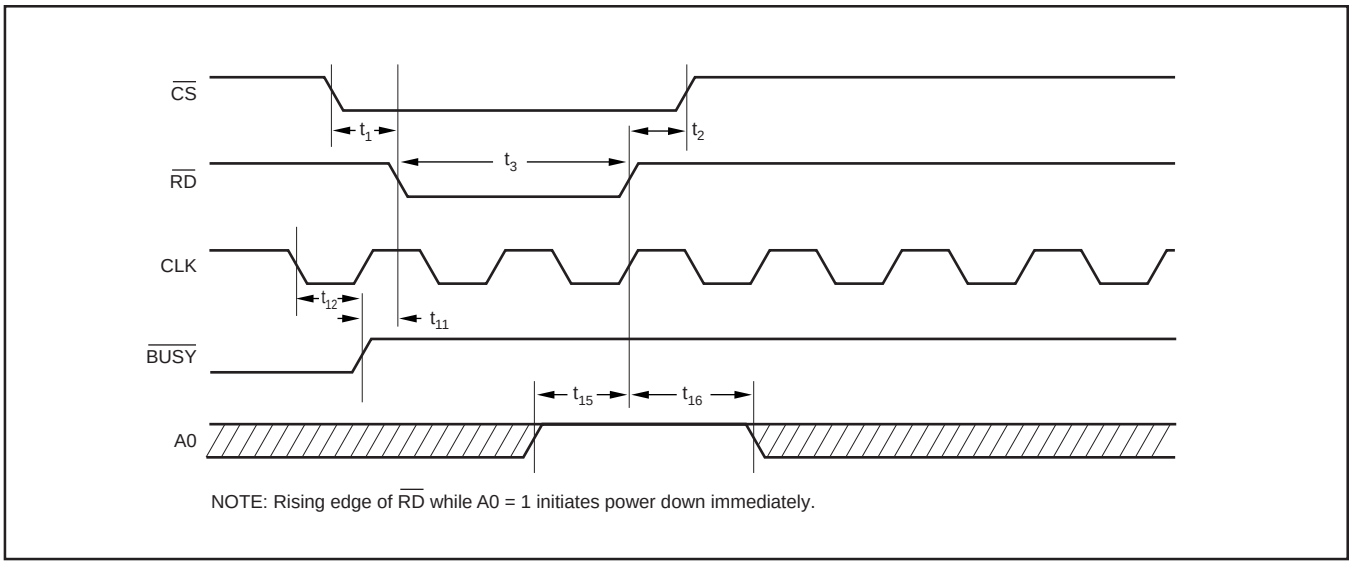
NOTE: (1) Addresses for next conversion (N + 1) latched in with rising edge of current $\overline{WR}$ (N).

FIGURE 3. Initiating a Conversion.



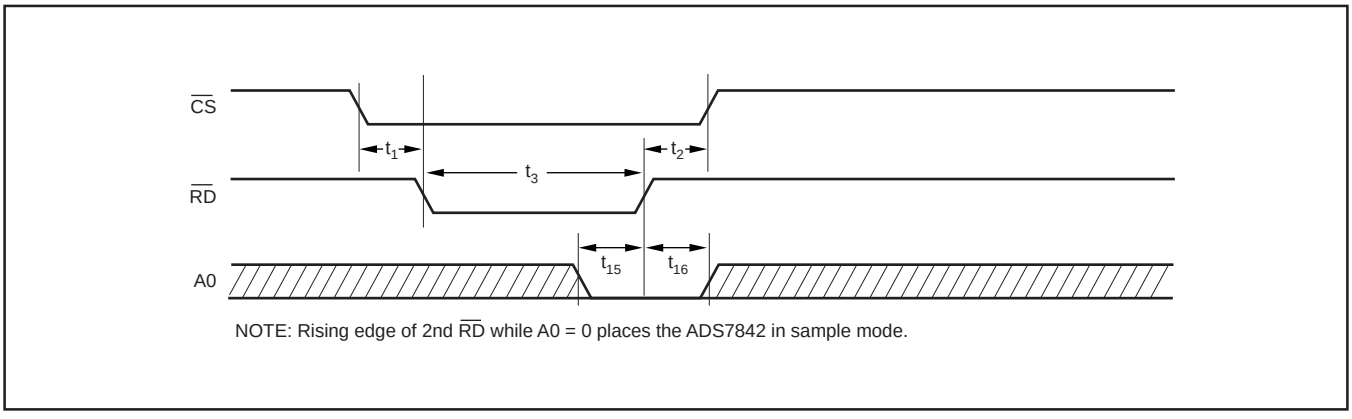
NOTE: Internal register of current conversion updated 1/2 clock cycle prior to $\overline{BUSY}$ going HIGH.

FIGURE 4. Read Timing Following a Conversion.



NOTE: Rising edge of $\overline{RD}$ while A0 = 1 initiates power down immediately.

FIGURE 5. Entering Power-Down Using $\overline{RD}$ and A0.



NOTE: Rising edge of 2nd $\overline{RD}$ while A0 = 0 places the ADS7842 in sample mode.

FIGURE 6. Initiating Wake-Up Using $\overline{RD}$ and A0.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7842 will operate with a reference in the range of 100mV to $+V_{CC}$.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, then it will typically be 10LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the CDAC portion of the ADS7842. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

Data Format

The ADS7842 output data is in Straight Offset Binary format, see Table IV. This table shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7842 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7842 should be clean and well bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1μF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7842 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of CLK during a conversion).

The ADS7842 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/06	C	4	Electrical Characteristics	Dynamic Characteristics—total harmonic distortion: added new conditions.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7842E	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7842E	Samples
ADS7842E/1K	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		ADS7842E	Samples
ADS7842EB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		ADS7842E B	Samples
ADS7842EB/1K	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		ADS7842E B	Samples
ADS7842EG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7842E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

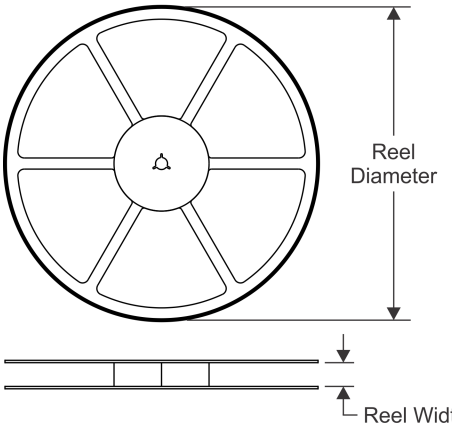
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

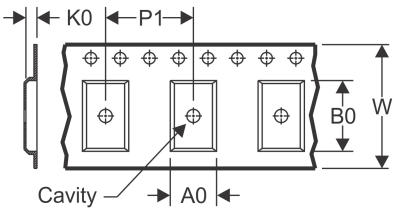
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

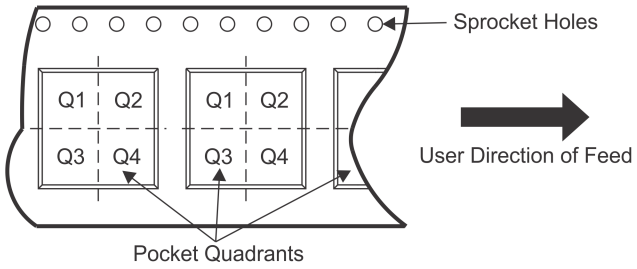


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

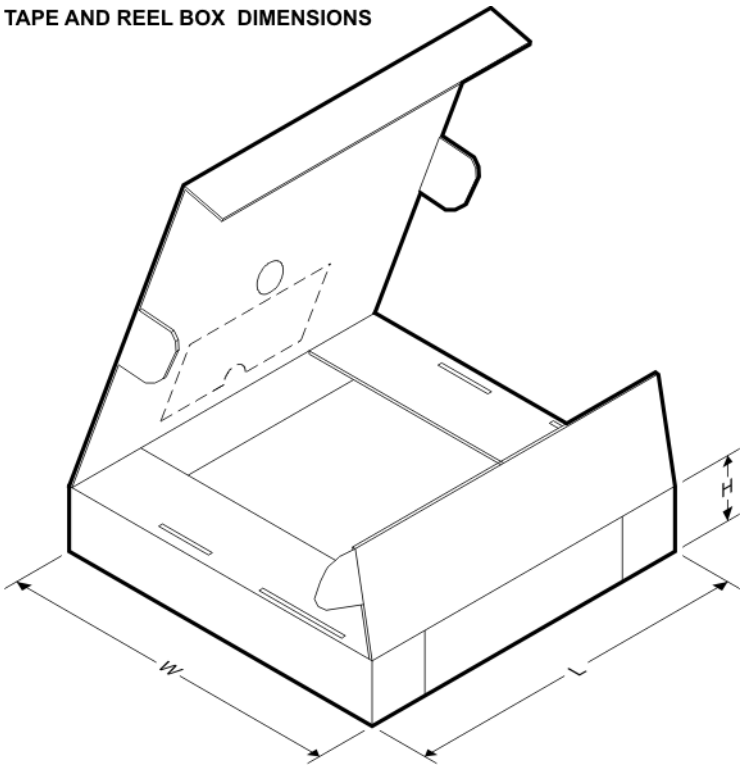
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7842E/1K	SSOP	DB	28	1000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
ADS7842EB/1K	SSOP	DB	28	1000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

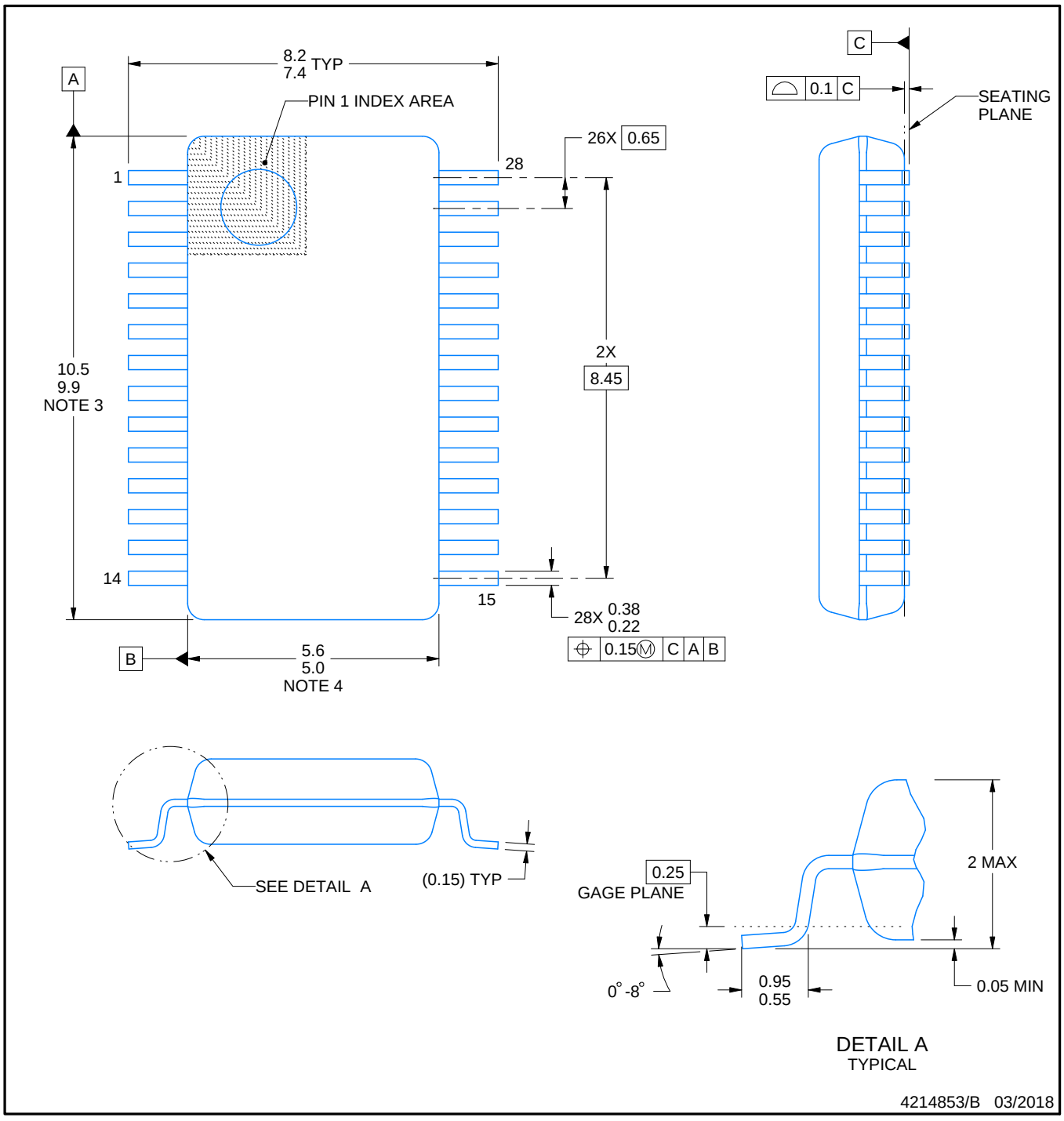
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7842E/1K	SSOP	DB	28	1000	367.0	367.0	38.0
ADS7842EB/1K	SSOP	DB	28	1000	367.0	367.0	38.0

PACKAGE OUTLINE

DB0028A

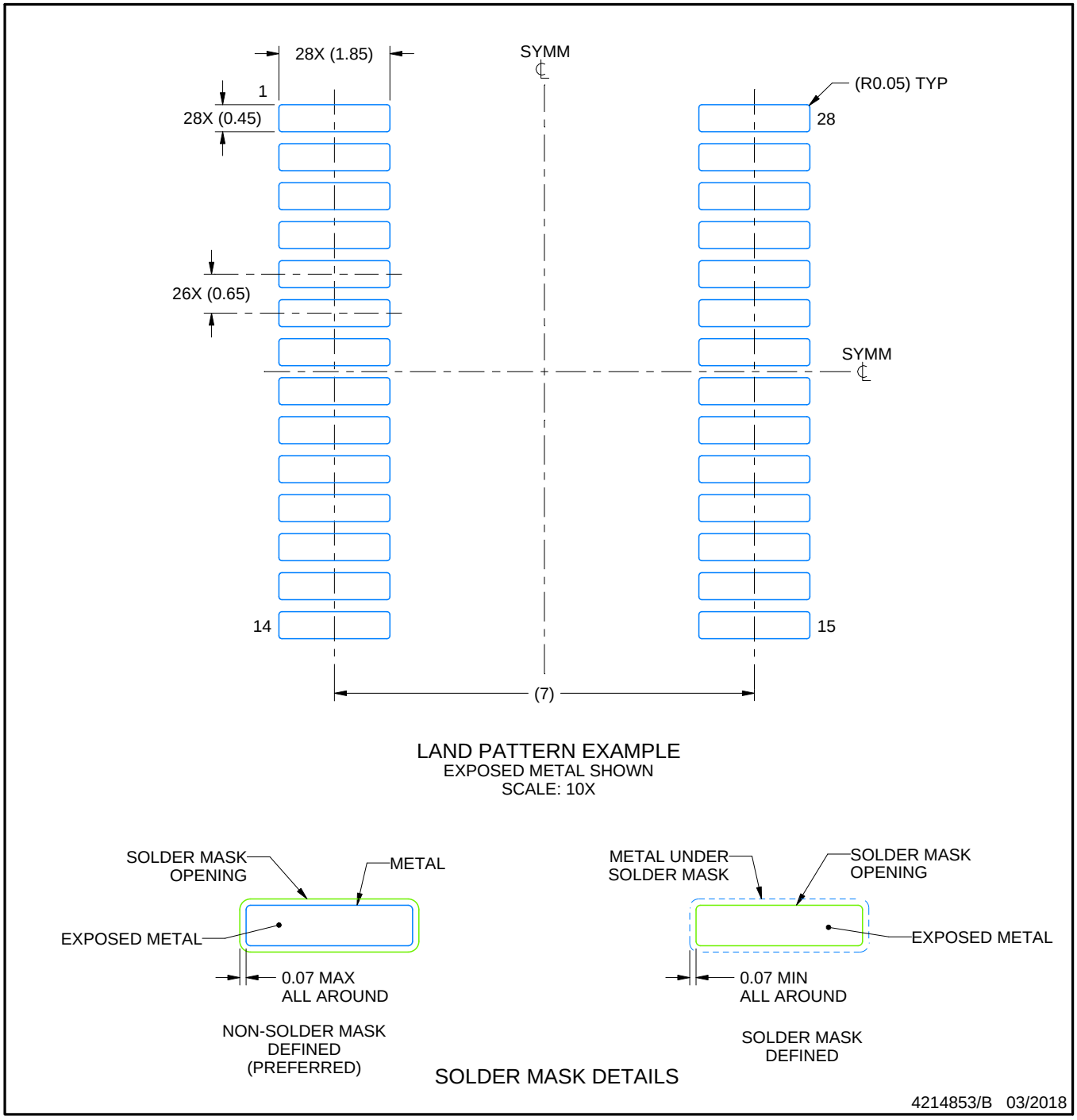
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



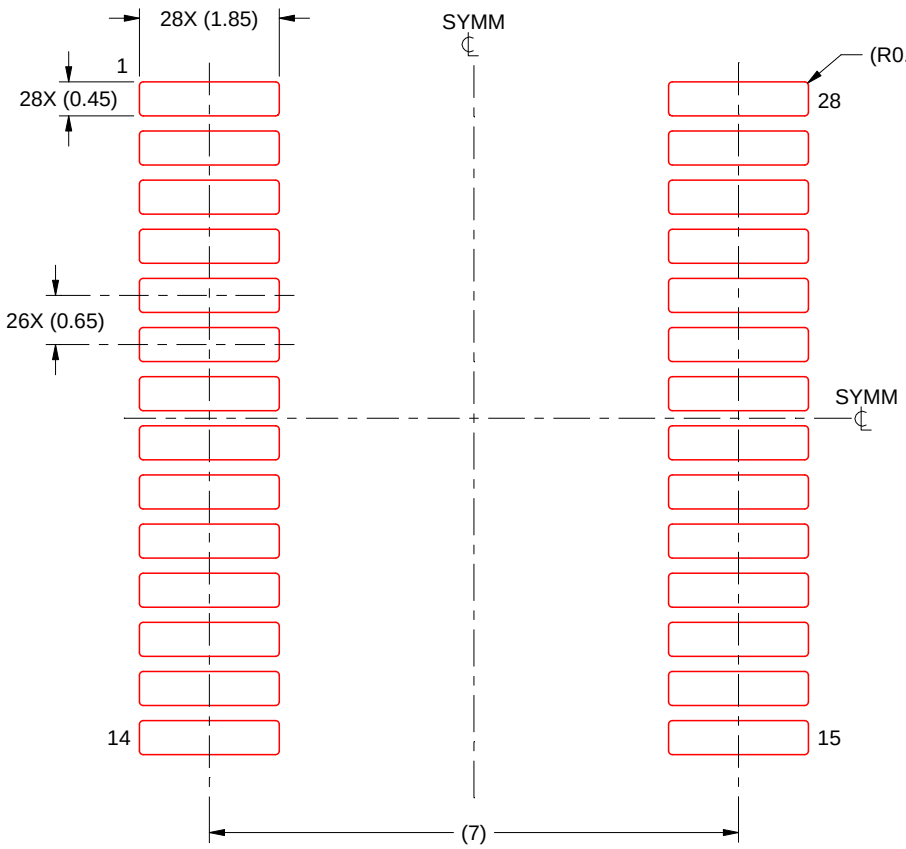
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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