ADS58J64 EVM

The ADS58J64EVM device is an evaluation board used to evaluate the ADS58J64 Integrated Receiver from TI. This User's Guide is intended to guide users through setting up and evaluating the ADC for the best performance.

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1 Overview

This evaluation board includes the following important features:

- Transformer-coupled signal input network, allows a single-ended signal source to the EVM.
- LMK04828, a system clock generator, generates the FPGA reference clock for the high-speed serial interface.
- Default transformer-coupled clock input network, tests the receiver performance with a very low-noise clock.
- High-speed serial data output over a standard FMC connector.
- Device registers programming through a USB connector and FTDI USB-to-SPI bus translator.

The ADS58J64EVM device is designed to work seamlessly with the TSW14J56EVM device, the JESD204B data-capture card from TI, and the High-Speed Data Converter Pro (HSDCPro) software tool. The ADS58J64EVM device is also compatible with many of the development kits from leading FPGA vendors that contain an FMC connector.

1.1 Required Hardware

The EVM evaluation kit includes the following equipment:

- ADS58J64EVM Evaluation Board (EVM)
- Mini-USB cable

The EVM evaluation kit *does not* include the following list of equipment, but these items are required for evaluation of this product, to achieve the best performance.

- 5-V DC power supply
- TSW14J56EVM data capture board, 5-V power supply, and Mini-USB cable
- Computer running Windows® 8, Windows 7, or Windows XP operating system
- Two low-noise signal generators
  - Recommendations: RF generator, > 17 dBm, < –40 dBc harmonics, < 500 fs jitter 20 k – 20 MHz, and 10 MHz to 2 GHz frequency range
  - Examples: TSW2170EVM, HP® HP8644B, and Rohde & Schwarz® SMA100A
- Bandpass filter for analog input (between 50 MHz to 500 MHz).
  - Recommendations: bandpass filter, ≥ 60 dB harmonic attenuation, ≤ 5% bandwidth, > 18 dBm power, and < 5 dB insertion loss
  - Examples: Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6, or KC7-series Fixed BPF
- Bandpass filter for clock input (various frequencies)
  - Recommendations: bandpass filter, ≥ 60 dB harmonic attenuation, ≤ 5% bandwidth, > 18 dBm power, <5 dB insertion loss
  - Examples: Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
- Signal path cables, SMA or BNC with BNC-to-SMA adapters
- 6 dB 50-Ω attenuator

1.2 Required Software

The following software is required and available online.

- To operate the ADS58J64EVM device: ADS58J64EVM_GUI_Installer.zip
- To operate the TSW14J56EVM device: High Speed Data Converter Pro software

See Section 1.4 for the software links.

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1.3 Evaluation Board Feature Identification Summary

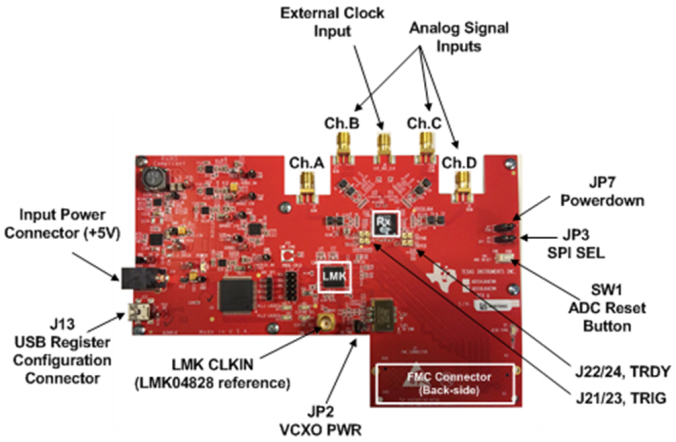


Figure 1. EVM Feature Locations

1.4 References

- ADS58J64EVM GUI software, schematics, layout, BOM
- ADS58J64 Data Sheet
- LMK04828 Data Sheet
- TSW14J56EVM User's Guide
- High-Speed Data Converter Pro User's Guide

2 Quick Start Guide

This section guides users through the EVM test procedure for obtaining a valid data capture from the ADS58J64EVM device, using the TSW14J56EVM capture card. This step is the starting point for all evaluations.

2.1 Software Installation

The proper software must be installed before beginning the evaluation. See Section 1.2 for a list of the required software. Section 1.4 of this document contains links to the required software on the TI website.

NOTE: The software must be installed before connecting the ADS58J64EVM and TSW14J56EVM devices to the computer for the first time.

2.1.1 ADS58J64 GUI Installation

The ADS58J64 GUI is used to control the ADS58J64EVM device. The GUI must be used to properly configure the devices on the EVM.

1. Download the GUI from ti.com.

NOTE: For pre-released EVMs, obtain the GUI from the local Field Applications contact.

2. Extract the files from the zip file.
3. Run setup.exe and follow the installation prompts.

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2.1.2 High-Speed Data Converter Pro GUI Installation

High-Speed Data Converter Pro (HSDC Pro) is used to control the TSW14J56EVM and analyze the captured data. Please see the HSDC Pro user's guide for more information.

1. Download HSDC Pro from the TI website. Section 1.2 contains the link to find the software on the TI website.
2. Extract the files from the zip file.
3. Run setup.exe and follow the installation prompts.

2.2 Hardware Setup Procedure

Figure 2 shows a typical test setup using the ADS58J64EVM and TSW14J56EVM REV D devices. This test setup is used for the quick start procedure. The rest of this section describes the hardware setup steps.

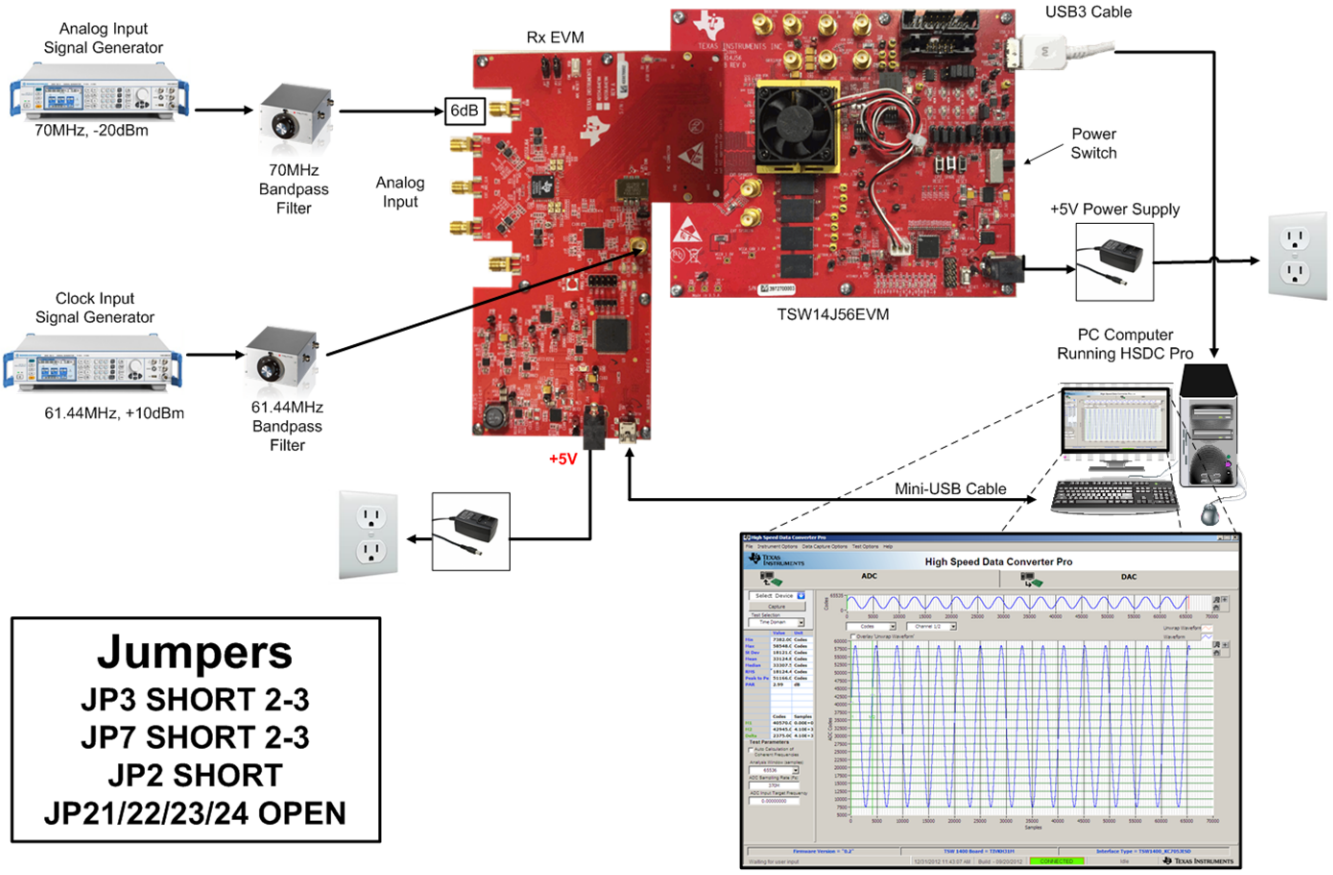


Figure 2. Quick Start Test Setup

2.2.1 TSW14J56EVM Setup

Set up the TSW14J56EVM device by following these instructions.

1. Connect the ADS58J64EVM device to the TSW14J56EVM device using the FMC connectors.
2. Connect the included 5-V power supply to connector J11 (5-V IN) of the TSW14J56EVM device.
3. Connect the included mini-USB cable to the USB connector (J9) of the TSW14J56EVM device.
4. Move the power switch (SW6) of the TSW14J56EVM device to the *on* position.

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2.2.2 ADS58J64EVM Setup

Set up the ADS58J64EVM device by following these instructions.

1. Connect the included 5-V power supply to the PWR IN (J14) connector.
2. Verify that JP7 and JP3 and are shorted at positions 2 – 3.
3. Verify that JP2 is shorted.
4. Connect the included mini-USB cable to the USB connector (J13).
5. Set the clock input signal generator for 61.44 MHz and 10 dBm.
6. Connect the Clock Signal generator to the LMK_CLK_IN (J12) connector.
7. Place the bandpass filter between the signal generator and the connector, to remove noise from the signal.
8. Set the analog input signal generator for 70 MHz and –20 dBm.
9. Connect the 6 dB attenuator to the DIN (J5) input.
10. Connect the Analog Input Signal generator to the 6 dB attenuator.
11. Place the bandpass filter between the analog signal generator and the attenuator input, to remove noise and harmonics from the signal generator.
12. Turn on all signal generators.

2.3 Software Setup Procedure

The software can be opened and configured once the hardware is properly set up.

2.3.1 ADS58J64 GUI Configuration

Set up the ADS58J64EVM GUI by following these instructions.

1. Open the ADS58J64EVM GUI from the Start Menu → All Programs → Texas Instruments → ADS58J64 EVM
2. After the GUI starts, verify that the green USB Status indicator in the top right corner of the GUI is lit.
3. From the INTRO tab, press the Configure LMK04828 button that corresponds to the desired sampling rate. To quickly evaluate device performance and check EVM functionality, the ADS58J64 EVM GUI has two sampling rate options to choose from, 983.04 MHz and 737.28 MHz.
4. Press the ADC_RESET (SW1) button on the ADS58J64EVM device.
5. Press the Configure ADS58J64 button that corresponds to the sampling rate selected in step .
6. Press the Disable LMK04828 SYSREF to ADC button.

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2.3.2 HSDC Pro GUI Configuration

Set up the HSDC Pro GUI by following these instructions.

1. Open High Speed Data Converter Pro from the Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro. Figure 3 shows the GUI main page.

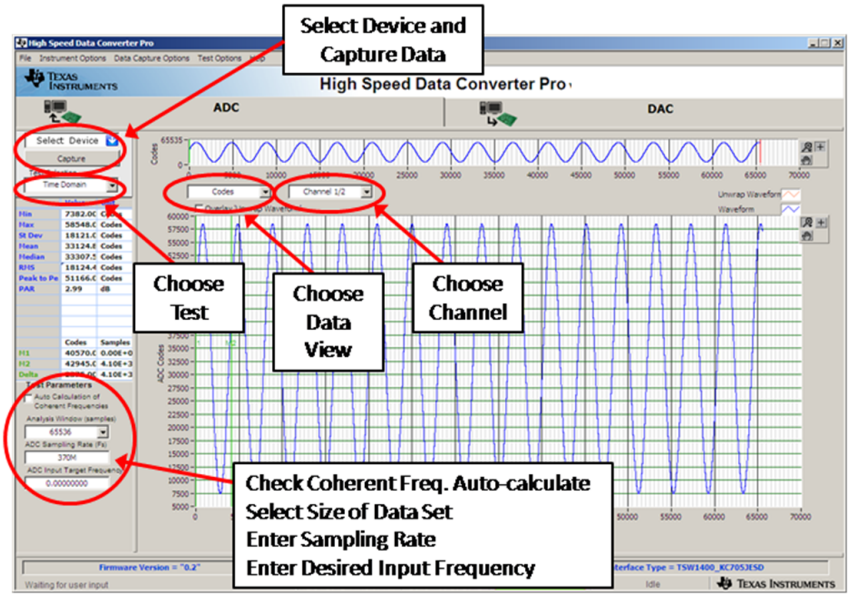


Figure 3. HSDC Pro GUI Main Panel

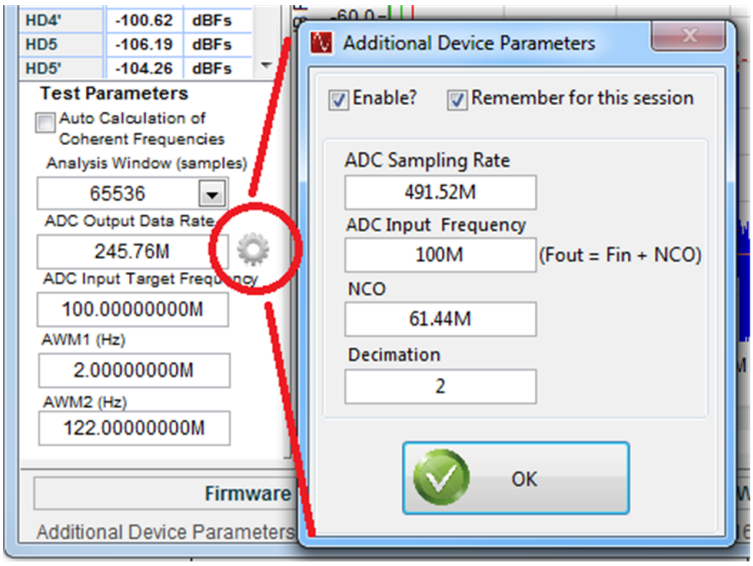


Figure 4. HSDC Pro Sampling Rate and Additional Device Parameters

2. When prompted to select the capture board, select the TSW14J56, whose serial number corresponds to the serial number on the TSW14J56EVM, and click OK.
3. Select the ADC tab at the top of the GUI.
4. Use the Select ADC drop-down menu in the top-left corner to select *ADS58J64_LMF_4841_mode01*.
5. When prompted to update the firmware for the ADC, click the Yes button, and wait for the firmware to download to the TSW14J56.

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6. Press the Additional Device Parameters symbol next to the ADC Output Data Rate (see Figure 4), and enter the following values, then press OK:
   - Check the Enable box.
   - ADC Sampling Rate = 491.52M
   - ADC Input Frequency = 70M
   - NCO = –122.88M
   - Decimation = 2
7. Press the CPU_RESET button on the TSW14J56EVM device.
8. Click the Instrument Options menu at the top of HSDC Pro, and select Reset Board.
9. Click Capture in HSDC Pro to capture data from the ADC.
10. In HSDCPRO, change the Test Selection to *Single Tone*.
11. Also in HSDCPRO, change the spectrum analysis from *Real FFT* to *Complex FFT*.
12. From the Test Options file menu, enable the *Analysis Window Markers*.
13. Set the of value of the Analysis Window markers in the lower left corner of the HSDC Pro window:
    - AWM1 = –120M
    - AWM2 = 120M
14. The results from the captured data of Channel 1 should resemble Figure 5, and the performance should be similar to Table 1. If this result was not achieved, then see Section 2.4 of this document.

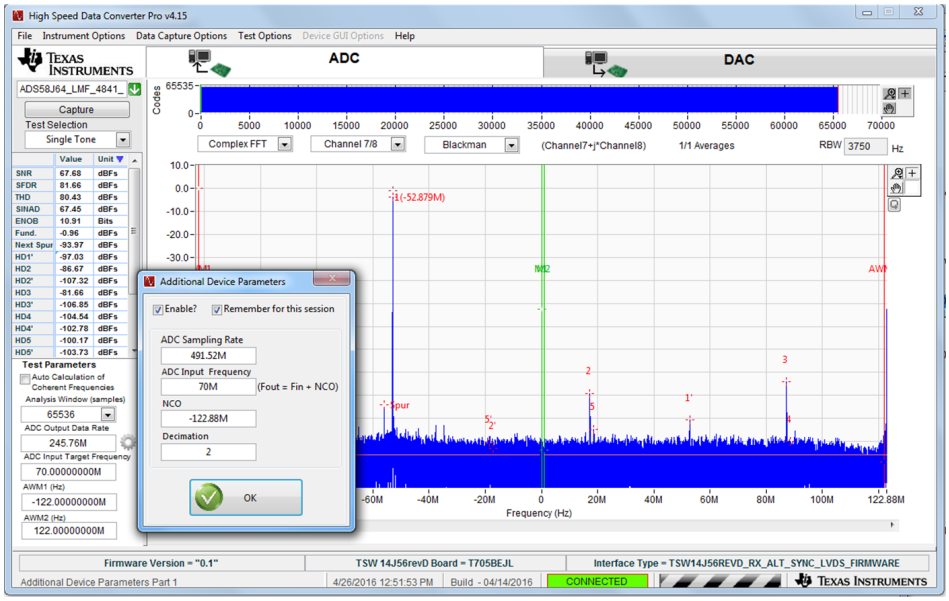


Figure 5. Data Capture Results from Quick Start Procedure

Table 1. Quick Start Performance Measurements

Result	Measured Value	Units
SNR	> 67	dBFS
SFDR	> 80	dBFS

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2.4 Quick Start Troubleshooting

Table 2 lists tips which can be used to assist with problems that may have occurred during the quick start procedure.

Table 2. Troubleshooting Tips

Issue	Troubleshooting Tips
General problems	Verify the test setup shown in Figure 2, and repeat the setup procedure as described in this document.
	Check power supplies to the EVM and TSW14J56EVM. Verify that the power switches are in the ON position.
	Check signal and clock connections to the EVM.
	Check that all boards are properly connected together.
	Try pressing the CPU_RESET button on the TSW14J56EVM.
	Try power-cycling the external power supply to the EVM and reprogram the LMK and ADC devices.
TSW14J56 LEDs are incorrect: D1, D5 – N/A D2, D4 – Flashing D3, D6, D7 – OFF D8, D28 – ON	Verify the settings of the configuration switches on the TSW14J56EVM.
	Verify that the EVM configuration GUI is communicating with the USB, and that the configuration procedure was followed.
	LEDs not flashing – reprogram the LMK device.
	Try pressing the CPU_RESET button on the TSW14J56EVM.
	Try capturing data in HSDC Pro to force an LED status update.
Device GUI is not working properly.	Verify that the USB cable is plugged into the EVM and the PC.
	Check the Device Manager of the computer, and verify that a *USB Serial Device* is recognized when the EVM is connected to the PC.
	Verify that the green *USB Status* LED light in the top-right corner of the GUI is lit. If the LED is not lit, press the Reconnect FTDI button.
	Try restarting the configuration GUI.
	Check default jumper connections as shown in Appendix A.
HSDC Pro Software is not capturing good data or analysis results are incorrect.	Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable, and that the board serial number is properly identified by the HSDP software.
	Check that the proper ADC device is selected. In default conditions, *ADS58J64_LMF_4841_mode01* must be selected.
	Check that the analysis parameters are properly configured.
HSDP Software gives a time-out error when capturing data.	Try to reprogram the LMK device and reset the JESD204 Link.
	Verify that the ADC sampling rate is correct in the HSDC Pro software.
Sub-optimal measured performance	Try pressing the Calibrate ADC button on the INTRO tab, to repeat the configuration GUI procedure for programming the EVM
	Check that the spectral analysis parameters are properly configured.
	Verify that bandpass filters are used in the clock and input signal paths, and that low-noise signal sources are used.

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3 Optimizing Evaluation Results

This section is meant to assist users in optimizing performance during evaluation of the product.

3.1 ADS58J64 Operating Mode

The ADS58J64 device may operate in eight different modes: Mode 0 through Mode 8 (excluding Mode 5). Each mode may require a different device selection in HSDC Pro, device configuration script in the ADS58J64 EVM GUI, and different sampling rate setup in HSDC Pro to operate correctly.

Table 3 shows the HSDC Pro sampling rate setup. The desired mode is selected from the ADS58J64EVM GUI → Mode tab in the configuration GUI.

Table 3. HSDC Pro ADC Output Data Rate

ADS58J64 Operating Mode	ADS58J64 Device Clock Frequency	HSDC Pro ADC Sampling Rate	Decimation	NCO
Mode 0	983.04 MHz	491.52M	2	–122.88M
	737.28 MHz	368.64M	2	–92.16M
Mode 1	983.04 MHz	491.52M	2	Depends on programmed NCO word
	737.28 MHz	368.64M	2	Depends on programmed NCO word
Mode 2	983.04 MHz	491.52M	2	0
	737.28 MHz	368.64M	2	0
Mode 3	983.04 MHz	491.52M	1	Depends on programmed NCO word
	737.28 MHz	368.64M	1	Depends on programmed NCO word
Mode 4	983.04 MHz	491.52M	2	Depends on programmed NCO word
	737.28 MHz	368.64M	2	Depends on programmed NCO word
Mode 6	Not yet supported.			
Mode 7[(1)]	983.04 MHz	491.52M	2	Depends on programmed NCO word
	737.28 MHz	368.64M	2	Depends on programmed NCO word
Mode 8	983.04 MHz	491.52M	1	0
	737.28 MHz	368.64M	1	0

(1) The ADC Sampling Rate used in HSDC Pro for Mode 7 depends on the .ini file used. The example shown here applies to selecting 'ADS58J64_LMF_4421_mode7' which strips the buffered 0s from the data stream.

For operating in a mode other that Mode 0, follow the default start-up procedure, and then perform the following:

1. From the ADS58J64 Mode tab in the configuration GUI, select the desired mode.
2. When selecting the device in HSDC Pro (), choose the device and enter the ADC Output Data Rate as reported by the configuration GUI on the ADS58J64 Mode tab.

Based on the sampling rate and mode of operation, adjust *ADC Output Rate Additional Device Parameters* to correctly label the harmonics. An example is shown in Figure 4 for Mode 0.

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3.2 LMK04828 Clocking Configuration

The sampling clock provided to the ADS58J64 device is generated by the LMK04828 device in the default EVM hardware configuration. Configuration scripts are provided with the Configuration GUI to set up the LMK04828 device in two different states, as shown in Table 4.

The states use the full PLL1 + PLL2 operation and use the onboard VCXO (Y1) for PLL1. If it is required to operate the LMK04828 device in clock distribution mode, the onboard VCXO must be disabled by removing the shorting jumper at JP2.

Table 4. LK04828 Macro States Provided in Configuration GUI

Macro State Script	LMK04828 Mode	ADS58J64 Device Clock Frequency	Clock Frequency Required at LMK_CLK_IN (J12)	Configuration GUI Shortcut	JP2
LMK04828_config2_737M.cfg	PLL1 + PLL2	737.26 MHz	61.44 MHz	Button on INTRO tab	Short
LMK04828_config2_983M.cfg	PLL1 + PLL2	983.04 MHz	61.44 MHz	Button on INTRO tab	Short
LMK04828_config1.cfg	Clock distribution	Equal to frequency at LMK_CLK_IN	Flexible	not available	Open

3.3 Using an External Clock

The LMK04828 device provides a very low-noise device clock, but the noise performance may not be as good as a premium bench RF signal generator, so the measured noise performance of the ADS58J64 device can be optimized by using an external signal generator as a clock source.

To provide the ADS58J64 device with an external clock (through EXT_ADC_CLK, J6 on the EVM), the following hardware changes must be performed on the EVM:

- Remove C47 and C48
- Place R35 and R39 with 0.1-µF 0402 capacitors.

The external clock is provided to the EVM through the J6 SMA connector at the full device clock rate (983.04 or 737.26 MHz), and amplitude of 6 dBm. This signal path must be filtered to reduce the broadband noise and remove any nonharmonic spurs. Narrow-band filters are recommended to remove as much noise as possible. If a signal generator output is used directly without filtering, significant degradation in SNR results.

A signal with the same frequency must also be provided to the LMK_CLK_IN J12 SMA connector with an amplitude of 6 dBm. If these signals are provided from different signal generators, the frequencies of the signals provided to J6 and J12 must be frequency locked together. Alternatively, a power splitter may be used to divide the signal from a single clock generator. When using an external clock, the LMK04828 device must be configured using the *LMK04828_config1.cfg* macro.

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Figure 6 shows the test setup using an external device clock source.

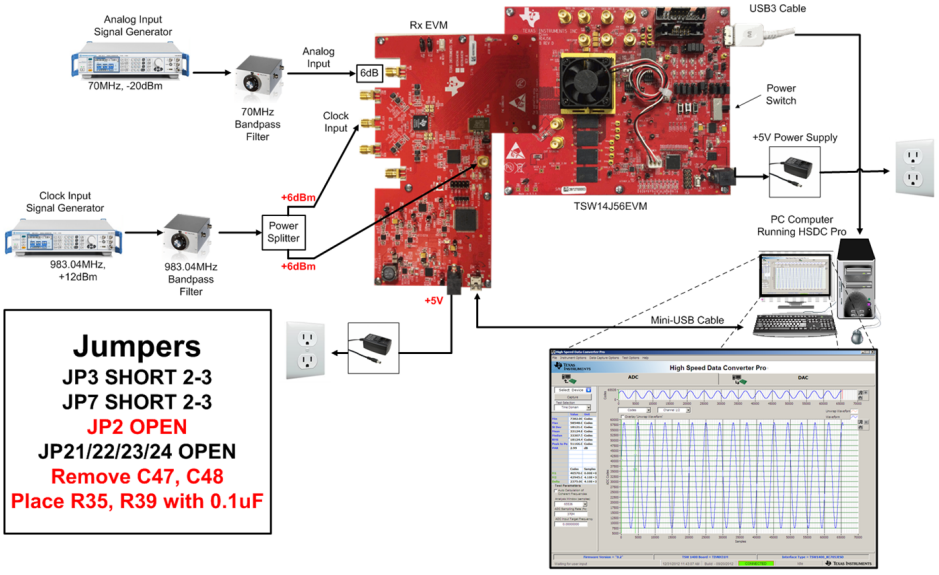


Figure 6. Test Setup Using an External Device Clock Source

3.4 Using a Coherent Input Source Frequency

A rectangular window function can be applied to the captured data when the sample rate and the input frequency are set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency). Coherent input and sampling frequencies may yield better SNR results. The clock and analog inputs must be frequency locked (such as through 10-MHz references) to achieve coherency.

3.5 HSDC Pro Settings

Table 5 lists the HSDC Pro options which can help improve the performance measurements.

Table 5. HSDC Pro Options for Optimal Analysis Results

HSDC Pro Feature	Description
Analysis window (samples)	Selects the number of samples to include in the selected test analysis. Collect more data to improve frequency resolution of FFT analysis.
Data windowing function	Select the desired windowing function applied to the data for FFT analysis. Select 'Blackman' when sampling a non-coherent input signal or 'Rectangle' when sampling a coherent input signal.
Test options → notch frequency bins	Select bins to be removed from the spectrum and back-filled with the average noise level. May also customize which Harmonics/Spurs are considered in SNR and THD calculations and select the method for calculating spur power.
Test options → analysis window markers	Enable markers to narrow the Single-Tone FFT test analysis to a specific bandwidth.
Data capture options → capture options	Configure the number of contiguous samples per capture (capture depth). May also enable Continuous Capture and FFT Averaging.

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4 Software Description

4.1 ADS58J64 GUI

Figure 7 shows the front page of the ADS58J64 GUI as it appears upon opening the GUI.

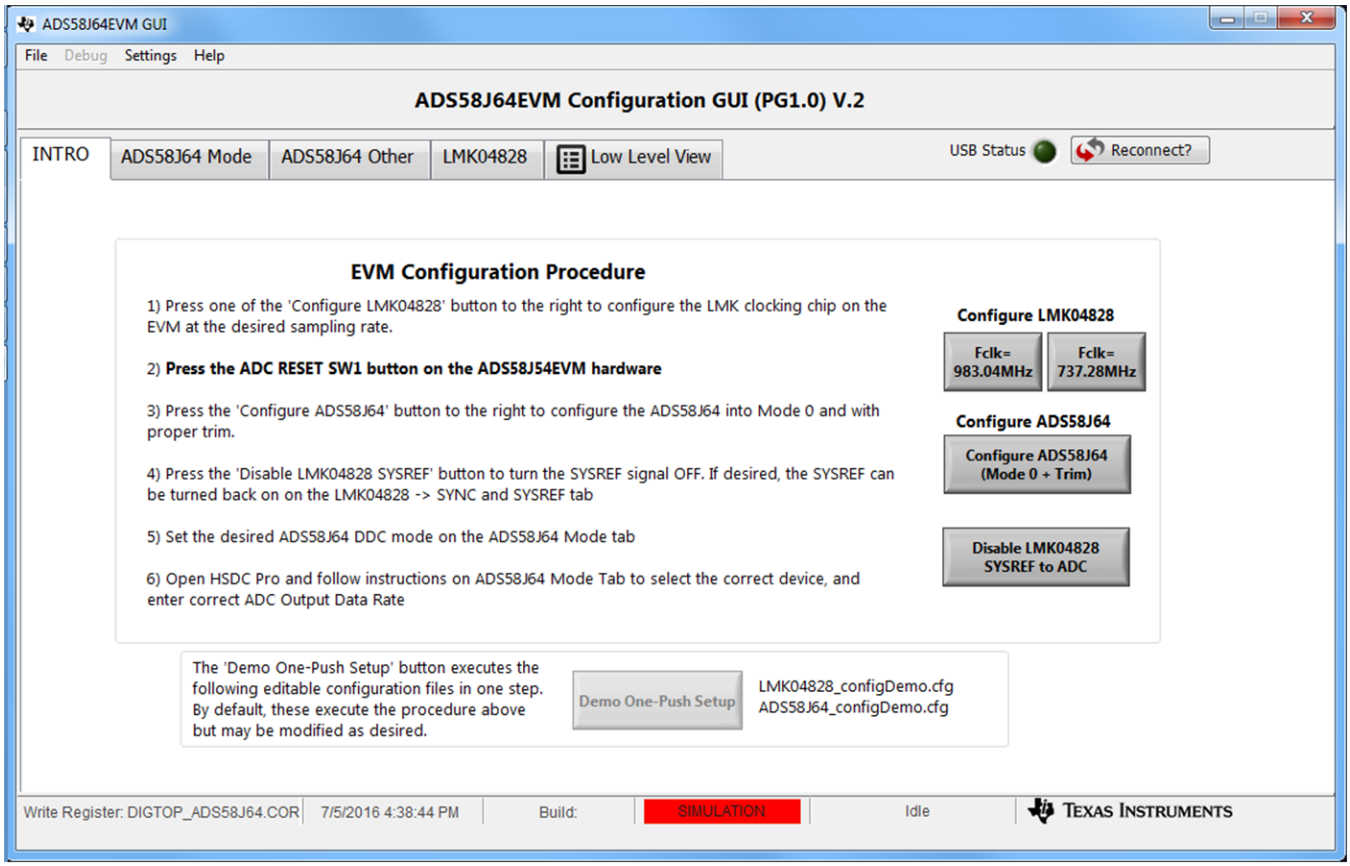


Figure 7. ADS58J64 GUI

Table 6 lists descriptions for each of the tabs of the GUI.

Table 6. ADS58J64 GUI Tab Descriptions

Tab	Description
INTRO	Quick configuration of the devices on the EVM for evaluation
ADS58J64 Mode	Provides DDC Mode control for the ADS58J64
ADS58J64 Other	Provides additional functionality controls for the ADS58J64
LMK04828	Provides controls for the LMK04828 features that can be used to customize evaluation or set up more advanced clocking schemes.
Low Level View	Allows write and read access to all device registers and bits. Also allows loading and saving of configuration files. The device configurations can be saved from this tab for use in the user's system.

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4.2 Low Level View

Figure 8 shows the Low Level View tab, which allows users to configure the ADS58J64 ADC at the register bit and field levels.

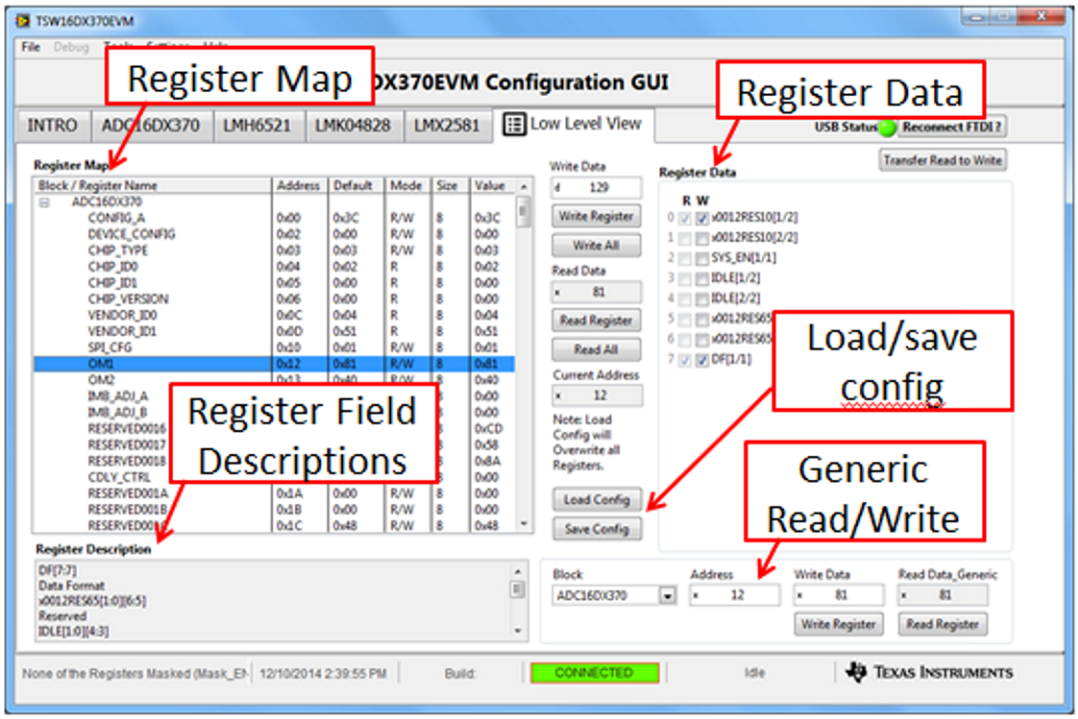


Figure 8. Low Level View Tab

At any time, the controls described in Table 7 can be used to configure or read from the device.

Table 7. Low Level View Controls

Control	Description
Register Map	Displays the devices on the EVM, registers for those devices, and the states of the registers. • Selecting a register field allows bit manipulation in the Register Data section. • The Value column shows the value of the register at the time the GUI was last updated due to a read or write event.
Write Register button	Write to the register highlighted in the Register Map with the value in the Write Data field. This button must be clicked after changing bits in the register data section.
Write All button	Update all registers shown in the Register Map with the values shown in the Register Map summary.
Read Register button	Read from the register highlighted in the Register Map and display the results in the Value column.
Read All button	Read from all registers in the Register Map and display current state of hardware. Also updates the controls in the other tabs.
Load Config button	Load a Configuration File from the disk and write the registers in the file.
Save Config button	Save a Configuration File to the disk that contains the current register configuration.
Register Data Cluster	Manipulate individual accessible bits of the register highlighted in the Register Map.
Generic Read/Write Register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the Address and Write Data information

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5 EVM Hardware Modifications from Default

The following hardware changes are required for proper operation of the ADS58J64EVM Rev.A default PCB, built and assembled with PG1.0 ADS58J64 silicon:

1. Replace C72/72 with 75 Ω 0402 resistors
2. Place R105/106 with 150 Ω 0402 resistors

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A.1 Jumper, Header, and Button Descriptions

Table 8 lists the EVM jumpers and buttons, as well as the default settings for the jumpers. If there are issues, use Table 8 to reset the EVM in the default configuration.

Table 8. Jumper and Button Descriptions and Default Settings

Jumper	Description	Default Setting
JP7	Rx Global Power-Down Short 1 – 2: Force as logic HIGH (power down) Short 2 – 3: Force as logic LOW (normal operation) **NOTE:** Open is not a valid state for this jumper.	Short 2 – 3
JP3	SPI Select, CPLD Short 1 – 2: Reserved. Do not use this state. Short 2 – 3: Default state **NOTE:** Open is not a valid state for this jumper.	Short 2 – 3
JP2	VCXO Power Short: Supplies 3.3 V to Y1 VCXO Open: Disconnects power from Y1 VCXO	Short
TRIGAB	External trigger for Burst Mode, channels A and B Pin 1: Trigger signal, 1.8-V logic Pin 2: Ground Open: Trigger function not used	Open
TRIGCD	External trigger input for Burst Mode, channels C and D Pin 1: Trigger signal, 1.8-V logic Pin 2: Ground Open: Trigger function not used	Open
TRDYAB	Trigger Ready output for Burst Mode, channel A and B Pin 1: Trigger ready signal, 1.8-V logic Pin 2: Ground	Open

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Table 8. Jumper and Button Descriptions and Default Settings (continued)

Jumper	Description	Default Setting
TRDYCD	Trigger Ready output for Burst Mode, channel C and D	Open
	Pin 1: Trigger ready signal, 1.8-V logic	
	Pin 2: Ground	
SW1	ADC Reset	N/A
	Press to reset ADC and its registers.	
J15	ADS58J64 SPI Monitoring Header, ADC SPI	OPEN
	Pin1: SCK	
	Pin2: SEN	
	Pin3: SDIO	
	Pin4: SDO	
J14	JTAG Programming Header for CPLD, U3	OPEN
	Pin1: TCK	
	Pin3: TDO	
	Pin4: +1.8 V	
	Pin5: TMS	
	Pin9: TDI	
	Pin2, Pin10: GND	

A.2 Connector Descriptions

Table 9 lists the EVM connectors and their function.

Table 9. Connector Descriptions

Connector	Description
AIN (J1)	Receiver (ADS58J64) analog input, channel A
BIN (J7)	Receiver (ADS58J64) analog input, channel B
CIN (J8)	Receiver (ADS58J64) analog input, channel C
DIN (J5)	Receiver (ADS58J64) analog input, channel D
EXT_ADC_CLK (J6)	Receiver (ADS58J64) external clock input
LMK_CLK_IN (J12)	LMK04828 reference clock input
J13	USB3 mini connector for device configuration
J14	5-V power connector

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A.3 LED Descriptions

Table 10 lists the EVM LEDs.

Table 10. LED Descriptions

LED	Description
PWR (D2)	Indicates status of input power
	OFF: Power is *not* provided at J14
	ON: Power *is* provided at J14
CLKIN0 SEL (D4)	Not functional
CLKIN1 SEL (D5)	Not functional
PLL1 LOCKED (D6)	LMK04828 lock detect, PLL1
	OFF: PLL is *not* locked
	ON: PLL *is* locked
PLL2 LOCKED (D3)	LMK04828 Lock Detect, PLL2
	OFF: PLL is *not* locked
	ON: PLL *is* locked
JESD_SYNC (D7)	Not functional. Always dimly lit.

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