

SBAS247E – MARCH 2002 – REVISED NOVEMBER 2005

8-Channel, 10-Bit, 40MSPS, 1.8V CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 8 DIFFERENTIAL ANALOG INPUTS
- $1V_{PP}$ DIFFERENTIAL INPUT RANGE
- INT/EXT VOLTAGE REFERENCE
- ANALOG/DIGITAL SUPPLY 1.8V
- DIGITAL I/O SUPPLY 1.8V/3.3V
- INTEGRAL NONLINEARITY: ±0.8LSB
- SIGNAL-TO-NOISE: 58dB at f_{IN} = 20MHz
- SPURIOUS-FREE DYNAMIC RANGE: 72dB at f_{IN} = 20MHz
- 794mW POWER DISSIPATION
- INDIVIDUAL CHANNEL POWER-DOWN
- 257-LEAD, 0.8 BALL PITCH, PLASTIC MicroSTAR BGA™ (16 • 16mm)

APPLICATIONS

- PORTABLE ULTRASOUND
- PORTABLE INSTRUMENTATION

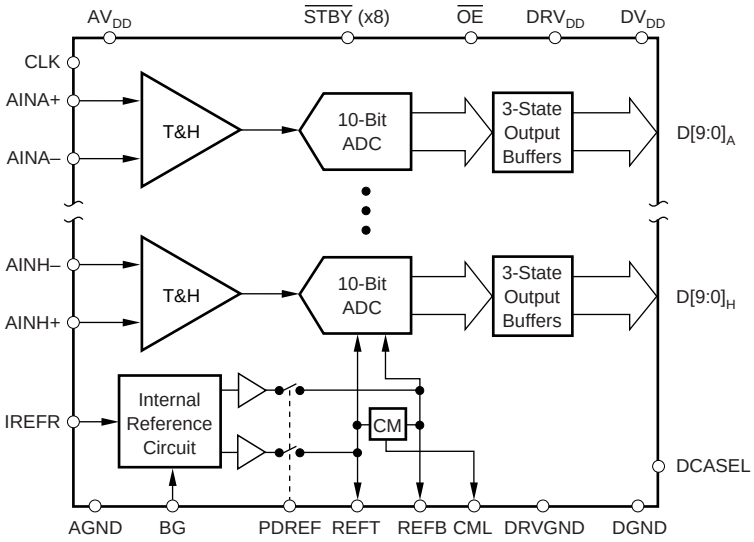
DESCRIPTION

The ADS5120 is a low-power, 8-channel, 10-bit, 40MSPS CMOS Analog-to-Digital Converter (ADC) that operates from a single 1.8V supply, while offering 1.8V and 3.3V digital I/O flexibility. A single-ended input clock is used for simultaneous sampling of up to eight analog differential input channels. The flexible duty cycle adjust circuit (DCASEL) allows the use of a non-50% clock duty cycle. Individual standby pins allow users the ability to power-down any number of ADCs. A sample-and-hold stage is added in front of the ADC and a digital error correction circuit is used to generate the final digital code.

The internal reference can be bypassed to use an external reference to suit the accuracy and temperature drift requirements of the application. A 10-bit parallel bus on eight channels is provided with 3-state outputs.

The speed, resolution, and low-power of the ADS5120 makes it ideal for applications requiring high-density signal processing in low-power environments.

The ADS5120 is characterized for operation from 0°C to 70°C.



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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage: AV_{DD} to AGND, DV_{DD} to DGND	–0.3V to +2.2V
DRV_{DD} to DGND	–0.3V to +4.0V
AGND to DGND	–0.3V to +0.3V
AV_{DD} to DV_{DD}	–2.2V to +2.2V
Reference Voltage Input Range REFT, REFB to AGND	–0.3V to AV_{DD} + 0.3V
Analog Input Voltage Range AIN to AGND	–0.3V to AV_{DD} + 0.3V
Clock Input CLK to DGND	–0.3V to DRV_{DD} + 0.3V
Digital Input to DGND	–0.3V to DV_{DD} + 0.3V
Digital Outputs to DRGND	–0.3V to DRV_{DD} + 0.3V
Operating Temperature Range (T_J)	0°C to +105°C
Storage Temperature Range (T_{STG})	–65°C + 150°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

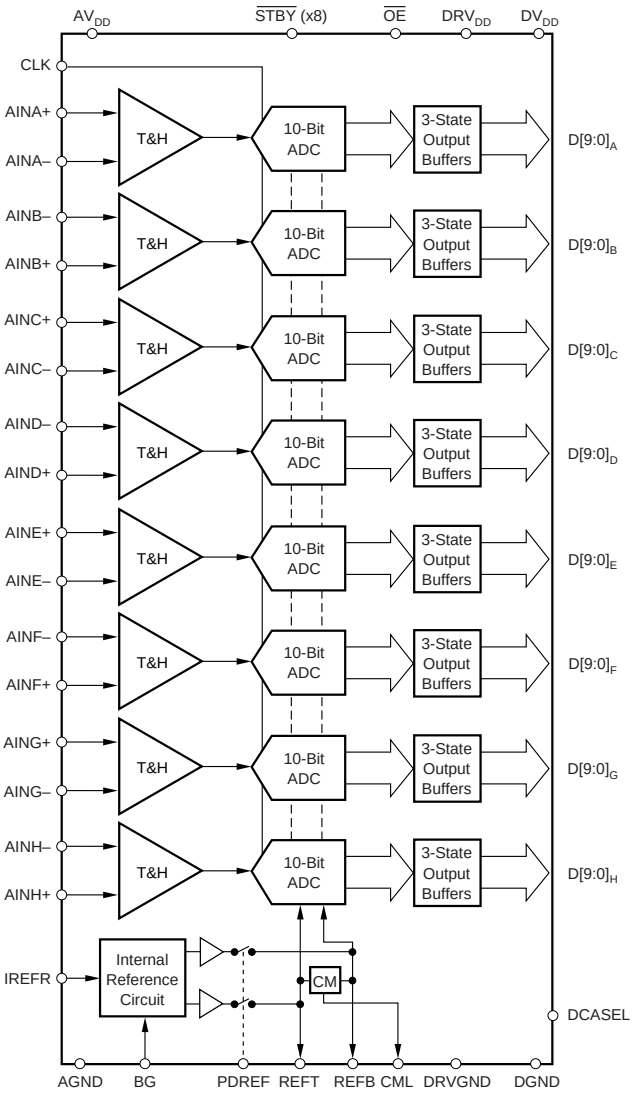
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5120	MicroSTAR BGA-257	GHK	0°C to +70°C	ADS5120CGHK	ADS5120CGHK	Tray, 90
ADS5120	ROHS-Compliant Microstar	ZHK	0°C to +70°C	ADS5120CZHK	ADS5120CZHK	Tray, 90

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BLOCK DIAGRAM



DC CHARACTERISTICS

AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, Clock = 40MSPS, 50% Clock Duty Cycle, –0.5dBFS Input Span, Internal Reference, T_{MIN} = 0°C, and T_{MAX} = +70°C, unless otherwise noted.

PARAMETER	CONDITION	ADS5120 MIN	ADS5120 TYP	ADS5120 MAX	UNITS
RESOLUTION			10		Bits
DC ACCURACY					
Differential Nonlinearity (DNL)		–0.9	±0.4	+1.0	LSB
Integral Nonlinearity (INL)		–1.5	±0.8	+1.5	LSB
No Missing Codes			Tested		
Gain Error	External Reference	–1.0	0.1	+1.0	%FSR
Offset Error	External Reference		0.2	+1.8	%FSR
Gain Temperature Coefficient			80		ppm/°C
Gain Matching			±0.4		%FSR
ANALOG INPUT					
Input Voltage Range (AIN+, AIN–)		REFB		REFT	V
Input Voltage, Differential Full-Scale			1		V_{PP}
Input Common-Mode Range			(REFT + REFB)/2		V
Input Resistance, R_{IN}	f_{CLK} = 40MSPS		83		kΩ
Input Capacitance, C_{IN}			5		pF
INTERNAL REFERENCE VOLTAGES					
Reference, Top (REFT)		1.30	1.34	1.40	V
Reference, Bottom (REFB)		0.76	0.81	0.85	V
Int Reference Temperature Coefficient			50		ppm/°C
EXTERNAL REFERENCE GENERATION					
Reference, Top (REFT)		1.15	1.25	1.35	V
Reference, Bottom (REFB)		0.65	0.75	0.85	V
Input Resistance, $REFR_{IN}$ (between REFB and REFT)			80		Ω
POWER SUPPLY	f_{IN} = 3.5MHz				
Operating Supply Current, I_{DD}			398	450	mA
Analog Operating Supply Current, IAV_{DD}			294	340	mA
Digital Operating Supply Current, IDV_{DD}			44	49	mA
Driver Operating Supply Current, $IDRV_{DD}$	C_L = 20pF		53	60	mA
Operating Voltage					
AV_{DD}		1.65	1.8	2.0	V
DV_{DD}		1.65	1.8	2.0	V
DRV_{DD}		1.65	1.8	3.6	V
Power Dissipation			794	850	mW
Standby Power ($\overline{STBY}$)	CLK Running		68		mW
	CLK Stopped		60		mW
	PDREF = 1, External REF, CLK Running		10	15	mW
	PDREF = 1, External REF, CLK Stopped		2.5	5	mW
PSRR, Power-Supply Rejection Ratio	±5%		0.8		mV/V

DC CHARACTERISTICS

AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, Clock = 40MSPS, 50% Clock Duty Cycle, –0.5dBFS Input Span, Internal Reference, and T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITION	ADS5120 MIN	ADS5120 TYP	ADS5120 MAX	UNITS
DIGITAL INPUTS ($\overline{STBY}$ A-H, PDREF, $\overline{OE}$, CLK)	DRV_{DD} = 3.3V/1.8V				
High-Level Input Voltage, V_{IH}	V_{IH} = DRV_{DD}	0.70 • DRV_{DD}			V
Low-Level Input Voltage, V_{IL}	V_{IL} = 0V			0.25 • DRV_{DD}	V
High-Level Input Current, I_{IH}				±1	µA
Low-Level Input Current, I_{IL}				±1	µA
DIGITAL INPUTS (DCASEL)					
High-Level Input Voltage, V_{IH}	V_{IH} = DV_{DD}	0.70 • DV_{DD}			V
Low-Level Input Voltage, V_{IL}	V_{IL} = 0V			0.25 • DV_{DD}	V
High-Level Input Current, I_{IH}				±1	µA
Low-Level Input Current, I_{IL}				±1	µA
DIGITAL OUTPUTS (DRV_{DD} = 3.3/1.8V)					
High-Level Output Voltage, V_{OH}	I_{OH} = –50µA	0.8 • DRV_{DD}			V
Low-Level Output Voltage, V_{OL}	I_{OL} = 50µA			0.2 • DRV_{DD}	V
External Load Capacitance, C_L			15		pF
3-State Leakage Current, I_{LEAK}	$\overline{OE}$ = HIGH			±1	µA

TARGETED AC CHARACTERISTICS

AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, 50% Clock Duty Cycle, CLK = 40MSPS, Analog input at –0.5dBFS Input Span, Internal voltage reference, T_{MIN} = 0°C, T_{MAX} = 70°C, and typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		CONDITION	ADS5120 MIN	ADS5120 TYP	ADS5120 MAX	UNITS
Signal-to-Noise Ratio	(SNR)	f_{IN} = 3.5MHz	55	58		dB
		f_{IN} = 10MHz	55	58		dB
		f_{IN} = 20MHz		58		dB
Signal-to-Noise and Distortion	(SINAD)	f_{IN} = 3.5MHz	55	57		dB
		f_{IN} = 10MHz	55	57		dB
		f_{IN} = 20MHz		57		dB
Effective Number of Bits	(ENOB)	f_{IN} = 3.5MHz	8.8	9.2		Bits
		f_{IN} = 10MHz	8.8	9.2		Bits
		f_{IN} = 20MHz	8.8	9.2		Bits
Spurious-Free Dynamic Range	(SFDR)	f_{IN} = 3.5MHz	65	73		dBc
		f_{IN} = 10MHz	65	72		dBc
		f_{IN} = 20MHz		72		dBc
2nd-Harmonic Distortion	(HD2)	f_{IN} = 3.5MHz	68	79		dBc
		f_{IN} = 10MHz	68	80		dBc
		f_{IN} = 20MHz		80		dBc
3rd-Harmonic Distortion	(HD3)	f_{IN} = 3.5MHz	65	76		dBc
		f_{IN} = 10MHz	65	78		dBc
		f_{IN} = 20MHz		73		dBc
2-Tone Intermodulation Distortion	(IMD)	f_1 = 4.43MHz, f_2 = 4.53MHz at –6.5dB		–69		dBFS
Channel-to-Channel Crosstalk		f_{IN} = 10MHz, DRV_{DD} = 3.3V		89		dB
Large-Signal Bandwidth	(FPBW)			300		MHz
Over-Voltage Recovery Time(1)				20		ns
Differential Gain(1)				±1		%
Differential Phase(1)				±0.25		Degree

NOTE: (1) Assured by design.

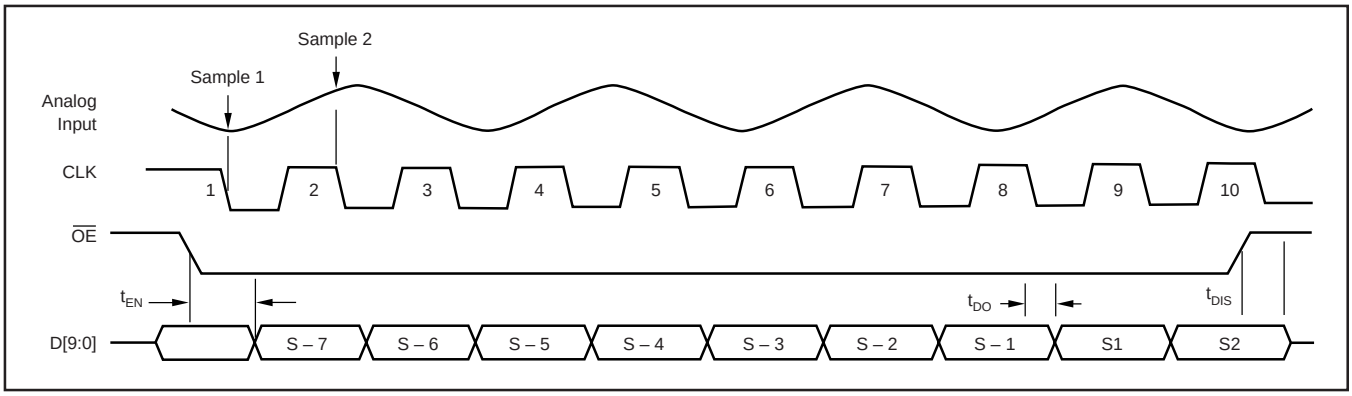
SWITCHING CHARACTERISTICS

AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, 50% Clock Duty Cycle, CLK = 40MSPS, Analog input at –0.5dBFS Input Span, Internal voltage reference, T_{MIN} = 0°C, and T_{MAX} = 70°C. Typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		CONDITION	ADS5120 MIN	ADS5120 TYP	ADS5120 MAX	UNITS
Maximum Conversion Rate			1		40	MSPS
Clock Duty Cycle		DCASEL Enabled		30 to 70		%
Data Latency(1)				7		Clk Cycles
Clock ↓ to Data Valid	t_{DO}(1)			8	10	ns
$\overline{OE}$ ↓ to Outputs Enabled	t_{EN}(1)			8		ns
$\overline{OE}$ ↑ Rising to Outputs Tri-Stated	t_{DIS}			8		ns
Aperture Delay				1		ns
Aperture Uncertainty (Jitter)				2		ps, rms

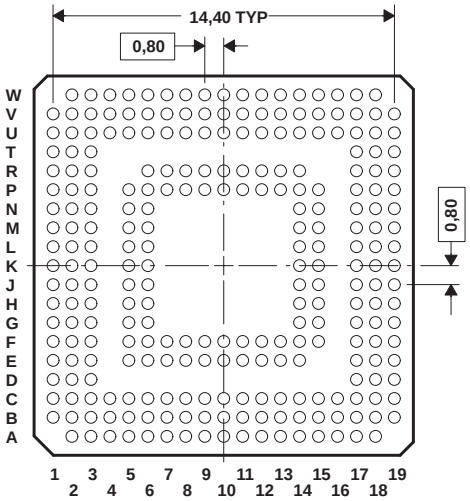
NOTE: (1) See Timing Diagram.

TIMING DIAGRAM (Per ADC Channel)



PIN CONFIGURATION

Bottom View **BGA**



PIN DESCRIPTIONS

NAME	PINS	I/O	TERMINAL DESCRIPTION
AV_{DD}	C6, C7, E6, F1, F2, F3, F5, F6, J6, N3, P3, P5, P6, P7, R6, V6, W6	I	Analog Supply, (1.8V)
AGND	A3, A5, B5, B9, C1, C5, C9, E3, E7, F7, G1, G5, G6, H6, J1, J2, M2, N5, N6, P8, R1, R2, R3, R7, U1, U5, U10, V5, V10, W3, W7	I	Analog Ground
AINA+	U7	I	Analog Input Channel A
AINA–	V7	I	Complementary Analog Input Channel A
AINB+	W4	I	Analog Input Channel B
AINB–	V4	I	Complementary Analog Input Channel B
AINC+	T1	I	Analog Input Channel C
AINC–	T2	I	Complementary Analog Input Channel C
AIND+	P2	I	Analog Input Channel D
AIND–	P1	I	Complementary Analog Input Channel D
AINE+	G3	I	Analog Input Channel E
AINE–	G2	I	Complementary Analog Input Channel E
AINF+	D1	I	Analog Input Channel F
AINF–	D2	I	Complementary Analog Input Channel F
AING+	A4	I	Analog Input Channel G
AING–	B4	I	Complementary Analog Input Channel G
AINH+	B6		Analog Input Channel H
AINH–	A6	I	Complementary Analog Input Channel H
CLK	W9	I	Clock Input
REFT	K3, L1, J3	I/O	Reference Top
REFB	K5, J5, L5	I/O	Reference Bottom
CML	L2, L3	O	Common-Mode Level Output
BG	K1	I/O	Bandgap Decoupling (Decouple with 1µF cap to AGND and 100kΩ to AV_{DD})
IREFR	K6	I	Internal Reference Bias Current (Connect 6.19kΩ resistor from this pin AGND to set internal bias amplifier current.)
DNC	W5	I	Do Not Connect
DNC	U6	I	Do Not Connect
NC	E1, E2, E5, K2, L6, M1	I	No Internal Connection
DCASEL	N2	I	Duty Cycle Adjust
DV_{DD}	C2, C3, C4, D3, E8, F8, H3, H5, M3, M5, R8, T3, U3, U4, U8, V3, P13, R13 P17, L15, J14, F17, F12, E12	I	Digital Supply (1.8V)
DGND	A2, A7, B1, B2, B3, B7, B13, C13, G15, H1, H2, H17, L17, M6, N1, N15, U2, U13, U14, V1, V2, V8, W2, W8	I	Digital Ground
PDREF	V9	I	Power-Down Ref: 0 = internal reference, 1 = external reference. In external reference mode connect REFT to BG pin.
$\overline{\text{STBY}}$ A	W10	I	Power-Down Channel A
$\overline{\text{STBY}}$ B	P9	I	Power-Down Channel B
$\overline{\text{STBY}}$ C	R9	I	Power-Down Channel C
$\overline{\text{STBY}}$ D	U9	I	Power-Down Channel D
$\overline{\text{STBY}}$ E	C8	I	Power-Down Channel E
$\overline{\text{STBY}}$ F	B8	I	Power-Down Channel F
$\overline{\text{STBY}}$ G	A8	I	Power-Down Channel G
$\overline{\text{STBY}}$ H	A9	I	Power-Down Channel H
$\overline{\text{OE}}$	P10	I	Enable all Digital Outputs, Ch A-H. $\overline{\text{OE}}$: 0 = Outputs Enable. $\overline{\text{OE}}$: 1 = Outputs disabled (3-State).
DRV_{DD}	B17, C16, D17, E9, E10, E11, E17, F9, H14, H15, K17, L14, N14, P12, P14, P15 R10, R12, R14	I	Driver Digital Supply (1.8V or 3.3V)
DRGND	E13, F10, F11, F13, F14, F15, G14, G17, M14, M15, M17, N17, U11, U12, U15, U16	I	Driver Digital Ground

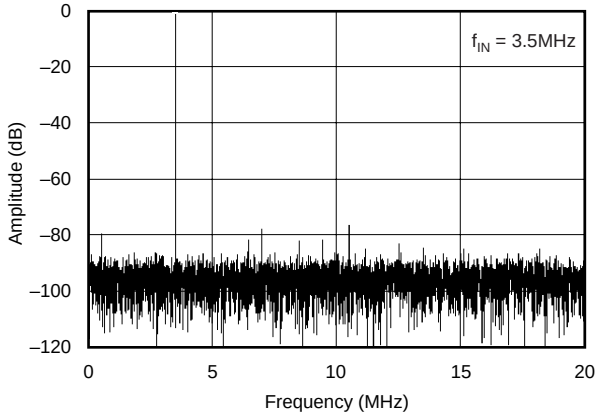
DATA OUTPUT PINS

NAME	PINS	I/O	TERMINAL DESCRIPTION	NAME	PINS	I/O	TERMINAL DESCRIPTION
D0A	V14	O	Bit 1, Channel A (LSB)	D0E	F18	O	Bit 1, Channel E (LSB)
D1A	W14	O	Bit 2, Channel A	D1E	F19	O	Bit 2, Channel E
D2A	V13	O	Bit 3, Channel A	D2E	G18	O	Bit 3, Channel E
D3A	W13	O	Bit 4, Channel A	D3E	G19	O	Bit 4, Channel E
D4A	V12	O	Bit 5, Channel A	D4E	H18	O	Bit 5, Channel E
D5A	W12	O	Bit 6, Channel A	D5E	H19	O	Bit 6, Channel E
D6A	R11	O	Bit 7, Channel A	D6E	J15	O	Bit 7, Channel E
D7A	P11	O	Bit 8, Channel A	D7E	J17	O	Bit 8, Channel E
D8A	V11	O	Bit 9, Channel A	D8E	J18	O	Bit 9, Channel E
D9A	W11	O	Bit 10, Channel A (MSB)	D9E	J19	O	Bit 10, Channel E (MSB)
D0B	V19	O	Bit 1, Channel B (LSB)	D0F	A18	O	Bit 1, Channel F (LSB)
D1B	V18	O	Bit 2, Channel B	D1F	B18	O	Bit 2, Channel F
D2B	U17	O	Bit 3, Channel B	D2F	C17	O	Bit 3, Channel F
D3B	W18	O	Bit 4, Channel B	D3F	B19	O	Bit 4, Channel F
D4B	V17	O	Bit 5, Channel B	D4F	C18	O	Bit 5, Channel F
D5B	W17	O	Bit 6, Channel B	D5F	C19	O	Bit 6, Channel F
D6B	V16	O	Bit 7, Channel B	D6F	D18	O	Bit 7, Channel F
D7B	W16	O	Bit 8, Channel B	D7F	D19	O	Bit 8, Channel F
D8B	V15	O	Bit 9, Channel B	D8F	E18	O	Bit 9, Channel F
D9B	W15	O	Bit 10, Channel B (MSB)	D9F	E19	O	Bit 10, Channel F (MSB)
D0C	P19	O	Bit 1, Channel C (LSB)	D0G	A14	O	Bit 1, Channel G (LSB)
D1C	P18	O	Bit 2, Channel C	D1G	B14	O	Bit 2, Channel G
D2C	R19	O	Bit 3, Channel C	D2G	C14	O	Bit 3, Channel G
D3C	R18	O	Bit 4, Channel C	D3G	A15	O	Bit 4, Channel G
D4C	R17	O	Bit 5, Channel C	D4G	B15	O	Bit 5, Channel G
D5C	T19	O	Bit 6, Channel C	D5G	E14	O	Bit 6, Channel G
D6C	T18	O	Bit 7, Channel C	D6G	C15	O	Bit 7, Channel G
D7C	U19	O	Bit 8, Channel C	D7G	A16	O	Bit 8, Channel G
D8C	U18	O	Bit 9, Channel C	D8G	B16	O	Bit 9, Channel G
D9C	T17	O	Bit 10, Channel C (MSB)	D9G	A17	O	Bit 10, Channel G (MSB)
D0D	K14	O	Bit 1, Channel D (LSB)	D0H	C10	O	Bit 1, Channel H (LSB)
D1D	K15	O	Bit 2, Channel D	D1H	B10	O	Bit 2, Channel H
D2D	K18	O	Bit 3, Channel D	D2H	A10	O	Bit 3, Channel H
D3D	K19	O	Bit 4, Channel D	D3H	C11	O	Bit 4, Channel H
D4D	L18	O	Bit 5, Channel D	D4H	B11	O	Bit 5, Channel H
D5D	L19	O	Bit 6, Channel D	D5H	A11	O	Bit 6, Channel H
D6D	M19	O	Bit 7, Channel D	D6H	A12	O	Bit 7, Channel H
D7D	M18	O	Bit 8, Channel D	D7H	B12	O	Bit 8, Channel H
D8D	N19	O	Bit 9, Channel D	D8H	C12	O	Bit 9, Channel H
D9D	N18	O	Bit 10, Channel D (MSB)	D9H	A13	O	Bit 10, Channel H (MSB)

TYPICAL CHARACTERISTICS

T_A = 25°C, AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, f_{IN} = –0.5dBFS, Internal Reference, Clock = 40MSPS, and Differential Input Range = $1V_{PP}$, unless otherwise noted.

SPECTRAL PERFORMANCE



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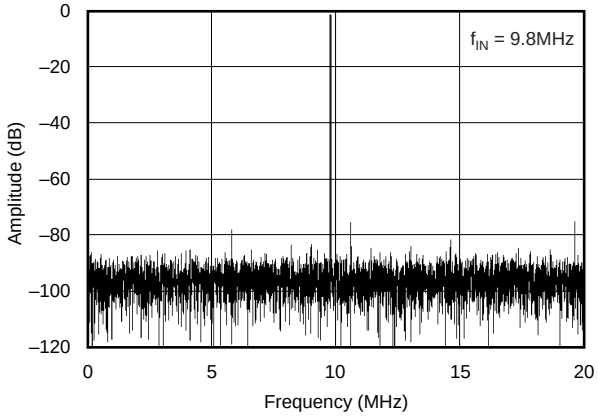
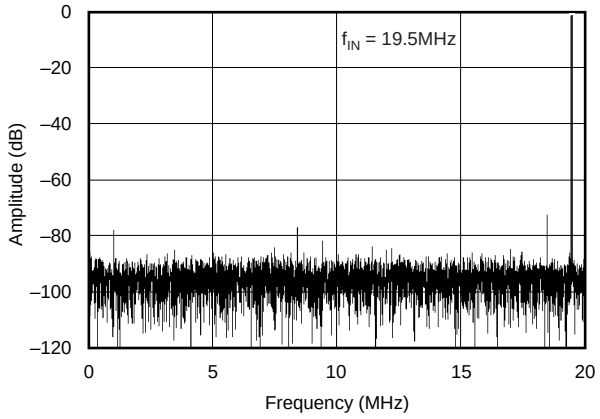
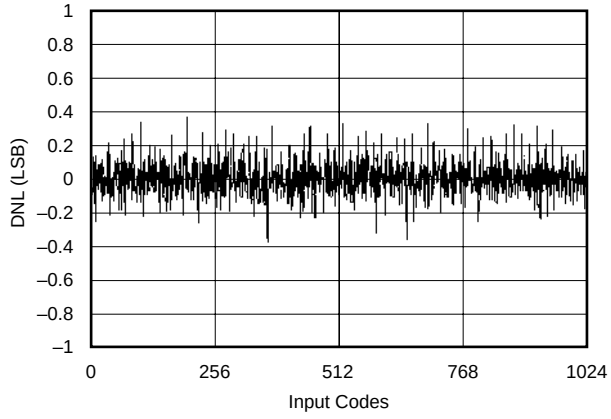


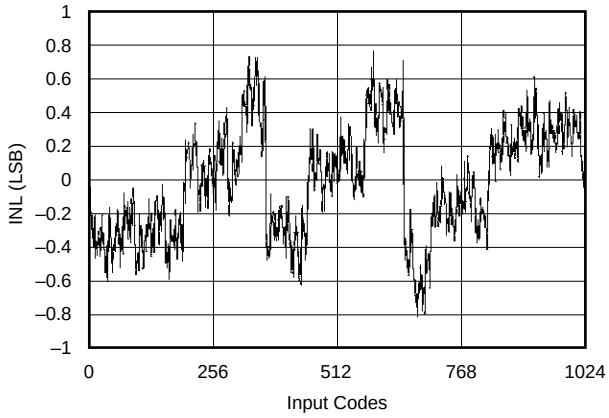
SPECTRAL PERFORMANCE



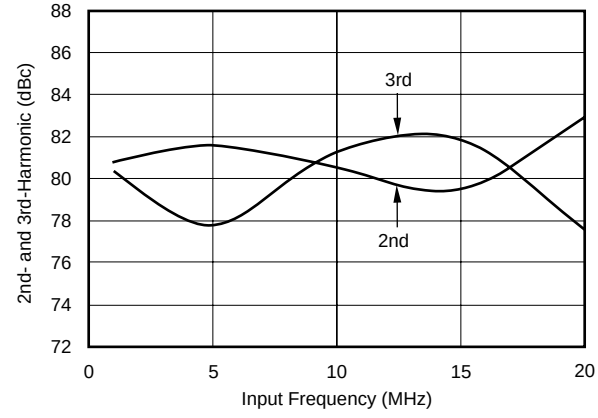
DIFFERENTIAL NONLINEARITY



INTEGRAL NONLINEARITY



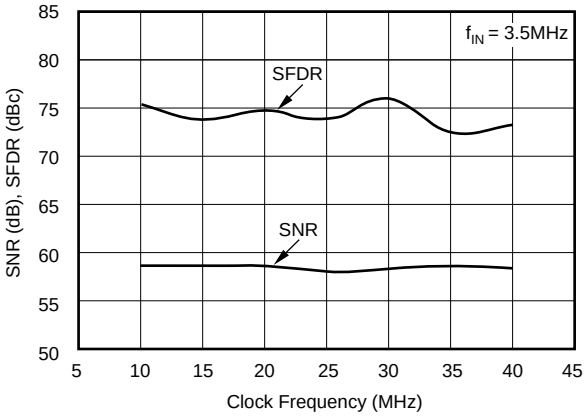
2ND- AND 3RD-HARMONIC vs INPUT FREQUENCY



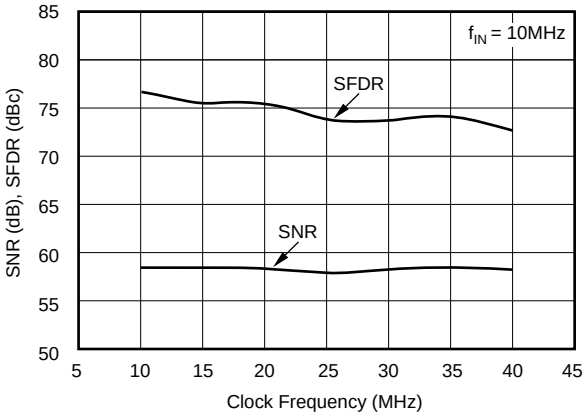
TYPICAL CHARACTERISTICS (Cont.)

T_A = 25°C, AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, f_{IN} = –0.5dBFS, Internal Reference, Clock = 40MSPS, and Differential Input Range = $1V_{PP}$, unless otherwise noted.

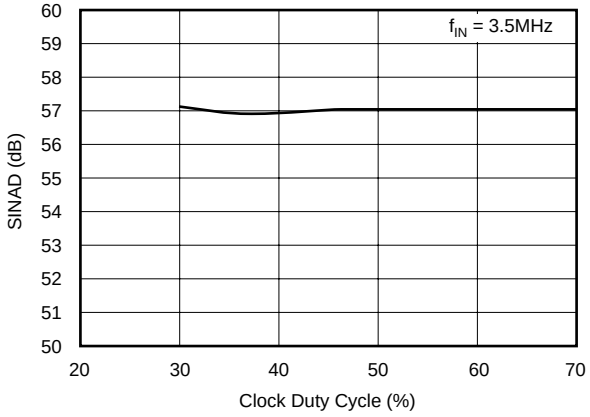
SNR AND SFDR vs CLOCK FREQUENCY



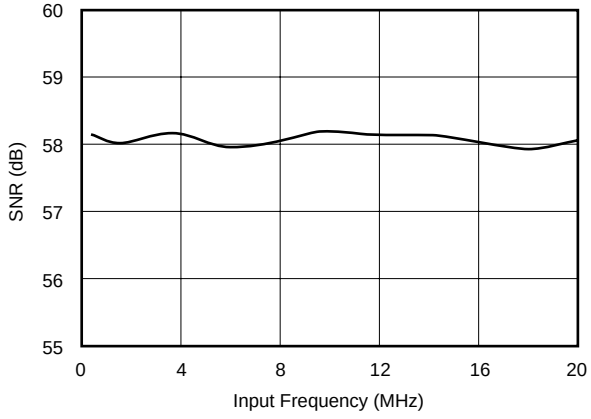
SNR AND SFDR vs CLOCK FREQUENCY



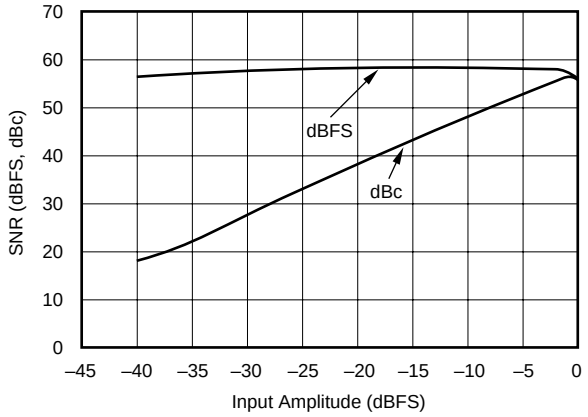
SINAD vs DUTY CYCLE
(DCASEL = ENABLE)



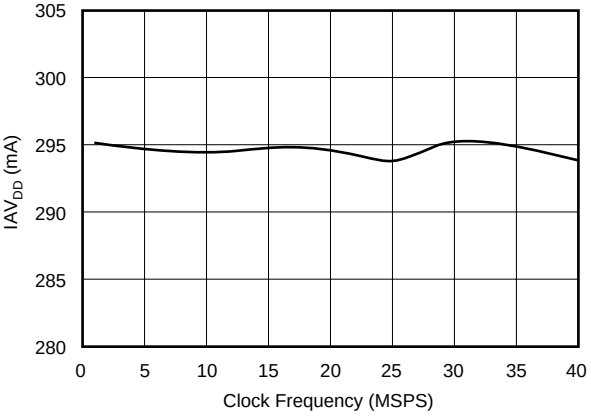
SNR vs INPUT FREQUENCY



SWEPT INPUT POWER (SNR)



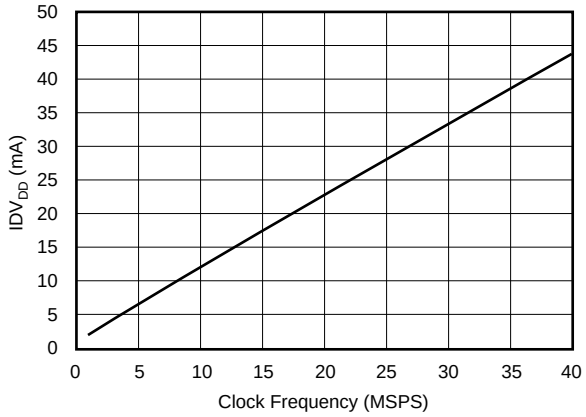
IAV_{DD} vs CLOCK FREQUENCY



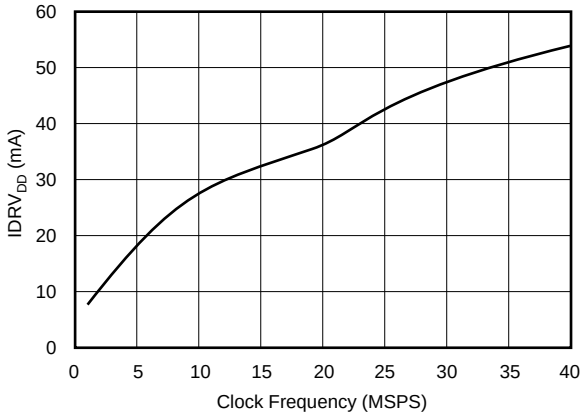
TYPICAL CHARACTERISTICS (Cont.)

T_A = 25°C, AV_{DD} = DV_{DD} = 1.8V, DRV_{DD} = 3.3V, f_{IN} = –0.5dBFS, Internal Reference, Clock = 40MSPS, and Differential Input Range = $1V_{PP}$, unless otherwise noted.

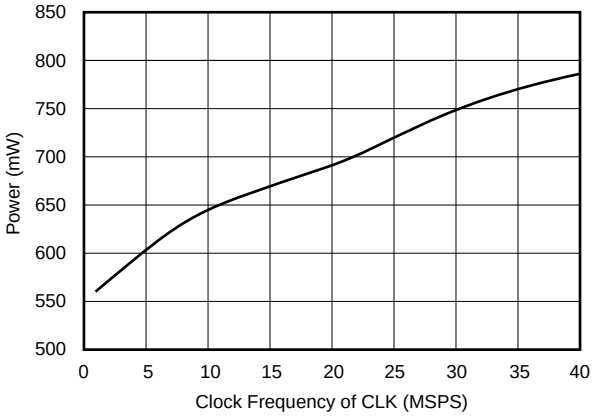
IDV$_{DD}$ vs CLOCK FREQUENCY



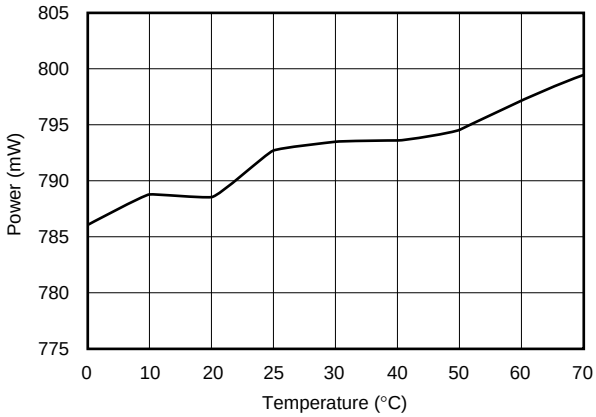
IDRV$_{DD}$ vs CLOCK FREQUENCY



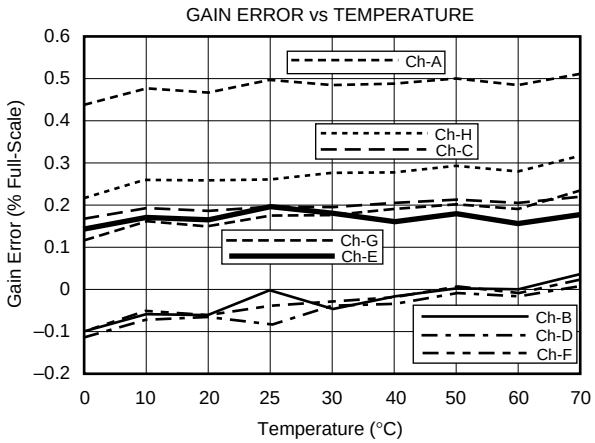
TOTAL POWER vs CLOCK FREQUENCY



POWER vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



APPLICATION INFORMATION

CONVERTER OPERATION

The ADS5120 is an 8-channel, simultaneous sampling ADC. Its low power (100mW/channel) and high sampling rate of 40MSPS is achieved using a state-of-the-art switched capacitor pipeline architecture built on an advanced low-voltage CMOS process. The ADS5120 primarily operates from a +1.8V single supply. For additional interfacing flexibility, the digital I/O supply (DRV_{DD}) can be set to either +1.8V or +3.3V. The ADC core of each channel consists of 10 pipeline stages. Each of the 10 stages produces one digital bit per stage. Both the rising and the falling clock edges are utilized to propagate the sample through the pipeline every half clock, for a total of five clock cycles. Two additional clock cycles are needed to pass the sample data through the digital error correction logic and the output latches. The total pipeline delay, or data latency, is therefore seven clock cycles long. Since a common clock controls the timing of all eight channels, the analog signal is sampled at the same time, as well as the data on the parallel ports which becomes updated simultaneously.

ANALOG INPUTS

The analog input for each channel of the ADS5120 consists of a differential track-and-hold amplifier implemented using a switched capacitor technique, shown in Figure 1. This differential input topology along with closely matched capacitors produces a high level of AC performance up to high sampling rates.

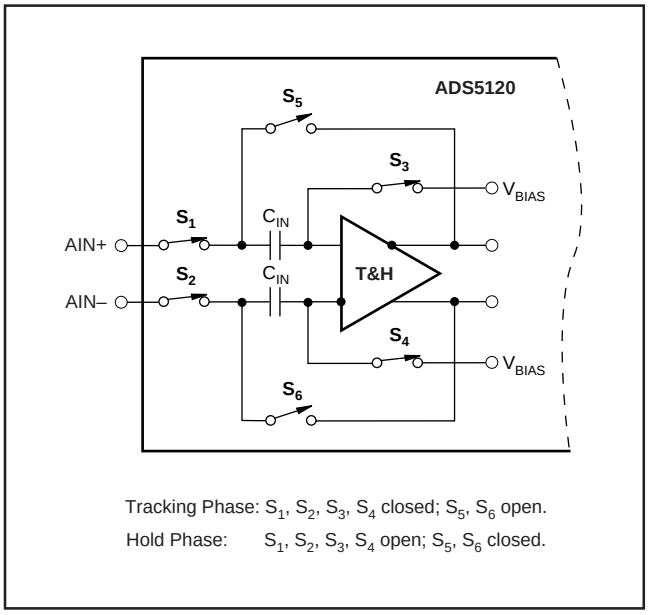


FIGURE 1. Simplified Circuit of Input Track-and-Hold.

INPUT IMPEDANCE

Because of the switched capacitor input track-and-hold amplifier, the input impedance of the ADS5120 is effectively capacitive, and the driving source needs to provide sufficient slew current to charge and discharge the input sampling capacitor while the track-and-hold amplifier is in track mode. The input impedance of the ADS5120 is also a function of the sampling rate. As the sampling frequency increases, the input impedance decreases linearly at a rate of 1/fs. For most applications, this does not represent a limitation since the impedance remains relatively high, for example, approximately 83kΩ at the max sampling rate of 40MSPS. For applications using an op amp to drive the ADC, it is recommended that a series resistor, typically 10Ω to 50Ω, be added between the amplifier output and the converter inputs. This will isolate the converter capacitive input from the driver and avoid potential gain peaking, or instability.

INPUT BIASING

The ADS5120 operates from a single +1.8V analog supply, and requires each of the analog inputs (AIN+, AIN–) to be externally biased by a suitable common-mode voltage. For example, with a common-mode voltage of +1V, the $1V_{PP}$ full-scale, differential input signal will swing symmetrically around +1V, or between 0.75V and 1.25V. This is determined by the two reference voltages, the top reference (REFT), and the bottom reference (REFB). Typically, the input common-mode level is related to the reference voltages and defined as (REFT + REFB)/2. This reference mid-point is provided at the CML pin and can directly be used for input biasing purposes. The voltage at CML will assume the mid-point for either internal or external reference operation. In any case, it is recommended to bypass the CML pin with a ceramic 0.1µF capacitor.

DRIVING THE ANALOG INPUTS

Differential versus Single-Ended

The analog input of the ADS5120 allows it to be driven either single-ended or differentially. Differential operation of the ADS5120 requires an input signal that consists of an in-phase and a 180° out-of-phase part simultaneously applied to the inputs (AIN+, AIN–). The full-scale input range of the ADS5120 is defined by the reference voltages according to FSR = 2 x (REFT – REFB). For a typical $1V_{PP}$ range, the differential input configuration only requires each input to see a signal swing of $0.5V_{PP}$. Operating the converter in single-ended configuration requires the full $1V_{PP}$ swing applied to the chosen input. The differential operation offers a number of advantages, which in most applications will be instrumental in achieving the best dynamic performance of the ADS5120:

- The signal swing is half of that required for the single-ended operation and is therefore less demanding to achieve while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom of the interface circuitry and therefore a wider selection of the best suitable driver op amp.
- Even-order harmonics are minimized.
- Improves the noise immunity based on the converter's common-mode input rejection.

For the single-ended mode, the signal is applied to one of the inputs while the other input is biased with a DC voltage to the required common-mode level. Both inputs are identical in terms of their impedance and performance. Applying the signal to the complementary input (AIN–) instead of the AIN+ input, however, will invert the orientation of the input signal relative to the output code. This could be helpful, for example, if the input driver operates in inverting mode using input AIN– as the signal input will restore the phase of the signal to its original orientation.

INPUT DRIVER CONFIGURATIONS

Transformer-Coupled Interface

If the application requires a signal conversion from a single-ended source to drive the ADS5120 differentially, an RF-transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC-grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs (AIN+ and AIN–) of the ADS5120 see matched impedances. Figure 2 shows the schematic for the suggested transformer-coupled interface circuit. The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency.

Single-Ended, AC-Coupled Driver

The circuit of Figure 3 shows an example for driving the inputs of the ADS5120 in a single-ended configuration. The signal is AC-coupled between the driver amplifier and the converter input (AIN+). This allows for setting the required common-mode voltages for the ADC and op amp separately. The single-supply op amp is biased at mid-supply by two resistors connected at its noninverting input. Connecting each input to the CML pin provides the required common-mode voltage for the inputs of the ADS5120. Here, two resistors of equal value ensure that the inputs see closely matched source impedances. If the op amp features a disable function, it could be easily tied together with the power-down pin of the ADS5120 channel ($\overline{\text{STBY}}$). In the circuit example depicted in Figure 3, the OPA355 EN pin is

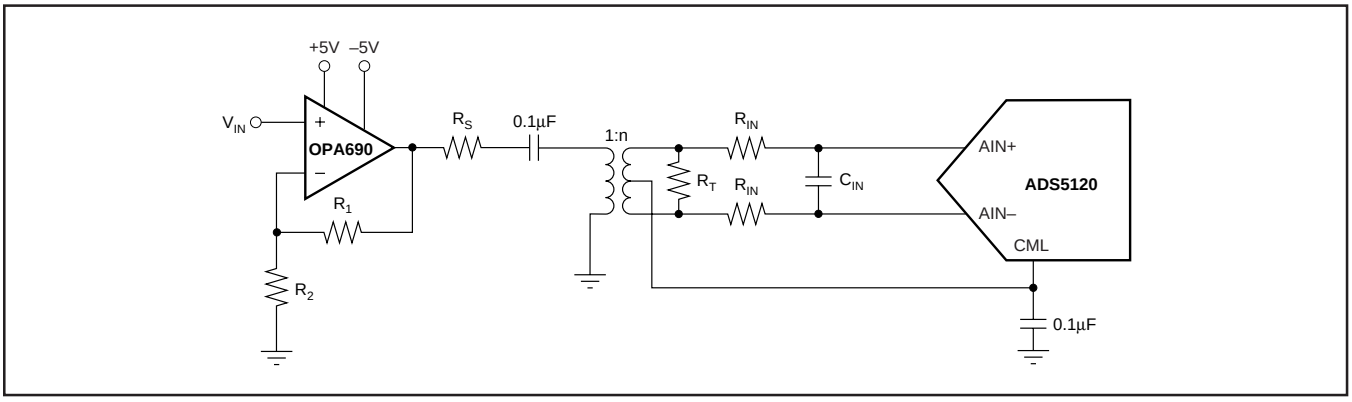


FIGURE 2. Converting a Single-Ended Input Signal into a Differential Signal Using an RF-Transformer.

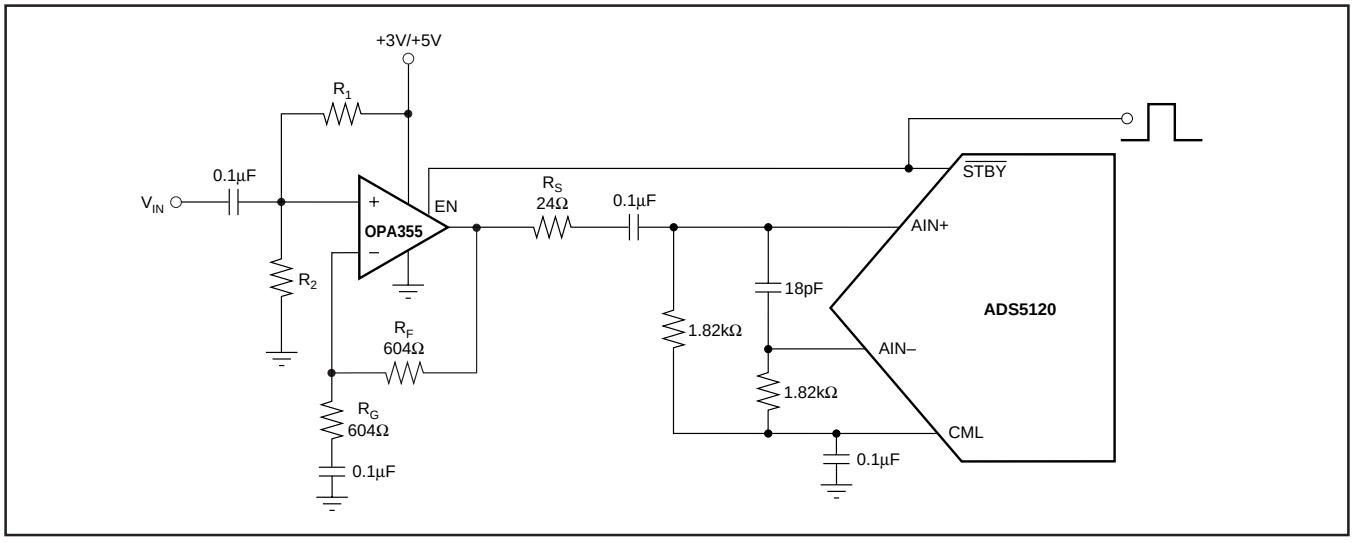


FIGURE 3. Single-Ended, AC-Coupled Driver Configuration for Single Supply.

directly connected to the $\overline{\text{STBY}}$ pin to allow for a power-down mode of the entire circuit. Other suitable op amps for single-supply driver applications include the OPA634, OPA635, or OPA690, for example.

DC-Coupled Interface with Differential Amplifier

Differential input/output amplifiers can simplify the driver circuit for applications requiring input DC-coupling. Flexible in their configurations, such amplifiers can be used for single-ended to differential conversion, allow for signal amplification, and also filtering prior to the ADC. Figure 4 shows one possible circuit implementation using the THS4130 amplifier. Here, the amplifier operates with a gain of +1. The common-mode voltage available at the CML pin can be conveniently connected to the amplifier VOCM pin to set the required input bias for the ADS5120.

REFERENCE OPERATION

For proper operation of the ADS5120 and its reference, an external 6.19kΩ resistor must be connected from the IREFR pin to analog ground, AGND (as shown in Figure 5). While a 1% resistor tolerance is adequate, deviating from this resistor value will cause altered and degraded performance.

To ensure proper operation with any reference configuration, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum. Figure 5 shows the recommended decoupling scheme. Good performance can be obtained using 0.1µF low inductance ceramic capacitors. Adding tantalum capacitors (1µF to 10µF) may lead to a performance improvement, depending on the application. All bypassing capacitors should be located as close to their respective pins as possible.

INTERNAL REFERENCE

The internal reference circuit of the ADS5120 consists of a bandgap voltage reference, the drivers for the top and bottom reference, and the resistive reference ladder. The corresponding reference pins are REFT, REFB, CML, IREFR, BG, and PDREF. In order to enable the internal reference,

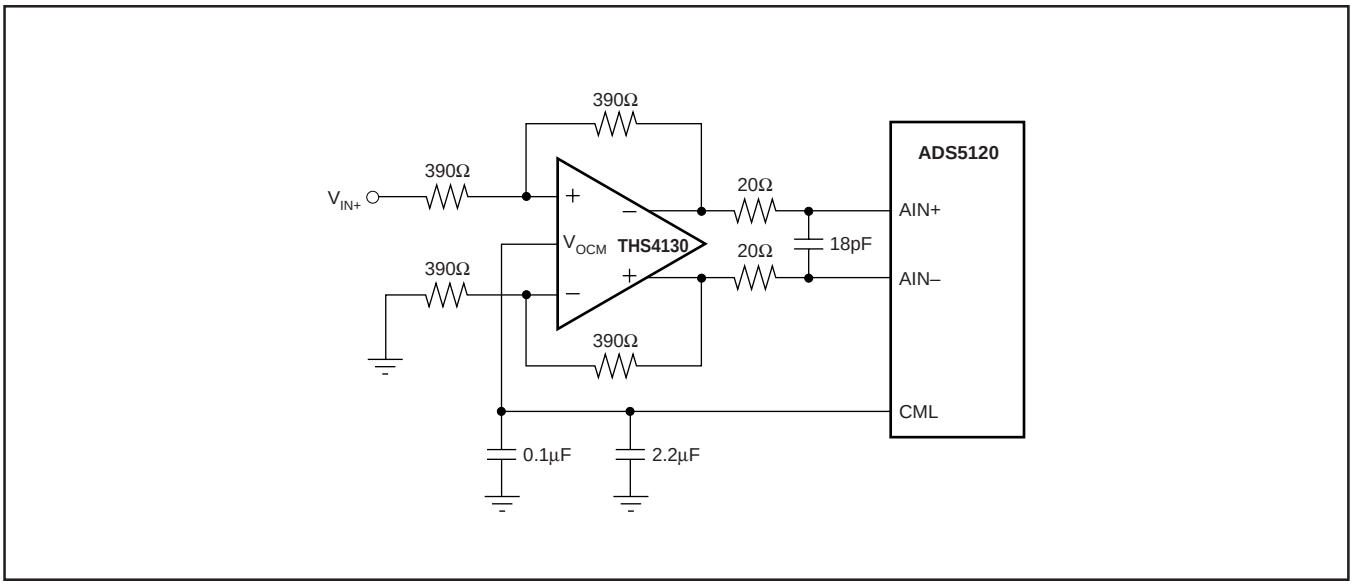


FIGURE 4. DC-Coupled Interface Using Differential I/O Amplifier THS4130.

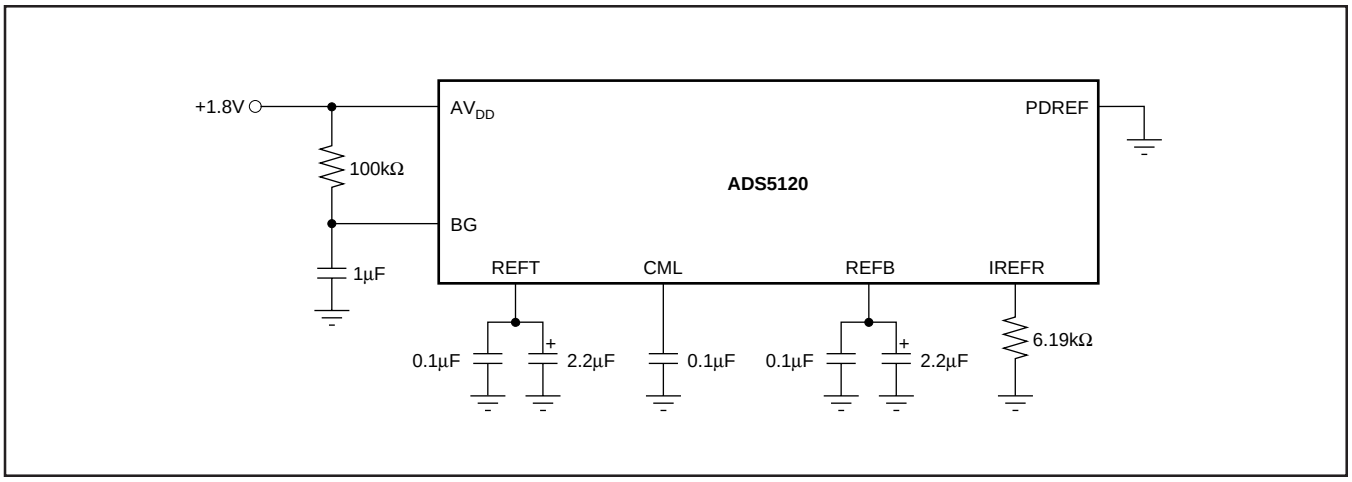


FIGURE 5. Internal Reference; Recommended Configuration and Bypassing.

pin PDREF must be at a logic LOW = 0 level. In addition, the bandgap pin BG must have a 100kΩ pull-up resistor to AV_{DD}, and should be decoupled with a 1µF capacitor. The reference circuit provides the reference voltages to each of the eight channels.

The reference buffers can be utilized to supply up to 1mA (sink and source) to an external circuitry. The common-mode level output pin, CML, represents the mid-point of the internal resistor ladder and is an unbuffered node. Loading of this pin should be avoided, as it will lead to degradation of the converter linearity.

USING EXTERNAL REFERENCES

For even more design flexibility, the internal reference can be disabled and an external reference voltage used. The utilization of an external reference may be considered for applications, requiring higher accuracy or improved temperature performance. Especially in multi-channel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

Setting the ADS5120 for external reference mode requires taking the PDREF pin HIGH. In addition, pins BG and REFT must be connected together (as shown in Figure 6). The common-mode voltage at the CML pin will be maintained at approximately the mid-point of the applied reference voltages, according to CML ≈ (VREFT – VREFB)/2. The internal buffer amplifiers for REFT and REFB are disabled when the ADS5120 operates in the external reference mode. The external reference circuit must be designed to drive the internal reference ladder (80Ω) located between the REFT and REFB pins. For example, setting REFT = +1.25V and REFB = +0.75V will require a current drive capability of at least 0.5V/80Ω = 6.25mA. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) stays within the range of +1.15V to +1.35V, and the external bottom reference ($REFB_{EXT}$) stays within +0.65V to +0.85V (as shown in Figure 7).

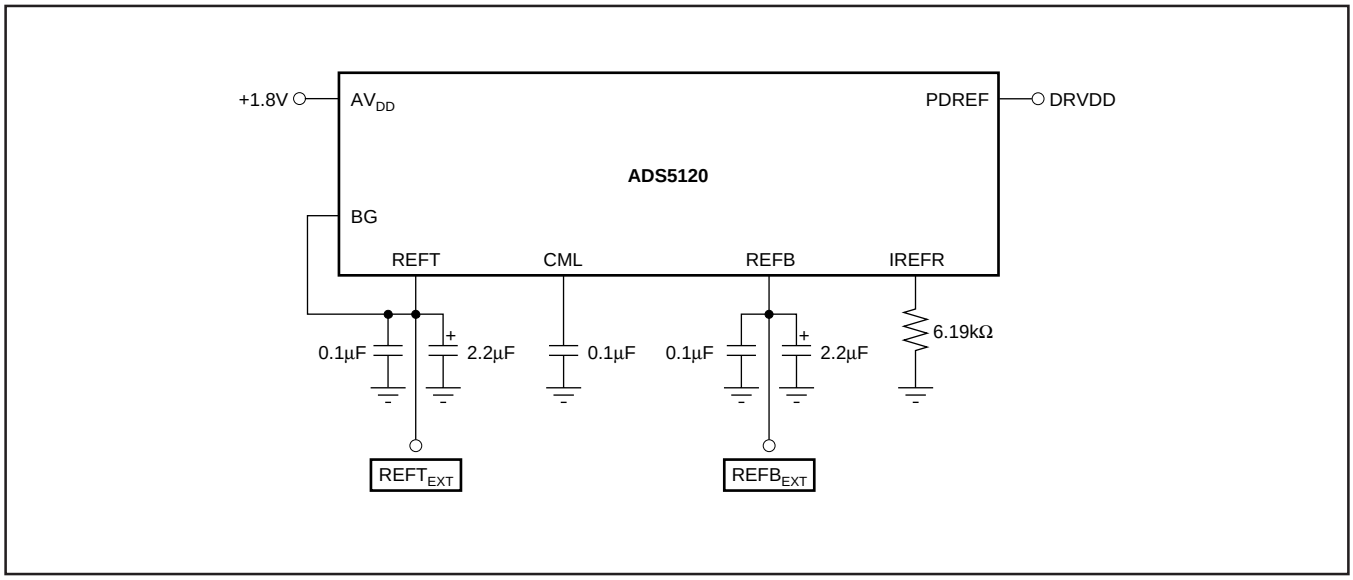


FIGURE 6. External Reference; Recommended Configuration and Bypassing.

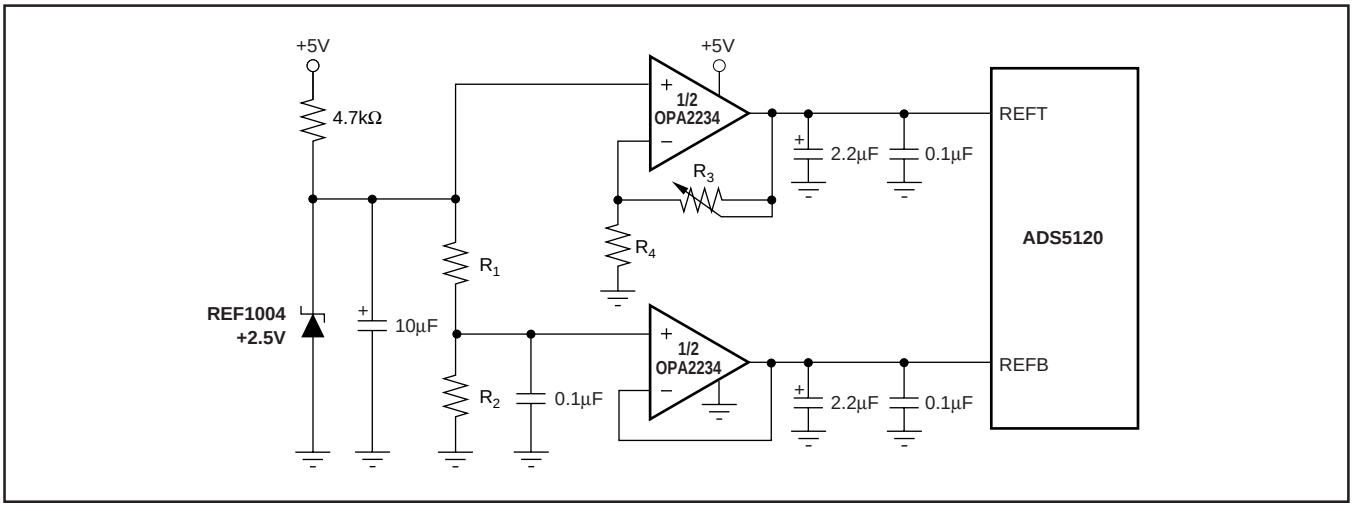


FIGURE 7. Circuit Example of an External Reference Circuit Using Single-Supply, Low-Power, Dual Op Amp (OPA2234).

DIGITAL INPUTS AND OUTPUTS

Clock Input

The clock input is designed to operate with +1.8V or +3.3V CMOS logic levels. The clock circuitry is internally connected to the DRV_{DD} supply. Therefore, the input HIGH and LOW levels will vary depending on the applied DRV_{DD} supply; see *DC Characteristics* tables. Since both edges of the clock are used in this pipeline ADC, the ideal clock should be a square-wave logic signal with a 50% duty-cycle.

Since this condition cannot always easily be met, the ADS5120 features an internal clock conditioning circuitry that can be activated through the duty-cycle adjust pin (DCASEL).

The DCASEL pin is a logic input, with its logic levels related to the DV_{DD} supply (+1.8V only):

a) DCASEL = LOW (GND); in this mode the clock conditioning circuitry is disabled. Use this setting if the applied clock signal is a square-wave clock with a duty cycle of 50%; or if the duty cycle stays within a range of 48% to 52%.

b) DCASEL = HIGH (DV_{DD}); in this mode the clock conditioning circuitry is enabled. Use this setting if the applied external clock signal is a square-wave clock that does not meet the criteria listed above, but has a duty cycle in the range of 30% to 70%.

MINIMUM SAMPLING RATE

The pipeline architecture of the ADS5120 uses a switched capacitor technique for the internal track-and-hold stages. With each clock cycle, charges representing the captured signal level are moved within the ADC pipeline core. The high sampling rate necessitates the use of very small capacitor values. In order to hold the droop errors low, the capacitors require a minimum refresh rate. To maintain full accuracy of the acquired sample charge, the sampling clock of the ADS5120 should not be lower than the specified minimum of 1MSPS.

DATA OUTPUT FORMAT

The output data format of the ADS5120 is a positive Straight Offset Binary (SOB) code. Tables I and II show output coding of a single-ended and differential signal. For all data output channels, the MSBs are located at the D9x pins.

SINGLE-ENDED INPUT (AIN– = CML)	STRAIGHT OFFSET BINARY (SOB)
+FS – 1LSB (AIN+ = CML + FSR/2)	11 1111 1111
+1/2 FS	11 0000 0000
Bipolar Zero (AIN+ = CML)	10 0000 0000
–1/2 FS	01 0000 0000
–FS (AIN+ = CML – FSR/2)	00 0000 0000

TABLE I. Coding Table for Single-Ended Input Configuration with Input AIN– Tied to the Common-Mode Voltage (CML).

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)
+FS – 1LSB (AIN+ = REFT, AIN– = REFB)	11 1111 1111
+1/2 FS	11 0000 0000
Bipolar Zero (AIN+ = AIN– = CML)	10 0000 0000
–1/2 FS	01 0000 0000
–FS (AIN+ = REFB, AIN– = REFT)	00 0000 0000

TABLE II. Coding Table for Differential Input Configuration and $1V_{PP}$ Full-Scale Range.

DIGITAL OUTPUT LOADING

Minimizing the capacitive loading on the digital outputs is very important in achieving the best performance. The total load capacitance is typically made up of two sources: the next stage input capacitance and the parasitic/printed circuit board (PDB) capacitance. It is recommended to keep the total capacitive loading on the data lines as low as possible (≤ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing states. High current surges may cause feedback into the analog portion of the ADS5120 and affect the performance. If necessary, external buffers or latches close to the converter output pins may be used to minimize the capacitive loading. A suggested device is the SN74AVC16827 (20-bit buffer/driver), a member of the Advanced Very Low Voltage CMOS logic family (AVC). Using such a logic device can also provide the added benefit of isolating the ADS5120 from any digital noise activities on the bus coupling back high-frequency noise. Some applications may also benefit from the use of series resistors (≤ 100Ω) in the data lines. This will provide a current limit and reduce any existing over- or undershoot.

OUTPUT ENABLE

The ADS5120 provides one output enable pin ($\overline{OE}$) that controls the digital outputs of all channels simultaneously. A LOW (L = 0) level on the $\overline{OE}$ pin will have all channels active and the converter in normal operation. Taking the $\overline{OE}$ pin HIGH (H = 1) will disable or tri-state the outputs of all channels. Note that the $\overline{OE}$ pin has no internal pull-up resistor and therefore requires a defined potential to be applied. The timing relations between $\overline{OE}$ and the output bus enable/disable times are shown in the Timing Diagram.

POWER-UP SEQUENCE

Ideally, the three main power supplies for the ADS5120 should be applied and ramped up simultaneously. If this cannot be ensured, the following power-up sequence is recommended:

1. AV_{DD} (+1.8 typ)
2. DV_{DD} (+1.8 typ)
3. DRV_{DD} (+3.3 typ)

The clock signal should also be applied with proper logic levels during power-up of the ADS5120. Deviating from this power-up sequence may cause the device to enter a mode such that the digital outputs do not approach the full specified output levels.

POWER-DOWN (STANDBY)

The ADS5120 is equipped with a power-down function for each of the eight channels. Labeled as $\overline{\text{STBY}}$ pins, the normal operational mode is when this pin is connected to logic high (H = 1). The selected ADC channel will be in a power-down mode if the corresponding $\overline{\text{STBY}}$ pin is connected to logic LOW (L = 0). The logic levels for the $\overline{\text{STBY}}$ pins are dependent on the DRV_{DD} supply. The power-down function controls internal biasing nodes, and as a consequence, any data present in the pipeline of the converter will become invalid. This is independent of whether the clock remains applied during power-down, or not. Following a power-up, new, valid data will become available after a minimum of seven clock cycles. As a note, the operation of the $\overline{\text{STBY}}$ pins is not intended for the use of dynamically multiplexing between the eight channels of the ADS5120.

DIGITAL OUTPUT DRIVER SUPPLY, DRV_{DD}

The ADS5120 uses a dedicated supply connection for the output logic drivers, DRV_{DD}, along with its digital driver ground connections, labeled DRGND.

Setting the voltage at DRV_{DD} to either +3.3V or +1.8V the output logic levels are set accordingly, allowing the ADS5120 to directly interface to a selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS5120 with a +1.8V driver supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply lines, which otherwise may affect the AC performance of the converter. In some applications it might be advantageous to decouple the DRV_{DD} supply with additional capacitors or a pi-filter.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PCBs are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS5120 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. The ground pins should directly connect to an analog ground plane covering the PCB area under the converter. While designing the layout it is important to keep the analog signal traces separated from any digital line to prevent noise coupling onto the analog signal path. Due to its high sampling rate, the ADS5120 generates high-frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. In most cases 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PCB in proximity of the converter circuit.

LAYOUT OF THE PCB WITH A MICROSTAR BGA PACKAGE

The ADS5120 is housed in a polyimide film-based chipscale package (CSP). Like most CSPs, solder alloy balls are used as the interconnect between the package substrate and the PCB on which the package is soldered. For detailed information regarding these packages, please refer to literature number SSYZ015B, MicroStar BGA Packaging Reference Guide, which addresses the specific considerations required when integrating a MicroStar BGA package into the PCB design. This document can be found at:

http://www-s.ti.com/sc/psheets/ssyz015b/ssyz015b.pdf

TERMINOLOGY

ANALOG BANDWIDTH

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3dB.

APERTURE DELAY

The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

APERTURE UNCERTAINTY (JITTER)

The sample-to-sample variation in aperture delay.

EFFECTIVE NUMBER OF BITS (ENOB)

The ENOB is calculated from the measured SINAD based on the equation:

$$\text{ENOB} = \left(\frac{\text{SINAD} - 1.76\text{dB}}{6.02} \right)$$

GAIN ERROR

Gain Error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

GAIN MATCHING

Variation in Gain Error between adjacent channels.

HARMONIC DISTORTION, SECOND

The ratio of the rms signal amplitude to the rms value of the 2nd-harmonic component, reported in dBc.

HARMONIC DISTORTION, THIRD

The ratio of the rms signal amplitude to the rms value of the 3rd-harmonic component, reported in dBc.

INTERMODULATION DISTORTION (IMD)

The 2-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) Intermodulation products. The individual input tone levels are at –6.5dB full-scale, and their envelope is at –0.5dB full-scale.

OFFSET ERROR (ZERO-SCALE ERROR)

The first transition should occur for an analog value 1/2 LSB above negative full-scale. Offset error is defined as the deviation of the actual transition from that point.

OFFSET MATCHING

The change in offset error between adjacent channels.

POWER-SUPPLY REJECTION RATIO (PSRR)

The ratio of a change in input offset voltage to a change in power-supply voltage.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the rms signal amplitude (set 0.5dB below full-scale) to the rms value of the sum all other spectral components, including harmonics but excluding DC.

SIGNAL-TO-NOISE RATIO (WITHOUT HARMONICS)

The ratio of the rms signal amplitude (set 0.5dB below full-scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and DC.

SPURIOUS-FREE DYNAMIC RANGE (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full-scale).

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
11/05	E	2 17	Package/Ordering Table Application Information	Include the new package designator ZHK for green/Pb-free package. Added Revision History Table
7/05	D	6	Using External References	Correct Figure 6: Added DRV_{DD} to PDREF
6/04	C	2	Abs Max Table	Changed incorrect spec. Was: Clock Input CLK to DGND: –0.3V to AV_{DD} + 0.3V, Changed to: Clock Input CLK to DGND: –0.3V to DRV_{DD} +0.3V
		3	DC Characteristics	Added CLK to Digital Inputs list
		10	Driving Analog Inputs	Added definition of full-scale input range and clarified differential input configuration requirements.
		14	Power-Up Sequence	Added Power-Up Sequence section
		15	PCB Layout	"Polymide" corrected to "polyimide"
11/02	B	1	Front Page	Added Portable Ultrasound and Portable Instrumentation to Applications Removed Available Options table Moved diagram to page 5 and replaced with new figure
		5	Pin Descriptions Table	AV_{DD} row, added F2; NC row, added ES; DV_{DD} row, deleted U3; IREFR row, changes 6.19Ω to 6.19kΩ
		6	Data Output Pins Table	D5C row, changed R19 to T19
		7	Typical Characteristics	Replaced 2nd- and 3rd-Harmonic vs Input Frequency curve
		11	Figure 3	Resistor R_L was changed to R_2
6/02	A	1	Front Page	Removed ESD-DCM statement from the front of the data sheet.
		2	Abs Max Table	Removed ESD Com row.
		3	DC Characteristics	Add/clarify information for Standby Power
		5	Pin Descriptions Table	DNC row, changed L6 to W5 and M1 to U6. NC row, changed U6, W5 to L6, M1
		8-9	Typical Characteristics	Title changes
		10	Figure 1	Added V_{BIAS}
		12	Application Information	Second paragraph text: Changed +2 to +1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS5120CGHK	ACTIVE	BGA MICROSTAR	GHK	257	90	TBD	SNPB	Level-3-220C-168 HR	Request Free Samples
ADS5120CZHK	ACTIVE	BGA MICROSTAR	ZHK	257	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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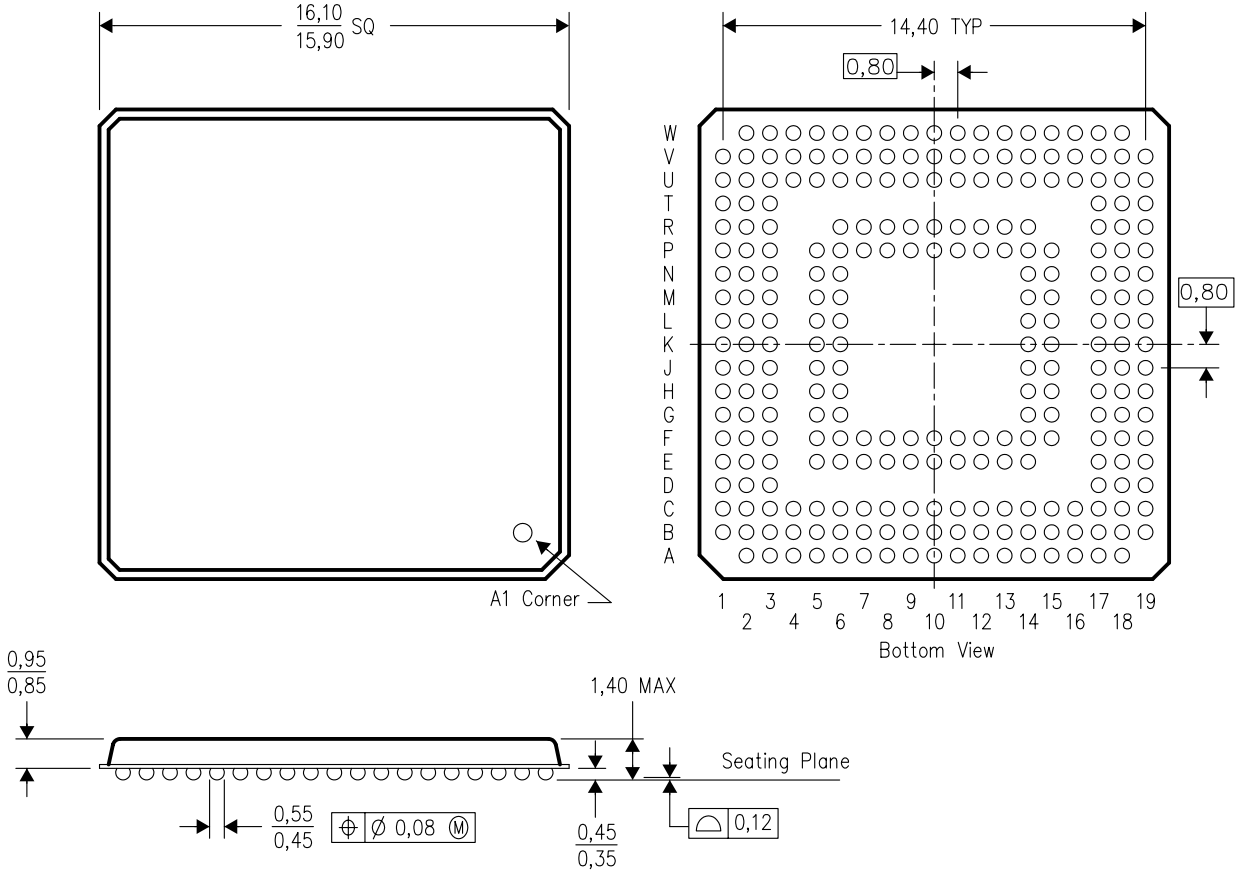
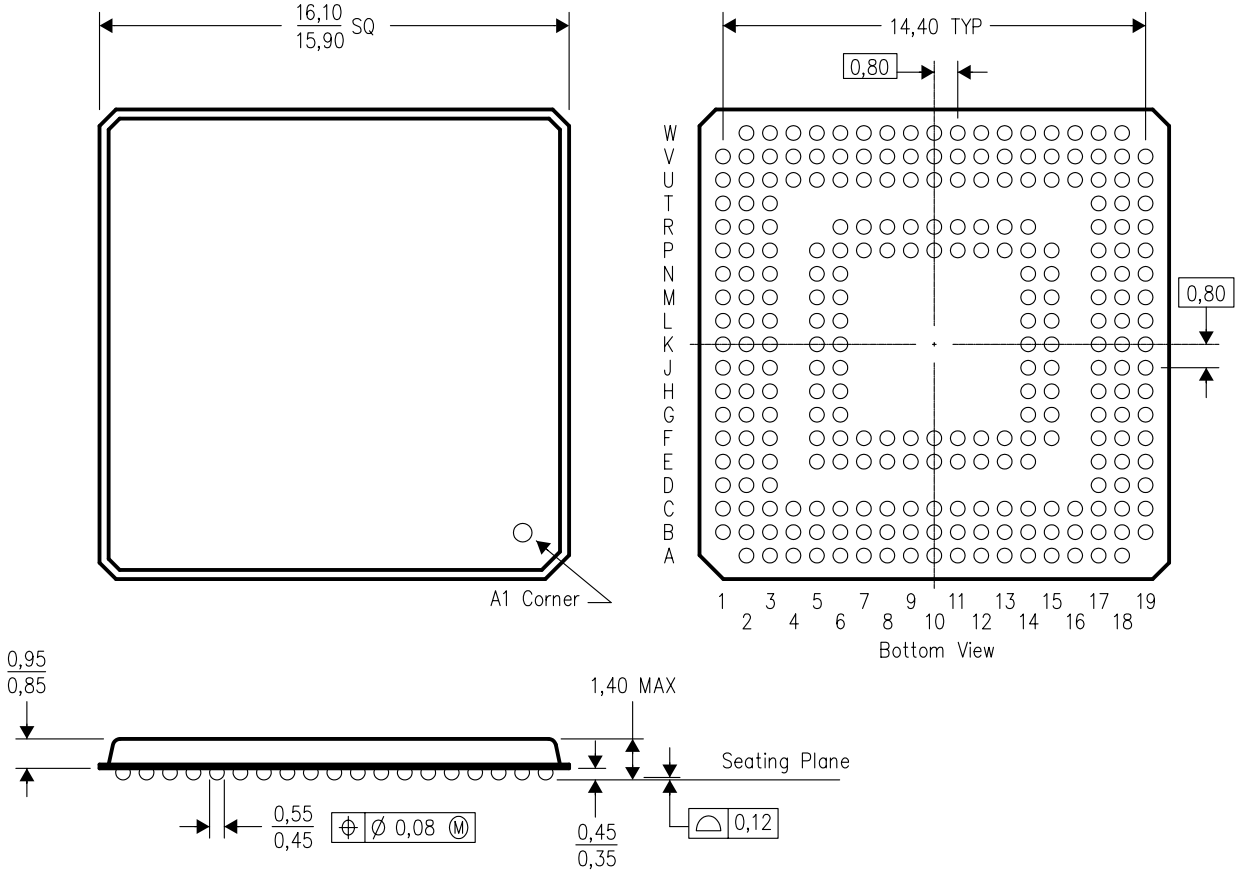
GHK (S–PBGA–N257) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

ZHK (S–PBGA–N257) PLASTIC BALL GRID ARRAY



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C. This is a lead–free solder ball design.

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