INNOVATION and EXCELLENCE

PRELIMINARY PRODUCT DATA

ADS-933

16-Bit, 3MHz Sampling A/D Converters

FEATURES

- **16-bit resolution**
- **3MHz sampling rate**
- **Functionally complete**
- **No missing codes over full military temperature range**
- **Edge-triggered**
- **±5V supplies, 1.85 Watts**
- **Small, 40-pin, ceramic TDIP**
- **85dB SNR, –84dB THD**
- **Ideal for both time and frequency-domain applications**



GENERAL DESCRIPTION

The low-cost ADS-933 is a 16-bit, 3MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-933 has been optimized to achieve a signal-to-noise ratio (SNR) of 85dB and a total harmonic distortion (THD) of –84dB.

Packaged in a 40-pin TDIP, the functionally complete ADS-933 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-933 only requires the rising edge of the start convert pulse to operate.

Requiring only ±5V supplies, the ADS-933 dissipates 1.85 Watts. The device is offered with a bipolar (±2.75V) analog input range and a unipolar 0 to –5.5V input range. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range. Typical applications include medical imaging, radar, sonar, communications and instrumentation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+3.2V REF. OUT	40	NO CONNECTION
2	UNIPOLAR	39	NO CONNECTION
3	ANALOG INPUT	38	+5V ANALOG SUPPLY
4	ANALOG GROUND	37	–5V SUPPLY
5	OFFSET ADJUST	36	ANALOG GROUND
6	GAIN ADJUST	35	$\overline{\text{COMP. BITS}}$
7	DIGITAL GROUND	34	$\overline{\text{OUTPUT ENABLE}}$
8	FIFO/$\overline{\text{DIR}}$	33	OVERFLOW
9	FIFO READ	32	$\overline{\text{EOC}}$
10	FSTAT1	31	+5V DIGITAL SUPPLY
11	FSTAT2	30	DIGITAL GROUND
12	START CONVERT	29	$\overline{\text{BIT 1 (MSB)}}$
13	BIT 16 (LSB)	28	BIT 1 (MSB)
14	BIT 15	27	BIT 2
15	BIT 14	26	BIT 3
16	BIT 13	25	BIT 4
17	BIT 12	24	BIT 5
18	BIT 11	23	BIT 6
19	BIT 10	22	BIT 7
20	BIT 9	21	BIT 8

POWER AND GROUNDING	
+5V ANALOG SUPPLY	38
+5V DIGITAL SUPPLY	31
–5V SUPPLY	37
ANALOG GROUND	4, 36
DIGITAL GROUND	7, 30
NO CONNECTION	39, 40

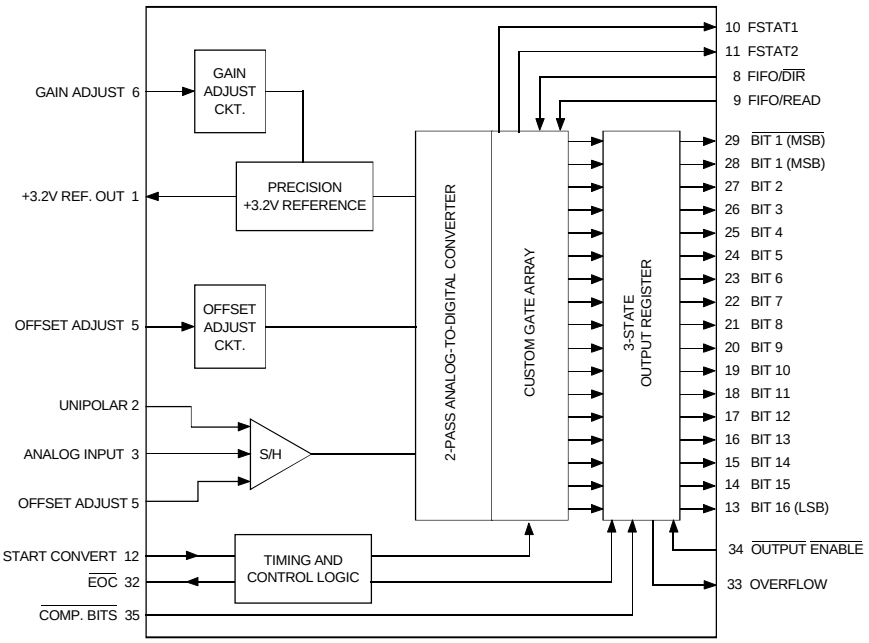


Figure 1. ADS-933 Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 31, 38)	0 to +6	Volts
–5V Supply (Pin 37)	0 to –6	Volts
Digital Inputs (Pins 8, 9, 12, 34, 35)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)	±5	Volts
Lead Temperature (10 seconds)	+300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-933MC	0	—	+70	°C
ADS-933MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	4	—	°C/Watt
θca	—	18	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, metal-sealed, ceramic TDIP			
Weight	0.56 ounces (16 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±5V, +V_{DD} = +5V, 3MHz sampling rate, and a minimum 3 minute warm-up ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range										
Unipolar	—	0 to –5.5	—	—	0 to –5.5	—	—	0 to –5.5	—	Volts
Bipolar	—	±2.75	—	—	±2.75	—	—	±2.75	—	Volts
Input Resistance Pin 3	655	687	—	655	687	—	655	687	—	Ω
Input ResistancePin 2	418	426	—	418	426	—	418	426	—	Ω
Input Capacitance	—	10	15	—	10	15	—	10	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	20	50	—	20	50	—	20	50	—	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±1	—	—	±1.5	—	—	±2	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1.0	–0.95	±0.5	+1.0	–0.95	±0.5	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
(Unipolar offset spec same as Bipolar zero)										
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	16	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	—	81	—	–86	—	—	–86	—	dB
500kHz to 1MHz	—	–84	80	—	–84	—	—	–84	—	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–84	80	—	–84	—	—	–84	—	dB
500kHz to 1MHz	—	–83	80	—	–83	—	—	–83	—	dB
Signal-to-Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 500kHz	81	85	—	—	85	—	—	85	—	dB
500kHz to 1MHz	81	85	—	—	85	—	—	85	—	dB
Signal-to-Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 500kHz	78	82	—	—	82	—	—	82	—	dB
500kHz to 1MHz	78	81	—	—	81	—	—	81	—	dB
Noise	—	80	—	—	80	—	—	80	—	µVrms
Two-Tone Intermodulation										
Distortion (f_{in} = 200kHz,										
240kHz, f_S = 3MHz, –0.5dB)	—	–87	—	—	–87	—	—	–87	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	9.8	—	—	9.8	—	—	9.8	—	MHz
Large Signal (–0.5dB input)	—	10.2	—	—	10.2	—	—	10.2	—	MHz
Feedthrough Rejection										
(f_{in} = 1MHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±120	—	—	±120	—	—	±120	—	V/µs
Aperture Delay Time	—	+8	—	—	+8	—	—	+8	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	psrms
S/H Acquisition Time										
(to ±0.001%FSR, 5.5V step)	—	180	—	—	180	—	—	180	—	ns

DYNAMIC PERFORMANCE (Cont.)	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 TO +70°C MIN.	0 TO +70°C TYP.	0 TO +70°C MAX.	–55 TO +125°C MIN.	–55 TO +125°C TYP.	–55 TO +125°C MAX.	UNITS
ANALOG OUTPUT										
Overvoltage Recovery Time ⑤	—	—	333	—	—	333	—	—	333	ns
A/D Conversion Rate	3	—	—	3	—	—	3	—	—	MHz
Internal Reference										
Voltage	3.15	+3.2	—	—	+3.2	—	—	+3.2	—	Volts
Drift	—	±30	—	—	±30	—	—	±30	—	ppm/°C
External Current	—	5	—	—	5	—	—	5	—	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Offset Binary / Complementary Offset Binary / Two's Complement / Complementary Two's Complement									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Currents										
+5V Supply	—	+220	260	—	+220	260	—	+220	260	mA
–5V Supply	–140	–150	—	–140	–150	—	–140	–150	—	mA
Power Dissipation	—	1.85	2.0	—	1.85	2.0	—	1.85	2.0	Watts
Power Supply Rejection	—	—	±0.07	—	—	±0.07	—	—	±0.07	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warm-up periods. The device must be continuously converting during this time.

② When COMP. BITS (pin 35) is low, logic loading "0" will be –350µA.

③ A 3MHz clock with a 50nsec positive pulse width is used for all production testing. See Timing Diagram for more details.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

⑥ The minimum supply voltages of +4.9V and –4.9V for ±V_{DD} are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-933 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (2, 4, 7, 30 and 36) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +3.2V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-933 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warm-up. To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.

3. Pin 35 ($\overline{\text{COMP. BITS}}$) is used to select the digital output coding format of the ADS-933. See Tables 2a and 2b. When this pin has a TTL logic "0" applied, it complements all of the ADS-933's digital outputs.

   When pin 35 has a logic "1" applied, the output coding is complementary offset binary. Applying a logic "0" to pin 35 changes the coding to offset binary. Using the $\overline{\text{MSB}}$ output (pin 29) instead of the MSB output (pin 28) changes the respective output codings to complementary two's complement and two's complement.

   Pin 35 is TTL compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 35 allowing it to be either connected to +5V or left open when a logic "1" is required.

4. To enable the three-state outputs, connect $\overline{\text{OUTPUT ENABLE}}$ (pin 34) to a logic "0" (low). To disable, connect pin 34 to a logic "1" (high).

5. Applying a start convert pulse while a conversion is in progress (EOC = logic "1") will initiate a new and probably inaccurate conversion cycle. Data from both the interrupted and subsequent conversions will be invalid.
6. Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the rising edge of EOC to the falling edge of EOC).
7. The OVERFLOW bit (pin 33) switches from 0 to 1 when the input voltage exceeds that which produces an output of all 1's or when the input equals or exceeds the voltage that produces all 0's. When COMP BITS is activated, the above conditions are reversed.

INTERNAL FIFO OPERATION

The ADS-933 contains an internal, user-initiated, 18-bit, 16-word FIFO memory. Each word in the FIFO contains the 16 data bits as well as the MSB and overflow bits. Pins 8 (FIFO/DIR) and 9 (FIFO READ) control the FIFO's operation. The FIFO's status can be monitored by reading pins 10 (FSTAT1) and 11 (FSTAT2).

When pin 8 (FIFO/DIR) has a logic "1" applied, the FIFO is inserted into the digital data path. When pin 8 has a logic "0" applied, the FIFO is transparent and the output data goes directly to the output three-state register (whose operation is controlled by pin 34 (ENABLE)). Read and write commands to the FIFO are ignored when the ADS-933 is operated in the "direct" mode. It takes a maximum of 20ns to switch the FIFO in or out of the ADS-933's digital data path.

FIFO Write and Read Modes

Once the FIFO has been enabled (pin 8 high), digital data is automatically written to it, regardless of the status of FIFO READ (pin 9). Assuming the FIFO is initially empty, it will accept data (18-bit words) from the next 16 consecutive A/D conversions. As a precaution, pin 9 (which controls the FIFO's READ function) should not be low when data is first written to an empty FIFO.

When the FIFO is initially empty, digital data from the first conversion (the "oldest" data) appears at the output of the FIFO immediately after the first conversion has been completed and remains there until the FIFO is read.

If the output three-state register has been enabled (logic "0" applied to pin 34), data from the first conversion will appear at the output of the ADS-933. Attempting to write a 17th word to a full FIFO will result in that data, and any subsequent conversion data, being lost.

Once the FIFO is full (indicated by FSTAT1 and FSTAT2 both equal to "1"), it can be read by dropping the FIFO READ line (pin 9) to a logic "0" and then applying a series of 15 rising edges to the read line. Since the first data word is already present at the FIFO output, the first read command (the first rising edge applied to FIFO READ) will bring data from the second conversion to the output. Each subsequent read command/rising edge brings the next word to the output lines. After the 15th rising edge brings the 16th data word to the FIFO output, the subsequent falling edge on READ will update the status outputs (after a 20ns maximum delay) to FSTAT1 = 0, FSTAT2 = 1 indicating that the FIFO is empty.

If a read command is issued after the FIFO empties, the last word (the 16th conversion) will remain present at the outputs.

FIFO Reset Feature

At any time, the FIFO can be reset to an empty state by putting the ADS-933 into its "direct" mode (logic "0" applied to pin 8, FIFO/DIR) and also applying a logic "0" to the FIFO READ line (pin 9). The empty status of the FIFO will be indicated by FSTAT1 going to a "0" and FSTAT2 going to a "1". The status outputs change 40ns after applying the control signals.

FIFO Status, FSTAT1 and FSTAT2

Monitor the status of the data in the FIFO by reading the two status pins, FSTAT1 (pin 10) and FSTAT2 (pin 11).

CONTENTS	FSTAT1	FSTAT2
Empty (0 words)	0	1
<half full (<8 words)	0	0
half-full or more (≥8 words)	1	0
Full (16 words)	1	1

Table 1. FIFO Delays

DELAY	PIN	TRANSITION	MIN.	TYP.	MAX.	UNITS
Direct mode to FIFO enabled	8	0→1	–	10	20	ns
FIFO enabled to direct mode	8	1→0	–	10	20	ns
FIFO READ to output data valid	9	0→1	–	–	40	ns
FIFO READ to status update when changing from <half full (1 word) to empty	9	1→0	–	–	20	ns
FIFO READ to status update when changing from ≥half full (8 words) to <half full (7 words)	9	0→1	–	–	110	ns
FIFO READ to status update when changing from full (16 words) to ≥half full (15 words)	9	0→1	–	–	190	ns
Falling edge of EOC to status update when writing first word into empty FIFO	32	1→0	–	–	190	ns
Falling edge of EOC to status update when changing FIFO from <half full (7 words) to ≥half full (8 words)	32	1→0	–	–	110	ns
Falling edge of EOC to status update when filling FIFO with 16th word	32	1→0	–	–	28	ns

CALIBRATION PROCEDURE

Connect the converter per Figure 2. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuits in Figure 2 are guaranteed to compensate for the ADS-933's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-933, offset adjusting is normally accomplished when the analog input is 0 minus ½ LSB (–42µV). See Table 2b for the proper bipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1½ LSB's (+2.749874V).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

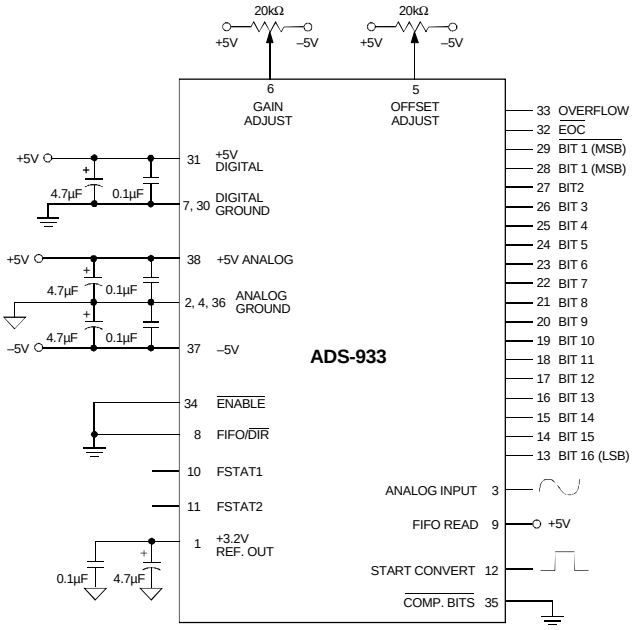


Figure 2. Connection Diagram

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 12) so that the converter is continuously converting.
2. For zero/offset adjust, apply –42µV to the ANALOG INPUT (pin 3).
3. Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 35 tied high (complementary offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 35 tied low (offset binary).
4. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$ (pin 29). With pin 35 tied low, adjust the trimpot until the output code flickers between all 0's and all 1's.

Gain Adjust Procedure

1. For gain adjust, apply +2.749874V to the ANALOG INPUT (pin 3).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 35 tied high (complementary offset binary) or until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 35 tied low (offset binary).
3. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$ (pin 29). With pin 35 tied low, adjust the gain trimpot until the output code flickers equally between 0111 1111 1111 1111 and 0111 1111 1111 1110.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2b.

Table 2a. Setting Output Coding Selection (Pin 35)

OUTPUT FORMAT	PIN 35 LOGIC LEVEL
Complementary Offset Binary	1
Offset Binary	0
Complementary Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	1
Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	0

Table 2b. Output Coding

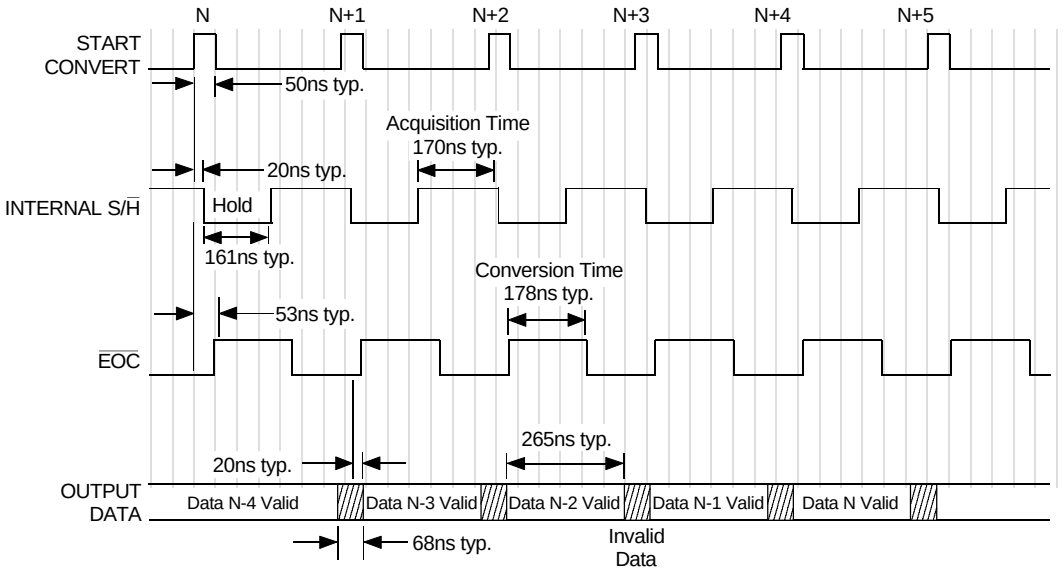
OUTPUT CODING				INPUT RANGE ±2.75V	BIPOLAR SCALE
MSB LSB	MSB LSB	$\overline{\text{MSB}}$ LSB	$\overline{\text{MSB}}$ LSB		
1111 1111 1111 1111	0000 0000 0000 0000	0111 1111 1111 1111	1000 0000 0000 0000	+2.749916	+FS –1 LSB
LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	+2.749874	+FS –1 1/2 LSB
1110 0000 0000 0000	0001 1111 1111 1111	0110 0000 0000 0000	1001 1111 1111 1111	+2.062500	+3/4 FS
1100 0000 0000 0000	0011 1111 1111 1111	0100 0000 0000 0000	1011 1111 1111 1111	+1.375000	+1/2 FS
1000 0000 0000 0000	0111 1111 1111 1111	0000 0000 0000 0000	1111 1111 1111 1111	0.000000	0
0111 1111 1111 1111	1000 000 000 0000	1111 1111 1111 1111	0000 0000 0000 0000	–0.000084	–1 LSB
0100 0000 0000 0000	1011 1111 1111 1111	1100 0000 0000 0000	0011 1111 1111 1111	–1.375000	–1/2 FS
0010 0000 0000 0000	1101 1111 1111 1111	1010 0000 0000 0000	0101 1111 1111 1111	–2.062500	–3/4 FS
0000 0000 0000 0001	1111 1111 1111 1110	1000 0000 0000 0001	0111 1111 1111 1110	–2.749916	–FS +1 LSB
LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	–2.749958	–FS + 1/2 LSB
0000 0000 0000 0000	1111 1111 1111 1111	1000 0000 0000 0000	0111 1111 1111 1111	–2.750000	–FS
OFFSET BINARY	COMP. OFF. BIN.	TWO'S COMP.	COMP. TWO'S COMP.		

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters," or contact DATEL directly, for additional information.



Notes: 1. Scale is approximately 50ns per division. fs = 3MHz.

2. This device has three pipeline delays. Four start convert pulses (clock cycles) must be applied for valid data from the first conversion to appear at the output of the A/D.

3. The start convert positive pulse width must be between either 20 and 60nsec or 200 and 310nsec (when sampling at 3MHz) to ensure proper operation. For sampling rates lower than 3MHz, the start pulse can be wider than 310nsec, however a minimum pulse width low of 20nsec should be maintained. A 3MHz clock with a 50nsec positive pulse width is used for all production testing.

Figure 3. ADS-933 Timing Diagram

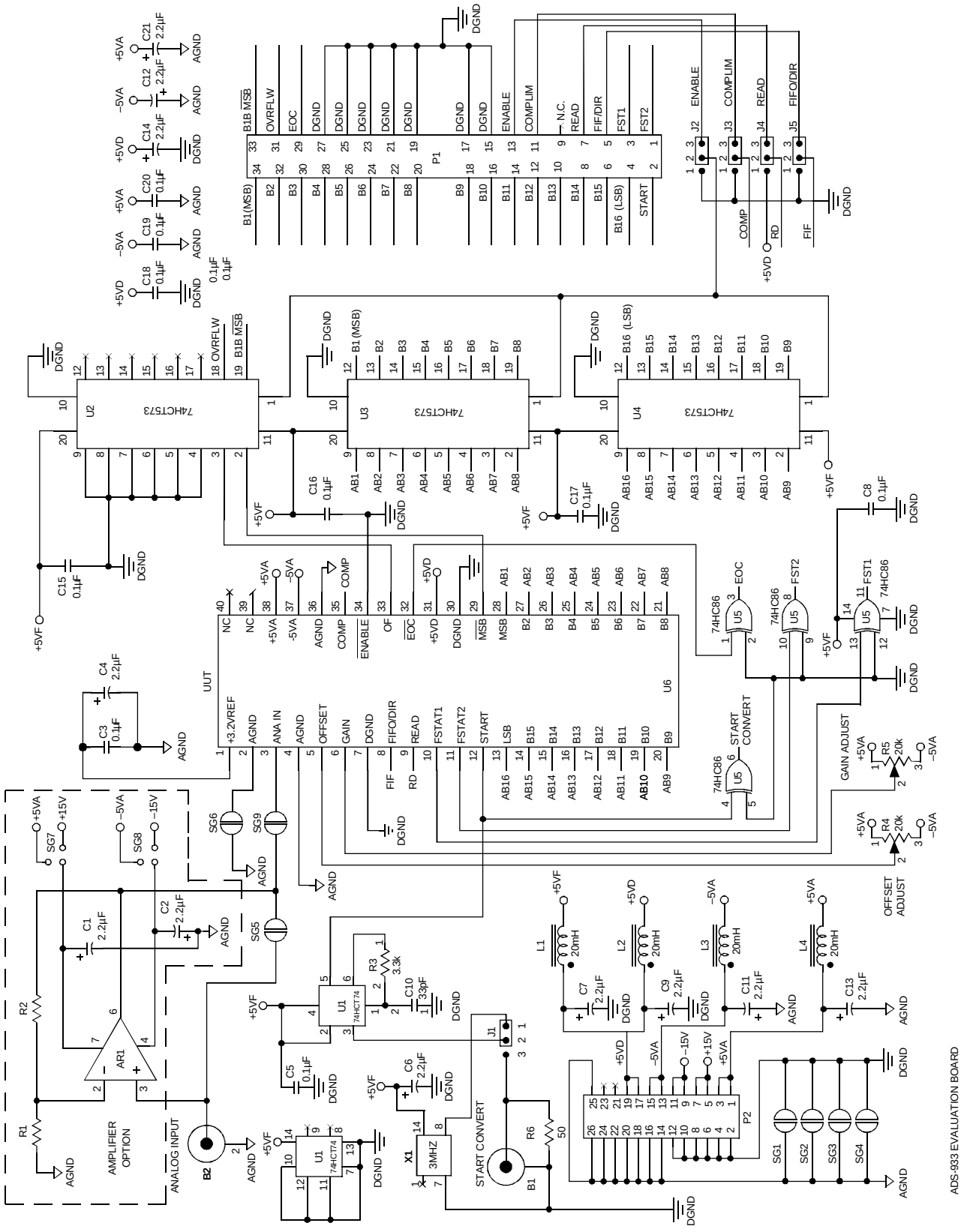
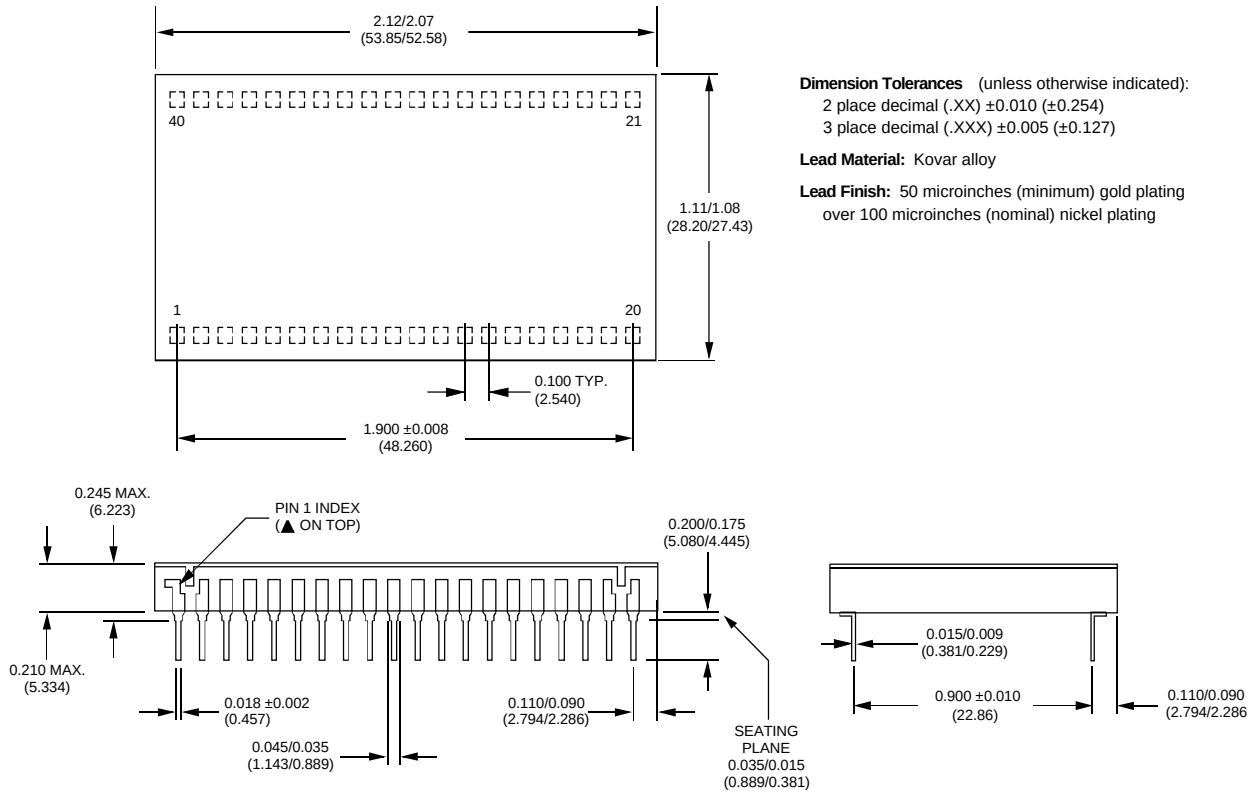


Figure 5. ADS-933 Evaluation Board Schematic.

MECHANICAL DIMENSIONS INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-933MC	0 to +70°C	Bipolar (±2.75V)
ADS-933MM	–55 to +125°C	Bipolar (±2.75V)

ACCESSORIES

ADS-B933	Evaluation Board (without ADS-933)
HS-40	Heat Sink for all ADS-933 models

Receptacles for PC board mounting can be ordered through AMP, Inc., Part # 3-331272-8 (Component Lead Socket), 40 required. For MIL-STD-883 product, or surface mount packaging, contact DATEL.

INNOVATION and EXCELLENCE

ISO 9001 REGISTERED

DS-0367P 05/97

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