695 MHz to 2700 MHz, Quadrature Demodulator with Integrated Fractional-N PLL and VCO

Data Sheet

ADRF6820

FEATURES

I/Q demodulator with integrated fractional-N PLL
RF input frequency range: 695 MHz to 2700 MHz
Internal LO frequency range: 356.25 MHz to 2850 MHz
Input P1dB: 14.5 dBm at 1900 MHz RF
Input IP3: 35 dBm at 1900 MHz RF
Programmable HD3/IP3 trim
Single pole, double throw (SPDT) RF input switch
RF digital step attenuation range: 0 dB to 15 dB
Integrated RF tunable balun for single-ended 50 Ω input
Multicore integrated VCO
Demodulated 1 dB bandwidth: 600 MHz
Demodulated 3 dB bandwidth: 1400 MHz
4 selectable baseband gain and bandwidth modes
Digital programmable LO phase offset and dc nulling
Programmable via 3-wire serial port interface (SPI)
40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

Cellular W-CDMA/GSM/LTE
Digital predistortion (DPD) receivers
Microwave point-to-point radios

FUNCTIONAL BLOCK DIAGRAM

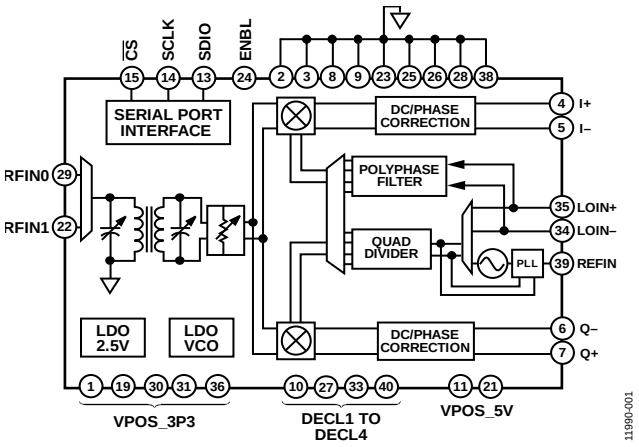


Figure 1.

GENERAL DESCRIPTION

The ADRF6820 is a highly integrated demodulator and synthesizer ideally suited for next generation communication systems. The feature rich device consists of a high linearity broadband I/Q demodulator, an integrated fractional-N phase-locked loop (PLL), and a low phase noise multicore, voltage controlled oscillator (VCO). The ADRF6820 also integrates a 2:1 RF switch, an on-chip tunable RF balun, a programmable RF attenuator, and two low dropout (LDO) regulators. This highly integrated device fits within a small 6 mm × 6 mm footprint.

The high isolation 2:1 RF switch and on-chip tunable RF balun enable the ADRF6820 to support two single-ended, 50 Ω terminated RF inputs. A programmable attenuator ensures an optimal differential RF input level to the high linearity demodulator core. The integrated attenuator offers an attenuation range of 0 dB to 15 dB with a step size of 1 dB.

The ADRF6820 offers two alternatives for generating the differential local oscillator (LO) input signal: externally via a high frequency, low phase noise LO signal or internally via the on-chip fractional-N synthesizer. The integrated synthesizer enables continuous LO coverage from 356.25 MHz to 2850 MHz. The PLL reference input can support a wide frequency range because the divide or multiplication blocks can increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD).

When selected, the output of the internal fractional-N synthesizer is applied to a divide-by-2 quadrature phase splitter. From the external LO path, a 1× LO signal can be applied to the built-in polyphase filter, or a 2× LO signal can be used with the divide-by-2 quadrature phase splitter to generate the quadrature LO inputs to the mixers.

The ADRF6820 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, RoHS-compliant, 6 mm × 6 mm LFCSP package with an exposed paddle. Performance is specified over the −40°C to +85°C temperature range.

Rev. C Document Feedback
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REVISION HISTORY

8/2016—Rev. B to Rev. C

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Updated Outline Dimensions ... 45

4/2015—Rev. A to Rev. B

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12/2013—Revision 0: Initial Version

SPECIFICATIONS

SYSTEM SPECIFICATIONS

VPOS_5V = 5 V, VPOS_3P3 = 3.3 V, ambient temperature (T_A) = 25°C, high-side LO injection, internal LO mode, RF attenuation range = 0 dB, input IP2/input IP3 tone spacing = 5 MHz and −5 dBm per tone, f_{IF} = 40 MHz for BWSEL = 0 and f_{IF} = 200 MHz for BWSEL = 2.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT					MHz
RF Frequency Range		695		2700	MHz
Return Loss			15		dB
Input Impedance			50		Ω
Input Power				18	dBm
LO FREQUENCY					MHz
Internal LO Frequency Range		356.25		2850	MHz
External LO Frequency Range		350		6000	MHz
LO Input Level		−6		+6	dBm
LO Input Impedance			50		Ω
LO Harmonic Rejection[1]	2× LO at output of external LO (LO = 1900 MHz)		−30		dBc
SUPPLY VOLTAGE[2]					V
VPOS_3P3		3.1	3.3	3.5	V
VPOS_5V		4.7	5.0	5.25	V
RF ATTENUATION RANGE	Step size = 1 dB	0		15	dB
Digital Step Attenuator (DSA)	Step error between two adjacent DSA code		±0.5		dB
	Attenuation accuracy		±1.0		dB
IF OUTPUTS					
Gain Flatness	Across any 20 MHz bandwidth		0.2		dB
Quadrature Phase Error	No correction applied		1		Degrees
I/Q Amplitude Imbalance	No correction applied		0.1		dB
Output DC Offset	No correction applied		20		mV
Output Common Mode		1.5		2.4	V
I/Q Output Impedance	Differential		50		Ω
TOTAL POWER CONSUMPTION	External LO, polyphase filter LO path		1100		mW
	Internal PLL/VCO, 2× LO path		1400		mW

[1] Measured with a nominal device with normal supply and temperature.
[2] For information about power supply sequencing, see the Power Supply Sequencing section.

DYNAMIC PERFORMANCE

Table 2.

		BWSEL0[1]			BWSEL2[1]			
Parameter	Test Conditions/Comments	Min	Typ	Max	Min	Typ	Max	Unit
DEMODULATION BANDWIDTH	1 dB bandwidth, f_{LO} = 2100 MHz		240			600		MHz
	3 dB bandwidth, f_{LO} = 2100 MHz		480			1400		MHz
f_{RF} = 900 MHz								
Conversion Gain	Voltage gain		+3.5			−2.5		dB
Input P1dB			11			14		dBm
Input IP3			34			38		dBm
Input IP2			65			61		dBm
Noise Figure	Internal LO		17			19		dB
	External LO		16			18.5		dB

Parameter	Test Conditions/Comments	BWSEL0[1] Min	BWSEL0[1] Typ	BWSEL0[1] Max	BWSEL2[1] Min	BWSEL2[1] Typ	BWSEL2[1] Max	Unit
LO to RF Leakage			−82			−82		dBm
RF to LO Leakage			−67			−67		dBm
LO to IF Leakage	With respect to −5 dBm RF input power		−78.5			−78.5		dBc
RF to IF Leakage	With respect to −5 dBm RF input power		−49			−49		dBc
Isolation[2]	Isolation between RFIN0 to RFIN1		−55			−55		dBc
	Isolation between RFIN1 to RFIN0		−55			−55		dBc
f_{RF} = 1900 MHz								
Conversion Gain	Voltage gain		+3			−3		dB
Input P1dB			12			14.5		dBm
Input IP3			33			35		dBm
Input IP2			58			57		dBm
Noise Figure	Internal LO		18			20		dB
	External LO		17.5			19.5		dB
LO to RF Leakage			−75			−75		dBm
RF to LO Leakage			−64			−64		dBm
LO to IF Leakage	With respect to −5 dBm RF input power		−64.5			−64.5		dBc
RF to IF Leakage	With respect to −5 dBm RF input power		−43.5			−43.5		dBc
Isolation[2]	Isolation between RFIN0 to RFIN1		−51			−51		dBc
	Isolation between RFIN1 to RFIN0		−39			−39		dBc
f_{RF} = 2100 MHz								
Conversion Gain	Voltage gain		+2.5			−3		dB
Input P1dB			12			15.5		dBm
Input IP3			37			34		dBm
Input IP2			58			55		dBm
Noise Figure	Internal LO		18			20.5		dB
	External LO		18			20		dB
LO to RF Leakage			−72.5			−72.5		dBm
RF to LO Leakage			−62			−62		dBm
LO to IF Leakage	With respect to −5 dBm RF input power		−71			−71		dBc
RF to IF Leakage	With respect to −5 dBm RF input power		−45			−45		dBc
Isolation[2]	Isolation between RFIN0 to RFIN1		−48.5			−48.5		dBc
	Isolation between RFIN1 to RFIN0		−36.5			−36.5		dBc
f_{RF} = 2650 MHz								
Conversion Gain	Voltage gain		+1.5			−4		dB
Input P1dB			13			16.5		dBm
Input IP3			33			33		dBm
Input IP2			64			55		dBm
Noise Figure	Internal LO		19.5			22		dB
	External LO		19.5			21.5		dB
LO to RF Leakage			−70			−70		dBm
RF to LO Leakage			−57			−57		dBm
LO to IF Leakage	With respect to −5 dBm RF input power		−76			−76		dBc
RF to IF Leakage	With respect to −5 dBm RF input power		−46			−46		dBc
Isolation[2]	Isolation between RFIN0 to RFIN1		−40.5			−40.5		dBc
	Isolation between RFIN1 to RFIN0		−33			−33		dBc

[1] See Table 15.
[2] This is the isolation between the RF inputs. An input signal was applied to RFIN0, while RFIN1 was terminated with 50 Ω. The IF signal amplitude was measured at the baseband output. Next, the internal switch was configured for RFIN1, and the feedthrough was measured as a delta from the fundamental. This difference is recorded as the isolation between RFIN0 and RFIN1.

SYNTHESIZER/PLL SPECIFICATIONS

VPOS_5V = 5 V, VPOS_3P3 = 3.3 V, ambient temperature (T_A) = 25°C, f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm, f_{PFD} = 38.4 MHz, loop filter bandwidth = 20 kHz, measured at LO output, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
Frequency		12		320	MHz
Amplitude			4	14	dBm
PLL Step Size[1]	PFD = 30.72 MHz	468.76			Hz
PLL Lock Time[2]	PFD = 30.72 MHz, charge pump = 500 µA, loop bandwidth = 40 kHz, antibacklash delay = 0.5 ns, charge pump bleed current = 78.125 µA down		5		ms
PFD FREQUENCY		24		40	MHz
INTERNAL VCO RANGE		2850		5700	MHz
REFERENCE SPURS	f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz, f_{LO} = 1809.6 MHz				
	$f_{PFD}/4$		<−100		dBc
	$f_{PFD}/2$		<−100		dBc
	$f_{PFD} \times 1$		−90.67		dBc
	$f_{PFD} \times 2$		−95		dBc
	$f_{PFD} \times 3$		−97		dBc
	$f_{PFD} \times 4$		<−100		dBc
	$f_{PFD} \times 5$		<−100		dBc
INTEGRATED PHASE NOISE[3]	1 kHz to 40 MHz integration bandwidth, PFD = 38.4 MHz, f_{REF} = 153.6 MHz, divide by 4, charge pump = 250 µA, loop bandwidth = 20 kHz, antibacklash delay = 0 ns, charge pump bleed current = 46.8 µA down, LO frequency = 1562.5 MHz		0.6		°rms
CLOSED-LOOP PERFORMANCE	f_{LO} = 1809.6, f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz				
20 kHz Loop Filter	10 kHz offset		−94.7		dBc/Hz
	20 kHz offset		−95.8		dBc/Hz
	100 kHz offset		−113		dBc/Hz
	200 kHz offset		−122.4		dBc/Hz
	600 kHz offset		−136.5		dBc/Hz
	1 MHz offset		−141.5		dBc/Hz
	10 MHz offset		−153.3		dBc/Hz
	40 MHz offset		−154.6		dBc/Hz

[1] Minimum PLL step size is a function of PFD. Value shown is based on PFD = 30.72 MHz, LO_DIV = 2, and the formula $f_{PFD}/65535 \times 2/LO_DIV$.
[2] Lock time is defined as the time it takes from the end of a register write for a change in frequency to the point where the frequency of the output is within 500 Hz of the intended frequency.
[3] Measured with a nominal device with normal supply and temperature.

DIGITAL LOGIC SPECIFICATIONS

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage High, V_{IH}		1.4			V
Input Voltage Low, V_{IL}				0.70	V
Output Voltage High, V_{OH}	I_{OH} = −100 µA	2.3			V
Output Voltage Low, V_{OL}	I_{OL} = 100 µA	0.2			V
Serial Clock Period	t_{SCLK}	38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}	8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}	8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	t_S	10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	t_H	10			ns
Minimum Period SCLK in a Logic High State	t_{HIGH}	10			ns
Minimum Period SCLK in a Logic Low State	t_{LOW}	10			ns
Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}			231	ns
Maximum Time Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	t_Z			5	ns

Timing Diagram

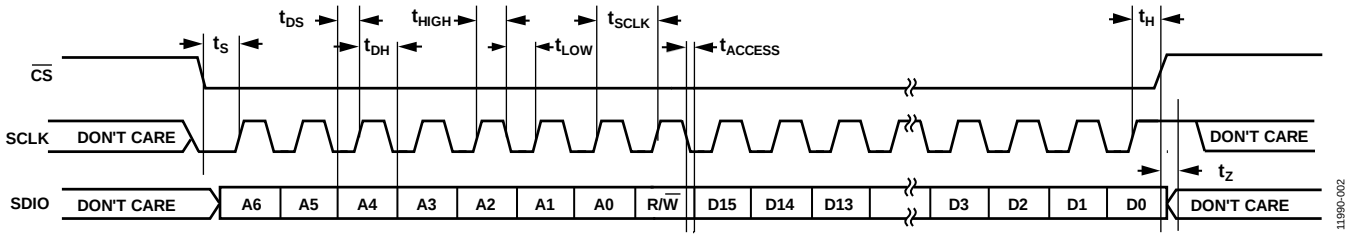


Figure 2. Setup and Hold Timing Measurements

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VPOS_5V	−0.5 V to +5.5 V
VPOS_3P3	−0.3 V to +3.6 V
VOCM	−0.3 V to +3.6 V
$\overline{CS}$, SCLK, SDIO	−0.3 V to +3.6 V
RFSW	−0.3 V to +3.6 V
RFIN0, RFIN1	2.5 V peak, ac-coupled
ENBL	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
LOIN−, LOIN+	16 dBm, differential
REFIN	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	31.93	1.12	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

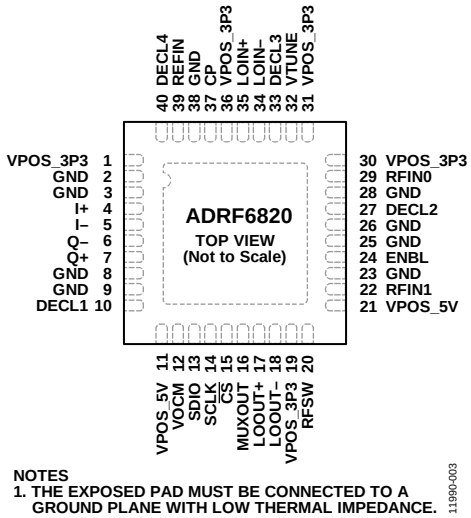


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 19, 30, 31, 36	VPOS_3P3	3.3 V Power Supply.
2, 3, 8, 9, 23, 25, 26, 28, 38	GND	Ground.
4, 5	I+, I–	Differential Baseband Outputs, I Channel.
6, 7	Q–, Q+	Differential Baseband Outputs, Q Channel.
10	DECL1	Decoupling for Mixer Load. Connect a 0.22 µF capacitor from DECL1 to GND.
11, 21	VPOS_5V	5 V Power Supply.
12	VOCM	Reference Voltage Input. This pin sets the output common-mode level.
13	SDIO	SPI Data.
14	SCLK	SPI Clock.
15	$\overline{CS}$	Chip Select, Active Low.
16	MUXOUT	Multiplexer Output. Output pin providing the PLL reference signal or the PLL lock detect.
17, 18	LOOUT+, LOOUT–	Differential LO Outputs.
20	RFSW	RF Switch Select. Selects between RFIN0 and RFIN1.
22, 29	RFIN1, RFIN0	RF Inputs. Single pole, double throw switch input.
24	ENBL	Enable, Active High.
27, 33	DECL2, DECL3	VCO LDO Decoupling.
32	VTUNE	VCO Tuning Voltage Input.
34, 35	LOIN–, LOIN+	Differential LO Inputs.
37	CP	PLL Charge Pump Output.
39	REFIN	PLL Reference Input.
40	DECL4	2.5 V LDO Decoupling.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

VPOS_5V = 5 V, VPOS_3P3 = 3.3 V, RFDSA_SEL = 0, RFSW = 0 (RFIN0), high-side LO, −5 dB per tone for two-tone measurement with 5 MHz tone spacing, unless otherwise noted. For BWSEL0, f_{IF} = 40 MHz, and for BWSEL2, f_{IF} = 200 MHz. For BAL_CIN, BAL_COUT, MIX_BIAS, DEMOD_RDAC, and DEMOD_CDAC, refer to Table 16.

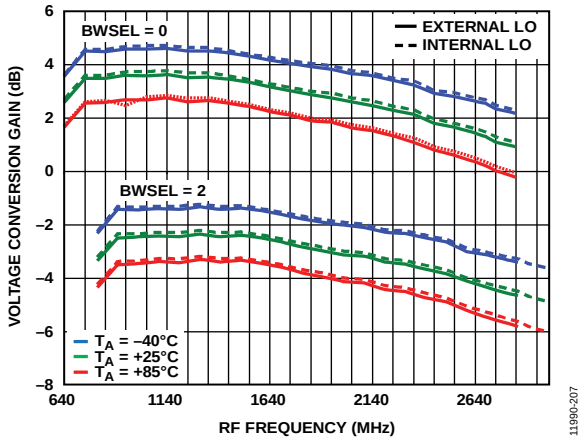


Figure 4. Voltage Conversion Gain vs. RF Frequency over Temperature

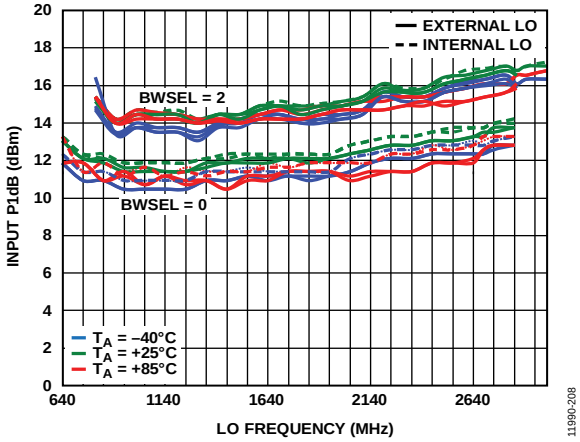


Figure 7. Input P1dB vs. LO Frequency

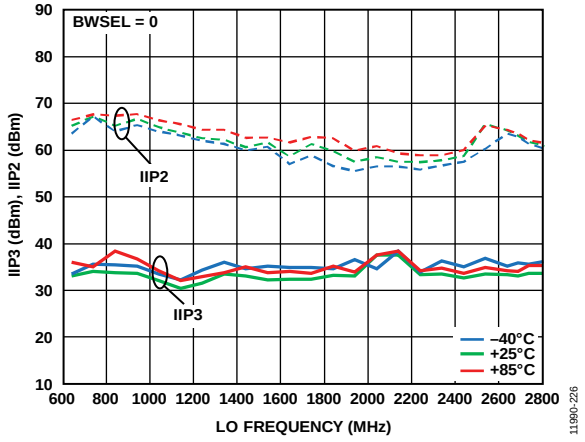


Figure 5. Input IP3 (IIP3) and Input IP2 (IIP2) vs. LO Frequency over Temperature, BWSEL = 0

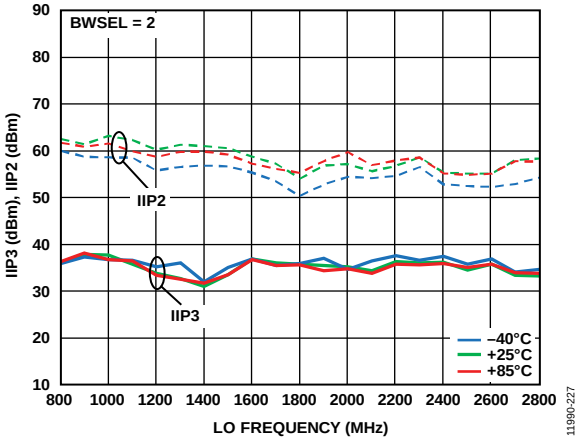


Figure 8. Input IP3 (IIP3) and Input IP2 (IIP2) vs. LO Frequency over Temperature, BWSEL = 2

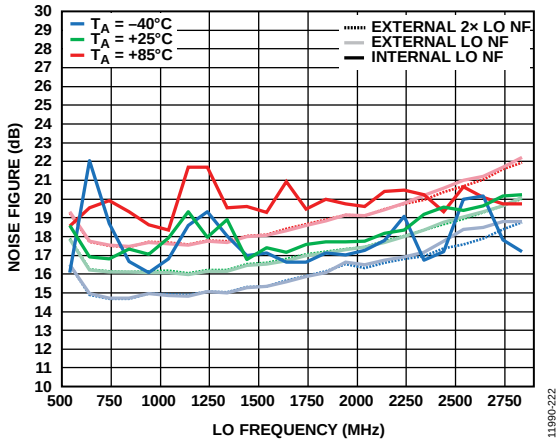


Figure 6. Noise Figure vs. LO Frequency, BWSEL = 0

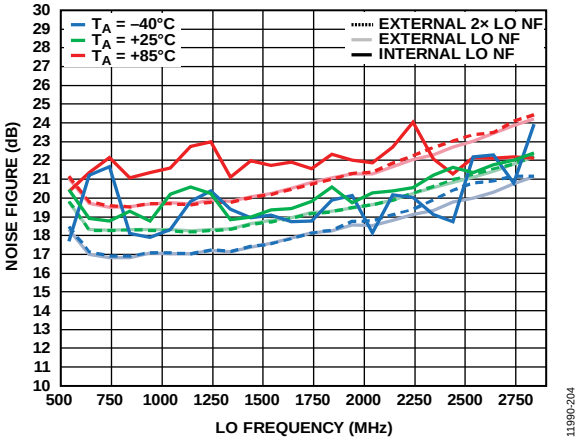


Figure 9. Noise Figure vs. LO Frequency, BWSEL = 2

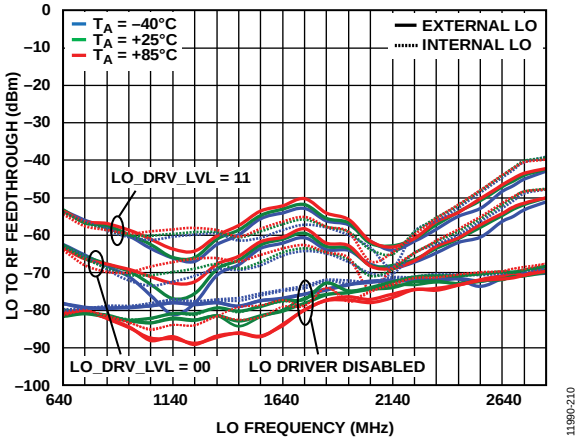


Figure 10. LO to RF Feedthrough vs. LO Frequency

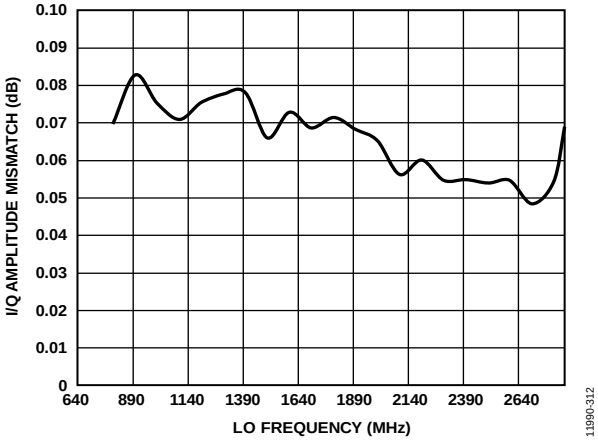


Figure 13. I/Q Amplitude Mismatch vs. LO Frequency

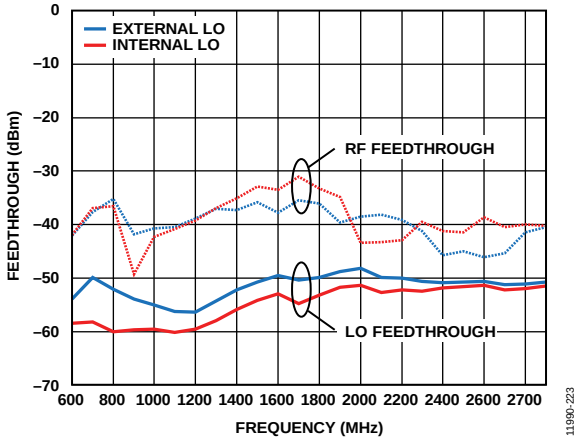


Figure 11. RF and LO Feedthrough to IF Output, RF Input = –5 dBm

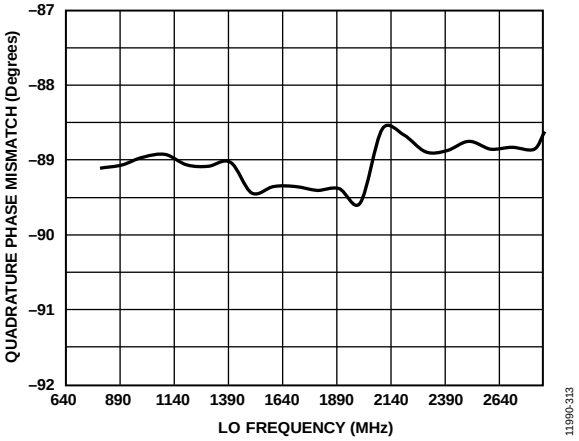


Figure 14. Quadrature Phase Mismatch vs. LO Frequency

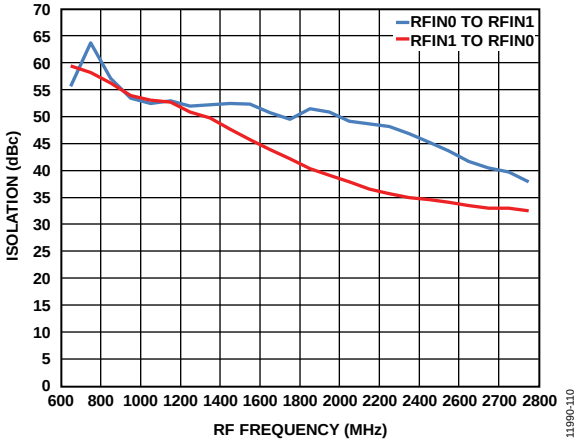


Figure 12. Switch Isolation vs. RF Frequency

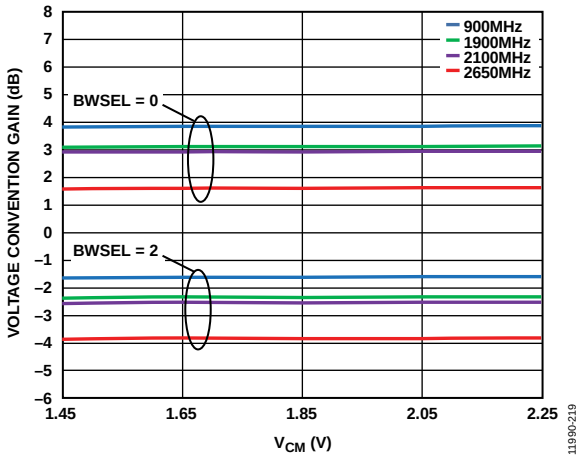


Figure 15. Gain vs. Common-Mode Voltage (V_{CM}) for f_{RF} = 900 MHz, f_{RF} = 1900 MHz, f_{RF} = 2100 MHz, and f_{RF} = 2650 MHz for BWSEL = 0 and BWSEL = 2

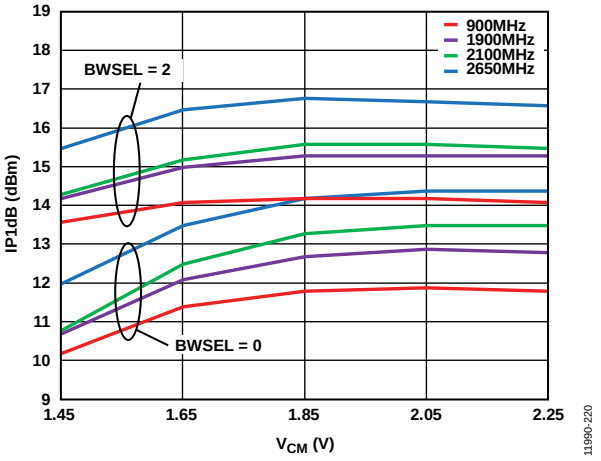


Figure 16. Input P1dB (IP1dB) vs. Common-Mode Voltage (V_{CM}) for f_{RF} = 900 MHz, f_{RF} = 1900 MHz, f_{RF} = 2100 MHz, and f_{RF} = 2650 MHz

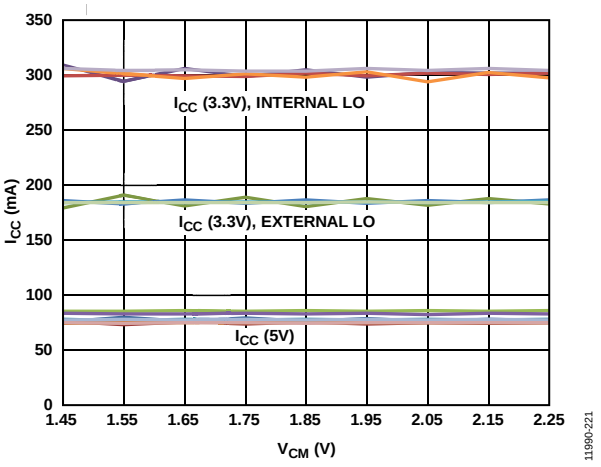


Figure 17. Current Consumption (I_{CC}) vs. Common-Mode Voltage (V_{CM}), Internal and External LO, f_{RF} = 900 MHz, f_{RF} = 1900 MHz, f_{RF} = 2100 MHz, f_{RF} = 2100 MHz, and f_{RF} = 2650 MHz

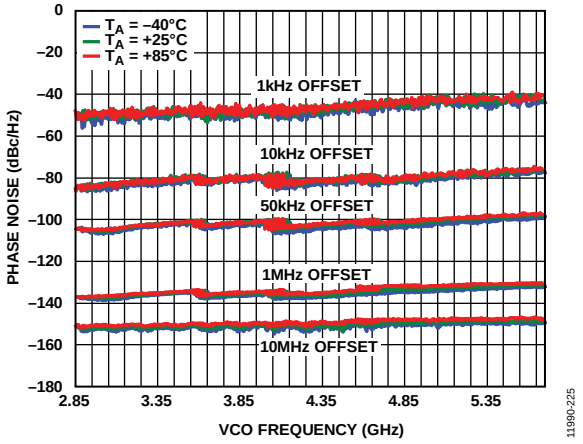


Figure 18. Open-Loop Phase Noise for 1 kHz, 10 kHz, 50 kHz, 1 MHz, and 10 MHz Offsets

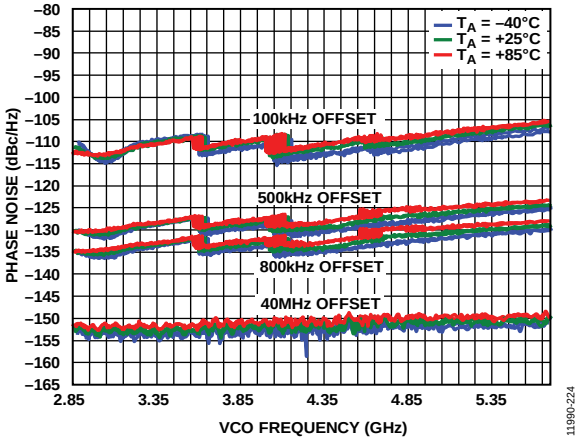


Figure 19. Open-Loop Phase Noise for 100 kHz, 500 kHz, 800 kHz, and 40 MHz Offsets

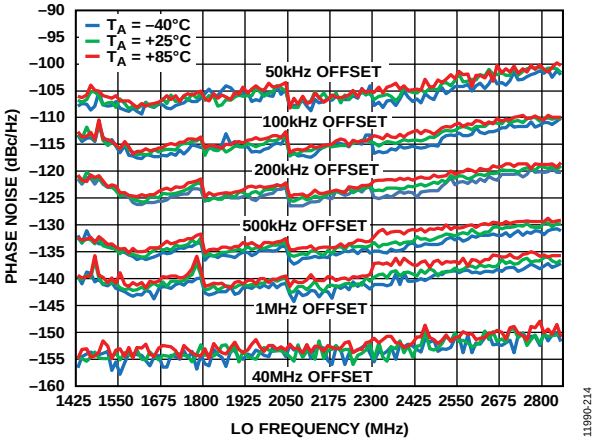


Figure 20. Closed-Loop Phase Noise vs. LO Frequency, 20 kHz Bandwidth Loop Filter, Measured with DIV4_EN = 1 (Divide by 2)

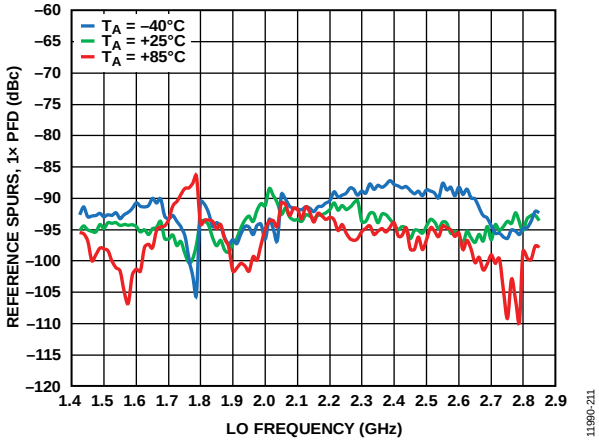


Figure 21. 1× PFD Spurs vs. LO Frequency, Measured with DIV4_EN = 1 (Divide by 2)

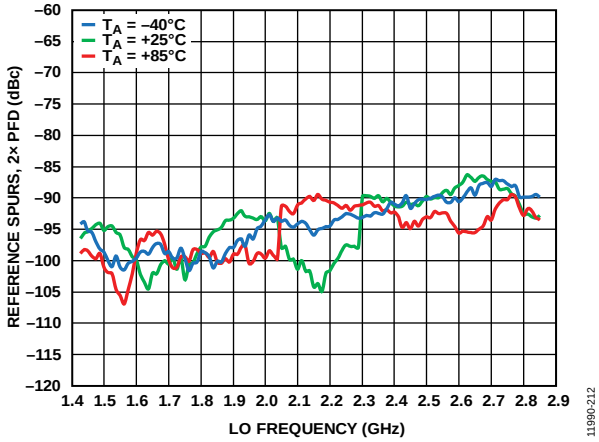


Figure 22. 2× PFD Spurs vs. LO Frequency, Measured with DIV4_EN = 1 (Divide by 2)

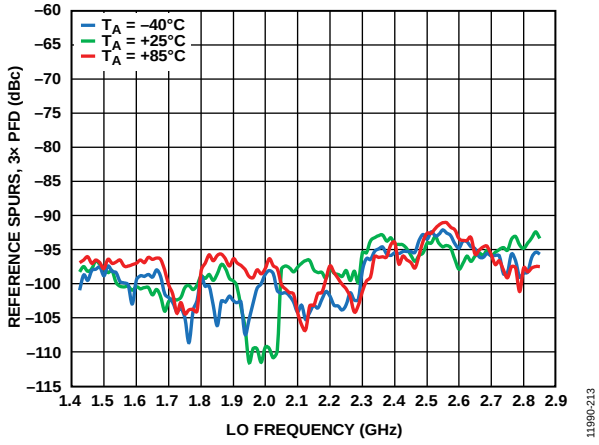


Figure 23. 3× PFD Spurs vs. LO Frequency, Measured with DIV4_EN = 1 (Divide by 2)

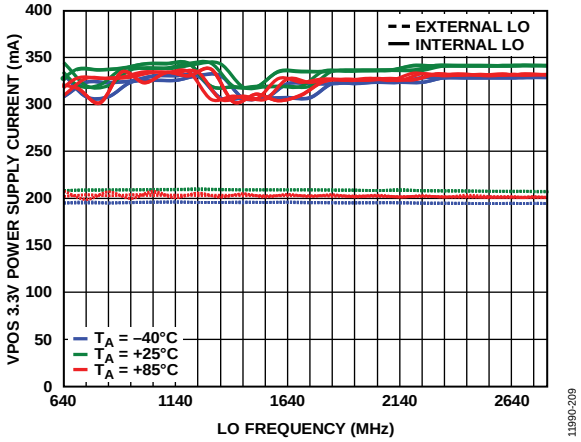


Figure 24. VPOS_3P3 Power Supply Current vs. LO Frequency

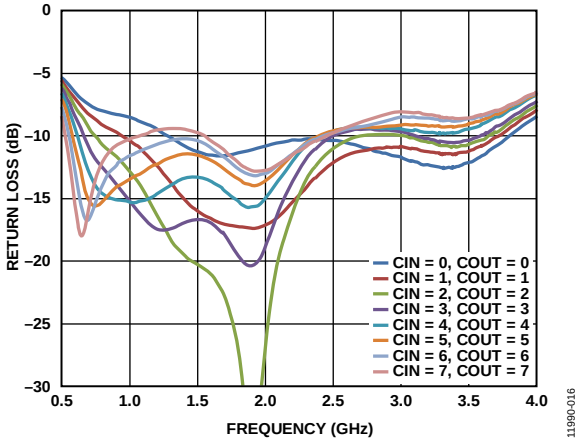


Figure 25. RFIN0/RFIN1 Return Loss for Multiple BAL_CIN and BAL_COUT Combinations

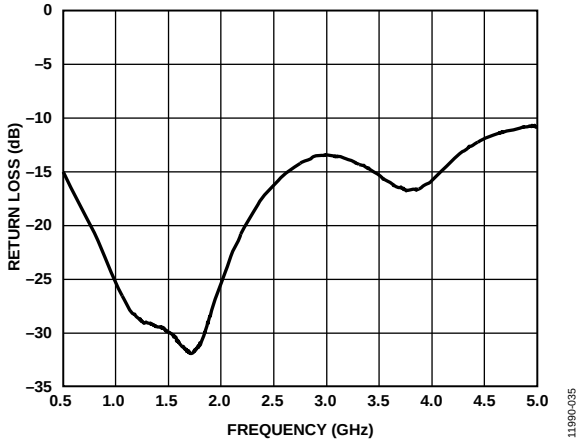


Figure 26. Return Loss of Unused RFINx Port vs. Frequency

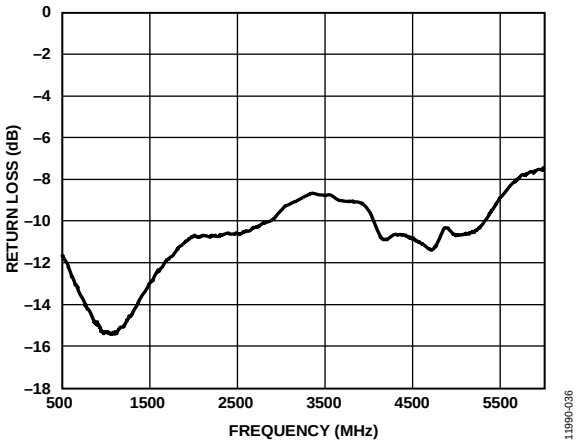


Figure 27. LO Input Return Loss vs. Frequency

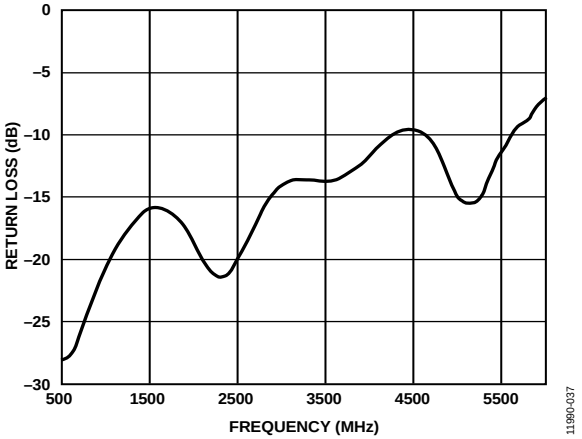


Figure 28. LO Output Return Loss vs. Frequency

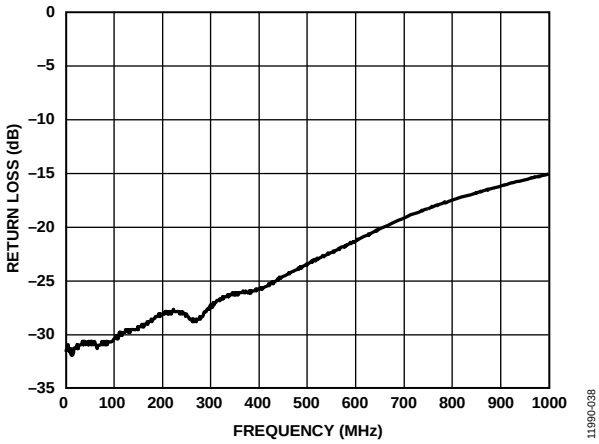


Figure 29. I/Q Return Loss vs. Frequency

THEORY OF OPERATION

The ADRF6820 integrates many of the essential building blocks for a high bandwidth quadrature demodulator and receiver, especially for the feedback downconverter path for the digital predistortion in cellular base stations. The main features include a single pole, double throw (SPDT) RF input switch, a variable RF attenuator, a tunable balun, a pair of active mixers, and two baseband buffers. Additionally, the local oscillator (LO) signals for the mixers are generated by a fractional-N synthesizer and a multicore voltage controlled oscillator (VCO), covering an octave frequency range with low phase noise. A pair of flip-flops then divides the LO frequency by two and generates the in-phase and quadrature phase LO signals to drive the mixers. The synthesizer uses a fractional-N phase-locked loop (PLL) with additional frequency dividers to enable continuous LO coverage from 356.25 MHz to 2850 MHz. Alternatively, a polyphase phase splitter is also available to generate LO signals in quadrature from an external LO source.

Putting all the building blocks of the ADRF6820 together, the signal path through the device starts at one of two RF inputs selected by the input multiplexer (mux) and is converted to a differential signal via a tunable balun. The differential RF signal is attenuated to an optimal input level via the digital step attenuator with 15 dB of attenuation range in 1 dB steps. The RF signal is then mixed with the LO signal in the Gilbert cell mixers down to an intermediate frequency (IF) or baseband. The emitter followers further buffer the outputs of the mixers with an adjustable output common-mode level.

The different sections of the ADRF6820 are controlled through registers programmable via a serial port interface (SPI).

RF INPUT SWITCH

The ADRF6820 integrates a SPDT switch where one of two RF inputs is selected. Selection of the desired RF input is achieved externally via a control pin or serially via register writes to the SPI. When compared to the serial write approach, pin control allows faster switching between the RF inputs. Using the RFSW pin (Pin 20), the RF input can switch within 100 ns. When serial port control is used, the switching time is dominated by the latency of the SPI programming, which is 2.4 µs minimum for a 10 MHz serial clock.

The RFSW_MUX bit (Register 0x23, Bit 11) selects whether the RF input switch is controlled via the external pins or via the SPI (see Table 8). By default at power-up, the device is configured for pin control. Connecting RFSW to GND selects RFIN0, and connecting RFSW to VPOS_3P3 selects RFIN1. In serial mode control, writing to the RFSW_SEL bit (Register 0x23, Bit 9) allows selection of one of the two RF inputs. If only one RFINx port is used, the unused RF input must be properly terminated to improve isolation. The RFIN0/REFIN1 ports are internally terminated with 50 Ω resistors, and the dc level is 2.5 V. To avoid disrupting the dc level, the recommended termination is a dc blocking capacitor to GND. Figure 30 shows the recommended configuration when only RFIN0 is selected.

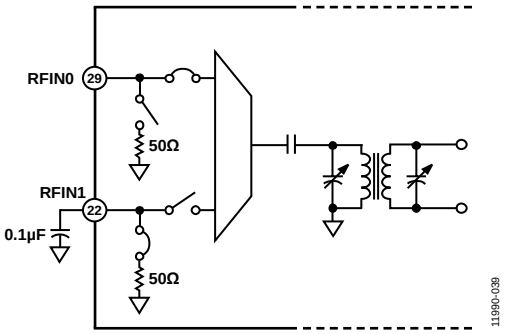


Figure 30. Terminating Unused RF Input Ports

TUNABLE BALUN

The ADRF6820 integrates a programmable balun operating over a 695 MHz to 2700 MHz frequency range. The tunable balun offers the benefit of ease of drivability with single-ended, 50 Ω RF inputs, and the single-ended-to-differential conversion of the integrated balun provides additional common-mode noise rejection.

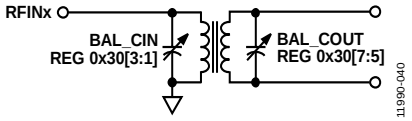


Figure 31. Integrated Tunable Balun

To accomplish RF balun tuning, switch the parallel capacitances on the primary and secondary sides of the balun by writing to Register 0x30. The added capacitance in parallel with the inductive windings of the balun changes the resonant frequency of the inductor capacitor (LC) tank. Therefore, selecting the proper combination of BAL_CIN (Register 0x30, Bits[3:1]) and BAL_COUT (Register 0x30, Bits[7:5]) sets the desired frequency and optimizes gain. Under most circumstances, the input and output capacitances are tuned together; however, sometimes for matching reasons, it is advantageous to tune them independently.

Table 8. RF Input Selection Table

RFSW_MUX (Register 0x23, Bit 11)	RFSW_SEL SPI Control (Register 0x23, Bit 9)	RFSW Pin Control (Pin 20)	RF Input
0	0	X[1]	RFIN0
0	1	X[1]	RFIN1
1	X[1]	0	RFIN0
1	X[1]	1	RFIN1

[1] X = don't care.

RF ATTENUATOR

The RF digital step attenuator (RFDSA) follows the tunable balun, and the attenuation range is 0 dB to 15 dB with a step size of 1 dB. The RFDSA_SEL bits (Register 0x23, Bits[8:5]) in the DGA_CTL register determine the setting of the RFDSA.

LO GENERATION BLOCK

The ADRF6820 supports the use of both internal and external LO signals for the mixers. The internal LO is generated by an on-chip VCO, which is tunable over an octave frequency range of 2850 MHz to 5700 MHz. The output of the VCO is phase locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce in-phase and quadrature phase LO signals over the 356.25 MHz to 2850 MHz frequency range to drive the mixers, steer the VCO outputs through a combination of frequency dividers, as shown in Figure 32.

Alternatively, an external signal can be used with the dividers or a polyphase phase splitter to generate the LO signals in quadrature to the mixers. In demanding applications that require the lowest possible phase noise performance, it may be necessary to source the LO signal externally. The different methods in quadrature LO generation and the control register programming needed are listed in Table 9.

Internal LO Mode

For internal LO mode, the ADRF6820 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 32, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and divides it down by a factor of 2, 4, or 8 or multiplies it by a factor of 1 or a factor of 2, and then passes it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends an up/down signal to the charge pump if the VCO signal is slow/fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (VTUNE).

The ADRF6820 integrates four VCO cores covering an octave range of 2.85 GHz to 5.7 GHz.

Table 9 lists the frequency range covered by each VCO. The desired VCO can be selected by addressing the VCO_SEL bits (Register 0x22, Bits[2:0]).

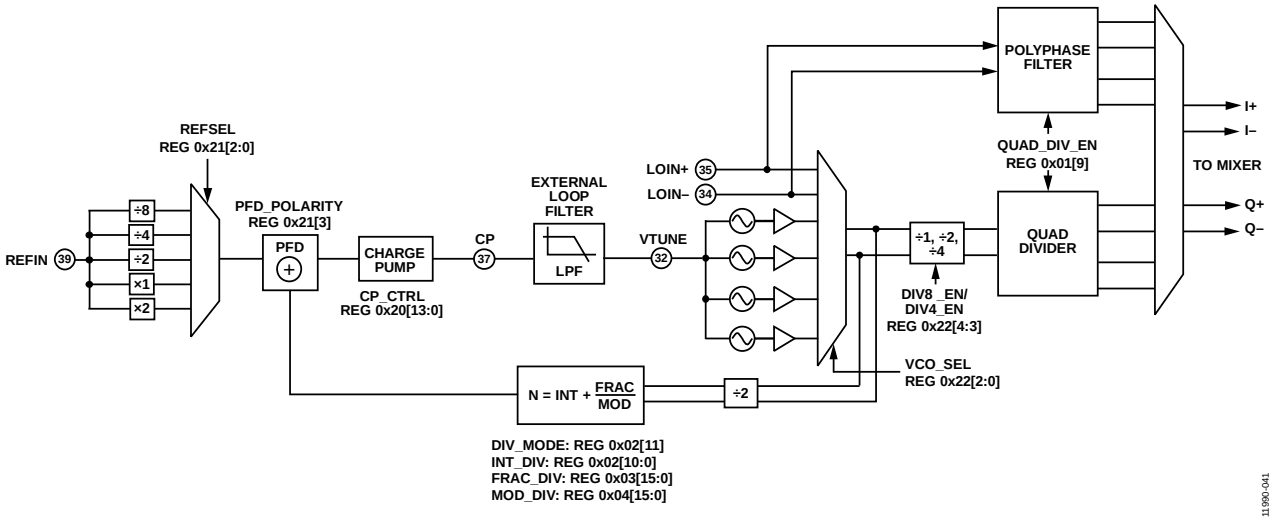


Figure 32. LO Generation Block Diagram

Table 9. LO Mode Selection

LO Selection	f_{VCO} or f_{EXT} (GHz)	Quadrature Generation	QUAD_DIV_EN, Register 0x01[9]	LO Enables, Register 0x01[6:0]	VCO_SEL, Register 0x22[2:0]
Internal (VCO)	2.85 to 3.5	Divide by 2	1	111 111X	011
	3.5 to 4.02	Divide by 2	1	111 111X	010
	4.02 to 4.6	Divide by 2	1	111 111X	001
	4.6 to 5.7	Divide by 2	1	111 111X	000
External (2× LO)	0.7 to 6.0	Divide by 2	1	101 000X	1XX
External (1× LO)	0.35 to 3.5	Polyphase	0	000 000X	XXX

LO Frequency and Dividers

The signal coming from the VCO or the external LO inputs goes through a series of dividers before it is buffered to drive the active mixers. Two programmable divide-by-two stages divide the frequency of the incoming signal by 1, 2, or 4 before reaching the quadrature divider that further divides the signal frequency by 2 to generate the in-phase and quadrature-phase LO signals for the mixers. The control bits (Register 0x22, Bits[4:3]) needed to select the different LO frequency ranges are listed in Table 10.

Table 10. LO Frequency and Dividers

LO Frequency Range (MHz)	f_{VCO}/f_{LO} or $f_{EXT\ LO}/f_{LO}$	DIV8_EN (Register 0x22, Bit 4)	DIV4_EN (Register 0x22, Bit 3)
1425 to 2850	2	0	0
712.5 to 1425	4	0	1
356.25 to 712.5	8	1	1

PLL Frequency Programming

The N divider divides down the differential VCO signal to the PFD frequency. The N divider can be configured for fractional or integer mode by addressing the DIV_MODE bit (Register 0x02, Bit 11). The default configuration is set for fractional mode. Use the following equations to determine the N value and PLL frequency:

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{f_{PFD} \times 2 \times N}{LO_DIVIDER}$$

where:
f_{PFD} is the phase frequency detector frequency.
f_{VCO} is the VCO frequency.
N is the fractional divide ratio ($INT + FRAC/MOD$).
INT is the integer divide ratio programmed in Register 0x02.
$FRAC$ is the fractional divider programmed in Register 0x03.
MOD is the modulus divide ratio programmed in Register 0x04.
f_{LO} is the LO frequency going to the mixer core when the loop is locked.
$LO_DIVIDER$ is the final frequency divider ratio that divides the frequency of the VCO or the external LO signal down by 2, 4, or 8 before it reaches the mixer, as shown in Table 10.

PLL Lock Time

The time it takes to lock the PLL after the last register is written breaks down into two parts: VCO band calibration and loop settling.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration takes approximately 94,208 PFD cycles. For a 40 MHz f_{PFD}, this corresponds to 2.36 ms. After calibration completes, the feedback action of the PLL causes the VCO to lock to the correct frequency eventually. The speed with which this lock occurs depends on the nonlinear cycle slipping behavior, as well as the small signal settling of the loop. For an accurate estimation of the lock time, download the ADIsimPLL tool to capture these effects correctly. In general, higher bandwidth loops tend to lock more quickly than lower bandwidth loops.

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with a logic high signifying that the loop is locked. The control for the MUXOUT pin is located in the REF_MUX_SEL bits (Register 0x21, Bits[6:4]), and the default configuration is for PLL lock detect.

Buffered LO Outputs

A buffered version of the internal LO signal is available differentially at the LOOUT+ and LOOUT− pins (Pin 17 and Pin 18). When the quadrature LO signals are generated using the quadrature divider, the output signal is available at either 2× or 1× the frequency of the LO signal at the mixer. Set the output to different drive levels by accessing the LO_DRV_LVL bits (Register 0x22, Bits[7:6]), as shown in Table 11.

The availability of the LO signal makes it possible to daisy-chain many devices synchronously. One ADRF6820 device can serve as the master where the LO signal is sourced, and the subsequent slave devices share the same LO output signal from the master. This flexibility substantially eases the LO requirements of a system requiring multiple LOs.

Table 11. LO Output Level

LO_DRV_LVL (Register 0x22, Bits[7:6])	Amplitude (dBm)	DC Level (V)
00	−5	3.0
01	−1	2.85
10	+2	2.7
11	+4	2.5

External LO Mode

Use the VCO_SEL bits (Register 0x22, Bits[2:0]) to select external or internal LO mode. To configure for external LO mode, set Register 0x22, Bits[2:0] to 4 decimal and apply the differential LO signals to Pin 34 (LOIN−) and Pin 35 (LOIN+). The external LO frequency range is 350 MHz to 6 GHz. When the polyphase phase splitter is selected, a 1× LO signal is required for the active mixer, or a 2× LO signal can be used with the internal quadrature divider, as shown in Table 9.

The LOIN+ and LOIN− input pins must be ac-coupled. When not in use, leave the LOIN+ and LOIN− pins unconnected.

Required PLL/VCO Settings and Register Write Sequence

In addition to writing to the necessary registers to configure the PLL and VCO for the desired LO frequency and phase noise performance, the registers in Table 12 are required register writes.

To ensure that the PLL locks to the desired frequency, follow the proper write sequence of the PLL registers. Configure the PLL registers accordingly to achieve the desired frequency, and the last writes must be to Register 0x02 (INT_DIV), Register 0x03 (FRAC_DIV), or Register 0x04 (MOD_DIV). When Register 0x02, Register 0x03, and Register 0x04 are programmed, an internal VCO calibration initiates, which is the last step to locking the PLL.

Table 12. Required PLL/VCO Register Writes

Address[Bits]	Bit Name	Setting	Description
0x21[3]	PFD_POLARITY	0x1	Negative polarity
0x49[15:0]	RESERVED, SET_1, SET_0	0x14B4	Internal settings

ACTIVE MIXERS

The signal from the RFDSA is split to drive a pair of double balanced, Gilbert cell active mixers, to be downconverted by the LO signals to baseband. Program the current in the mixers by changing the value of the MIX_BIAS bits (Register 0x31, Bits[12:10]) for trade-off between output noise and linearity.

The active mixers employ a distortion correction circuit for cancelling the third-order distortions coming from the mixers. Determine the amplitude and phase of the correction signals by the combination of control register entries DEMOD_RDAC and DEMOD_CDAC (Register 0x31, Bits[8:5] and Register 0x31, Bits[3:0], respectively). Refer to the IP3 and Noise Figure Optimization section for more information.

Demodulator gain and bandwidth are set by the resistance and capacitance in the mixer loads, which are controlled by the BWSEL bits (Register 0x34, Bits[9:8]) according to Table 15. Refer to the Bandwidth Select Modes section for more information.

BASEBAND BUFFERS

Emitter followers buffer the signals at the mixer loads and drive the baseband output pins (I+, I−, Q−, and Q+). Bias currents of the emitter followers are controlled by the BB_BIAS bits (Register 0x34, Bits[11:10]), as shown in Table 13. Set the bias current according to the load driving capabilities needed (that is, BB_BIAS = 1 for the specified 200 Ω load, and BB_BIAS = 2 for the 50 Ω or 100 Ω loads are recommended). The differential impedance of the baseband outputs is 50 Ω; however, the ADRF6820 output load must be high (that is, 200 Ω) for optimized linearity performance. Refer to the I/Q Output Loading section for supporting data.

Table 13. Baseband Buffer Bias

BB_BIAS (Register 0x34, Bits[11:10])	Bias Current (mA)
00	0
01	4.5
10	9
11	13.5

SERIAL PORT INTERFACE (SPI)

The SPI of the ADRF6820 allows the user to configure the device for specific functions or operations through a structured register space provided inside the chip. This interface provides users with added flexibility and customization. Addresses are accessed via the serial port interface and can be written to or read from the serial port interface.

The serial port interface consists of three control lines: SCLK, SDIO, and $\overline{CS}$. SCLK (serial clock) is the serial shift clock, and it synchronizes the serial interface reads and writes. SDIO is the serial data input or the serial data output depending on the instruction sent and the relative position in the timing frame. $\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. The falling edge of $\overline{CS}$ in conjunction with the rising edge of SCLK determines the start of the frame. When $\overline{CS}$ is high, all SCLK and SDIO activity is ignored. See Table 4 for the serial timing and its definitions.

The ADRF6820 protocol consists of 7 register address bits, followed by a read/write and 16 data bits. Both the address and data fields are organized with the most significant bit (MSB) first and end with the least significant bit (LSB).

On a write cycle, up to 16 bits of serial write data is shifted in, MSB to LSB. If the rising edge of $\overline{CS}$ occurs before the LSB of the serial data is latched, only the bits that were latched are written to the device. If more than 16 data bits are shifted in, the 16 most recent bits are written to the device. The ADRF6820 input logic level for the write cycle supports an interface as low as 1.8 V.

On a read cycle, up to 16 bits of serial read data is shifted out, MSB first. Data shifted out beyond 16 bits is undefined. Read back content at a given register address does not necessarily correspond with the write data of the same address. The output logic level for a read cycle is 2.5 V.

POWER SUPPLY SEQUENCING

The ADRF6820 operates from two nominal supply voltages, 3.3 V and 5 V. Careful consideration must be exercised to ensure that the voltage on all pins connected to VPOS_3P3 never exceed the voltage on all pins connected to VPOS_5V.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

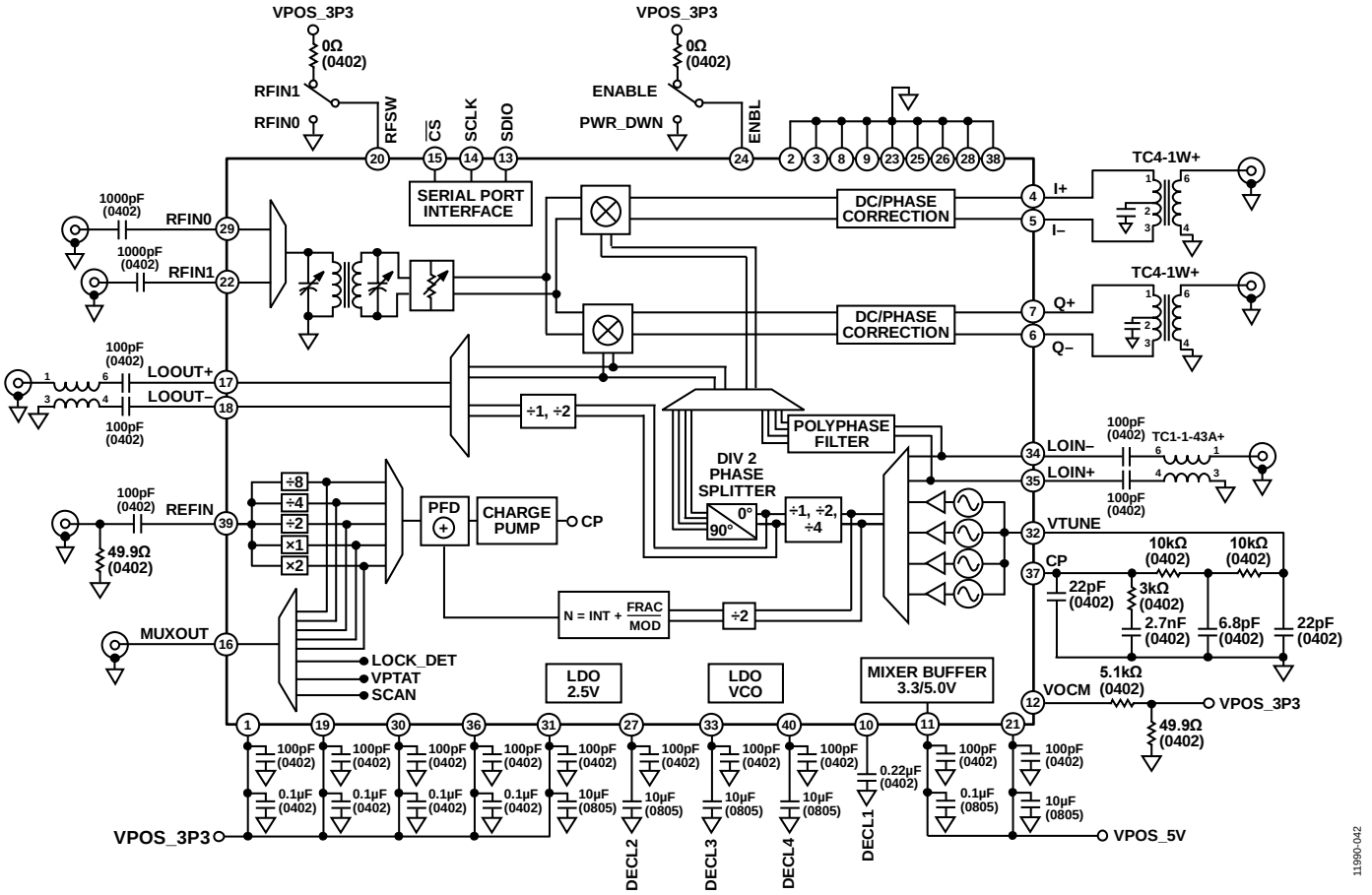


Figure 33. Basic Connections

Table 14.

Pin No.	Mnemonic	Description	Basic Connection
5 V Power			
11	VPOS_5V	Mixer power supply	Decouple this power supply pin via a 100 pF and a 0.1 µF capacitor to ground. Ensure that the decoupling capacitors are located close to the pin.
21	VPOS_5V	RF front-end power supply	Decouple this power supply pin via a 100 pF and a 10 µF (0805) capacitor to ground. Ensure that the decoupling capacitors are located close to the pin.
3.3 V Power			The voltage on any and all pins connected to VPOS_3P3 must never exceed the voltage on any and all pins connected to VPOS_5V.
1	VPOS_3P3	Digital power supply	Decouple this pin via a 100 pF and a 0.1 µF capacitor to ground.
19	VPOS_3P3	LO power supply	Decouple this pin via a 100 pF and a 0.1 µF capacitor to ground.
30	VPOS_3P3	LO power supply	Decouple this pin via a 100 pF and a 0.1 µF capacitor to ground.
31	VPOS_3P3	VCO power supply	Decouple this pin via a 100 pF and a 10 µF capacitor to ground.
36	VPOS_3P3	PLL power supply	Decouple this pin via a 100 pF and a 0.1 µF capacitor to ground.

Pin No.	Mnemonic	Description	Basic Connection
PLL/VCO			
37	CP	Synthesizer charge pump output voltage	Connect to the VTUNE pin through the loop filter.
39	REFIN	Synthesizer reference frequency input	Nominal input level is 1 V p-p. Input range is 12 MHz to 320 MHz. This pin is internally biased to VPOS_3P3/2 and must be ac-coupled.
17, 18	LOOUT+, LOOUT−	Differential LO outputs	The differential output impedance is 50 Ω. These pins are internally biased and must be ac-coupled. The dc level varies with LO output drive level. See Table 11.
34, 35	LOIN−, LOIN+	Differential LO inputs	Differential input impedance of 50 Ω. These pins are internally biased and must be ac-coupled.
16	MUXOUT	PLL multiplex output	This output pin provides the PLL reference signal or the PLL lock detect signal.
32	VTUNE	VCO tuning voltage	This pin is driven by the output of the loop filter, and the nominal input voltage range is 1 V to 2.8 V.
RF Inputs			
22, 29	RFIN1, RFIN0	RF inputs	The single-ended RF inputs have a 50 Ω input impedance. These pins are internally biased to VPOS_5V/2. AC-couple the RF inputs. Refer to the Layout section for the recommended printed circuit board (PCB) layout for improved channel-to-channel isolation. Terminate unused RF inputs with a dc blocking capacitor to GND to improve isolation.
20	RFSW	Pin control of the RF inputs	For RFIN0, set RFSW to logic low, and for RFIN1, set RFSW to logic high. For logic high, connect this pin to 3.3 V.
Demodulator Outputs			
4, 5, 6, 7	I+, I−, Q−, Q+	I and Q channel mixer baseband outputs	The I and Q mixer outputs have a 50 Ω differential output impedance (25 Ω per pin). The VOCM pin sets the output common-mode level.
12	VOCM	Mixer output common-mode voltage	This input pin sets the common-mode voltage of the I and Q complex outputs. VOCM needs a clean voltage source within the 1.5 V to 2.4 V range. Linearity performance degrades when the voltage is outside this range.
Enable			
24	ENBL	External enable pin control	Set this pin high for enable and low for power-down of the internal blocks. To specify the internal blocks, write to Register 0x10, PWRDWN_MSK.
Serial Port Interface			
13	SDIO	SPI data input and output	3.3 V tolerant logic levels.
14	SCLK	SPI clock	3.3 V tolerant logic levels.
15	$\overline{CS}$	SPI chip select	Active low. 3.3 V tolerant logic levels.
LDO Decoupling			
10	DECL1	Mixer LDO decoupling	Decouple this pin via a 0.22 µF capacitor to ground. Ensure the decoupling capacitor is located close to the pin.
27	DECL2	VCO2 LDO decoupling	Decouple this power supply pin via 100 pF and 10 µF (0805) capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
33	DECL3	VCO LDO decoupling	Decouple this power supply pin via 100 pF and 10 µF (0805) capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
40	DECL4	2.5V LDO decoupling	Decouple this power supply pin via 100 pF and 10 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
GND			
2, 3, 8, 9, 23, 25, 26, 28, 38	GND	Ground	Connect these pins to the GND of the PCB.
	EPAD	Exposed pad (EPAD)	The exposed thermal pad is on the bottom of the package. Solder the exposed pad to ground.

RF BALUN INSERTION LOSS OPTIMIZATION

As shown in Figure 34 to Figure 37, the gain of the ADRF6820 mixer was characterized for every combination of BAL_CIN and BAL_COUT (Register 0x30, Bits[7:0]). As shown, a range of BAL_CIN and BAL_COUT values can be used to optimize the gain of the ADRF6820. The optimized values do not change with temperature. After the values are chosen, the absolute gain changes over temperature; however, the signature of the BAL_CIN and BAL_COUT values is fixed.

At lower input frequencies, more capacitance is needed. This capacitance increase is achieved by programming higher codes into BAL_CIN and BAL_COUT. At higher frequencies, less capacitance is required; therefore, lower BAL_CIN and BAL_COUT codes are appropriate. Figure 38 shows the change in gain over frequency for various BAL_CIN and BAL_COUT codes. Use Figure 34 to Figure 38 only as guides; do not interpret them in the absolute sense because every application and PCB design varies. Additional fine-tuning may be necessary to achieve the maximum gain. Table 16 shows the recommended BAL_CIN and BAL_COUT settings for various RF frequencies.

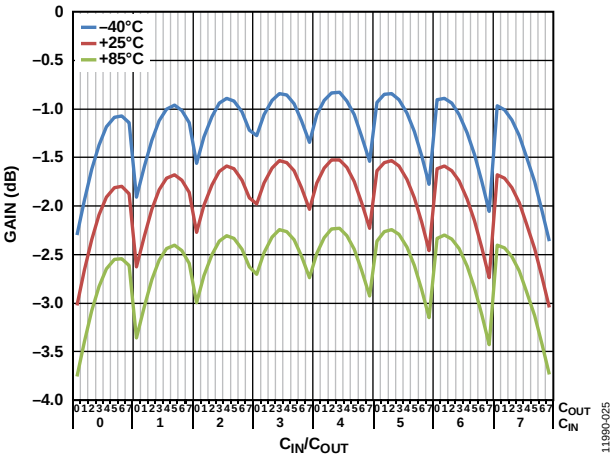


Figure 34. Gain vs. BAL_CIN and BAL_COUT at f_{RF} = 900 MHz

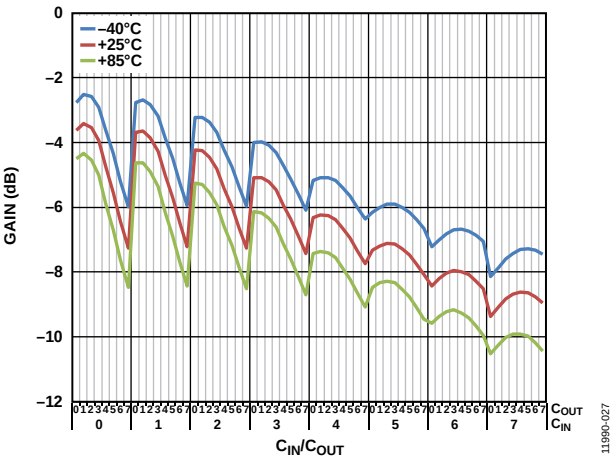


Figure 35. Gain vs. BAL_CIN and BAL_COUT at f_{RF} = 2200 MHz

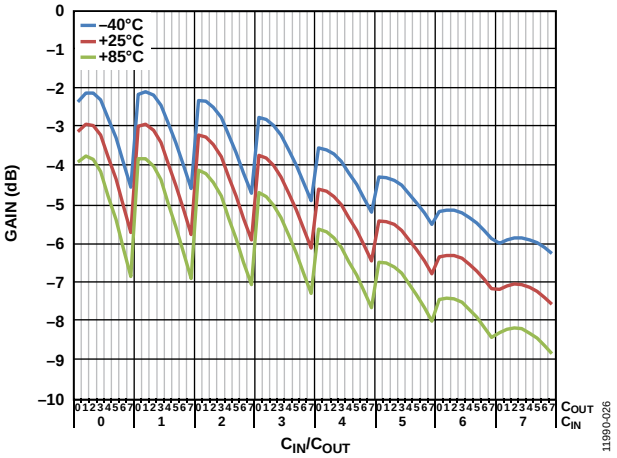


Figure 36. Gain vs. BAL_CIN and BAL_COUT at f_{RF} = 1900 MHz

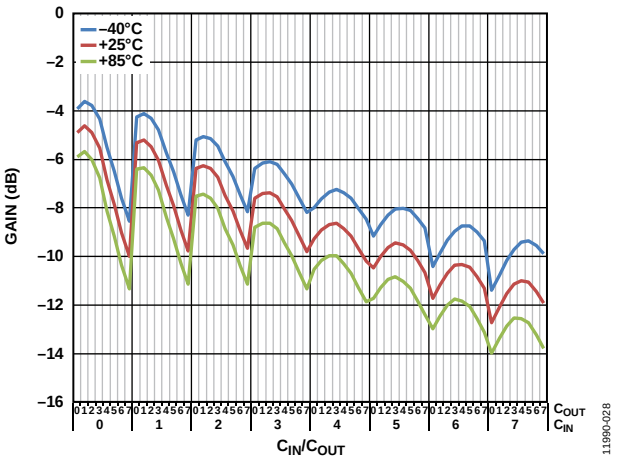


Figure 37. Gain vs. BAL_CIN and BAL_COUT at f_{RF} = 2600 MHz

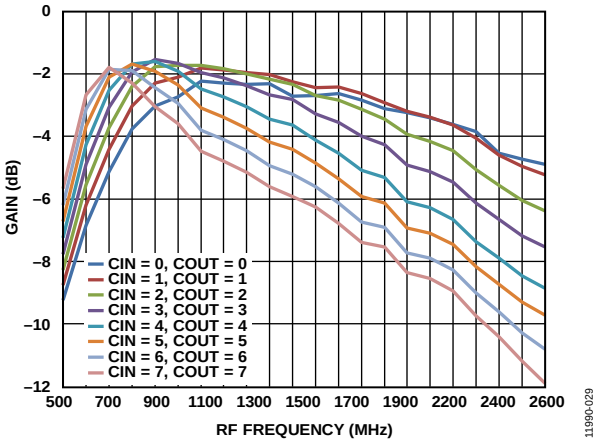


Figure 38. Gain vs. RF Frequency for Various BAL_CIN and BAL_COUT Codes

BANDWIDTH SELECT MODES

The ADRF6820 offers four bandwidth select modes, as specified in Table 15. The bandwidth select modes include either high gain and low bandwidth or low gain and high bandwidth. The selection of the resistance and capacitance in the mixer load determines the IF gain and bandwidth. Use Register 0x34, Bits[9:8] to select one of the four modes.

The high gain modes, BWSEL0 and BWSEL1, have equivalent performance in terms of gain, noise figure, and linearity. Similarly, the low gain modes, BWSEL2 and BWSEL3, share the same performance specifications. However, the factor that distinguishes the different modes is the IF bandwidth. Figure 39 to Figure 42 show the voltage gain, pass-band flatness, and 1 dB bandwidth of the bandwidth modes for the various LO frequencies. Table 15 summarizes the results of Figure 39 to Figure 42.

Table 15. Mixer Gain and Bandwidth Select Modes[1]

BWSEL (Reg. 0x34[9:8])	Mode	Voltage Gain (dB)	1 dB BW (MHz)	3 dB BW (MHz)
00	BWSEL0	+2	240	480
01	BWSEL1	+2	180	340
10	BWSEL2	−3	600	1400
11	BWSEL3	−3	500	900

[1] f_{LO} = 2100 MHz, high-side LO injection.

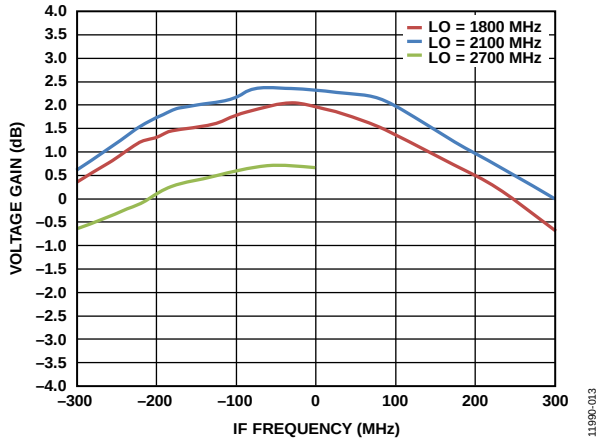


Figure 39. Voltage Gain vs. IF Frequency, BWSEL = 0, LO Fixed and RF Swept

The LO frequency was set to 1800 MHz, 2100 MHz, and 2700 MHz, and the RF frequency was swept. With this measurement approach, Figure 39 to Figure 42 show the effects of both the RF and IF roll-off. The RF roll-off is determined by the integrated RF balun, and the IF roll-off is set by the bandwidth select mode. The effect of both the RF roll-off and IF roll-off is most evident in the widest bandwidth mode (BWSEL2), as shown in Figure 41. Figure 41 shows the flattest and widest bandwidth when the LO frequency is at 2700 MHz because the RF frequency is farthest from the roll-off of the integrated RF balun. In the f_{LO} = 1800 MHz and f_{LO} = 2100 MHz sweeps, the effect of the RF balun becomes evident, resulting in a narrower 1 dB bandwidth.

It is very difficult to accurately measure the voltage gain flatness of the ADRF6820 because the signal generators and spectrum analyzers introduce their own amplitude inaccuracies. Additionally, at higher frequencies, the board traces are not as well matched, resulting in signal reflections. With the amplitude errors/inaccuracies from the signal generators and spectrum analyzers included in the measurement, the gain flatness of the ADRF6820 is approximately 0.3 dB for any 100 MHz bandwidth, or approximately 0.2 dB for any 20 MHz bandwidth. By design, the gain flatness of the ADRF6820 is substantially better than this; however, the measurement approach is the limiting factor, and the result is quoted as such.

Figure 39 to Figure 42 show data for both positive and negative IF frequencies; positive IF frequencies represent low-side LO injection, and negative frequencies represent high-side LO injection.

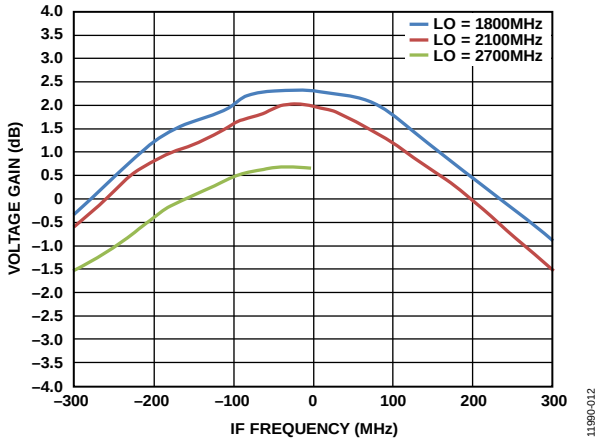


Figure 40. Voltage Gain vs. IF Frequency, BWSEL = 1, LO Fixed and RF Swept

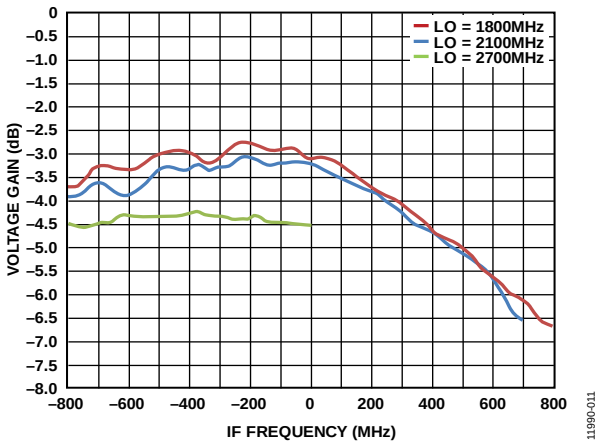


Figure 41. Voltage Gain vs. IF Frequency, BWSEL = 2, LO Fixed and RF Swept

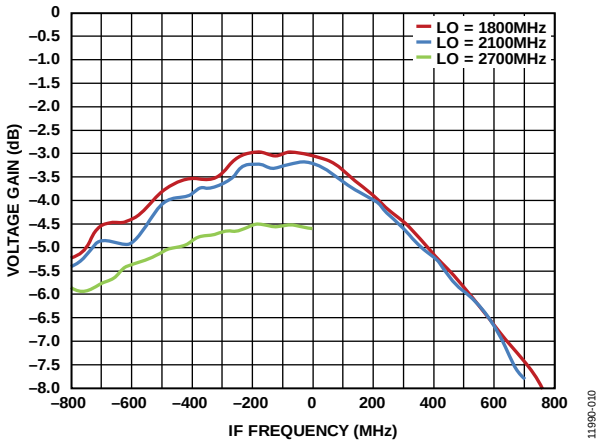


Figure 42. Voltage Gain vs. IF Frequency, BWSEL = 3, LO Fixed and RF Swept

IP3 AND NOISE FIGURE OPTIMIZATION

The ADRF6820 can be configured for either improved performance or reduced power consumption. In applications where performance is critical, the ADRF6820 offers IP3 or noise figure optimization. However, if power consumption is the priority, the mixer bias current can be reduced to save on overall power at the expense of degraded performance. Depending on the application specific needs, the ADRF6820 offers configurability that balances performance and power consumption.

Adjustments to the mixer bias setting have the most impact on performance and power. For this reason, first adjust the mixer bias. The active mixer core of the ADRF6820 is a linearized transconductor. With increased bias current, the transconductor becomes more linear, resulting in higher IP3. The higher IP3, however, is at the expense of degraded noise figure and increased power consumption. For a 1-bit change of the mixer bias (MIX_BIAS, Register 0x31, Bits[12:10]), the total mixer current increases by 8 mA.

Inevitably, there is a limit on how much the bias current can increase before the improvement in linearity no longer justifies the increase in power and noise. The mixer core reaches a point where further increases in bias current do not translate to improved linearity performance. When that point is reached, decrease the bias current to a level where the desired performance is achieved. Depending on the system specifications of the customer, a balance between linearity, noise figure, and power can be attained.

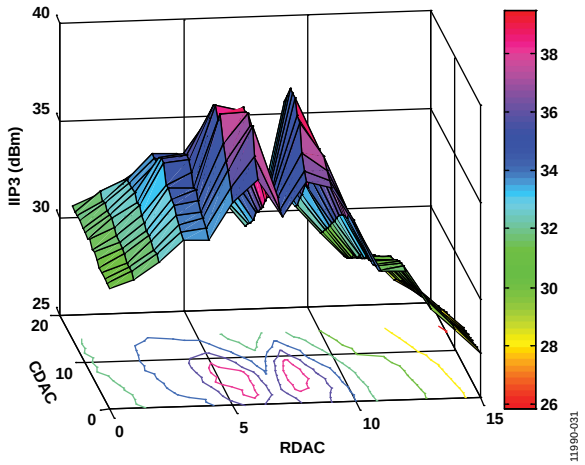


Figure 43. IIP3 vs. DEMOD_CDAC and DEMOD_RDAC, MIX_BIAS = 3 at f_{RF} = 900 MHz

In addition to bias optimization, the ADRF6820 also has configurable distortion cancellation circuitry. The linearized transconductor input of the ADRF6820 is composed of a main path and a secondary path. Through adjustments of the amplitude and phase of the secondary path, the distortion generated by the main path can be canceled, resulting in improved IP3 performance. The amplitude and phase adjustments are located in the following serial interface bits: DEMOD_RDAC (Register 0x31, Bits[8:5]) and DEMOD_CDAC (Register 0x31, Bits[3:0]).

Figure 43 to Figure 46 show the input IP3 and noise figure sweeps for all DEMOD_RDAC, DEMOD_CDAC, and MIX_BIAS combinations. The input IP3 vs. DEMOD_RDAC and DEMOD_CDAC figures show both a surface and a contour plot in one figure. The contour plot is located directly underneath the surface plot. The best approach for reading the figures is to locate the peaks on the surface plot, which indicate maximum input IP3, and to follow the same color pattern to the contour plot to determine the optimized DEMOD_RDAC and DEMOD_CDAC values. The overall shape of the input IP3 plot does not vary with the MIX_BIAS setting; therefore, only MIX_BIAS = 011 is displayed. Table 16 shows the recommended MIX_BIAS, DEMOD_RDAC, and DEMOD_CDAC settings for various RF frequencies. Use Table 16 and Figure 43 to Figure 46 as guides only; do not interpret them in the absolute sense because every application and input signal varies.

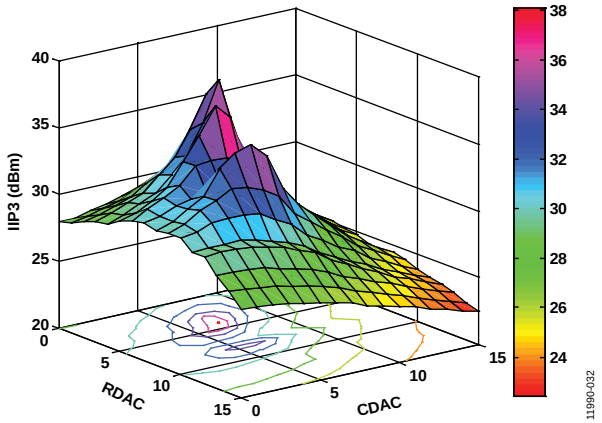


Figure 44. IIP3 vs. DEMOD_CDAC and DEMOD_RDAC, MIX_BIAS = 2 at f_{RF} = 1900 MHz

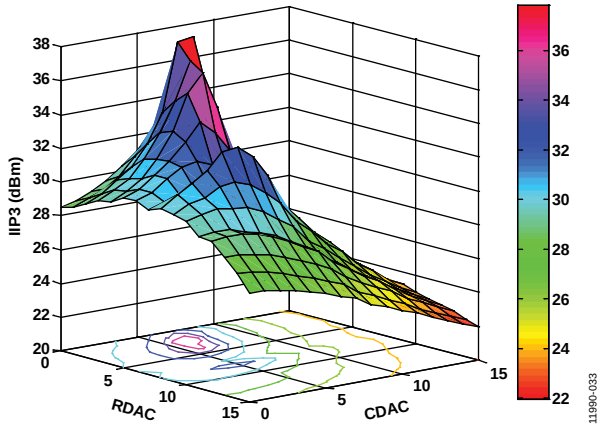


Figure 45. IIP3 vs. DEMOD_CDAC and DEMOD_RDAC, MIX_BIAS = 2 at f_{RF} = 2100 MHz

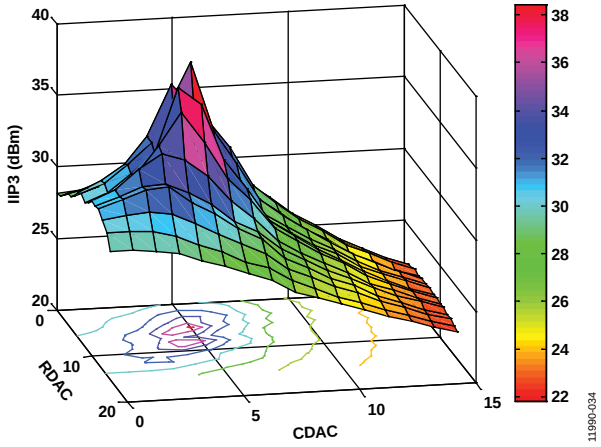


Figure 46. IIP3 vs. DEMOD_CDAC and DEMOD_RDAC, MIX_BIAS = 2 at f_{RF} = 2700 MHz

Recommended Settings for BAL_CIN, BAL_COUT, MIX_BIAS, DEMOD_RDAC, and DEMOD_CDAC Settings

Table 16. Recommended Settings

BWSEL	f_{RF} (MHz)	BAL_CIN	BAL_COUT	MIX_BIAS	DEMOD_RDAC	DEMOD_CDAC
0	500	7	7	2	9	10
0	600	7	7	2	9	10
0	700	7	7	2	8	11
0	800	7	3	2	9	4
0	900	6	2	1	8	7
0	1000	5	1	1	8	9
0	1100	3	2	1	9	6
0	1200	3	1	1	8	8
0	1300	2	1	2	8	7
0	1400	2	1	2	9	3
0	1500	1	1	2	9	4
0	1600	1	1	1	8	5
0	1700	1	0	1	8	5
0	1800	1	1	1	8	6
0	1900	1	0	1	8	5
0	2000	1	0	2	8	4
0	2100	1	0	2	8	4
0	2200	1	0	2	9	2
0	2300	1	0	2	9	3
0	2400	1	0	2	7	3
0	2500	1	0	2	7	3
0	2600	1	0	2	7	3
0	2700	1	0	1	8	4
0	2800	1	0	1	8	4

BWSEL	f_{RF} (MHz)	BAL_CIN	BAL_COUT	MIX_BIAS	DEMOD_RDAC	DEMOD_CDAC
2	500	7	7	3	5	7
2	600	7	7	3	5	7
2	700	7	7	2	4	9
2	800	7	3	3	8	4
2	900	6	2	3	9	5
2	1000	5	1	3	7	7
2	1100	3	2	2	6	9
2	1200	3	1	2	8	9
2	1300	2	1	2	3	9
2	1400	2	1	3	8	5
2	1500	1	1	3	8	6
2	1600	1	1	2	8	5
2	1700	1	0	2	8	5
2	1800	1	1	2	8	7
2	1900	1	0	2	5	6
2	2000	1	0	3	5	7
2	2100	1	0	2	4	6
2	2200	1	0	2	4	6
2	2300	1	0	3	8	6
2	2400	1	0	3	8	6
2	2500	1	0	3	9	6
2	2600	1	0	3	9	6
2	2700	1	0	2	8	5
2	2800	1	0	2	8	5

I/Q OUTPUT LOADING

The I and Q baseband outputs of the ADRF6820 have a 50 Ω differential impedance. However, voltage gain and linearity performance are optimized with the use of a 200 Ω differential load. This may not be the most favorable termination for every application; therefore, performance trade-offs can be made for lower output loads.

The output load on the differential I/Q outputs has a direct impact on the voltage gain where the gain decreases with lighter loads. The 50 Ω differential source impedance (R_S) of the ADRF6820 forms a voltage divider with the external load resistor (R_L). The performance of the ADRF6820 was optimized for and specified with a differential load termination of 200 Ω. For a 200 Ω differential load termination, the voltage divider ratio is given by

$$V_{OUT}/V_{IN} = R_L/(R_L + R_S)$$

where R_S = 50 Ω.

The change in gain due to different load impedance is given by

$$\frac{Gain(R_{L2})}{Gain(R_{L1})} = \frac{\frac{R_{L2}}{(R_{L2}+R_S)}}{\frac{R_{L1}}{(R_{L1}+R_S)}}$$

where:
R_{L1} = 200 Ω.
R_{L2} is the new load impedance.

The conversion gain of the ADRF6820 at f_{RF} = 2100 MHz and f_{IF} = 200 MHz is −3.2 dB. For the same test conditions with a 100 Ω load, the gain decreases by 20log(5/6) = −1.58 dB to a voltage gain of −4.6 dB. Figure 47 shows the voltage gain vs. IF frequency for f_{LO} = 1840 MHz and BWSEL = 2 for common output loads.

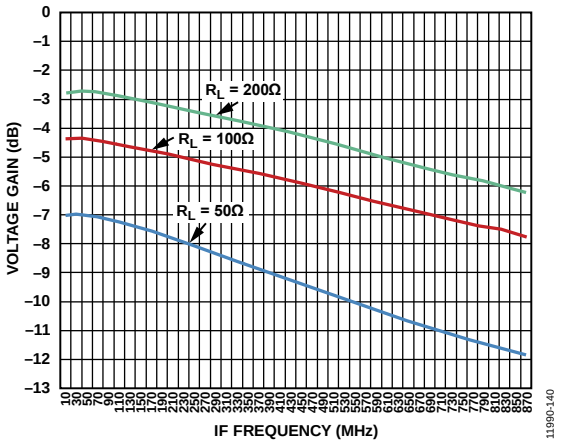


Figure 47. Voltage Gain vs. IF Frequency for LO = 1840 MHz, BWSEL = 2

In addition to the lower conversion gain, the effect of lower output load impedance is degraded linearity performance. The degraded performance is a result of the emitter follower buffers, after the mixers, needing to deliver more load current; therefore, they operate closer to their nonlinear region. To improve performance with lighter loads, such as 50 Ω, increase the bias current of the emitter follower by increasing BB_BIAS (Register 0x34, Bits[11:10]) to its maximum of 13.5 mA. Refer to Table 13 for the bias current settings.

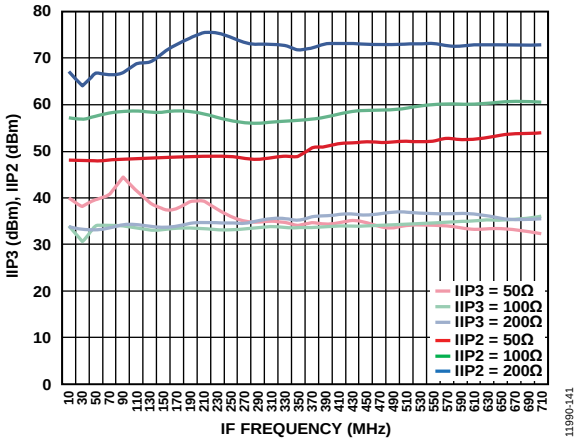


Figure 48. IIP3 and IIP2 vs. IF Frequency for f_{LO} = 1840 MHz and BWSEL = 2

Figure 48 shows input IP3 and input IP2 performance vs. IF frequency for 50 Ω, 100 Ω, and 200 Ω loads. For the 100 Ω and 200 Ω load impedance, the bias current was configured to its default of 9 mA, whereas for the 50 Ω load, the current was increased to the maximum to achieve the same level of input IP3 performance as the higher output loads.

IMAGE REJECTION

The amplitude and phase mismatch of the baseband I and Q paths directly translates to degradations in image rejection, and for direct conversion systems, maximizing image rejection is key to achieving performance and optimizing bandwidth. The ADRF6820 offers phase adjustment of the I and Q paths independently to allow quadrature correction. The quadrature correction can be accessed by writing to Register 0x32, Bits[3:0] for the I path correction and Register 0x32, Bits[7:4] for the Q path correction. Figure 49 shows the available correction range for various LO frequencies.

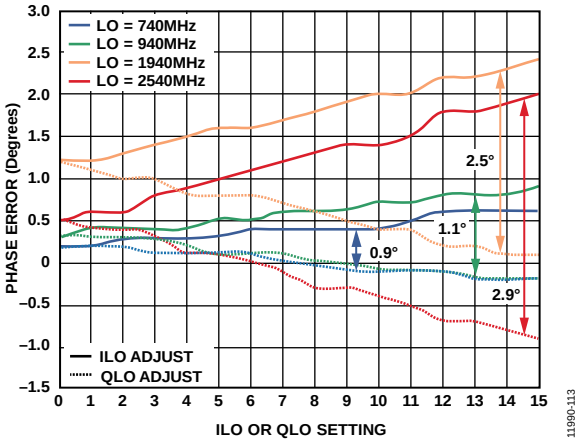


Figure 49. Quadrature Correction Range

Use the following equation to translate the gain and quadrature phase mismatch to image rejection ratio (IRR) performance.

$$IRR\,(dB) = 10\log\frac{\left|1+A_e{}^2+2A_e\cos(\varphi_e)\right|}{\left|1+A_e{}^2-2A_e\cos(\varphi_e)\right|}$$

where:
A_e is the amplitude error.
φ_e is the phase error.

One of the dominant sources of phase error in a system originates from the demodulator where the quadrature phase split of the LO signal occurs. Figure 50 to Figure 52 show the level of image rejection achievable from the ADRF6820 across different sweep parameters with no correction applied.

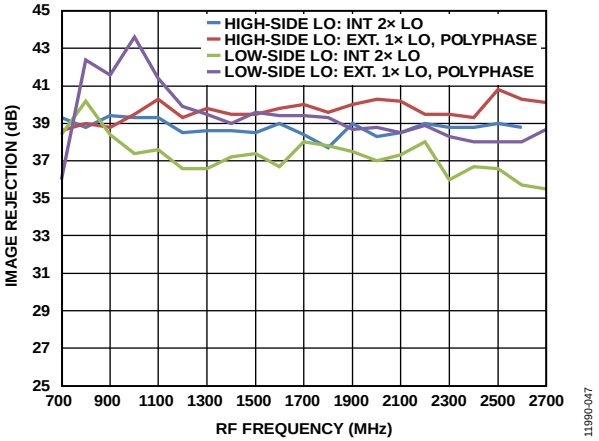


Figure 50. Image Rejection vs. RF Frequency, f_{IF} = 200 MHz

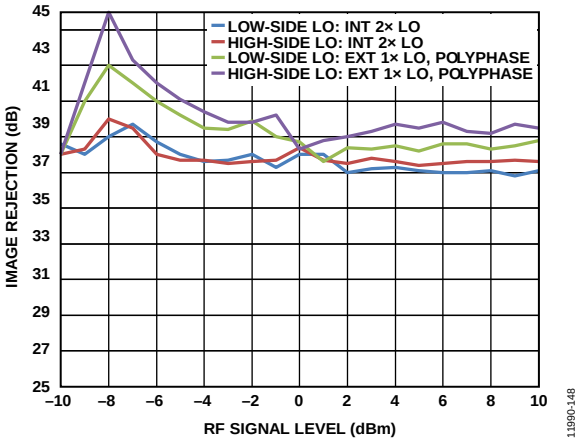


Figure 51. Image Rejection vs. RF Signal Level, IF = 200 MHz, for High-Side LO Injection f_{LO} = 2000 MHz and f_{RF} = 1800 MHz and Vice Versa for Low-Side Injection

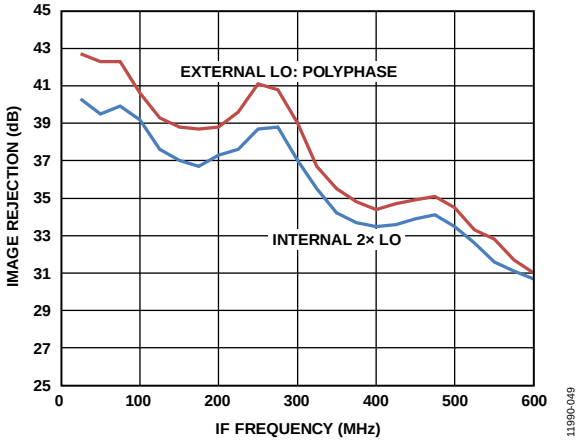


Figure 52. Image Rejection vs. IF Frequency, f_{LO} = 1800 MHz

I/Q POLARITY

The ADRF6820 offers the flexibility of specifying the polarity of the I/Q outputs, where I can lead Q or vice versa. By addressing POLI (Register 0x32, Bits[9:8]) or POLQ (Register 0x32, Bits[11:10]), both the I and Q outputs can be inverted from their default configuration. The flexibility of specifying the polarity becomes important when the I and Q outputs are processed simultaneously in the complex domain, I + jQ.

At power up, depending on whether high-side or low-side injection of the LO frequency is applied, the I channel can either lead or lag the Q channel by 90°. When the RF frequency is greater than the LO frequency (low-side LO injection), the I channel leads the Q channel (see Figure 53). On the contrary, if the RF frequency is less than the LO frequency (high-side LO injection), the Q channel leads the I channel by 90° (see Figure 54).

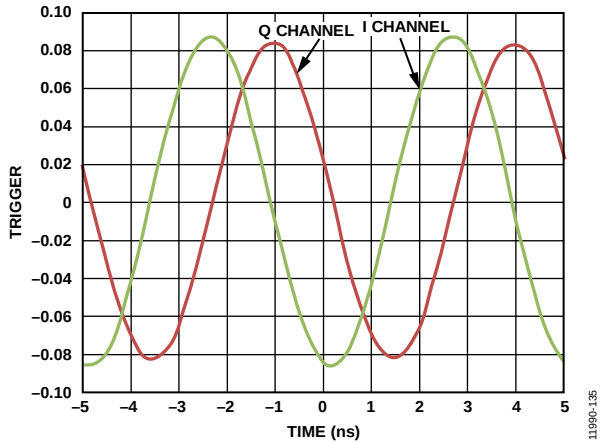


Figure 53. POLI = 1, POLQ = 2, I Channel Normal Polarity, Q Channel Normal Polarity, f_{RF} = 2040 MHz, and f_{LO} = 1840 MHz

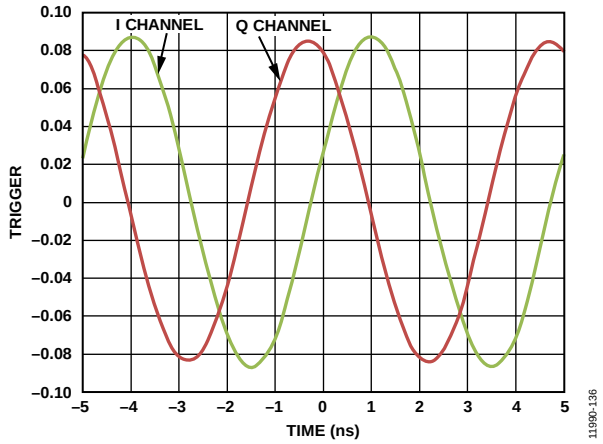


Figure 54. POLI = 1, POLQ = 2, I Channel Normal Polarity, Q Channel Normal Polarity, f_{RF} = 2040 MHz, and f_{LO} = 2240 MHz

Both the I and Q channels can be inverted to achieve the desired polarity, as shown in Figure 55 to Figure 57, by writing to POLI (Register 0x32, Bits[9:8]) or POLQ (Register 0x32, Bits[11:10]).

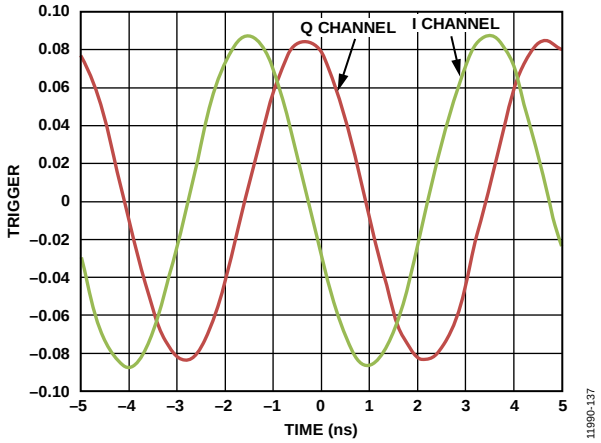


Figure 55. POLI = 2, POLQ = 2, I Channel Invert Polarity, Q Channel Normal Polarity, f_{RF} = 2040 MHz, and f_{LO} = 2240 MHz

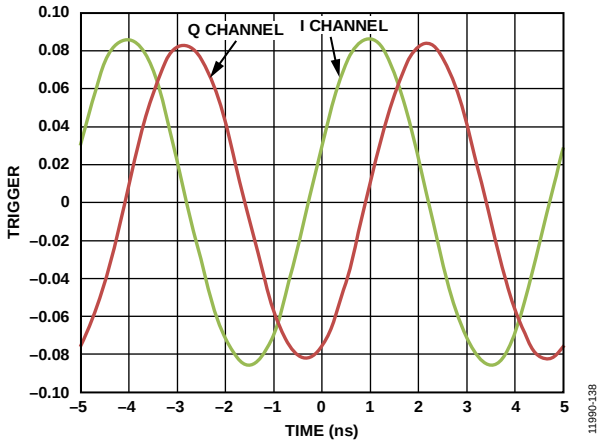


Figure 56. POLI = 1, POLQ = 1, I Channel Normal Polarity, Q Channel Invert Polarity, f_{RF} = 2040 MHz, and f_{LO} = 2240 MHz

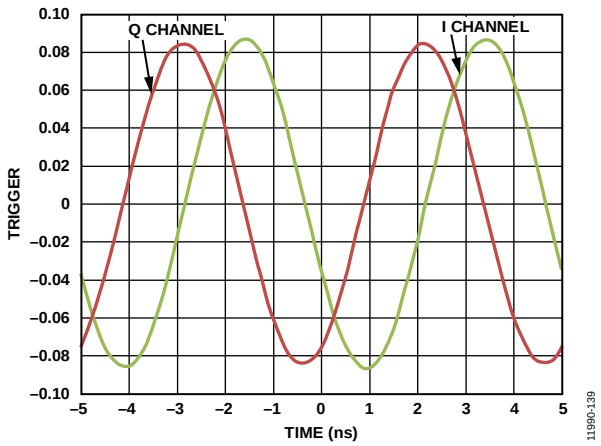


Figure 57. POLI = 2, POLQ = 1, I Channel Invert Polarity, Q Channel Invert Polarity, f_{RF} = 2040 MHz, and f_{LO} = 2240 MHz

LAYOUT

Careful layout of the ADRF6820 is necessary to optimize performance and minimize stray parasitics. The ADRF6820 supports two RF inputs; therefore, the layout of the RF section is critical in achieving isolation between each channel. Figure 58 shows the recommended layout for the RF inputs. Each RF input, RFIN0 and RFIN1, is isolated between ground pins, and the best layout approach is to keep the traces short and direct. To achieve this, connect the pins directly to the center ground pad of the exposed pad of the ADRF6820. This approach minimizes the trace inductance and promotes better isolation between the channels. In addition, for improved isolation, do not route the RFIN0 and RFIN1 traces in parallel to each other; split the traces immediately after each one leaves the pins. Keep the traces as far away from each other as possible to prevent cross coupling.

The input impedance of the RF inputs is 50 Ω, and the traces leading to the pin must also have a 50 Ω characteristic impedance. For unused RF inputs, terminate the pins with a dc blocking capacitor to ground.

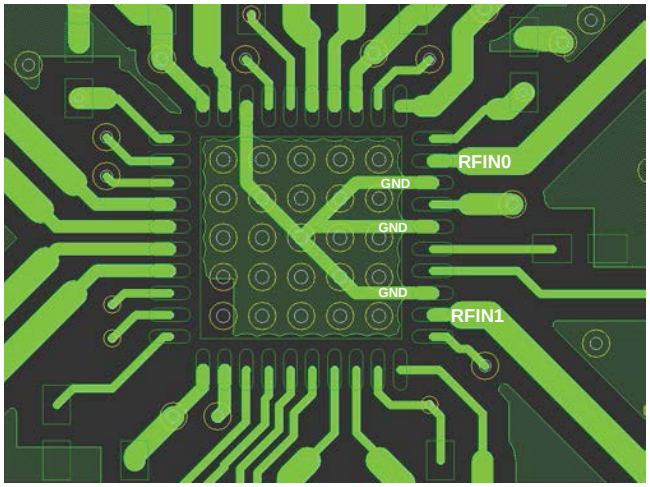


Figure 58. Recommended RF Input Layout

REGISTER MAP

Table 17.

Hex Addr.	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
00	SOFT_RESET	[15:8]	RESERVED								0x0000	W
		[7:0]	RESERVED							SOFT_RESET		
01	Enables	[15:8]	RESERVED					DMOD_EN	QUAD_DIV_EN	LO_DRV2X_EN	0xFE7F	RW
		[7:0]	LO_DRV1X_EN	VCO_MUX_EN	REF_BUF_EN	VCO_EN	DIV_EN	CP_EN	VCO_LDO_EN	RESERVED		
02	INT_DIV	[15:8]	RESERVED				DIV_MODE	INT_DIV			0x002C	RW
		[7:0]	INT_DIV									
03	FRAC_DIV	[15:8]	FRAC_DIV								0x0128	RW
		[7:0]	FRAC_DIV									
04	MOD_DIV	[15:8]	MOD_DIV								0x0600	RW
		[7:0]	MOD_DIV									
10	PWRDWN_MASK	[15:8]	RESERVED					DMOD_MASK	QUAD_DIV_MASK	LO_DRV2X_MASK	0xFE7F	RW
		[7:0]	LO_DRV1X_MASK	VCO_MUX_MASK	REF_BUF_MASK	VCO_MASK	DIV_MASK	CP_MASK	VCO_LDO_MASK	RESERVED		
20	CP_CTL	[15:8]	RESERVED	CPSEL	CSCALE				RESERVED		0x0C26	RW
		[7:0]	RESERVED		BLEED							
21	PFD_CTL	[15:8]	RESERVED								0x0003	RW
		[7:0]	RESERVED	REF_MUX_SEL			PFD_POLARITY	REFSEL				
22	VCO_CTL	[15:8]	RESERVED				RESERVED				0x2A03	RW
		[7:0]	LO_DRV_LVL		DRVDIV2_EN	DIV8_EN	DIV4_EN	VCO_SEL				
23	DGA_CTL	[15:8]	RESERVED				RFSW_MUX	RESERVED	RFSW_SEL	RFDSA_SEL	0x0000	RW
		[7:0]	RFDSA_SEL			RESERVED						
30	BALUN_CTL	[15:8]	RESERVED								0x0000	RW
		[7:0]	BAL_COUT			RESERVED	BAL_CIN			RESERVED		
31	MIXER_CTL	[15:8]	RESERVED			MIX_BIAS			RESERVED	DEMOD_RDAC	0x1101	RW
		[7:0]	DEMOD_RDAC			RESERVED	DEMOD_CDAC					
32	MOD_CTL0	[15:8]	RESERVED				POLQ		POLI		0x0900	RW
		[7:0]	QLO				ILO					
33	MOD_CTL1	[15:8]	DCOFFI								0x0000	RW
		[7:0]	DCOFFQ									
34	MOD_CTL2	[15:8]	RESERVED				BB_BIAS		BWSEL		0x0B00	RW
		[7:0]	RESERVED				RESERVED					
40	PFD_CTL2	[15:8]	RESERVED								0x0010	RW
		[7:0]	RESERVED	ABLDLY		CPCTRL			CLKEDGE			
42	DITH_CTL1	[15:8]	RESERVED								0x000E	RW
		[7:0]	RESERVED				DITH_EN	DITH_MAG		DITH_VAL		
43	DITH_CTL2	[15:8]	DITH_VAL								0x0001	RW
		[7:0]	DITH_VAL									
44	DIV_SM_CTL	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED							BANDCAL_DIVD_CLR		
45	VCO_CTL2	[15:8]	RESERVED								0x0000	RW
		[7:0]	VCO_BAND_SRC	BAND								
46	VCO_RB	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED		VCO_BAND							
49	VCO_CTL3	[15:8]	RESERVED		SET_1					SET_0	0x16BD	RW
		[7:0]	SET_0									

REGISTER ADDRESS DESCRIPTIONS

Address: 0x00, Reset: 0x0000, Name: SOFT_RESET

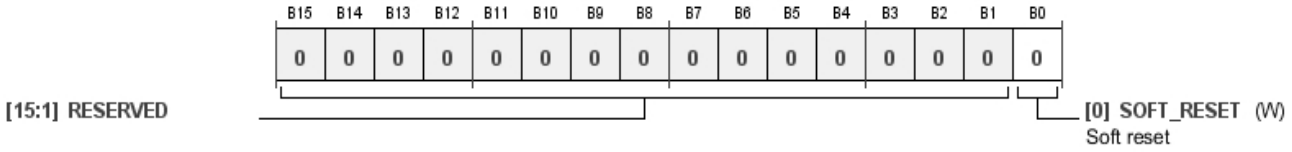


Table 18. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Settings	Description	Reset	Access
0	SOFT_RESET		Soft reset	0x0000	W

Address: 0x01, Reset: 0xFE7F, Name: Enables

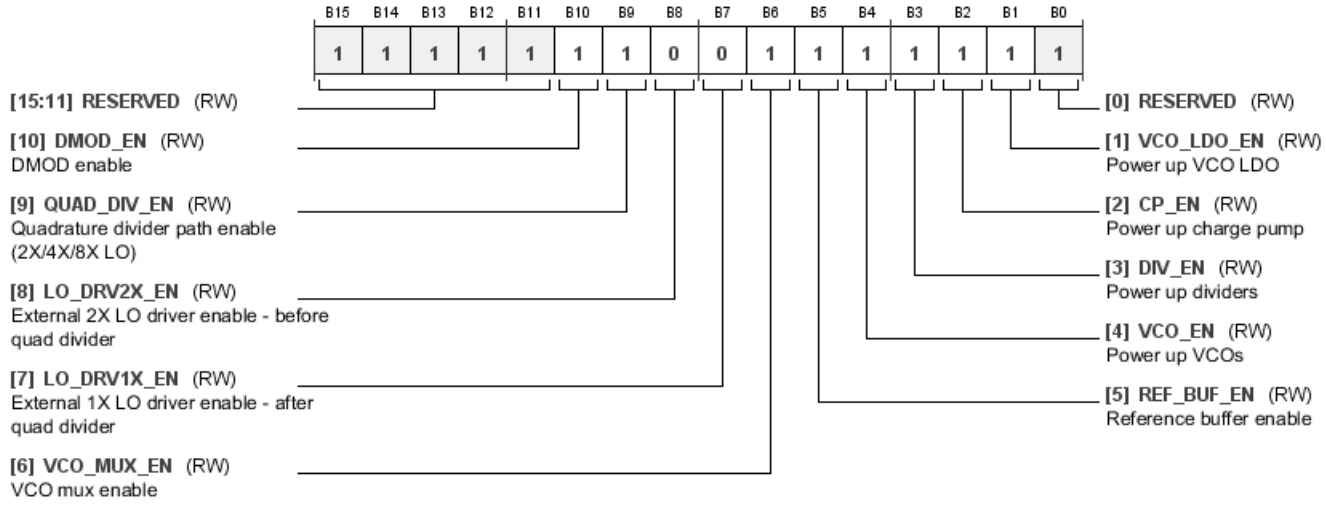


Table 19. Bit Descriptions for Enables

Bits	Bit Name	Settings	Description	Reset	Access
10	DMOD_EN		DMOD enable	0x1	RW
9	QUAD_DIV_EN		Quadrature divider path enable (2×/4×/8× LO)	0x1	RW
8	LO_DRV2X_EN		External 2× LO driver enable—before quad divider	0x0	RW
7	LO_DRV1X_EN		External 1× LO driver enable—after quad divider	0x0	RW
6	VCO_MUX_EN		VCO mux enable	0x1	RW
5	REF_BUF_EN		Reference buffer enable	0x1	RW
4	VCO_EN		Power up VCOs	0x1	RW
3	DIV_EN		Power up dividers	0x1	RW
2	CP_EN		Power up charge pump	0x1	RW
1	VCO_LDO_EN		Power up VCO LDO	0x1	RW

Address: 0x02, Reset: 0x002C, Name: INT_DIV

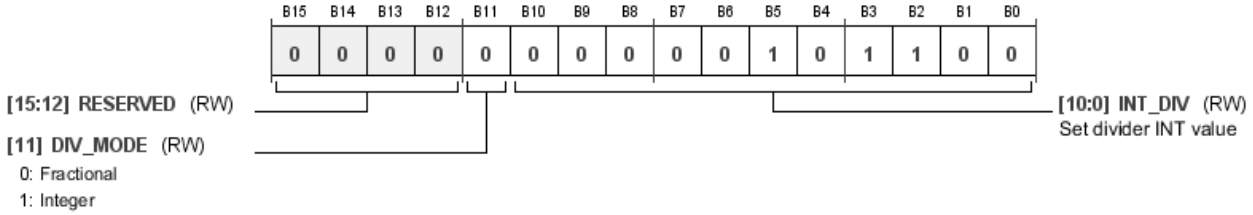


Table 20. Bit Descriptions for INT_DIV

Bits	Bit Name	Settings	Description	Reset	Access
11	DIV_MODE		Divide mode	0x0	RW
		0	Fractional		
		1	Integer		
[10:0]	INT_DIV		Set divider INT value Integer mode range: 21 to 123 Fractional mode range: 24 to 119	0x2C	RW

Address: 0x03, Reset: 0x0128, Name: FRAC_DIV

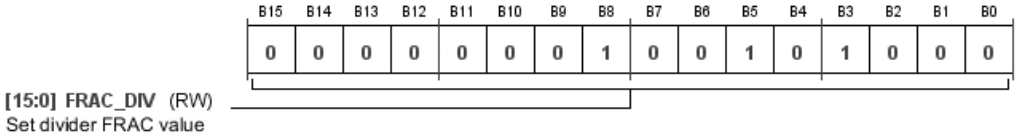


Table 21. Bit Descriptions for FRAC_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	FRAC_DIV		Set divider FRAC value	0x128	RW

Address: 0x04, Reset: 0x0600, Name: MOD_DIV

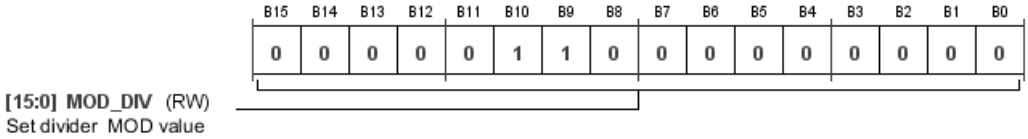


Table 22. Bit Descriptions for MOD_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	MOD_DIV		Set divider MOD value	0x600	RW

Address: 0x10, Reset: 0xFE7F, Name: PWRDWN_MASK

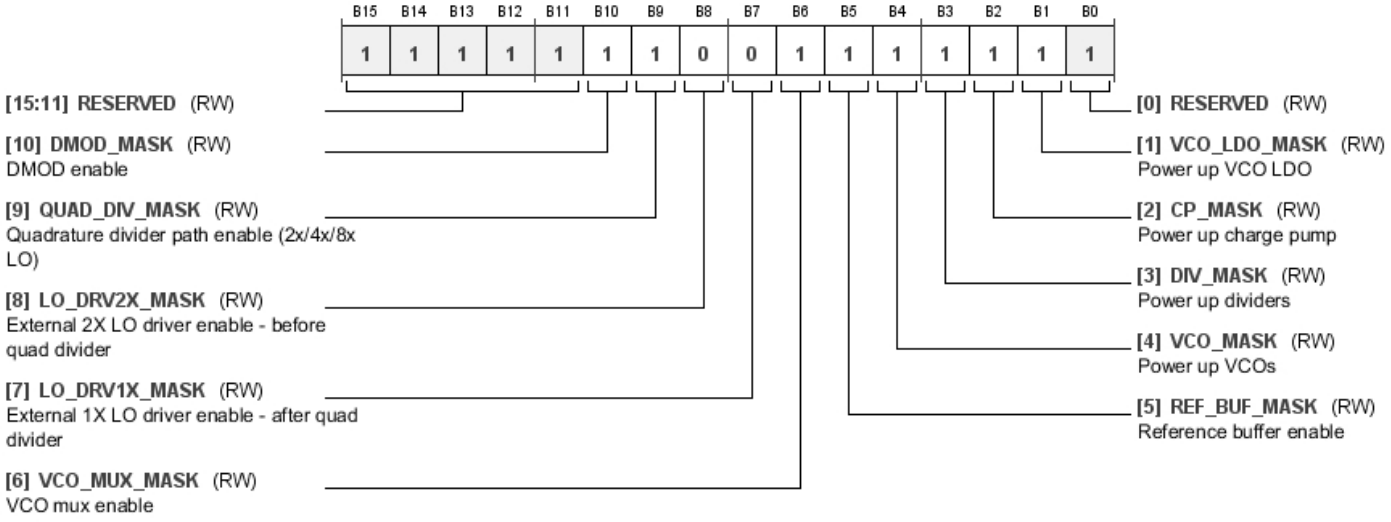


Table 23. Bit Descriptions for PWRDWN_MASK

Bits	Bit Name	Settings	Description	Reset	Access
10	DMOD_MASK		Demodulator (DMOD) enable	0x1	RW
9	QUAD_DIV_MASK		Quadrature divider path enable (2×/4×/8× LO)	0x1	RW
8	LO_DRV2X_MASK		External 2× LO driver enable—before quad divider	0x0	RW
7	LO_DRV1X_MASK		External 1× LO driver enable—after quad divider	0x0	RW
6	VCO_MUX_MASK		VCO mux enable	0x1	RW
5	REF_BUF_MASK		Reference buffer enable	0x1	RW
4	VCO_MASK		Power up VCOs	0x1	RW
3	DIV_MASK		Power up dividers	0x1	RW
2	CP_MASK		Power up charge pump	0x1	RW
1	VCO_LDO_MASK		Power up VCO LDO	0x1	RW

Address: 0x20, Reset: 0x0C26, Name: CP_CTL

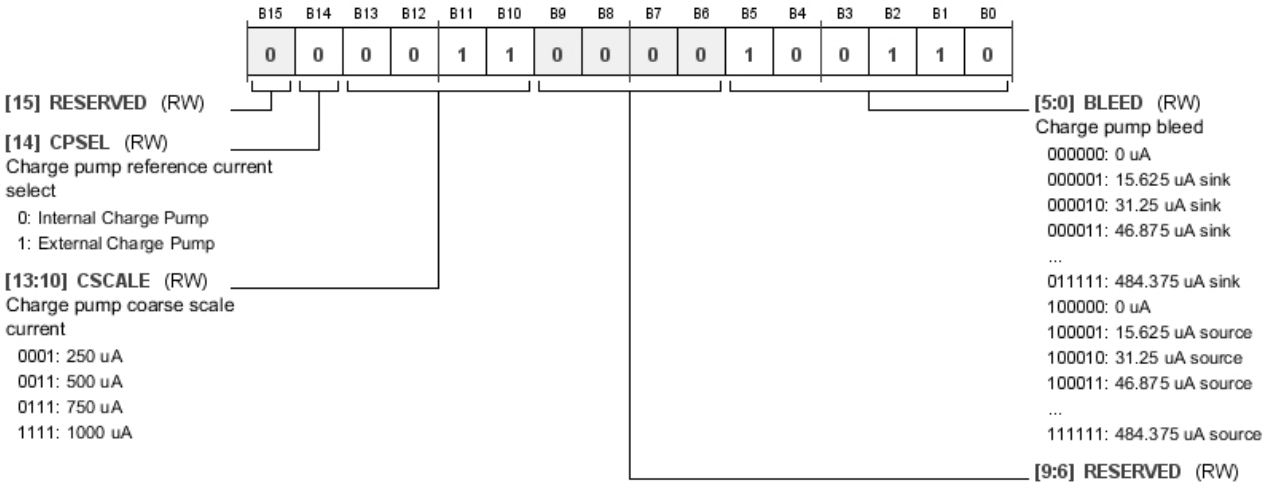


Table 24. Bit Descriptions for CP_CTL

Bits	Bit Name	Settings	Description	Reset	Access
14	CPSEL		Charge pump reference current select	0x0	RW
		0	Internal charge pump		
		1	External charge pump		
[13:10]	CSCALE		Charge pump coarse scale current	0x3	RW
		0001	250 µA		
		0011	500 µA		
		0111	750 µA		
		1111	1000 µA		
[5:0]	BLEED		Charge pump bleed	0x26	RW
		000000	0 µA		
		000001	15.625 µA sink		
		000010	31.25 µA sink		
		000011	46.875 µA sink		
		...			
		011111	484.375 µA sink		
		100000	0 µA		
		100001	15.625 µA source		
		100010	31.25 µA source		
		100011	46.875 µA source		
		...			
		111111	484.375 µA source		

Address: 0x21, Reset: 0x0003, Name: PFD_CTL

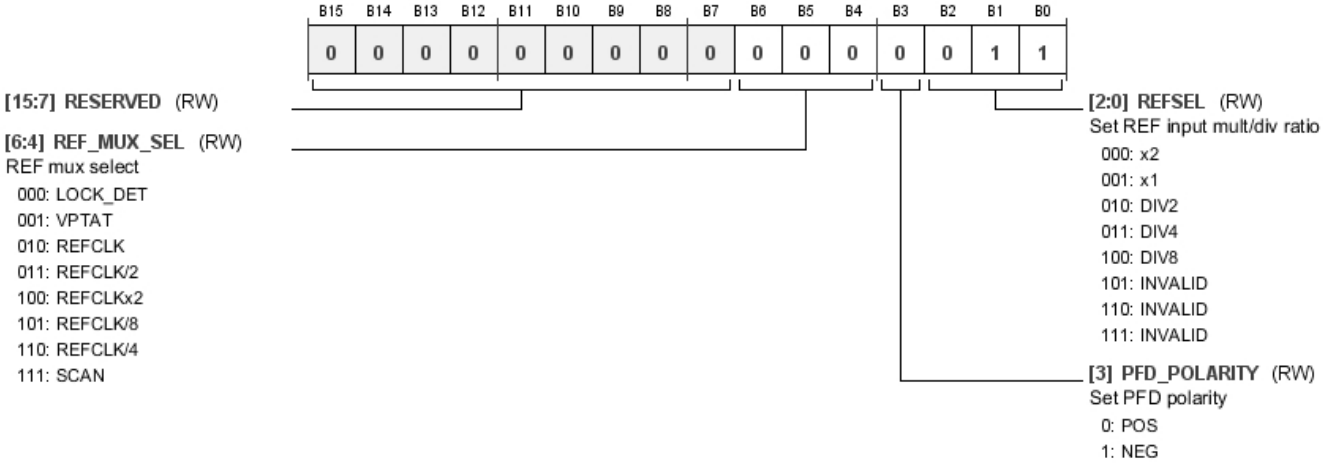


Table 25. Bit Descriptions for PFD_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	REF_MUX_SEL		Reference (REF) mux select	0x0	RW
		000	LOCK_DET		
		001	VPTAT		
		010	REFCLK		
		011	REFCLK/2		
		100	REFCLK × 2		
		101	REFCLK/8		
		110	REFCLK/4		
		111	SCAN		
3	PFD_POLARITY		Set PFD polarity	0x0	RW
		0	Positive		
		1	Negative		
[2:0]	REFSEL		Set REF input multiply/divide ratio	0x3	RW
		000	×2		
		001	×1		
		010	Divide by 2		
		011	Divide by 4		
		100	Divide by 8		

Address: 0x22, Reset: 0x2A03, Name: VCO_CTL

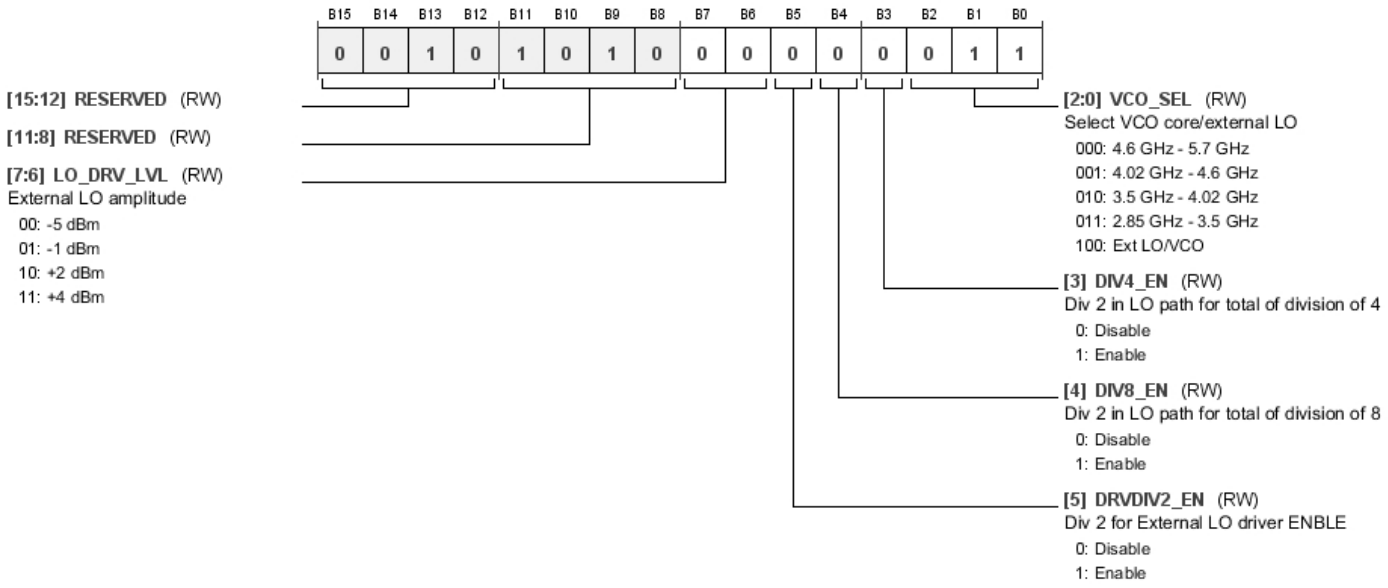


Table 26. Bit Descriptions for VCO_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LO_DRV_LVL		External LO amplitude	0x0	RW
		00	−5 dBm		
		01	−1 dBm		
		10	+2 dBm		
		11	+4 dBm		
5	DRVDIV2_EN		Divide by 2 for external LO driver enable	0x0	RW
		0	Disable		
		1	Enable		
4	DIV8_EN		Divide by 2 in LO path for total of division of 8	0x0	RW
		0	Disable		
		1	Enable		
3	DIV4_EN		Divide by 2 in LO path for total of division of 4	0x0	RW
		0	Disable		
		1	Enable		
[2:0]	VCO_SEL		Select VCO core/external LO	0x3	RW
		000	4.6 GHz to 5.7 GHz		
		001	4.02 GHz to 4.6 GHz		
		010	3.5 GHz to 4.02 GHz		
		011	2.85 GHz to 3.5 GHz		
		100	External LO/VCO		

Address: 0x23, Reset: 0x0000, Name: DGA_CTL

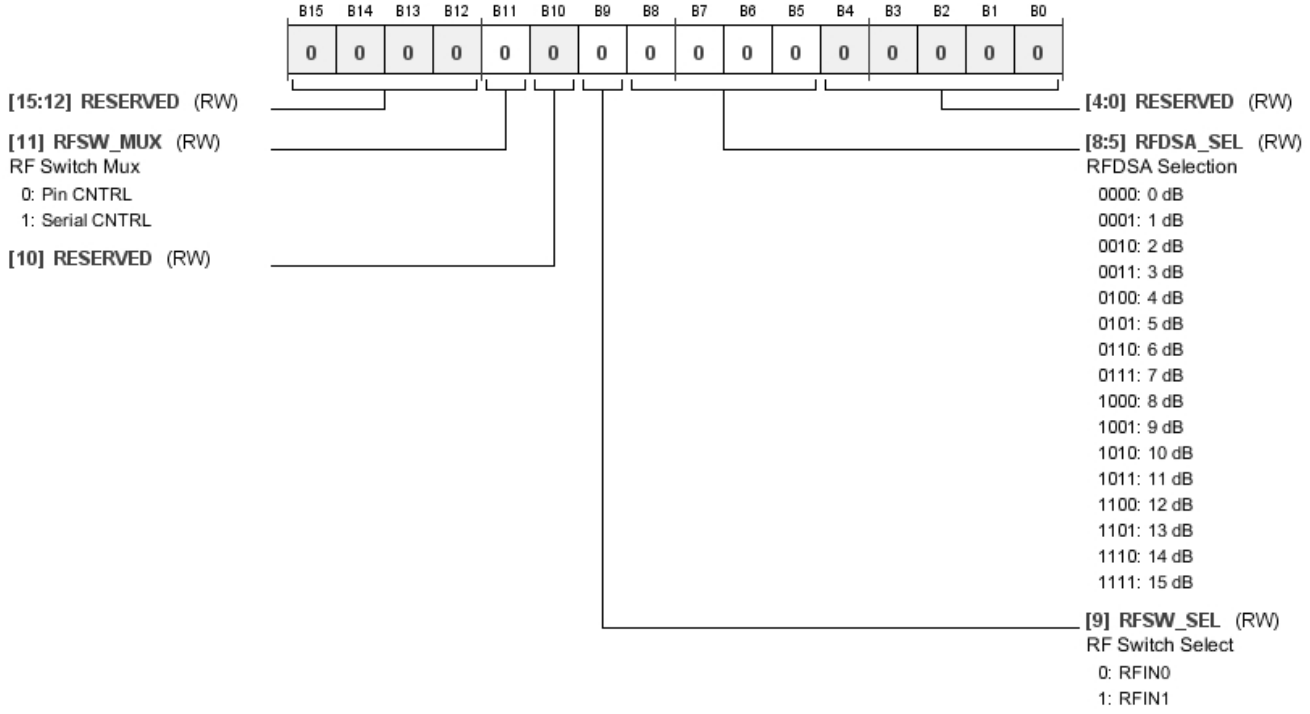


Table 27. Bit Descriptions for DGA_CTL

Bits	Bit Name	Settings	Description	Reset	Access
11	RFSW_MUX		RF switch mux	0x0	RW
		0	Pin control (CNTRL)		
		1	Serial control (CNTRL)		
9	RFSW_SEL		RF switch select	0x0	RW
		0	RFIN0		
		1	RFIN1		
[8:5]	RFDSA_SEL		RFDSA selection	0x0	RW
		0000	0 dB		
		0001	1 dB		
		0010	2 dB		
		0011	3 dB		
		0100	4 dB		
		0101	5 dB		
		0110	6 dB		
		0111	7 dB		
		1000	8 dB		
		1001	9 dB		
		1010	10 dB		
		1011	11 dB		
		1100	12 dB		
		1101	13 dB		
		1110	14 dB		
		1111	15 dB		

Address: 0x30, Reset: 0x0000, Name: BALUN_CTL

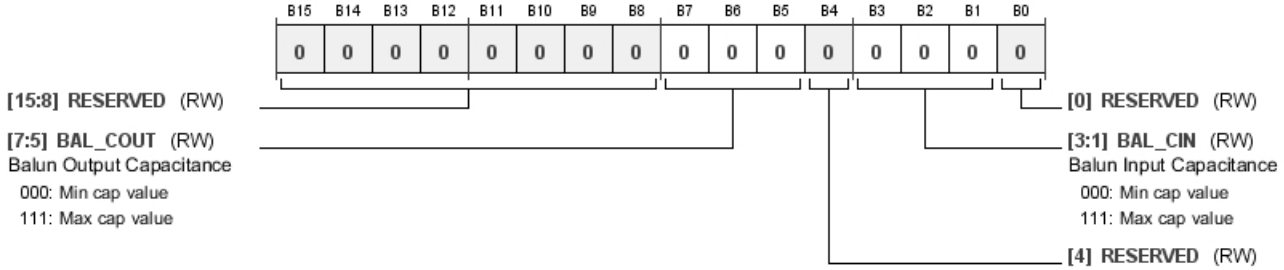


Table 28. Bit Descriptions for BALUN_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	BAL_COUT		Balun output capacitance	0x0	RW
		000	Minimum capacitance value		
		111	Maximum capacitance value		
[3:1]	BAL_CIN		Balun input capacitance	0x0	RW
		000	Minimum capacitance value		
		111	Maximum capacitance value		

Address: 0x31, Reset: 0x1101, Name: MIXER_CTL

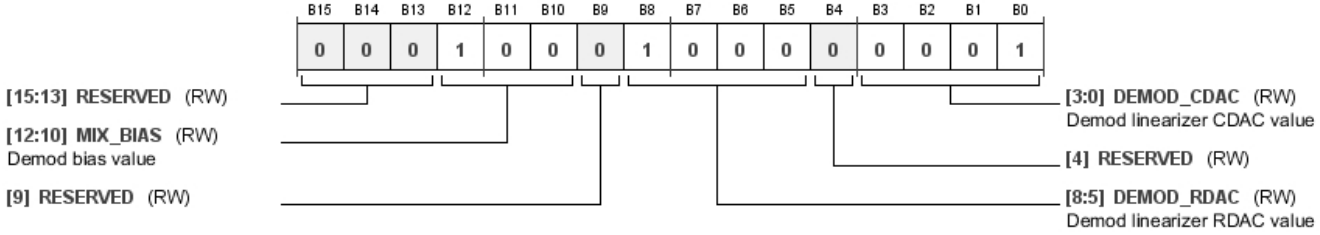


Table 29. Bit Descriptions for MIXER_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[12:10]	MIX_BIAS		Demodulator (demod) bias value	0x4	RW
[8:5]	DEMOD_RDAC		Demodulator linearizer RDAC value	0x8	RW
[3:0]	DEMOD_CDAC		Demodulator linearizer CDAC value	0x1	RW

Address: 0x32, Reset: 0x0900, Name: MOD_CTL0

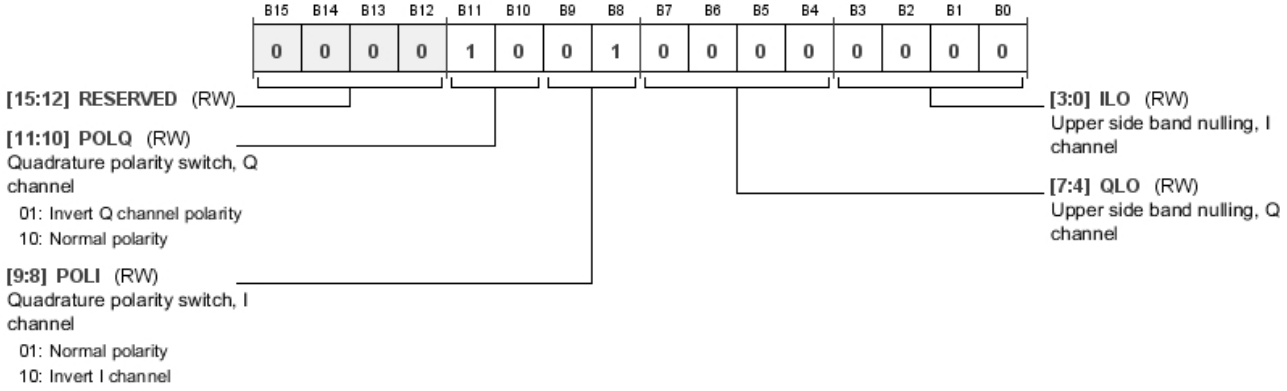


Table 30. Bit Descriptions for MOD_CTL0

Bits	Bit Name	Settings	Description	Reset	Access
[11:10]	POLQ		Quadrature polarity switch, Q channel	0x2	RW
		01	Invert Q channel polarity		
		10	Normal polarity		
[9:8]	POLI		Quadrature polarity switch, I channel	0x1	RW
		01	Normal polarity		
		10	Invert I channel		
[7:4]	QLO		Upper side band nulling, Q channel	0x0	RW
[3:0]	ILO		Upper side band nulling, I channel	0x0	RW

Address: 0x33, Reset: 0x0000, Name: MOD_CTL1

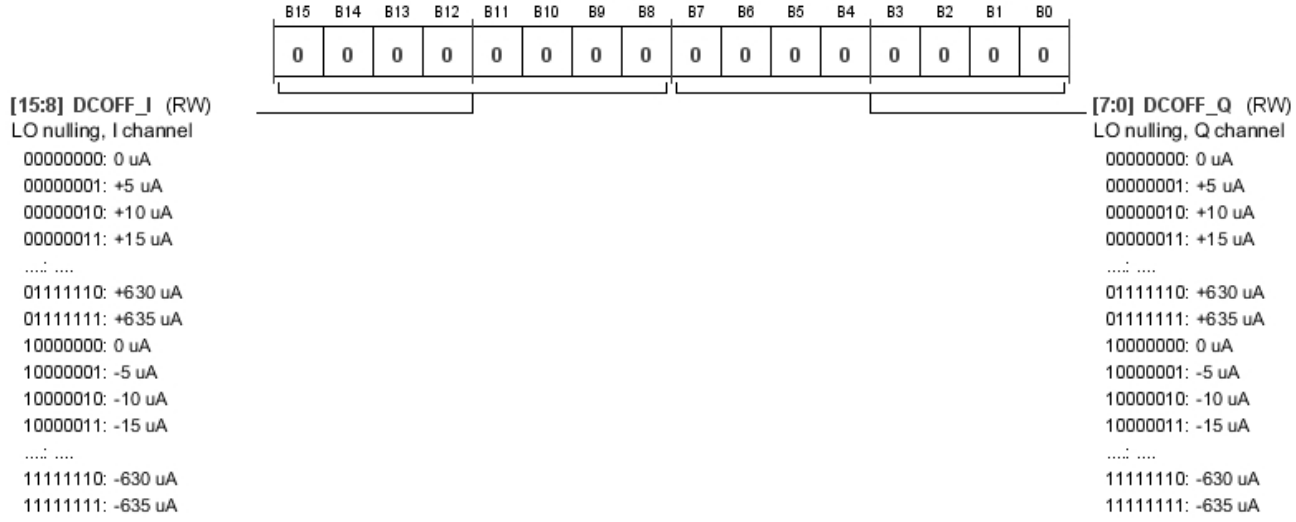


Table 31. Bit Descriptions for MOD_CTL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	DCOFFI		Baseband DC LO nulling, I channel	0x00	RW
		00000000	0 µA		
		00000001	+5 µA		
		00000010	+10 µA		
		00000011	+15 µA		
		01111110	+630 µA		
		01111111	+635 µA		
		10000000	0 µA		
		10000001	−5 µA		
		10000010	−10 µA		
		10000011	−15 µA		
		11111110	−630 µA		
		11111111	−635 µA		
[7:0]	DCOFFQ		Baseband DC LO nulling, Q channel	0x00	RW
		00000000	0 µA		
		00000001	+5 µA		
		00000010	+10 µA		
		00000011	+15 µA		
		01111110	+630 µA		
		01111111	+635 µA		
		10000000	0 µA		
		10000001	−5 µA		
		10000010	−10 µA		
		10000011	−15 µA		
		11111110	−630 µA		
		11111111	−635 µA		

Address: 0x34, Reset: 0x0B00, Name: MOD_CTL2

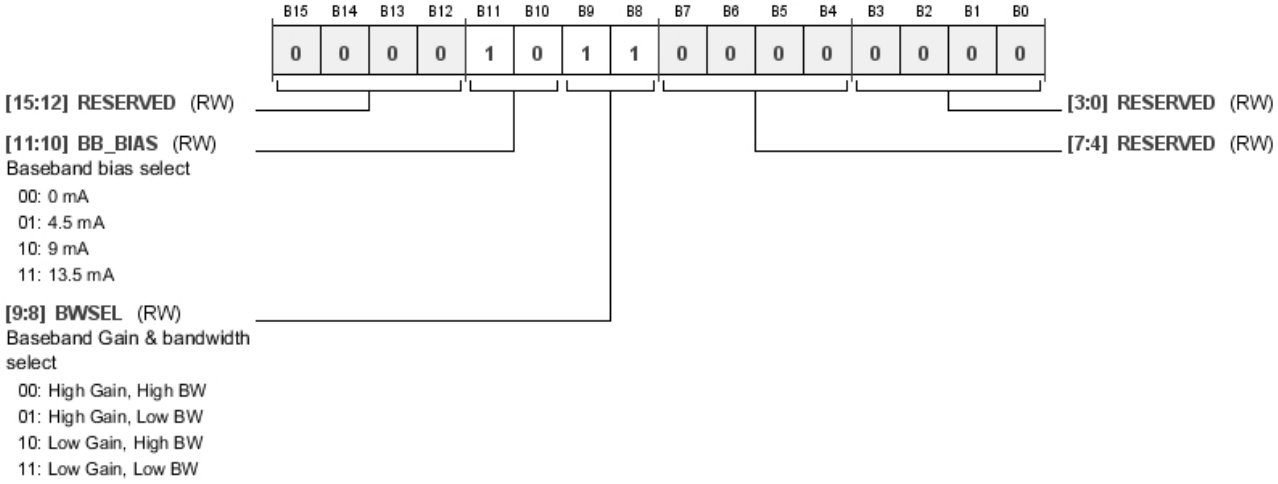


Table 32. Bit Descriptions for MOD_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[11:10]	BB_BIAS		Baseband bias select	0x2	RW
		00	0 mA		
		01	4.5 mA		
		10	9 mA		
		11	13.5 mA		
[9:8]	BWSEL		Baseband gain and bandwidth select	0x3	RW
		00	High gain, high bandwidth (refer to Table 15)		
		01	High gain, low bandwidth (refer to Table 15)		
		10	Low gain, high bandwidth (refer to Table 15)		
		11	Low gain, low bandwidth (refer to Table 15)		

Address: 0x40, Reset: 0x0010, Name: PFD_CTL2

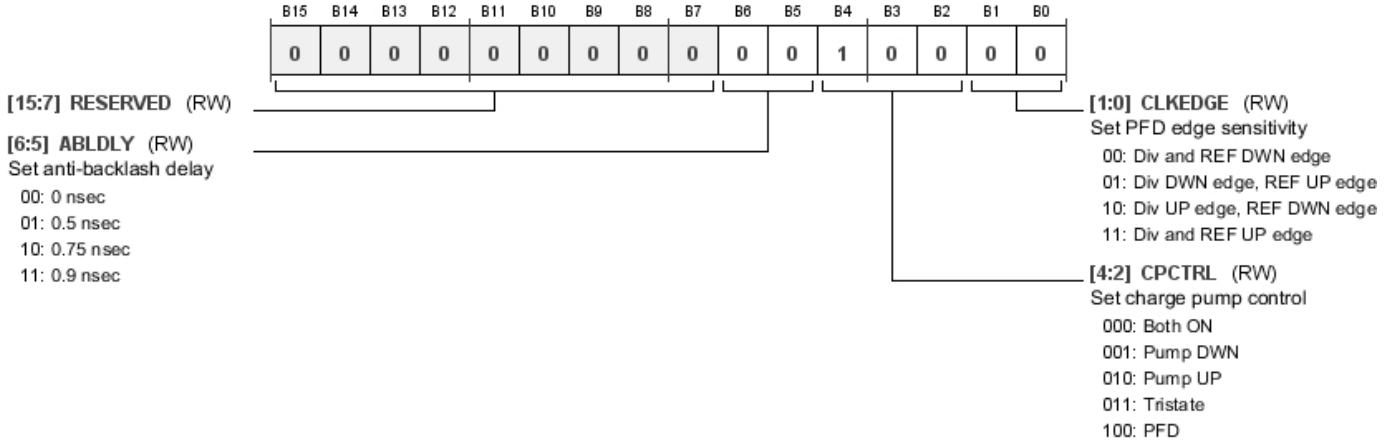


Table 33. Bit Descriptions for PFD_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[6:5]	ABLDLY		Set antibacklash delay	0x0	RW
		00	0 ns		
		01	0.5 ns		
		10	0.75 ns		
		11	0.9 ns		
[4:2]	CPCTRL		Set charge pump control	0x4	RW
		000	Both on		
		001	Pump down		
		010	Pump up		
		011	Tristate		
		100	PFD		
[1:0]	CLKEDGE		Set PFD edge sensitivity	0x0	RW
		00	Div and REF down edge		
		01	Div down edge, REF up edge		
		10	Div up edge, REF down edge		
		11	Div and REF up edge		

Address: 0x42, Reset: 0x000E, Name: DITH_CTL1

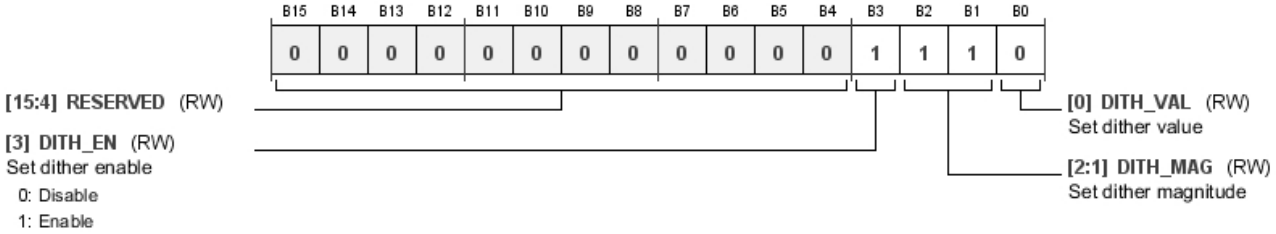


Table 34. Bit Descriptions for DITH_CTL1

Bits	Bit Name	Settings	Description	Reset	Access
3	DITH_EN		Set dither enable	0x1	RW
		0	Disable		
		1	Enable		
[2:1]	DITH_MAG		Set dither magnitude	0x3	RW
0	DITH_VAL		Set dither value	0x0	RW

Address: 0x43, Reset: 0x0001, Name: DITH_CTL2



Table 35. Bit Descriptions for DITH_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DITH_VAL		Set dither value	0x1	RW

Address: 0x44, Reset: 0x0000, Name: DIV_SM_CTL

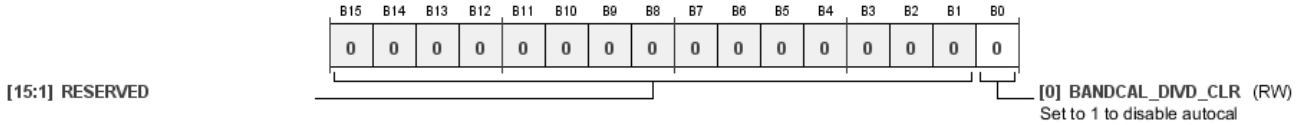


Table 36. Bit Descriptions for DIV_SM_CTL

Bits	Bit Name	Settings	Description	Reset	Access
0	BANDCAL_DIVD_CLR		Set to 1 to disable autocal	0x0	RW

Address: 0x45, Reset: 0x0000, Name: VCO_CTL2

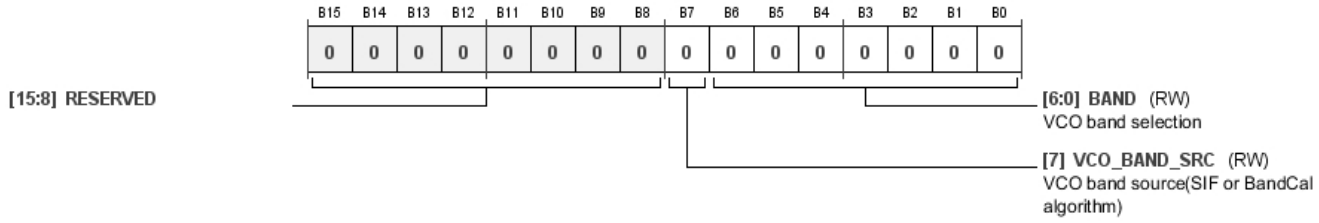


Table 37. Bit Descriptions for VCO_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
7	VCO_BAND_SRC		VCO band source (SIF or BANDCAL algorithm)	0x0	RW
[6:0]	BAND		VCO band selection	0x00	RW

Address: 0x46, Reset: 0x0000, Name: VCO_RB

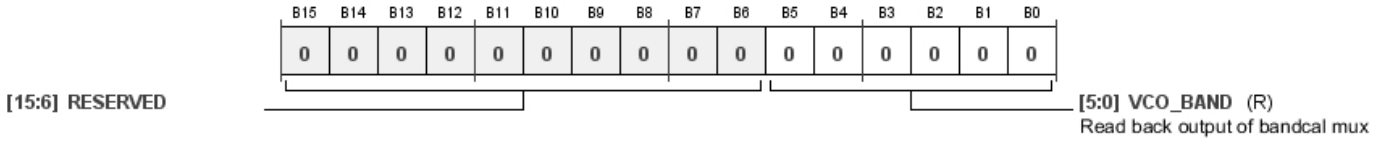


Table 38. Bit Descriptions for VCO_RB

Bits	Bit Name	Settings	Description	Reset	Access
[5:0]	VCO_BAND		Read back output of BANDCAL mux	0x00	R

Address: 0x49, Reset: 0x16BD, Name: VCO_CTL3

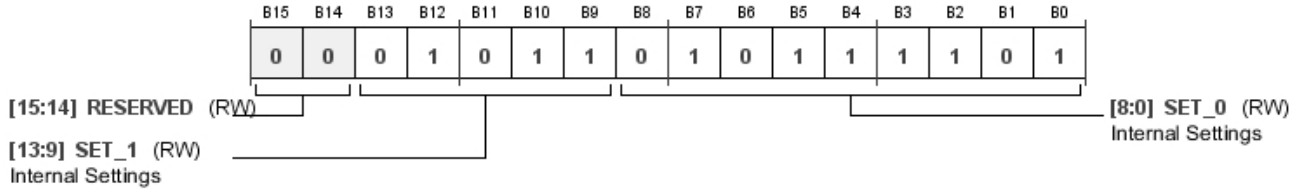


Table 39. Bit Descriptions for VCO_CTL3

Bits	Bit Name	Settings	Description	Reset	Access
[13:9]	SET_1		Internal settings (refer to the Required PLL/VCO Settings and Register Write Sequence section)	0xB	RW
[8:0]	SET_0		Internal settings (refer to the Required PLL/VCO Settings and Register Write Sequence section)	0xBD	RW

OUTLINE DIMENSIONS

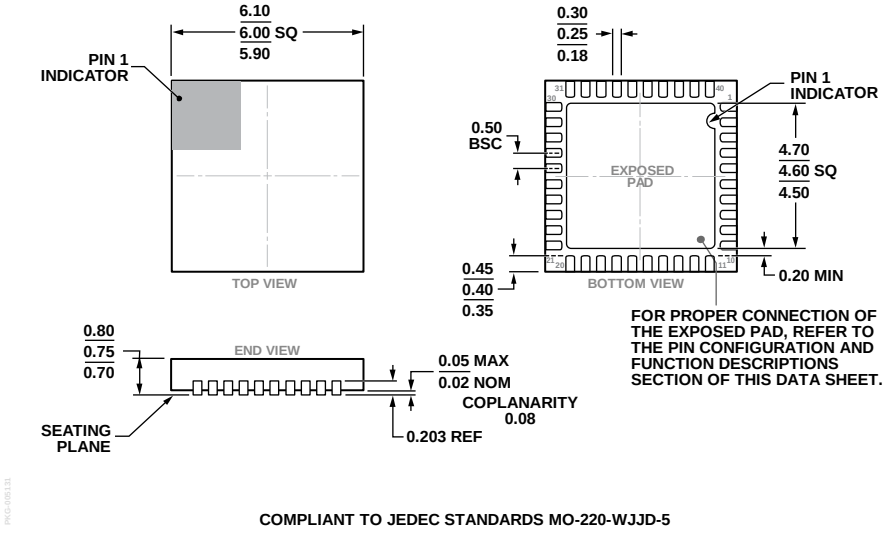


Figure 59. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6mm × 6mm Body and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6820ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADRF6820-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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