Broadband Up/Downconverting Mixer with Integrated Fractional-N PLL and VCO

Data Sheet **ADRF6655**

FEATURES

Broadband active mixer with integrated fractional-N PLL
RF input frequency range: 100 MHz to 2500 MHz
Internal LO frequency range: 1050 MHz to 2300 MHz
Flexible IF output interface
Input P1dB: 12 dBm
Input IP3: 29 dBm
Noise figure (SSB): 12 dB
Voltage conversion gain: 6 dB
Matched 200 Ω output impedance
SPI serial interface for PLL programming
40-lead 6 mm × 6 mm LFCSP

GENERAL DESCRIPTION

The ADRF6655 is a high dynamic range active mixer with integrated PLL and VCO. The synthesizer uses a programmable integer-N/fractional-N PLL to generate a local oscillator input to the mixer. The PLL reference input is nominally 20 MHz. The reference input can be divided by or multiplied by and then applied to the PLL phase detector. The PLL can support input reference frequencies from 10 MHz to 160 MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop filter. The loop filter output is then applied to an integrated VCO. The VCO output at $2 \times f_{LO}$ is then applied to a local oscillator (LO) divider as well as to a programmable PLL divider.

The programmable divider is controlled by an Σ-Δ modulator (SDM). The modulus of the SDM can be programmed between 1 and 2047.

The broadband, active mixer employs a bias adjustment to allow for enhanced IP3 performance at the expense of increased supply current. The mixer provides an input IP3 exceeding 25 dBm with 12 dB single sideband NF under typical conditions. The IIP3 can be boosted to ~29 dBm with roughly 20 mA of additional supplied current. The mixer provides a typical voltage conversion gain of 6 dB with a 200 Ω differential IF output impedance. The IF output can be externally matched to support upconversion over a limited frequency range.

The ADRF6655 is fabricated using an advanced silicon-germanium BiCMOS process. It is packaged in a 40-lead, exposed-paddle, Pb-free, 6 mm × 6 mm LFCSP. Performance is specified over a −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

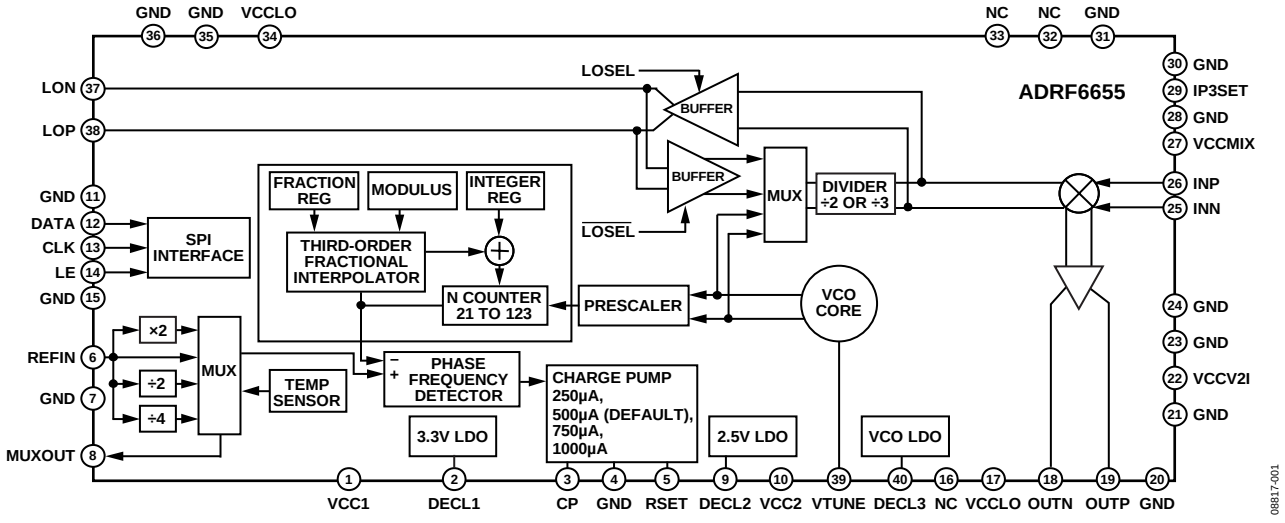


Figure 1.

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REVISION HISTORY

9/14—Rev. 0 to Rev. A

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2/10—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V; ambient temperature (T_A) = 25°C; REFIN = 20 MHz, phase frequency detector (PFD) frequency = 20 MHz, IF output loaded into 4-to-1 transformer matched to a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT FREQUENCY RANGE		100		2500	MHz
IF OUTPUT FREQUENCY RANGE	Can be matched externally for improved return loss at higher frequencies (see the Output Matching and Biasing section)	LF		2200	MHz
INTERNAL LO FREQUENCY RANGE	Divide-by-3 mode[1]	1050		1530	MHz
	Divide-by-2 mode[1]	1530		2300	MHz
EXTERNAL LO FREQUENCY RANGE	Divide-by-2 mode[2]	500		2300	MHz
MIXER					
Input Return Loss	INP, INN; relative to 50 Ω, from 350 MHz to 2200 MHz using TC1-1-13M+ balun[3]		12		dB
Output Return Loss	OUTP, OUTN; relative to 50 Ω out to 200 MHz using TC4-1W output transformer option[3]		12		dB
IF Output Impedance	OUTP, OUTN		200		Ω
Output Common Mode	OUTP, OUTN; external pull-up balun or inductors required		V_{POS}		V
Voltage Conversion Gain	IF output loaded into 200 Ω differential load		6		dB
Output Swing			2		V p-p
LO-to-IF Output Leakage	Can be improved using external filtering		−40		dBm
DYNAMIC PERFORMANCE	IP3Set = 3.2 V				
Upconversion	340 MHz RF input, 1200 MHz IF output using 1540 MHz LO (see Figure 56 for output matching network)				
Gain Flatness	Over ±50 MHz bandwidth for 1200 MHz output center frequency		0.25		dB p-p
Gain Temperature Coefficient	Average values from −40°C to +85°C		−10		mdB/°C
Output P1dB			11		dBm
Second-Order Output Intercept (IIP2)	−5 dBm each tone		60		dBm
Third-Order Output Intercept (IIP3)	−5 dBm each tone, IP3SET = 3.2 V		31		dBm
	−5 dBm each tone, IP3SET = open		28		dBm
Output Noise Spectral Density	IP3SET = 3.2 V, RF input terminated with 50 Ω		−160		dBm/Hz
	IP3SET = 3.2 V, RF input = −5 dBm, f_{LO} = 1315 MHz with f_{RF} = 380 MHz applied, measured noise at f_{IF} = 915 MHz		−155		dBm/Hz
Downconversion	1880 MHz RF input, 140 MHz IF output using 1740 MHz LO				
Gain Flatness	Over ±50 MHz bandwidth for 1880 MHz input center frequency		0.25		dB p-p
Gain Temperature Coefficient	Average values from −40°C to +85°C		−10		mdB/°C
Input P1dB	IP3SET = 3.2 V		14		dBm
	IP3SET = open		12		dBm
Second-Order Input Intercept (IIP2)	−5 dBm each tone		50		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each tone, IP3SET = 3.2 V		27		dBm
	−5 dBm each tone, IP3SET = open		26		dBm
SSB Noise Figure (NF)	IP3SET = 3.2 V		14		dB
	IP3SET = open		12		dB
SSB Noise Figure Under Blocking Conditions	−5 dBm RF input blocker applied at 995 MHz, f_{LO} = 1200 MHz, noise measured at 5 MHz offset from IF output blocker				
	IP3SET = 3.2 V		20.75		dB
	IP3SET = open		20.25		dB
IF/2 Spurious	−5 dBm RF input power		−65		dBc
LO OUTPUT	LOP, LON				
Output Level	1 × LO into a 50 Ω load, LO buffer enabled		−7		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to 1 × LO[4]				
Fundamental VCO Sensitivity	VCO tuning sensitivity before divide-by-2 or divide-by-3		75		MHz/V
Spurs	Measured at LO output				
Reference/PFD Spurs	$f_{PFD}/2$		−95		dBc
	f_{PFD}		−83		dBc
	$2 \times f_{PFD}$		−85		dBc
	$4 \times f_{PFD}$		−88		dBc
Phase Noise	PFD frequency = 20 MHz[4]				
LO Frequency = 1330 MHz					
	@ 10 kHz offset		−85		dBc/Hz
	@ 100 kHz offset		−114		dBc/Hz
	@ 1 MHz offset		−138		dBc/Hz
	@ 10 MHz offset		−154		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.3		°rms
LO Frequency = 1840 MHz					
	@ 10 kHz offset		−83		dBc/Hz
	@ 100 kHz offset		−111		dBc/Hz
	@ 1 MHz offset		−136		dBc/Hz
	@ 10 MHz offset		−152		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.4		°rms
PFD Frequency		19.33	20	40	MHz
REFERENCE CHARACTERISTICS	REF_{IN}, MUXOUT				
REFIN Input Frequency		10	20	160	MHz
REFIN Input Capacitance			4		pF
REFIN Input Current			±100		µA
REFIN Input Sensitivity	AC-coupled	0.25	1	3.3	V p-p
MUXOUT Output Levels	V_{OL} (lock detect output selected)			0.25	V
	V_{OH} (lock detect output selected)	2.7			V
CHARGE PUMP	CP				
Pump Current	Charge pump current adjustable using Register 4 and/or R_{SET} (see Pin 5 description)		500		µA
Output Compliance Range		1		2.8	V
LOGIC INPUTS	CLK, DATA, LE				
V_{INH}, Input High Voltage		1.4		3.3	V
V_{INL}, Input Low Voltage		0		0.7	V
I_{INH}/I_{INL}, Input Current			±1		µA
C_{IN}, Input Capacitance			3		pF
POWER SUPPLIES	VCC1, VCC2, VCCLO				
Voltage Range		4.75	5	5.25	V
Supply Current	LO output buffer disabled				
	PLL only		115		mA
	Normal TX mode, IP3SET = 3.2 V, $f_{LO} \leq 1530$ MHz (divide-by-3)		310		mA
	Normal TX mode, IP3SET = 3.2 V, $f_{LO} > 1530$ MHz (divide-by-2)		270		mA
	Normal RX mode, IP3SET = open, $f_{LO} \leq 1530$ MHz (divide-by-3)		285		mA
	Normal RX mode, IP3SET = open, $f_{LO} > 1530$ MHz (divide-by-2)		245		mA
	Power-down mode		15		mA

[1] Internal LO path divider programmed via serial interface. See the LO Signal Chain section for additional information.
[2] See the External LO Interface section.
[3] Improved return loss can be achieved using external matching. See the Circuit Description section for more details.
[4] Measured on standard evaluation board with 1.5 kHz loop filter (C13 = 47 nF, C14 = 0.1 µF, C15 = 4.7 µF, R9 = 270 Ω, R10 = 68 Ω).

TIMING CHARACTERISTICS

Table 2. Serial Interface Timing, V_{CC} = 5 V ± 5%

Parameter	Limit	Unit	Test Conditions/Comments
t_1	20	ns minimum	LE setup time
t_2	10	ns minimum	DATA to CLK setup time
t_3	10	ns minimum	DATA to CLK hold time
t_4	25	ns minimum	CLK high duration
t_5	25	ns minimum	CLK low duration
t_6	10	ns minimum	CLK to LE setup time
t_7	20	ns minimum	LE pulse width

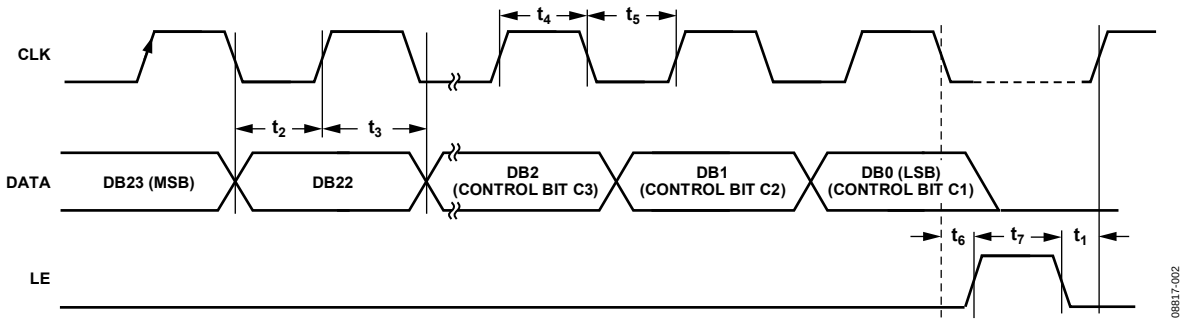


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{CC}	5.5 V
Digital I/O CLK, DATA, LE	−0.3 V to +3.6 V
OUTP, OUTN	V_{CC}
LOP, LON	16 dBm
INN, INP	20 dBm
DECL3 Using External Bias Option	3.5 V
θ_{JA} (Exposed Paddle Soldered Down)[1]	35°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Per JDEC standard JESD 51-2. For information on optimizing thermal impedance, see the Evaluation Board Layout and Thermal Grounding section.

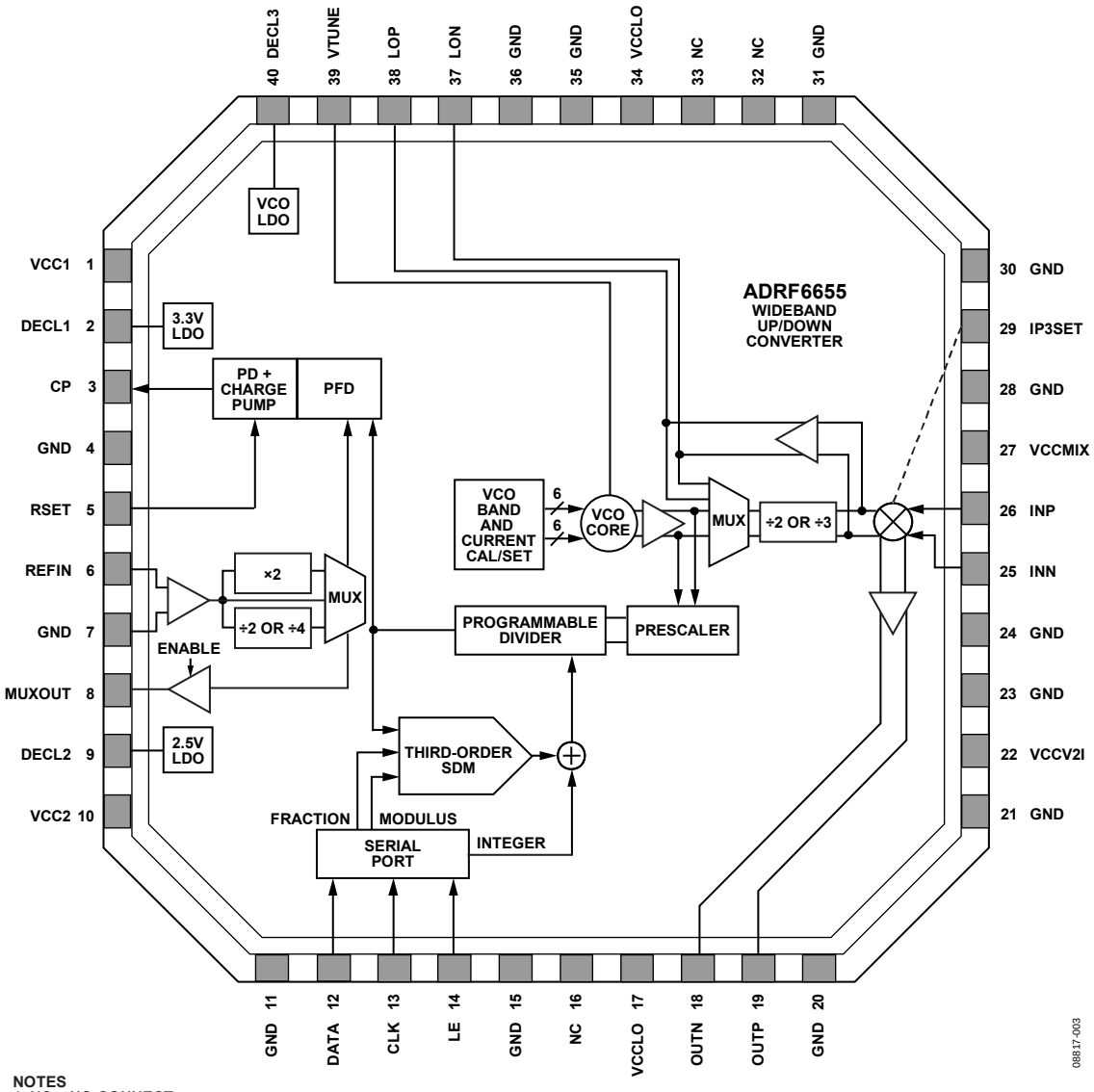
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESPCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PADDLE MUST BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC1	Power Supply for Internal 3.3 V LDO. The power supply voltage range is 4.75 V to 5.25 V. Supply pin should be decoupled with 100 pF and 0.1 µF capacitors located close to the pin.
2	DECL1	Decoupling Node for 3.3 V LDO. Pin should be decoupled with 100 pF, 0.1 µF, and 10 µF capacitors located close to the pin.
3	CP	Charge Pump Output Pin. Connect this pin to V_{TUNE} through the loop filter.
4, 7, 11, 15, 20, 21, 23, 24, 28, 30, 31, 35, 36	GND	Ground. Connect these pins to a low impedance ground plane.

Pin No.	Mnemonic	Description
5	RSET	Charge Pump Current. The nominal charge pump current can be set to either 250 µA, 500 µA, 750 µA, or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (internal reference current). In this mode, no external R_{SET} is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to $$RSET[\Omega] = \left[\frac{217.4 \times I_{CP,BASE}}{250}\right] - 37.8$$ where $I_{CP,BASE}$ is the base charge pump current in µA. For further details on the charge pump current, see the Register 4—Charge Pump, PFD, and Reference Path Control section.
6	REFIN	Reference Input. Nominal input level is 1 V p-p. Input range is 10 MHz to 160 MHz. This pin must be ac-coupled.
8	MUXOUT	Multiplexer Output. This output allows either a digital lock detect, a voltage proportional to temperature, or a buffered, frequency-scaled reference signal to be accessed externally. The output is selected by programming the appropriate bits in Register 4.
9	DECL2	Decoupling Node for 2.5 V LDO. Pin should be decoupled with 100 pF, 0.1 µF, and 10 µF capacitors located close to the pin.
10	VCC2	Power Supply for Internal 2.5 V LDO. The power supply voltage range is 4.75 V to 5.25 V. Supply pin should be decoupled with 100 pF and 0.1 µF capacitors located close to the pin.
12	DATA	Serial Data Input. The serial data input is loaded MSB first with the three LSBs being the control bits.
13	CLK	Serial Clock Input. This serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.
14	LE	Load Enable. When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word.
16, 32, 33	NC	No Connection.
17, 34	VCCLO	Power Supply for LO Path. The power supply voltage range is 4.75 V to 5.25 V. Supply pin should be decoupled with 100 pF and 0.1 µF capacitors located close to the pin.
18,19	OUTN, OUTP	Mixer IF Outputs. These pins should be pulled to VCC with RF chokes.
22	VCCV2I	Power Supply for Voltage to Current Input Stage. The power supply voltage range is 4.75 V to 5.25 V. Supply pin should be decoupled with 100 pF and 0.1 µF capacitors located close to the pin.
25, 26	INN, INP	Mixer RF Inputs. Differential RF Inputs. Internally matched to 50 Ω. This pin must be ac-coupled.
27	VCCMIX	Power Supply for Mixer. The power supply voltage range is 4.75 V to 5.25 V. Supply pin should be decoupled with 100 pF and 0.1 µF capacitors located close to the pin.
29	IP3SET	Connect Resistor to VCC to Adjust IP3.
37, 38	LON, LOP	Local Oscillator Input/Output. The internally generated $1 \times f_{LO}$ is available on these pins. When internal LO generation is disabled, an external $2 \times f_{LO}$ or $3 \times f_{LO}$ (depending on divider selection) can be applied to these pins. This pin must be ac-coupled.
39	VTUNE	VCO Control Voltage Input. This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1 V to 2.8 V.
40	DECL3	Decoupling Node for VCO LDO. Connect a 100 pF capacitor and a 10 µF capacitor between this pin and ground.
	EPAD (EP)	The exposed paddle must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, PFD = 20 MHz, REFIN = 20 MHz, IP3SET = 3.2 V, unless otherwise noted.

DOWNCONVERSION

Measured using typical downconversion circuit schematic with high-side LO and 140 MHz IF output, unless otherwise noted.

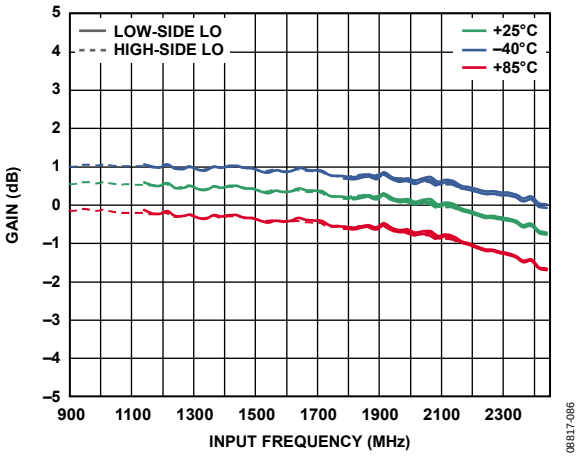


Figure 4. Conversion Gain vs. Input Frequency

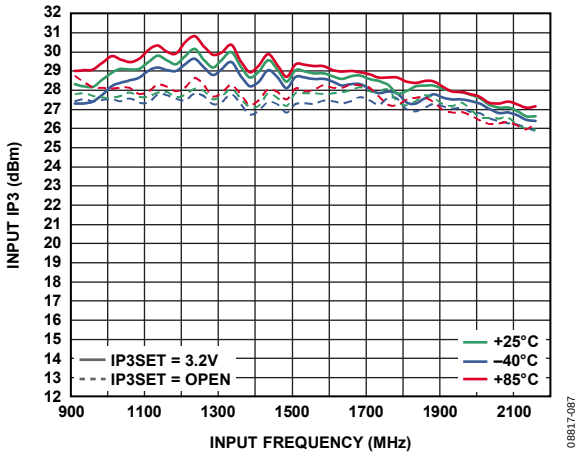


Figure 7. Input IP3 vs. Input Frequency

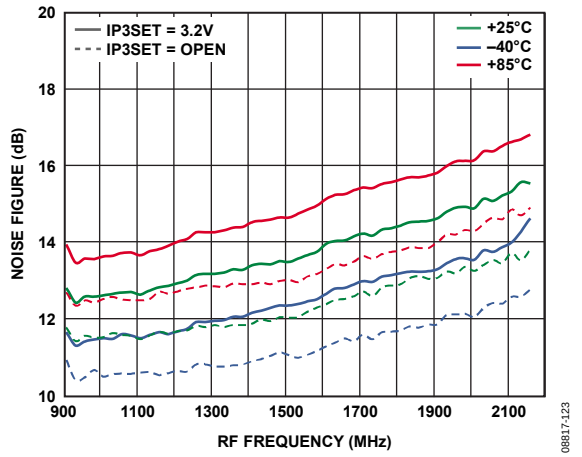


Figure 5. SSB Noise Figure vs. RF Frequency

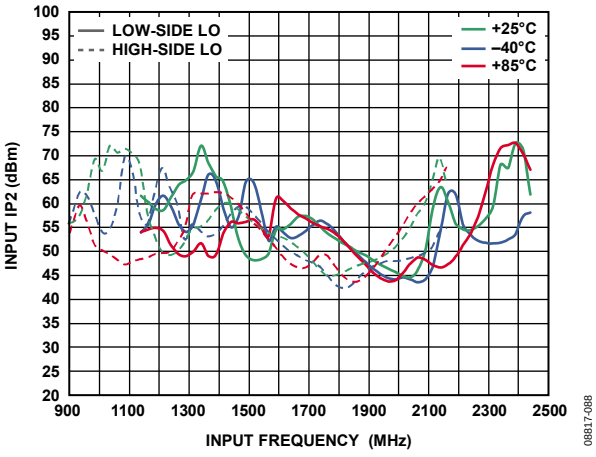


Figure 8. Input IP2 vs. Input Frequency

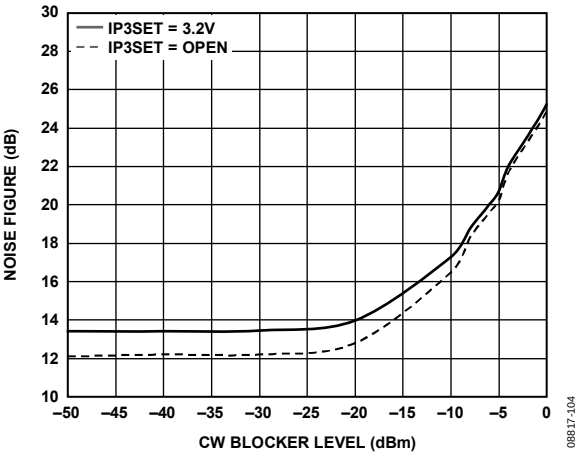


Figure 6. SSB Noise Figure vs. CW Blocker Level

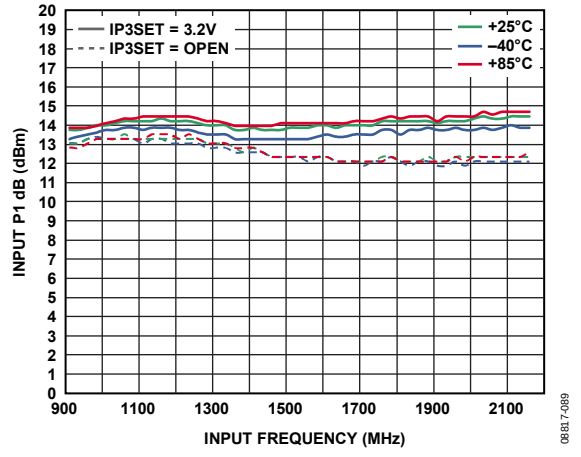


Figure 9. Input P1dB vs. Input Frequency

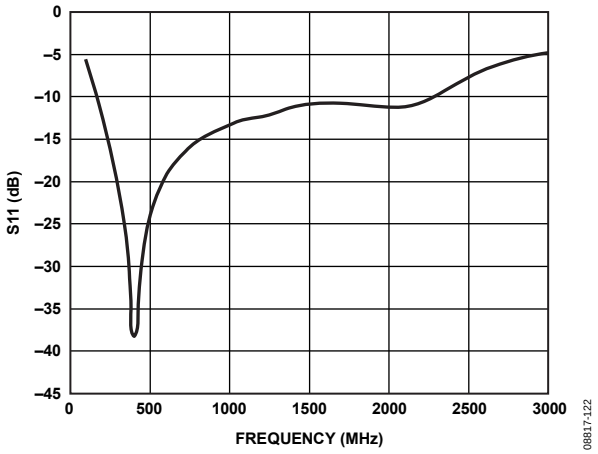


Figure 10. RF Port Input Return Loss (S11) vs. Frequency Measured through TC1-1-13M+

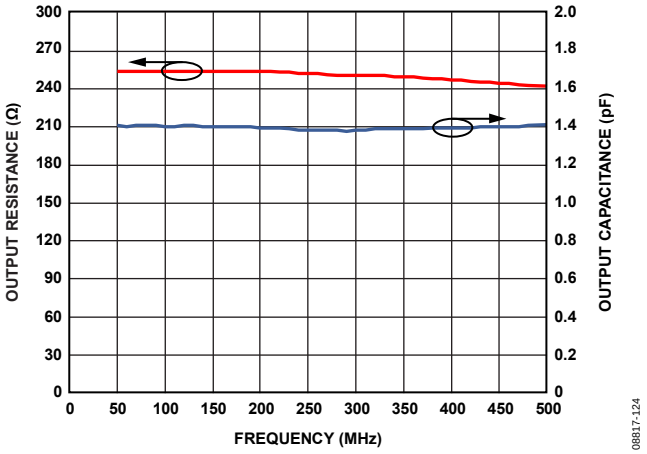


Figure 11. IF Port Output Impedance vs. Frequency

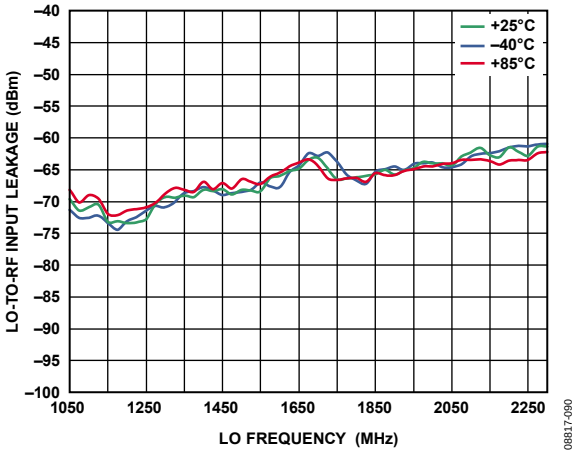


Figure 12. LO-to-RF Input Port Leakage vs. LO Frequency

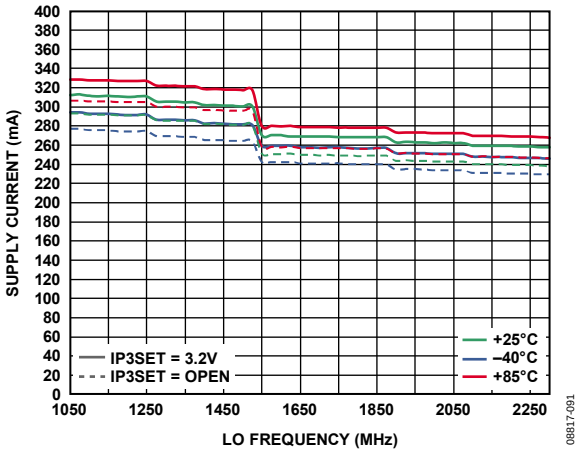


Figure 13. Supply Current vs. LO Frequency

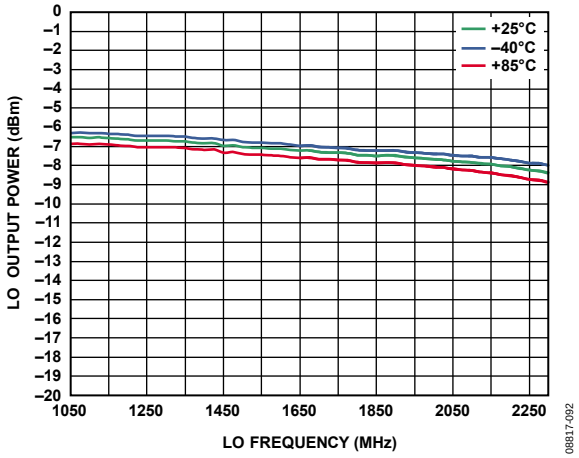


Figure 14. LO Port Output Power vs. LO Frequency

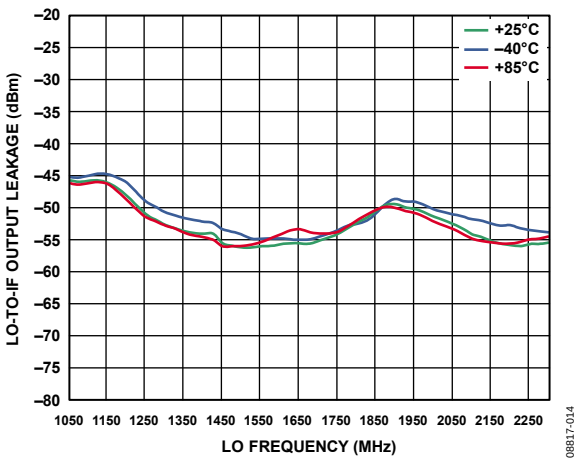


Figure 15. LO-to-IF Output Port Leakage vs. LO Frequency

UPCONVERSION

Measured using typical upconversion circuit schematic with high-side LO and 340 MHz RF input, unless otherwise noted.

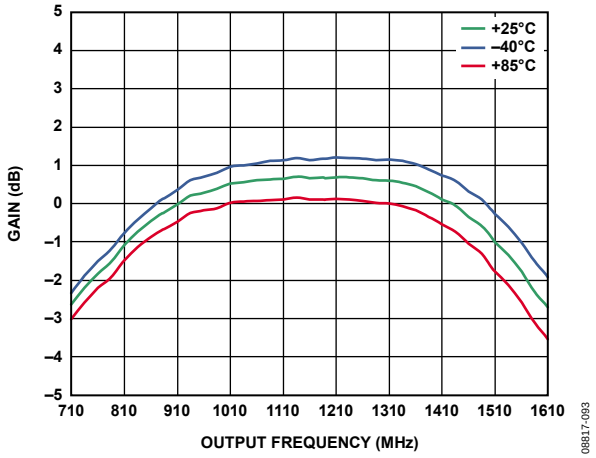


Figure 16. Conversion Gain vs. Output Frequency

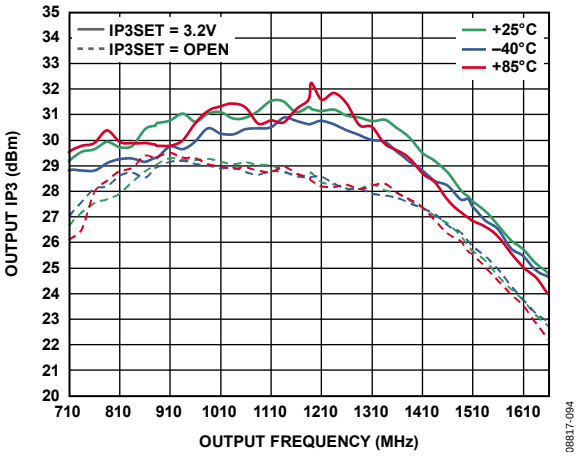


Figure 19. Output IP3 vs. Output Frequency

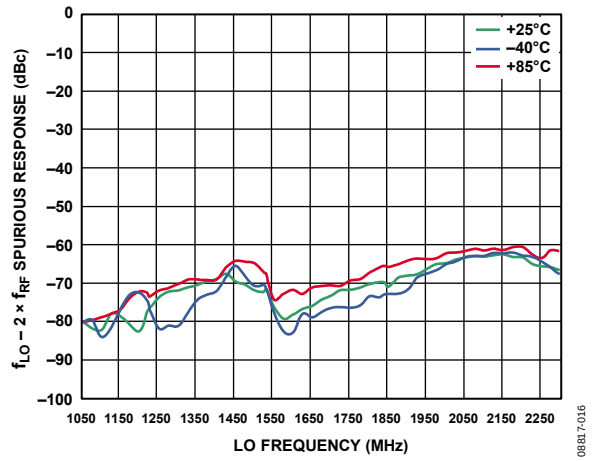


Figure 17. $f_{LO} - 2 \times f_{RF}$ Spurious Response vs. LO Frequency (Relative to IF Output Power)

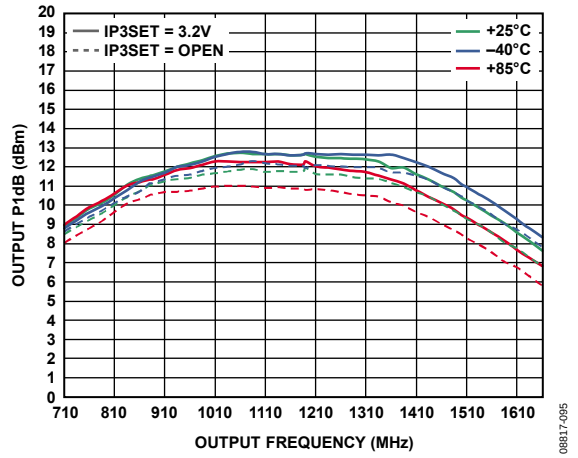


Figure 20. Output P1dB vs. Output Frequency

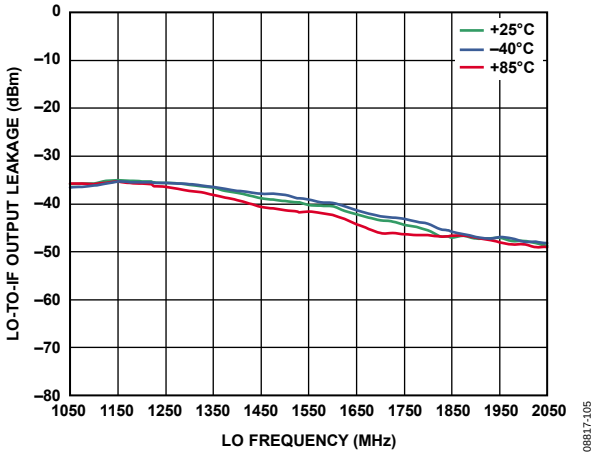


Figure 18. LO-to-IF Output Leakage vs. Frequency

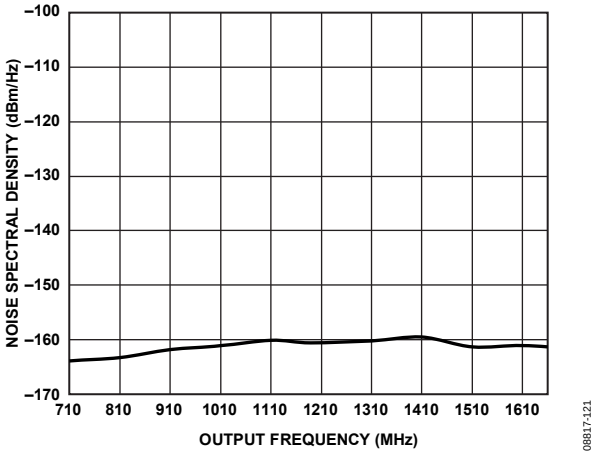


Figure 21. Output Noise Spectral Density vs. Output Frequency

PLL CHARACTERISTIC

Measured using typical downconversion circuit schematic with high-side LO and 140 MHz IF output, loop filter = 1.5 kHz, unless otherwise noted.

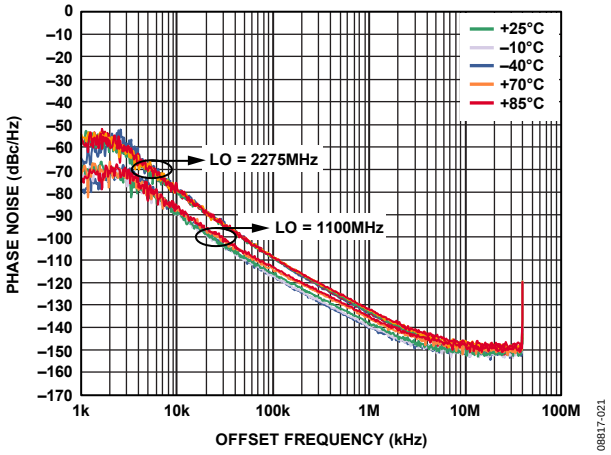


Figure 22. Typical Fractional-N Phase Noise Plot

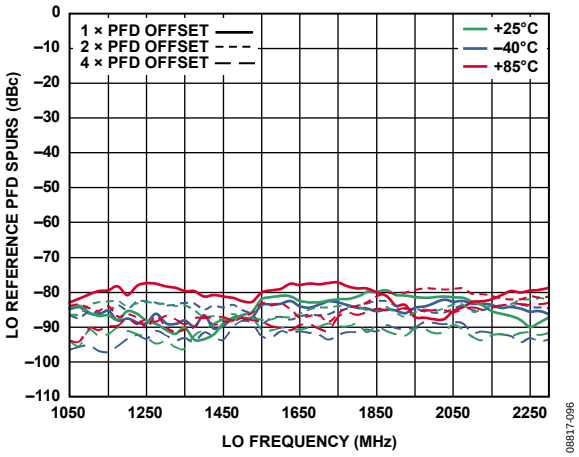


Figure 25. LO Reference/PFD Spurs vs. LO Frequency

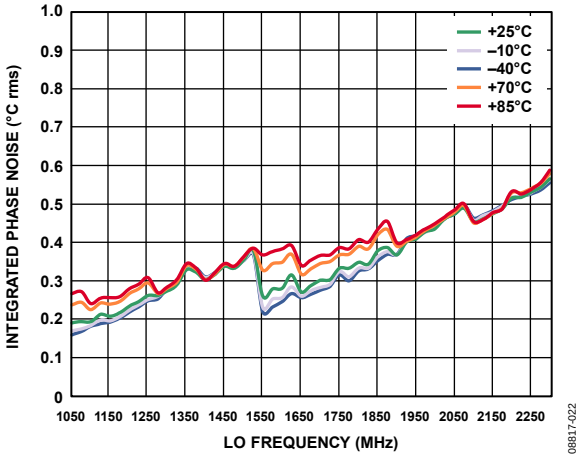


Figure 23.10 kHz to 40 MHz Integrated Phase Noise vs. LO Frequency

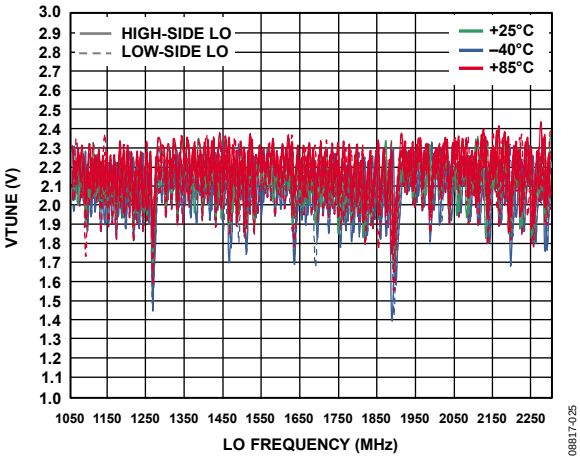


Figure 26. Tuning Voltage vs. LO Frequency

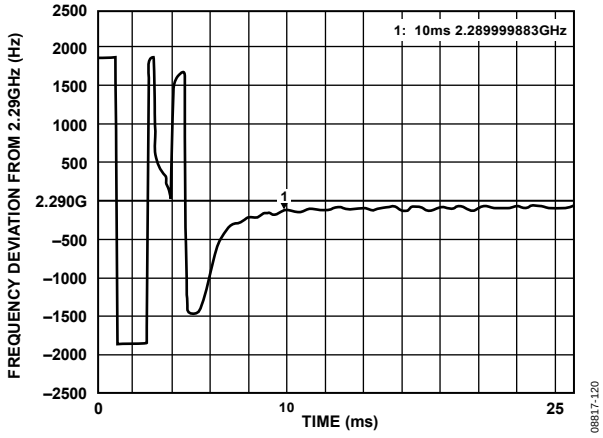


Figure 24. Lock Time for 10 MHz Step with 1.5 kHz Loop Filter

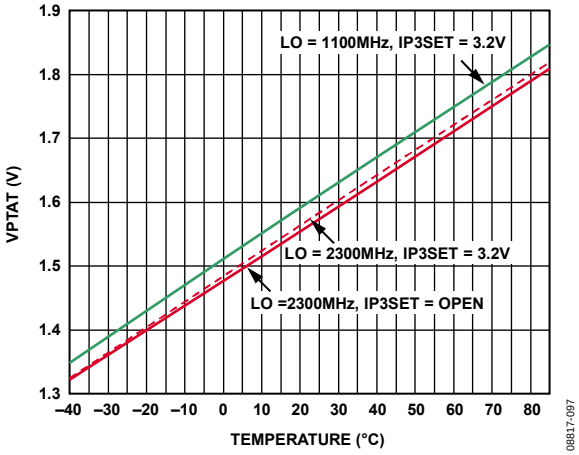


Figure 27. VPTAT MUXOUT Voltage vs. Temperature

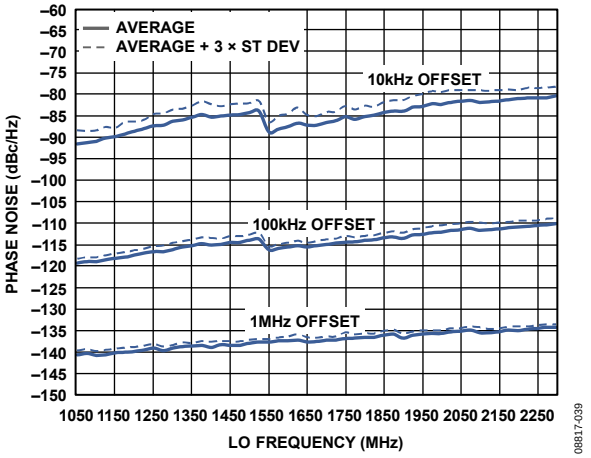


Figure 28. –40°C Spot Phase Noise vs. LO Frequency

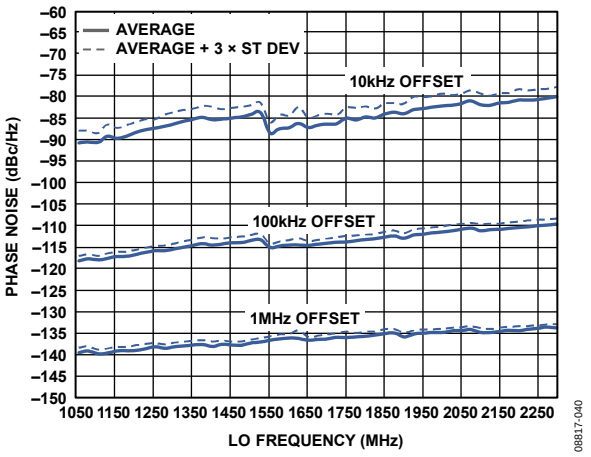


Figure 29. –10°C Spot Phase Noise vs. LO Frequency

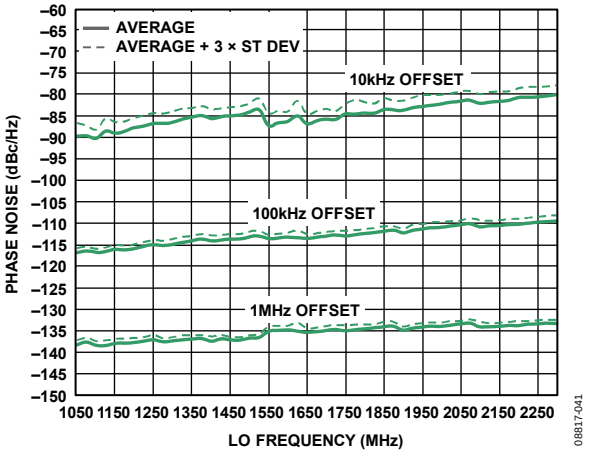


Figure 30. 25°C Spot Phase Noise vs. LO Frequency

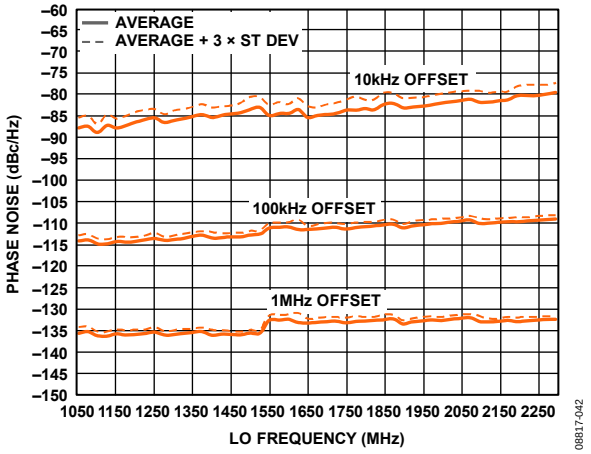


Figure 31. 70°C Spot Phase Noise vs. LO Frequency

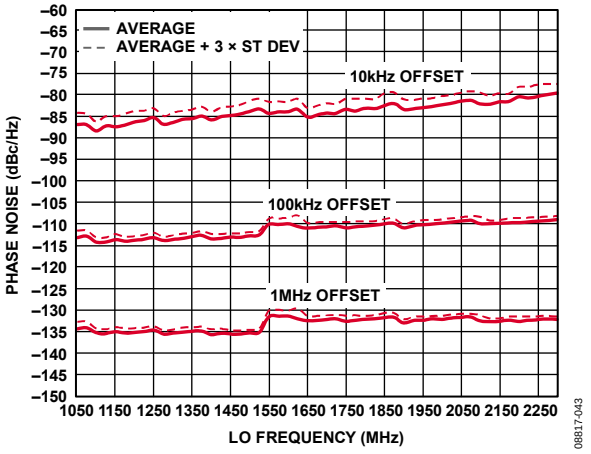


Figure 32. 85°C Spot Phase Noise vs. LO Frequency

COMPLIMENTARY CUMULATIVE DISTRIBUTION FUNCTION (CCDF): DOWNCONVERSION, LO = 1100 MHz, RF = 900 MHz

V_S = 5 V, T_A = 25°C, PFD = 20 MHz, REFIN = 20 MHz, IP3SET = open, as measured using typical downconversion circuit schematic with high-side LO and 200 MHz IF output, unless otherwise noted.

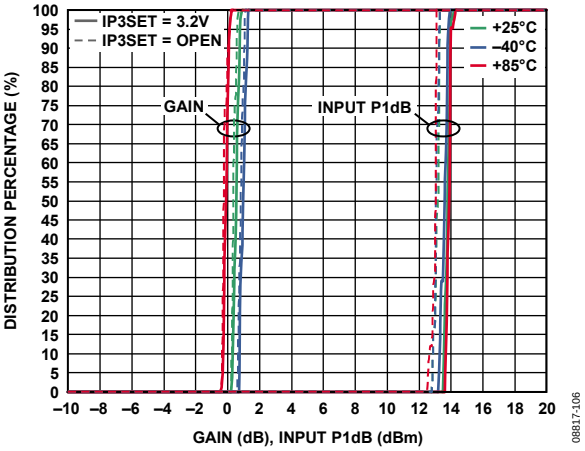


Figure 33. Gain and Input P1dB CCDF

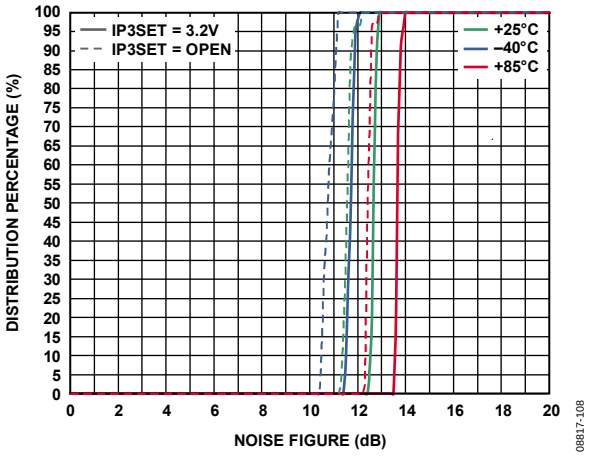


Figure 36. Noise Figure CCDF

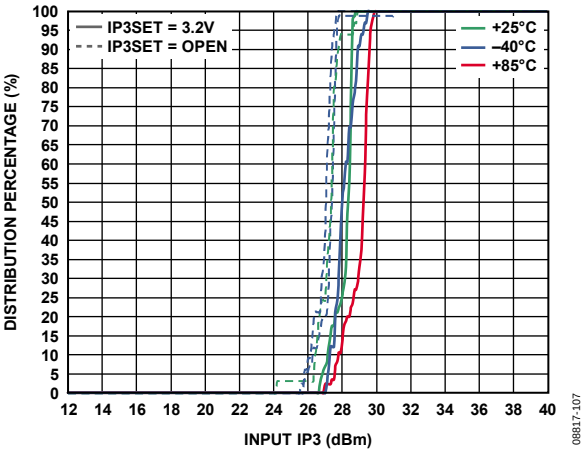


Figure 34. Rx Input IP3 CCDF

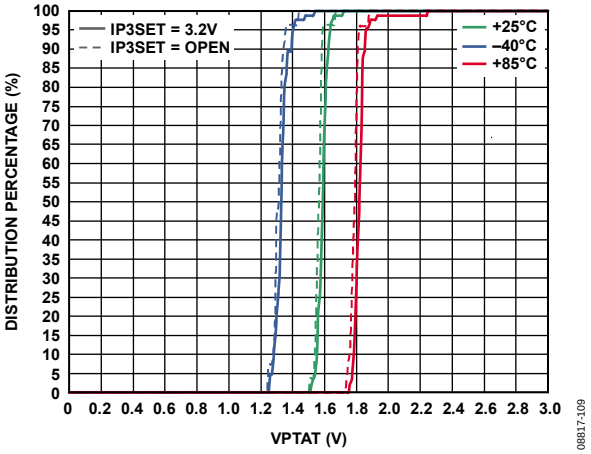


Figure 37. VPTAT MUXOUT Voltage

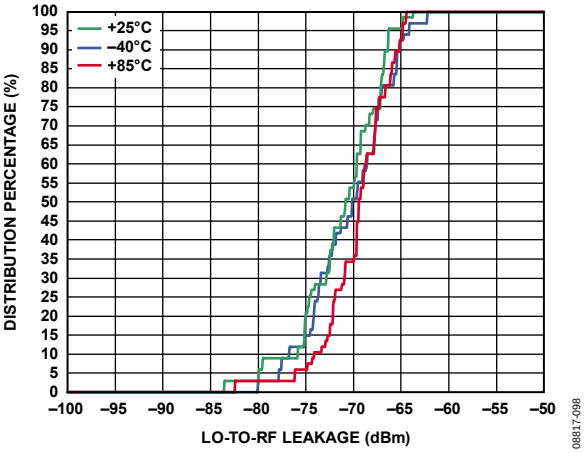


Figure 35. Rx LO-to-RF Leakage CCDF

COMPLIMENTARY CUMULATIVE DISTRIBUTION FUNCTION (CCDF): DOWNCONVERSION, LO = 1700 MHz, RF = 1900 MHz

V_S = 5 V, T_A = 25°C, PFD = 20 MHz, REFIN = 20 MHz, IP3SET = open, as measured using typical downconversion circuit schematic with high-side LO and 200 MHz IF output, unless otherwise noted.

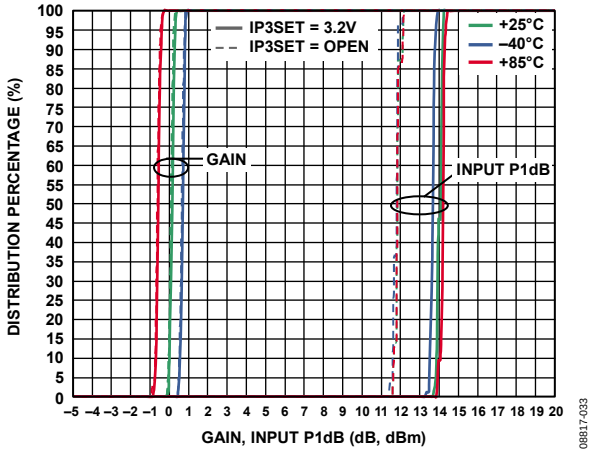


Figure 38. Gain and Input P1dB

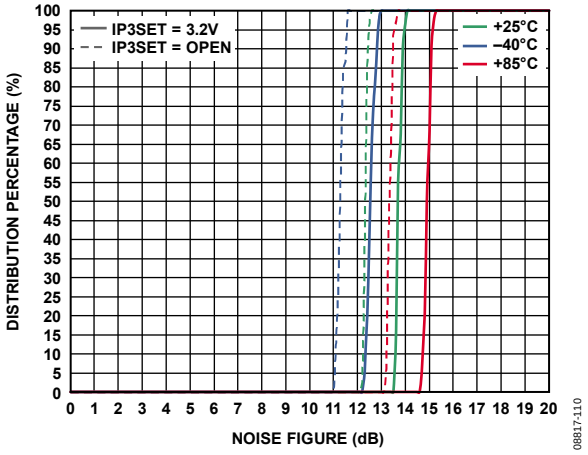


Figure 41. Rx Noise Figure CCDF

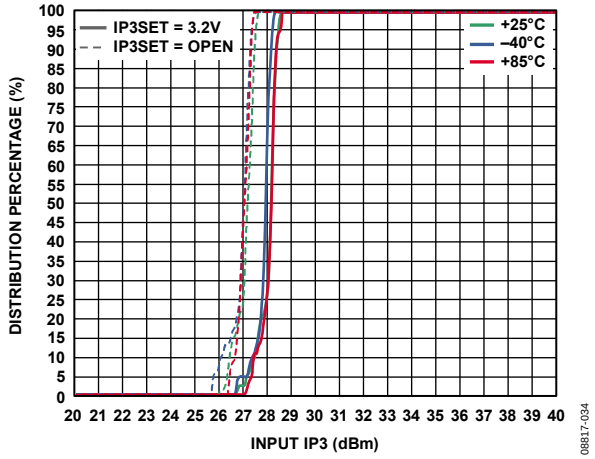


Figure 39. Rx Input IP3

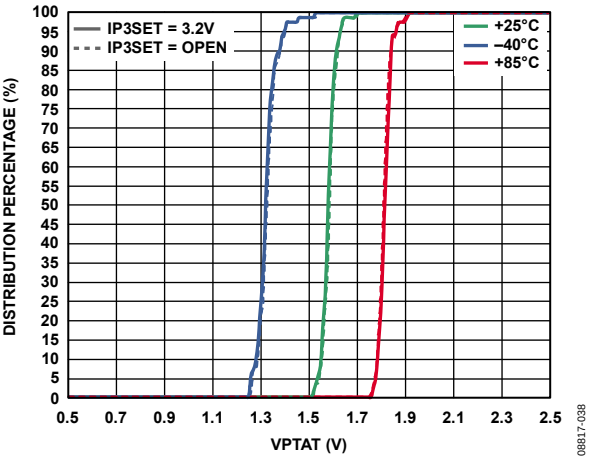


Figure 42. VPTAT MUXOUT Voltage

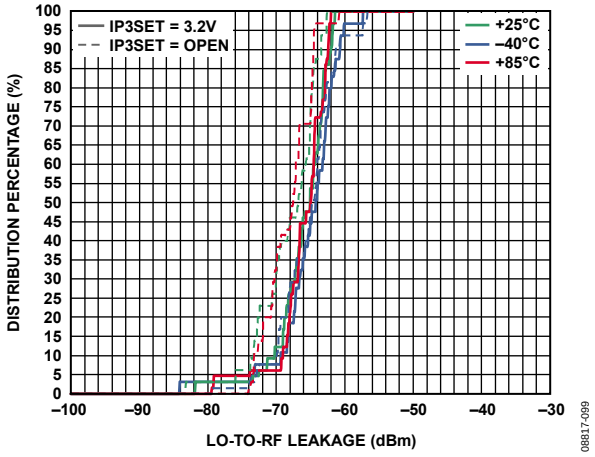


Figure 40. Rx LO-to-RF Leakage

COMPLIMENTARY CUMULATIVE DISTRIBUTION FUNCTION (CCDF): UPCONVERSION DISTRIBUTION

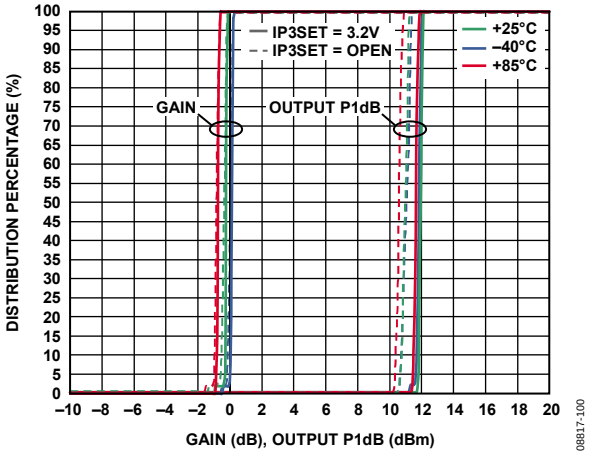


Figure 43. Gain and Output P1dB CCDF, LO = 1220 MHz, RF = 340 MHz

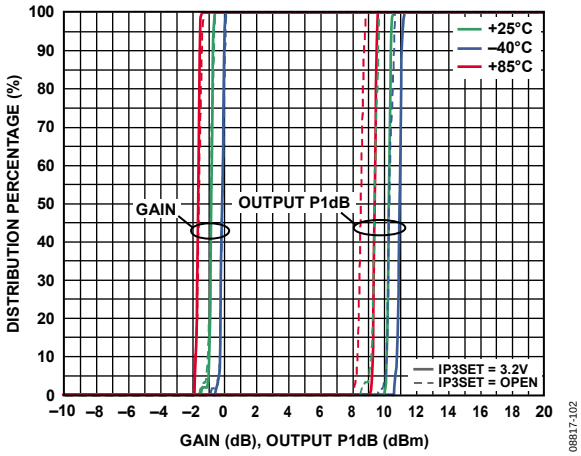


Figure 46. Gain and Output P1dB CCDF, LO = 1840 MHz, RF = 340 MHz

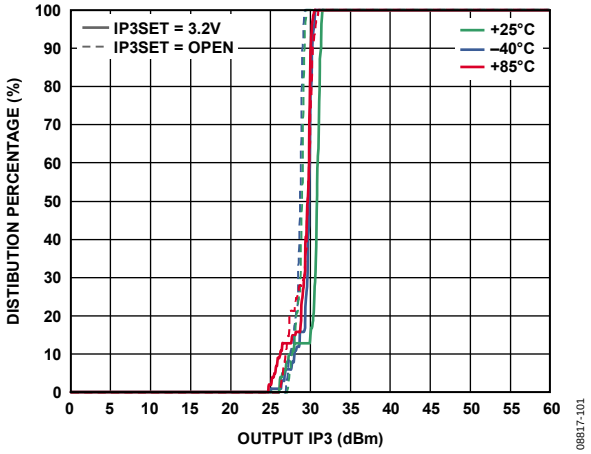


Figure 44. Output IP3 CCDF, LO = 1220 MHz, RF = 340 MHz

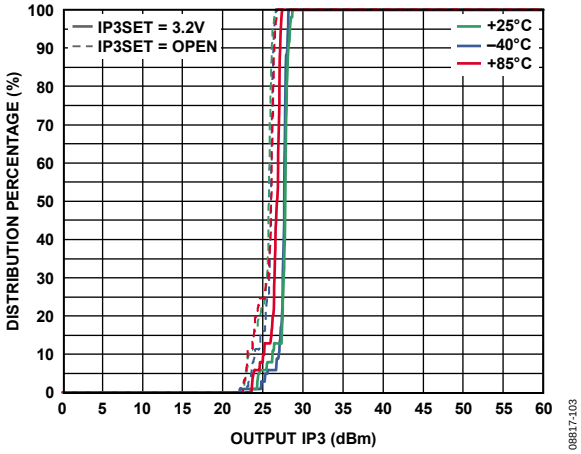


Figure 47. Output IP3 CCDF, LO = 1840 MHz, RF = 340 MHz

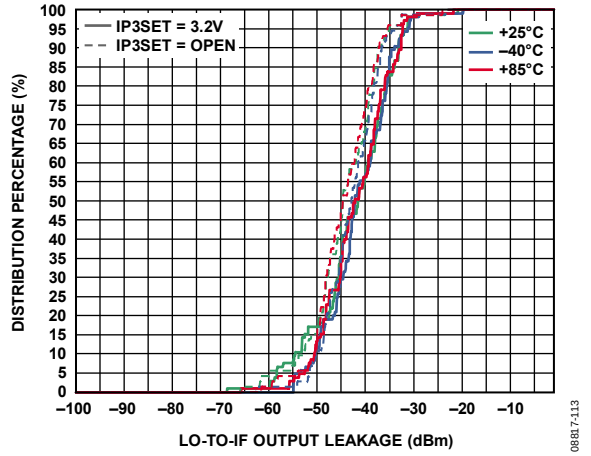


Figure 45. LO-to-IF Output Leakage CCDF, LO = 1220 MHz, RF = 340 MHz

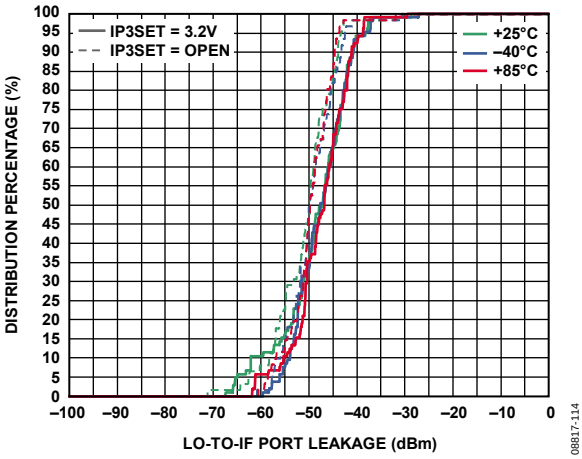


Figure 48. LO-to-IF Output Leakage CCDF, LO = 1840 MHz, RF = 340 MHz

CIRCUIT DESCRIPTION

The ADRF6655 can be subdivided into a PLL and VCO block and a mixer block. A detailed circuit description for each block follows.

PLL AND VCO BLOCK

The PLL and VCO block, shown in Figure 49, is made up of a reference input block, a phase and frequency detector (PFD), a charge pump, a VCO, and a divide-by-N modulus block. An off-chip loop filter completes the loop.

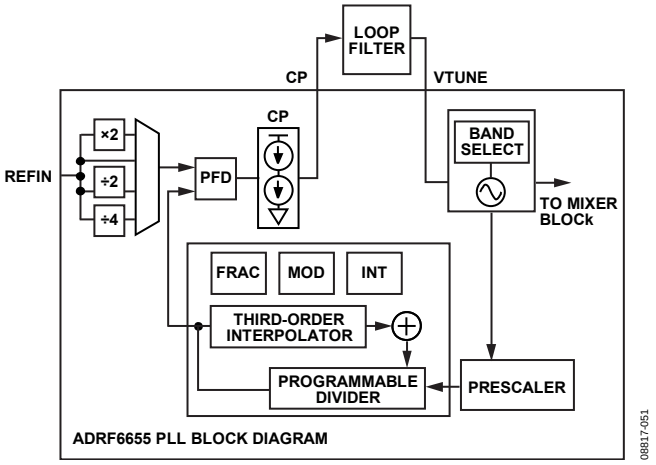


Figure 49. PLL and VCO Block

The VCO is implemented with a single core that consists of 64 overlapping bands, as shown in Figure 50. The correct band is selected automatically by the VCO band calibration circuit when Register R0, Register R1, or Register R2 is programmed. The VCO band selection takes roughly 4000 PFD cycles. During calibration, an internal mux is used to disconnect the VCO input voltage from the VTUNE pin and apply an internal reference voltage for calibration. When calibration is complete, the VCO input voltage is reconnected to the VTUNE pin and normal PLL operation resumes.

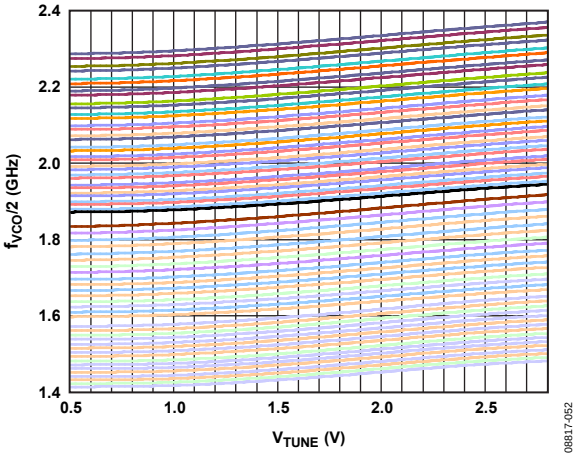


Figure 50. $f_{VCO}/2$ vs. Tuning Voltage for All 64 Bands

The VCO operates at twice the LO frequency for improved isolation. The nominal value of Kv is 75 MHz/V at the VCO output. As the VCO band is changed from 0 to 63, the size of the varactor is also changed, thus maintaining a roughly constant Kv across the entire operating range.

RF MIXER BLOCK

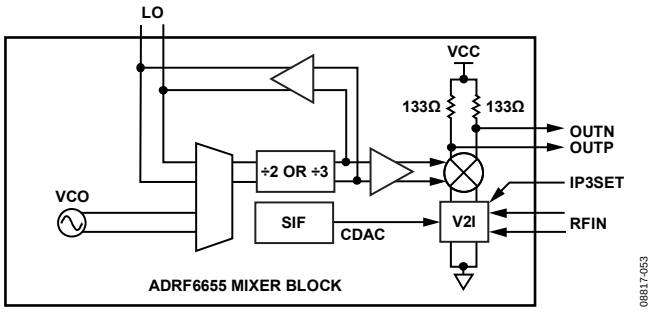


Figure 51. Mixer Block

The mixer portion of the ADRF6655, shown in Figure 51, consists of an LO signal chain, an RF voltage-to-current (V-to-I) converter, and a mixer core. The LO chain receives a signal from either the internal VCO or an external LO source. This LO signal then passes through a frequency divider, which can be set to divide-by-2 or divide-by-3, depending on the desired LO frequency. The differential RF inputs are converted into currents by the V-to-I converter and fed into the mixer core. A pair of 133 Ω pull-up resistors are used to present a ~250 Ω source impedance at the IF output.

LO Signal Chain

The LO chain consists of a mux that selects between the internal VCO and an external LO source. The LO signal can then be divided by 2 or divided by 3, providing a wide range of LO frequencies from 1050 MHz to 2300 MHz. A buffer then drives this divided down signal to the mixer core. The LO signal can also be observed via the LO I/O port when the internal VCO is selected. When the external LO buffer is enabled, the supply current and die temperature increase, resulting in a slight degradation of RF performance. In normal operation mode, the external LO buffer should be disabled to help minimize power consumption and provide optimal RF performance.

V-to-I Converter

The differential RF input signal is applied to a pair of resistively degenerated common-emitter stages, which converts the differential input voltage to output currents. The input stage also provides 50 Ω termination to the RF input port. The linearity of this V-to-I stage can be optimized for a given frequency with Pin IP3SET at the expense of power dissipation and noise figure. An additional way of improving linearity without affecting power dissipation or noise figure is provided by the CDAC signal controlled by serial port interface (SPI).

Mixer Core

The mixer core, based on the Gilbert cell design of four cross-connected transistors, takes the currents from the V-to-I stage and mixes them with the LO signal. This mixer core can be used as a downconvert mixer as is or as an upconvert mixer with an off-chip matching network for a given frequency range.

DIGITAL INTERFACES

The ADRF6655 provides access to the many programmable features available within the IC using a 3-wire SPI control interface. The minimum delays and hold times are presented in the timing diagram in Figure 2. The SPI interface provides digital control of the internal PLL/VCO as well as several other features related to the mixer core, on-chip referencing, and available system monitoring functions. The MUXOUT pin provides access to several output signals that can be selected via the SPI interface. The available outputs are buffered, frequency-scaled versions of the reference, a PLL lock-detect signal, and an internal voltage that is proportional to the IC junction temperature. Details regarding the register settings and initialization sequence are included in the Register Structure section.

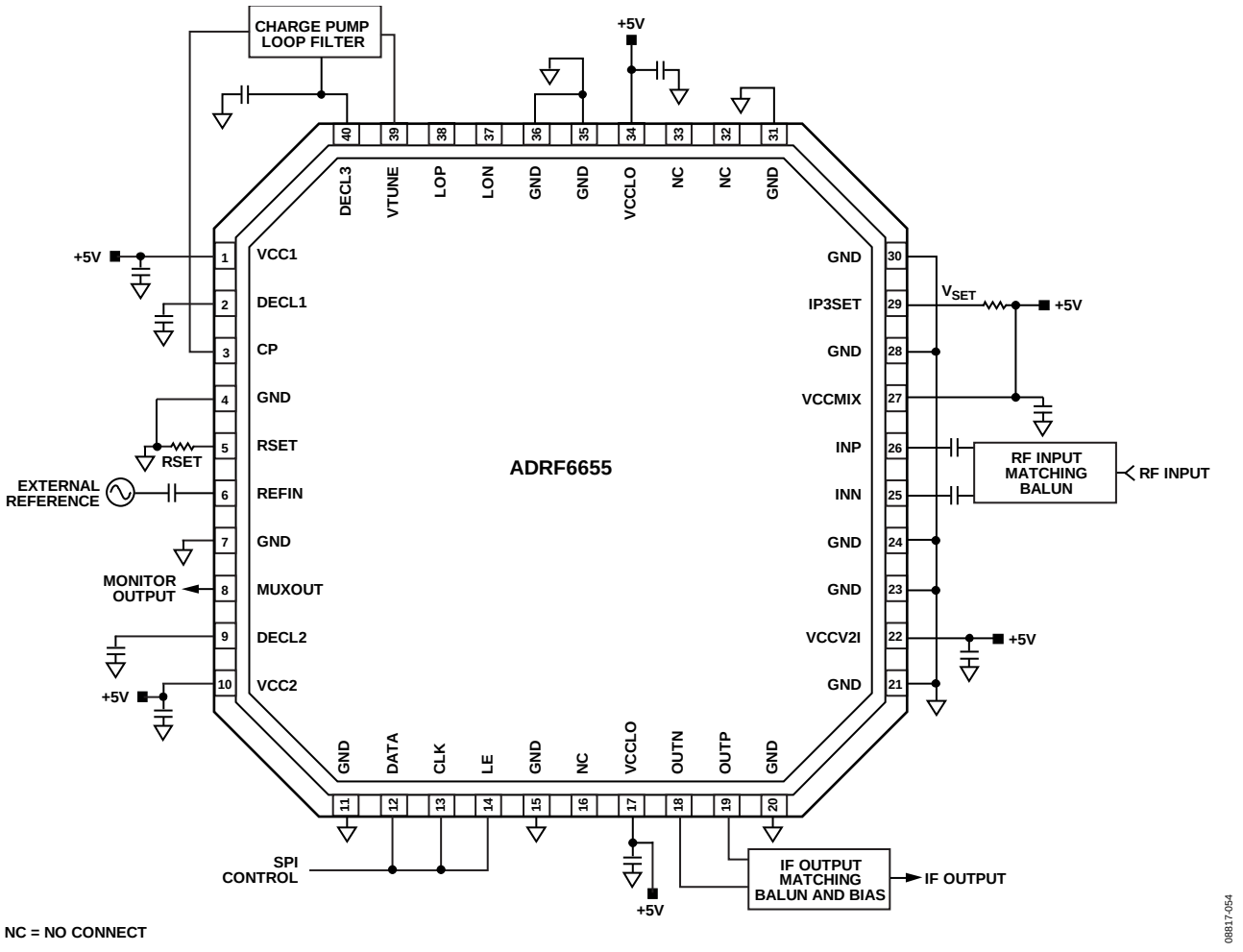


Figure 52. Basic Circuit Connections

ANALOG INTERFACES

The basic circuit connections for a typical ADRF6655 application are presented in Figure 52.

SUPPLY CONNECTIONS

The ADRF6655 has several supply connections and on-board regulated reference voltages that should be bypassed to ground using low inductance bypass capacitors located in close proximity to the supply and reference pins of the ADRF6655. Specifically Pin 1, Pin 2, Pin 9, Pin 10, Pin 17, Pin 22, Pin 27, and Pin 40 should be bypassed to ground using individual bypass capacitors. Pin 9 is the supply used for the on-board VCO, and for best phase noise performance, several bypass capacitors ranging from 100 pF to 10 µF may help to improve phase noise performance. For additional details on bypassing the supply nodes, refer to the evaluation board schematic in Figure 82.

SYNTHESIZER CONNECTIONS

The ADRF6655 includes an on-board VCO and PLL for LO synthesis. An external reference must be applied for the PLL to operate. The external reference should be ac-coupled and provide a ~1 V p-p nominal input level at Pin 6. The reference is compared to an internally divided version of the VCO output frequency to create a charge pump error current to control and lock the VCO. The charge pump output current is filtered and converted to a VTUNE control voltage through the external loop filter. ADIsimPLL™ can be a helpful tool when designing the external charge pump loop filter. The typical Kv of the VCO, the charge pump output current magnitude, and PFD frequency should all be considered when designing the loop filter. The charge pump current magnitude can be set internally or with an external RSET resistor connected to Pin 5 and ground, along with the internal digital settings applied to the PLL (see the Register 4—Charge Pump, PFD, and Reference Path Control section for more details).

OUTPUT MATCHING AND BIASING

The ADRF6655 output stage consists of collector connected output transistors with on-board pull-up resistors. The output transistors and pull-up network presents a 200 Ω differential output impedance in parallel with a small amount of shunt capacitance. The measured RC equivalent impedance of Pin 18 and Pin 19 is ~250 Ω//1.5 pF. This impedance needs to be taken into consideration when designing the external output matching network. In addition to matching the presented output source impedance to the intended load impedance, it is important to provide pull-up choke connections to the supply pins to allow for dc current to directly supply the mixer output transistors. The reactance of the pull-up chokes may need to be considered when designing the output matching network. For convenience, several output matching/bias networks are presented in Figure 53 through Figure 58 for reference.

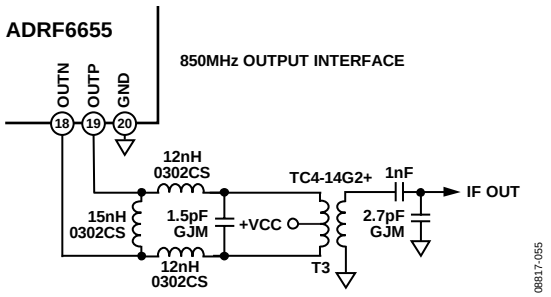


Figure 53. 850 MHz Output Matching Network Using the Center-Tap of the TC4-14T+ Transformer for Biasing the Open Collector Outputs (Output return loss measured to be better than 12 dB from 800 MHz to 925 MHz.)

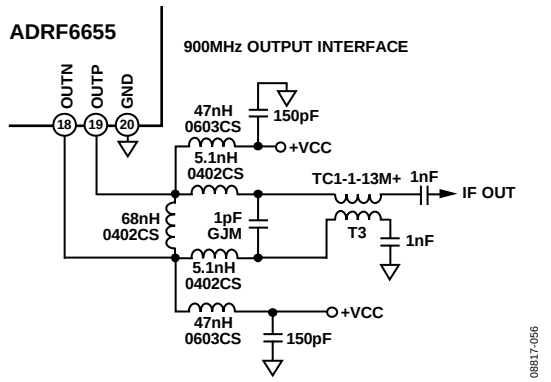


Figure 54. 900 MHz Output Matching Network Using the TC1-1-13M+ 1:1 Impedance Ratio Balun and External Pull-Up Choke Inductors (Output return loss measured to be better than 12 dB from 815 MHz to 1075 MHz.)

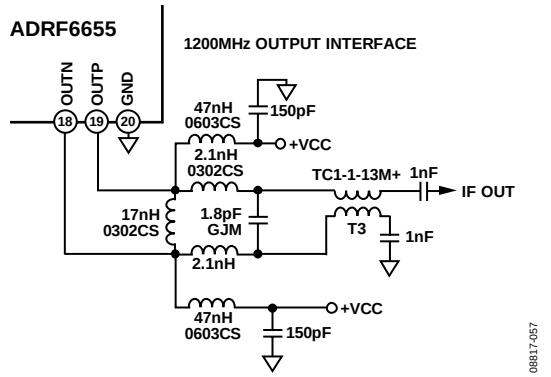


Figure 55. 1200 MHz Output Matching Network (Output return loss measured to be better than 12 dB from 950 MHz to 1500 MHz.)

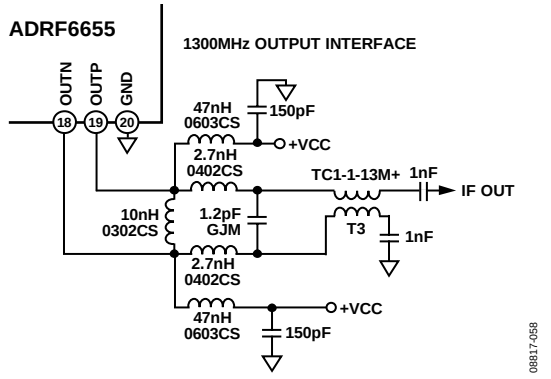


Figure 56. 1300 MHz Output Matching Network (Output return loss measured to be better than 12 dB from 1075 MHz to 1525 MHz.)

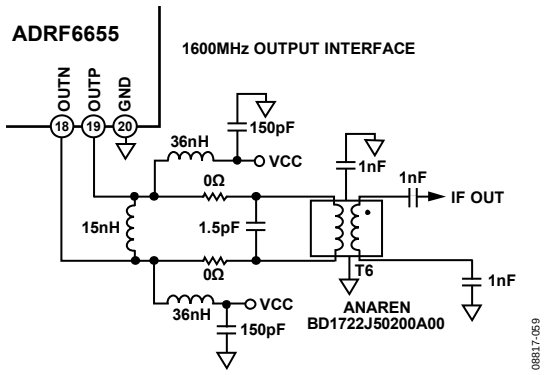


Figure 57. 1600 MHz Output Matching Network (Output return loss measured to be better than 12 dB from 1400 MHz to 1680 MHz.)

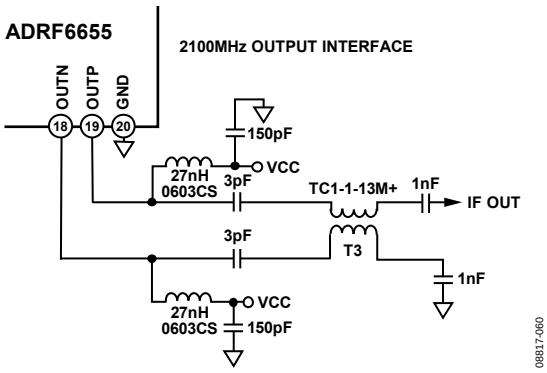


Figure 58. 2100 MHz Output Matching Network (Output return loss measured to be better than 12 dB from 2000 MHz to 2200 MHz.)

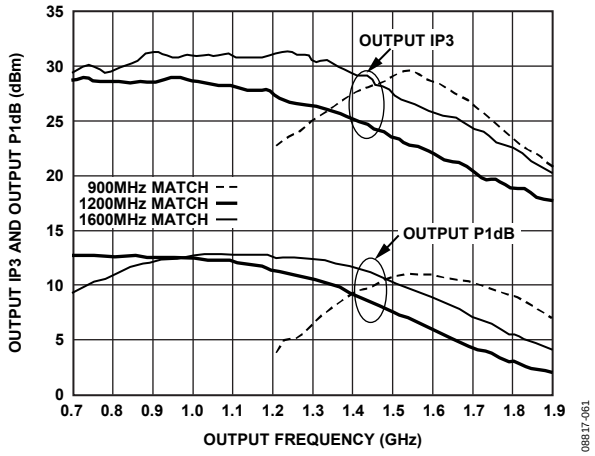


Figure 59. Measured Output Linearity for 900 MHz, 1200 MHz, and 1600 MHz Matching Networks (See Figure 54, Figure 55, and Figure 57 for Implementation)

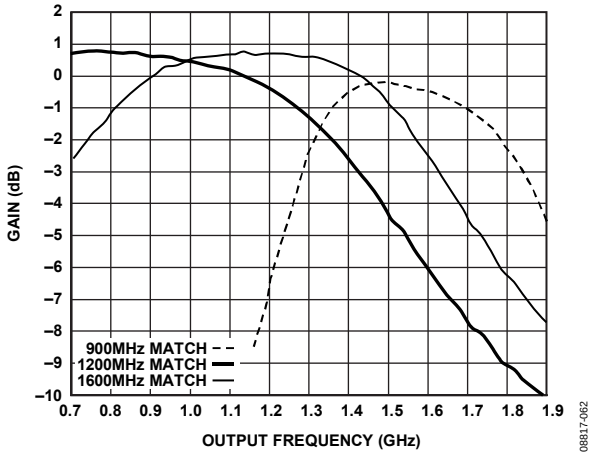


Figure 60. Measured Conversion Gain for 900 MHz, 1200 MHz, and 1600 MHz Matching Networks (See Figure 54, Figure 55, and Figure 57 for Implementation)

INPUT MATCHING

The ADRF6655 uses a balanced 50 Ω input impedance to help simplify external connections. For low loss interfacing, the driving source should be transformed to present a balanced 50 Ω source impedance. An appropriate 1:1 impedance ratio input balun should be used when attempting to interface to an unbalanced 50 Ω source. For input frequencies below ~1.5 GHz, the TC1-1-13M+ from Mini-Circuits or similar baluns should provide good return loss and maximum power gain. For higher frequencies, baluns, such as the TC1-1-43A+, are recommended for lowest insertion loss. The ac coupling capacitors can be optimized with the balun to provide optimum input match. A few examples are provided in Figure 61 for a range of different IF output frequencies.

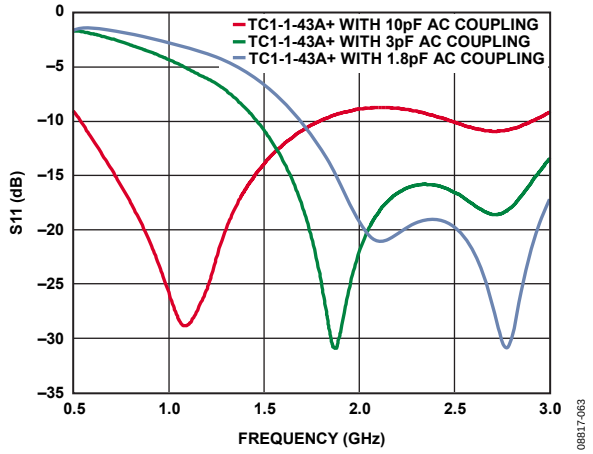


Figure 61. Measured RF Input Return Loss Using the TC1-1-43A+ 1:1 Balun (Plotted for Several AC Coupling Capacitor Values)

It is also possible to use lumped element LC lattice networks to transform an unbalanced source into a balanced source at the mixer input pins. In either case, the mixer input pins should be dc blocked using adequately sized series capacitors.

IP3SET LINEARIZATION FEATURE

The IP3SET pin (Pin 29) controls the overall current consumption of the mixer core depending on the applied voltage. If left open, the voltage on the IP3SET pin is ~2.3 V, and a typical input IP3 of ~25 dBm or higher can be expected across the operating frequency range. As the IP3SET voltage is increased, the overall supply current increases and the input IP3 can be improved from ~3 dB to 6 dB. For upconversion applications, an IP3SET voltage of ~3.2 V to 3.3 V results in very high output IP3 performance in excess of 30 dBm. Using an external resistor divider network connected between VCC and GND, the IP3SET voltage can be derived. Alternatively, the on-board 3.3 V LDO output (Pin 2) can be used to derive the applied IP3SET voltage. However, it is advisable to use good bypassing and a series inductor or ferrite choke to ensure good high frequency isolation between Pin 1 and Pin 29. If an auxiliary control DAC is available, the IP3SET pin can be driven dynamically in applications where power levels are changing over time, and it is desirable to conserve power at lower input signal levels. Figure 62 and Figure 63 illustrate the output linearity dependency on the IP3SET voltage. Note that gain is independent of the IP3SET voltage.

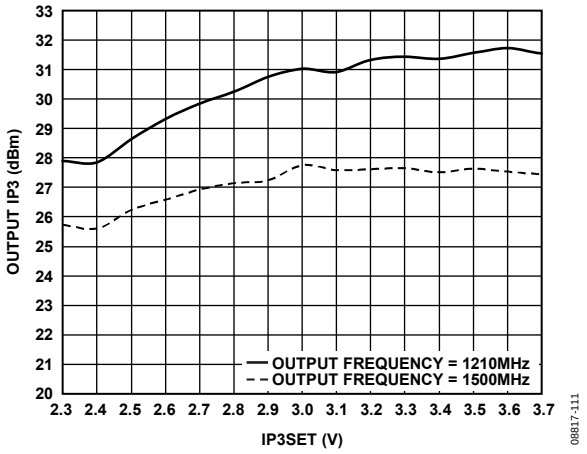


Figure 62. Output IP3 vs. IP3SET Voltage for Output Frequency

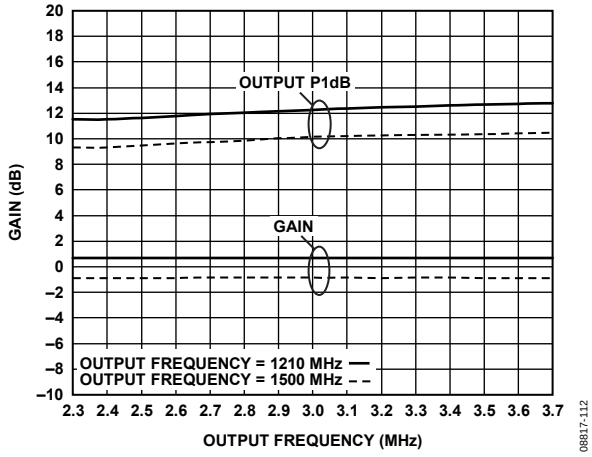


Figure 63. Output P1dB and Gain vs. IP3SET Voltage

CDAC LINEARIZATION FEATURE

In addition to the IP3SET broadband linearization solution, the ADRF6655 also includes a special linearizer designed to provide enhanced IP3 performance at higher input frequencies. At low input frequencies, the CDAC setting offers very little influence on input IP3, and a CDAC setting of 15 is usually recommended. At high input frequencies, the CDAC setting can boost input IP3 as much as 5 dB with essentially no increase in supplied power. At a given input frequency, the ADRF6655 offers an optimum CDAC setting to provide high input IP3 performance. The recommended optimum CDAC setting vs. RF input frequency is shown in Figure 64.

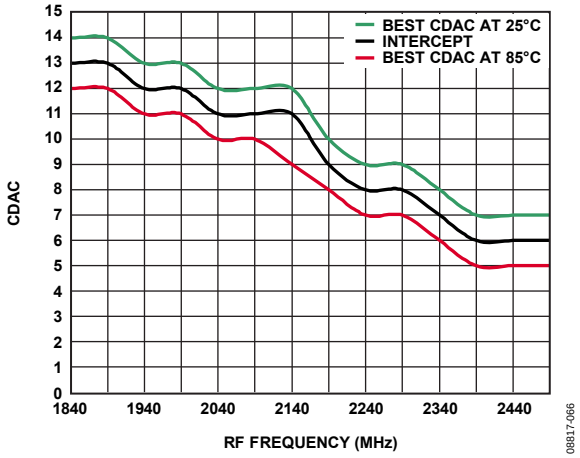


Figure 64. Optimum CDAC Setting for Downconversion vs. RF Input Frequency

EXTERNAL LO INTERFACE

The ADRF6655 provides the option to use an external signal source for the LO into the mixer. It is important to note that the applied LO signal is divided by 2 or divided by 3 prior to the actual mixer core within the ADRF6655. The divider is determined by the register settings in LO path and mixer control register, (see the Register 5—LO Path and Mixer Control section). The LO input pins (Pin 37 and Pin 38) present a broadband balanced 50 Ω input interface similar to the input pins (Pin 25 and Pin 26). The LOP and LON input pins should be dc blocked and driven from a balanced 50 Ω source. When not in use, the LOP and LON pins may be left unconnected.

USING AN EXTERNAL VCO

The ADRF6655 has the necessary provisions for interfacing an external VCO. A high performance discrete VCO may be desirable in applications that call for the very best phase noise performance. The basic circuit connections for interfacing an external VCO are included in Figure 65. It is important to select a VCO with a frequency tuning voltage range that covers the available charge pump output compliance range of 1 V to 2.8 V. The external VCO waveform needs to pass through the on-chip divide-by-2/divide-by-3 programmable dividers before reaching the mixer. As a result, the VCO center frequency should be selected to be roughly 2× or 3× the desired LO signal frequency. The available output power for the selected VCO should be greater than −10 dBm to ensure adequate signal levels into the mixer core. The charge pump loop filter components should be designed to provide adequate phase margin for the given K_{VCO} tuning sensitivity of the selected VCO. It is important to properly configure the digital registers for external VCO operation. When using an external VCO, the internal VCO should be disabled using DB17 in Register 6. Other register programmable LDOs, including the VCO LDO (DB18 in Register 6), should be enabled. For more information on programming the ADRF6655, see the ADRF6655 Control Software section.

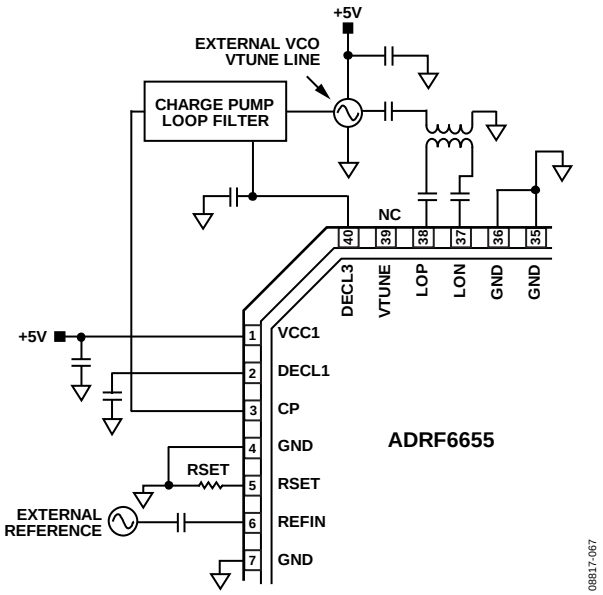


Figure 65. External VCO Connections

ADRF6655 CONTROL SOFTWARE

The ADRF6655 can be controlled from PCs that include a USB port. The basic user interfaces are shown in Figure 66 and Figure 67.

After launching the software, the user is prompted to select a device from the ADRF product family. Upon selecting the ADRF6655, the main control interface appears as shown in Figure 66. The main control interface allows the user to configure the device for various modes of operation. The internal synthesizer is controlled by clicking on any of the numeric values listed in the **RF Section**. Attempting to program the **Ref Input Frequency**, the **PFD Frequency**, the **VCO Frequency(2xLO)**, or other values in the **RF Section** launches the control module shown in Figure 67. From the synthesizer settings control interface, the user can enter the desired **Local Oscillator Frequency (MHz)**, **Channel Step Size (kHz)**, and **External Reference Frequency (MHz)**. The user can also enable the LO output buffer and divider options from this menu. After setting the desired values, it is important to click **Upload all registers** for the new settings to take effect.



Figure 66. ADRF6655 Software Control Interface

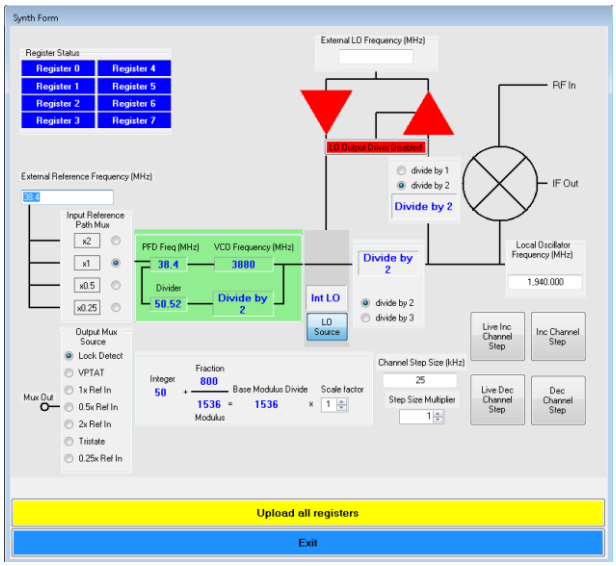


Figure 67. ADRF6655 Synthesizer Settings User Interface

PLL LOOP FILTER DESIGN

Designing the external loop filter, which connects between the charge pump output and VCO tuning control pin, is easy with the help of ADIsimPLL. ADIsimPLL is a free software application available from Analog Devices for designing PLL loop filters. Several passive filter topologies are support in ADIsimPLL along with the necessary component placements on the evaluation board.

When designing a PLL loop filter, it is important to consider settling time and phase noise requirements. Figure 68 provides measured phase noise performance for a typical fast and slow loop filter design. Note that the wider loop filter offers better close-in phase noise but degraded phase noise at greater offset frequencies. The narrow 1.5 kHz loop filter design provides the best phase noise at 100 kHz and 1 MHz carrier offsets but with the penalty of decreased frequency settling time and poorer close-in performance.

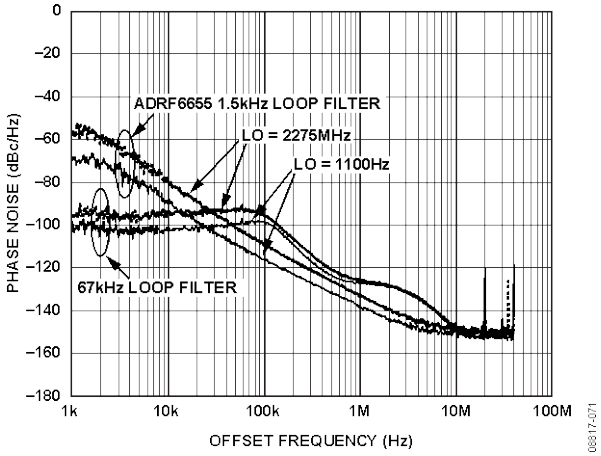


Figure 68. Phase Noise with Different Loop Filters

REGISTER STRUCTURE

INTEGER DIVIDE CONTROL REGISTER (R0)

RESERVED													DIVIDE MODE	INTEGER DIVIDE RATIO							CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

MODULUS DIVIDE CONTROL REGISTER (R1)

RESERVED										MODULUS DIVIDE VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

FRACTIONAL DIVIDE CONTROL REGISTER (R2)

RESERVED										FRACTIONAL DIVIDE VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	C3(0)	C2(1)	C1(0)

Σ-Δ MODULATOR DITHER CONTROL REGISTER (R3)

	DITHER MAGNITUDE	DITHER ENABLE	DITHER RESTART VALUE																	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

CHARGE PUMP, PFD, AND REFERENCE PATH CONTROL REGISTER (R4)

OUPUT MUX SOURCE			INPUT REF PATH SOURCE		CP REF	PDF PHASE OFFSET POLARITY	PFD PHASE OFFSET MULTIPLIER VALUE					CP CURRENT MULTIPLIER		CP CNTL SRC	CHARGE PUMP CONTROL		PFD EDGE SENSITIVITY		PFD ANTI-BACKLASH DELAY		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RMS2	RMS1	RMS0	RS1	RS0	CPM	CPBD	CPB4	CPB3	CPB2	CPB1	CPB0	CPP1	CPP0	CPS	CPC1	CPC0	PE1	PE0	PAB1	PAB0	C3(1)	C2(0)	C1(0)

LO PATH AND MIXER CONTROL REGISTER (R5)

RESERVED												CDAC DISTORTION COMPENSATION SETTING				MIXER BIAS ENABLE	PLL ENABLE	LO DIV 2/3	LO IN/OUT CNTRL	LO OUTPUT DRIVER ENABLE	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	CDAC3	CDAC2	CDAC1	CDAC0	MBE	PLEN	LDIV	LXL	LDRV	C3(1)	C2(0)	C1(1)

VCO CONTROL AND PLL ENABLES REGISTER (R6)

RESERVED			CHARGE PUMP ENABLE	LDO 3.3V ENABLE	VCO LDO ENABLE	VCO ENABLE	VCO SWITCH CONTROL	VCO AMPLITUDE SETTING						VCO BS SRC	VCO BAND SELECT						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CPEN	L3EN	LVEN	VCOEN	VCOSW	VC5	VC4	VC3	VC2	VC1	VC0	VBSRC	VBS5	VBS4	VBS3	VBS2	VBS1	VBS0	C3(1)	C2(1)	C1(0)

EXTERNAL VCO CONTROL REGISTER (R7)

RES	EXTERNAL VCO ENABLE	RESERVED																			CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	XVCO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(1)	C1(1)

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Figure 69. Register Maps for ADRF6655 (The three control bits determine which register is programmed.)

DEVICE PROGRAMMING

The device is programmed through a 3-pin SPI port. The timing requirements for the SPI port are described in Figure 2. There are eight programmable registers, each with 24 bits, controlling the operation of the device. The register functions can be broken down as follows:

- Register 0—integer divide control
- Register 1—modulus divide control
- Register 2—fractional divide control
- Register 3—Σ-Δ modulator dither control
- Register 4—charge pump, PFD, and reference path control
- Register 5—LO path and mixer control
- Register 6—VCO controls and PLL enables
- Register 7—external VCO control

Note that the PLL has internal calibration that must run whenever the device is programmed with a given frequency. This calibration is automatically run whenever Register 0, Register 1, or Register 2 is programmed. Software is available from Analog Devices that allows easy programming from an external PC. See the ADRF6655 Control Software section for additional details.

INITIALIZATION SEQUENCE

To ensure proper power-up of the ADRF6655, it is important to reset the PLL circuitry after the supply rail (VCC1, VCC2, VCCLO, VCCV2I, and VCCMIX) has settled to 5 V ± 0.25 V. Resetting the PLL ensures that the internal bias cells are properly configured even under poor supply start-up conditions. To ensure that the PLL is reset after power-up, the PLEN data bit (DB6) in Register 5 should be programmed to disable the PLL (PLEN = 0). After a delay of >100 ms, Register 5 should be programmed to enable the PLL (PLEN = 1). After this procedure, the registers should be programmed as follows:

1. Register 7
2. Register 6
3. Register 4
4. Register 3
5. Register 2
6. Register 1
7. Delay >1 ms
8. Register 0

When programming the frequency of the ADRF6655, normally only Register 2, Register 1, and Register 0 are programmed. When programming these registers, a short delay of >500 µs should be placed before programming the last register in the sequence (Register 0). This ensures that the VCO band calibration initiated by the first two register writes has sufficient time to complete before the final band calibration (for Register 0) is initiated.

REGISTER 0—INTEGER DIVIDE CONTROL

With R0[2:0] set to 000, the on-chip integer divide control register is programmed as shown in Figure 70.

Integer Divide Ratio

The integer divide ratio is used to set the INT value in Equation 1. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. The VCO frequency (F_{VCO}) equation is

$$f_{VCO} = 2 \times f_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where:
f_{VCO} is the output frequency of the internal VCO.
f_{PFD} is the frequency of operation of the phase-frequency detector.
INT is the preset integer divide ratio value (24 to 119 in fractional mode).
MOD is the preset fractional modulus (1 to 2047).
FRAC is the preset fractional divider ratio value (0 to MOD − 1).

Divide Mode

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the RF VCO output frequency (f_{VCO}) is calculated by

$$f_{VCO} = 2 \times f_{PFD} \times (INT) \quad (2)$$

where *INT* is the integer divide ratio value (21 to 123 in integer mode).

RESERVED													DIVIDE MODE	INTEGER DIVIDE RATIO							CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

DM	DIVIDE MODE
0	FRACTIONAL
1	INTEGER

ID6	ID5	ID4	ID3	ID2	ID1	ID0	INTEGER DIVIDE RATIO
0	0	1	0	1	0	1	21 (INTEGER MODE ONLY)
0	0	1	0	1	1	0	22 (INTEGER MODE ONLY)
0	0	1	0	1	1	1	23 (INTEGER MODE ONLY)
0	0	1	1	0	0	0	24
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
0	1	1	1	0	0	0	56
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
1	1	1	0	1	1	1	119
1	1	1	1	0	0	0	120 (INTEGER MODE ONLY)
1	1	1	1	0	0	1	121 (INTEGER MODE ONLY)
1	1	1	1	0	1	0	122 (INTEGER MODE ONLY)
1	1	1	1	0	1	1	123 (INTEGER MODE ONLY)

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Figure 70. Integer Divide Control Register (R0)

REGISTER 1—MODULUS DIVIDE CONTROL

With R1[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in Figure 71.

The MOD value is the preset fractional modulus ranging from 1 to 2047.

RESERVED										MODULUS DIVIDE RATIO											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	MODULUS VALUE
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
0	0	0	0	1	1	0	0	0	0	0	1536
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	2047

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Figure 71. Modulus Divide Control Register (R1)

REGISTER 2—FRACTIONAL DIVIDE CONTROL

With R2[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in Figure 72.

The FRAC value is the preset fractional modulus ranging from 0 to MOD − 1.

RESERVED										FRACTIONAL DIVIDE VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	FRACTIONAL VALUE
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
0	1	1	0	0	0	0	0	0	0	0	768
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
FRACTIONAL VALUE MUST BE LESS THAN MODULUS											<MDR

08817-074

Figure 72. Fractional Divide Control Register (R2)

REGISTER 3—Σ-Δ MODULATOR DITHER CONTROL

With R3[2:0] set to 011, the on-chip, Σ-Δ modulator, dither control register is programmed as shown in Figure 73.

The dither restart value can be programmed from 0 to $2^{17} - 1$, though a value of 1 is typically recommended.

	DITHER MAGNITUDE		DITHER ENABLE	DITHER RESTART VALUE																CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DITH1	DITH0	DITHER MAGNITUDE
0	0	15
0	1	7
1	0	3
1	1	1 (RECOMMENDED)

DEN	DITHER ENABLE
0	DISABLE (RECOMMENDED)
1	ENABLE

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	DITHER RESTART VALUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

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Figure 73. Σ-Δ Modulator Dither Control Register (R3)

REGISTER 4—CHARGE PUMP, PFD, AND REFERENCE PATH CONTROL

With R4[2:0] set to 100, the on-chip charge pump, PFD, and reference path control register is programmed as shown in Figure 74.

The charge pump current is controlled by the base charge pump current ($I_{CP, BASE}$) and the value of the charge pump current multiplier ($I_{CP, MULT}$).

The base charge pump current can be set using an internal or external resistor (according to DB18 of Register 4). When using an external resistor, the value of $I_{CP, BASE}$ can be varied according to

$$RSET[\Omega] = \left[\frac{217.4 \times I_{CP, BASE}}{250}\right] - 37.8 \quad (3)$$

When using the internal resistor, the base charge pump current is 250 μA. The actual charge pump current can be programmed to be a multiple (1, 2, 3, or 4) of the charge pump base current. The multiplying value ($I_{CP, MULT}$) is equal to 1 plus the value of Bit DB11 and Bit DB10 in Register 4.

The PFD phase offset multiplier ($\theta_{PFD, OFS}$), which is set by Bit DB16 to Bit DB12 of Register 4, causes the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-to-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by

$$|\Delta\Phi|[\text{deg}] = 22.5\frac{\theta_{PFD, OFS}}{I_{CP, MULT}}$$

Finally, the phase offset can be either positive or negative depending on the value of DB17 in Register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2×, 1×, 0.5×, or 0.25×. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The ADRF6655 also provides a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode is to provide a lock-detect output to allow the user to verify when the PLL has locked to the target frequency. In addition, several other internal signals may be passed to the MUXOUT pin, as described in Figure 74.

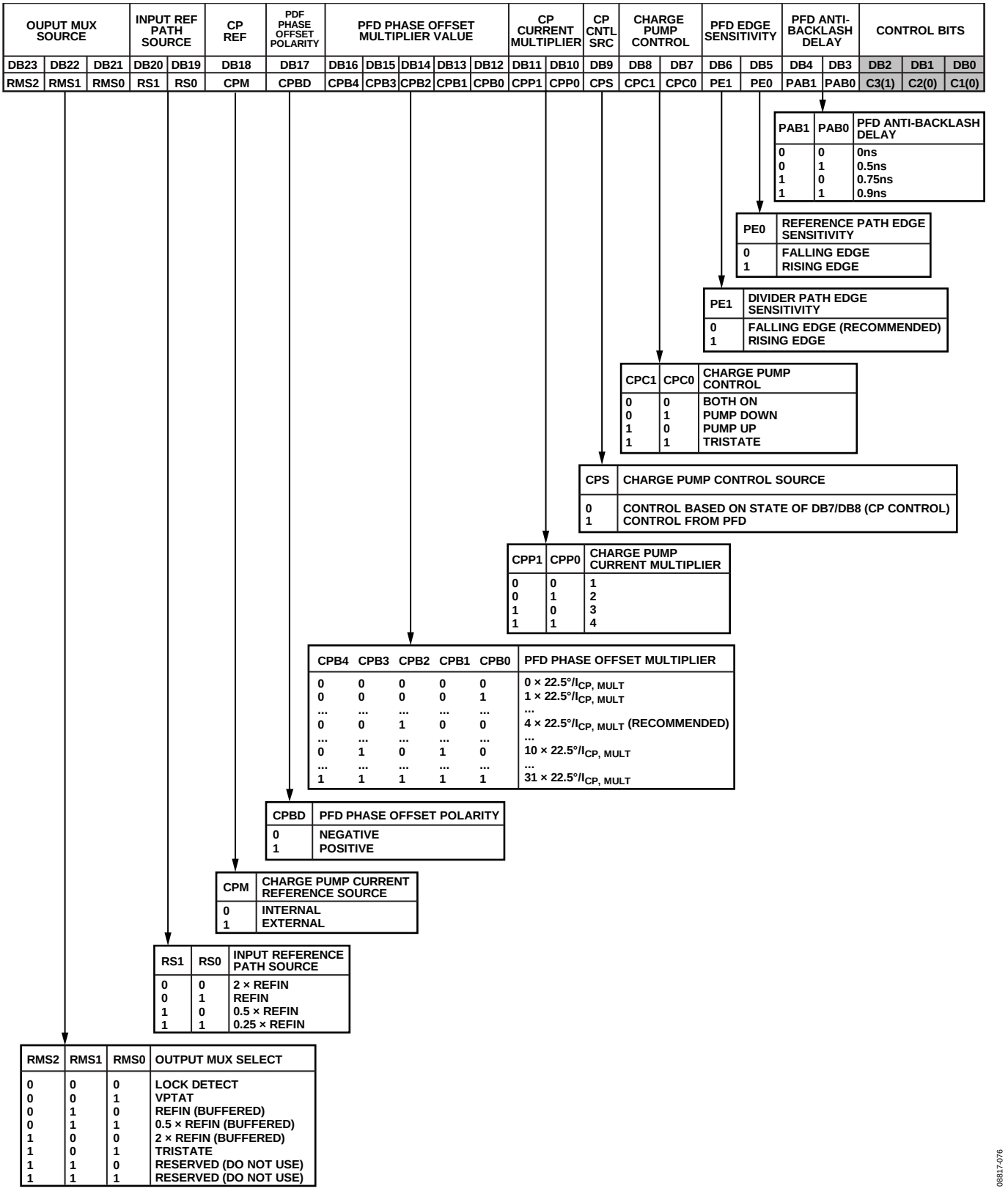


Figure 74. Charge Pump, PFD, and Reference Path Control Register (R4)

REGISTER 5—LO PATH AND MIXER CONTROL

With R5[2:0] set to 101, the LO path and mixer control register is programmed as shown in Figure 75.

The LO output driver can be enabled to allow the user to review the performance of the internally applied LO through the LOP and LON local oscillator input/output pins. The LO input/output control allows the user to disconnect the internal LO signal and apply an external LO signal to the LOP and LON local oscillator input/output pins. A divide-by-2 or divide-by-3 prescaler can be selected to divide the frequency of the externally or internally applied oscillator signal before the mixer.

When using an external frequency, stable local oscillator signal to commutate the mixer core, it is possible to shut down the PLL circuitry through the PLL enable address (DB6) of Register 5.

The internal mixer can be disabled using the mixer bias enable address (DB7) of Register 5.

Register 5 also provides access to the CDAC Distortion Compensation Setting (DB11:DB8). CDAC control can allow the user to optimize the internal linearization circuitry to enhance IP3 performance for high frequency RF input signals.

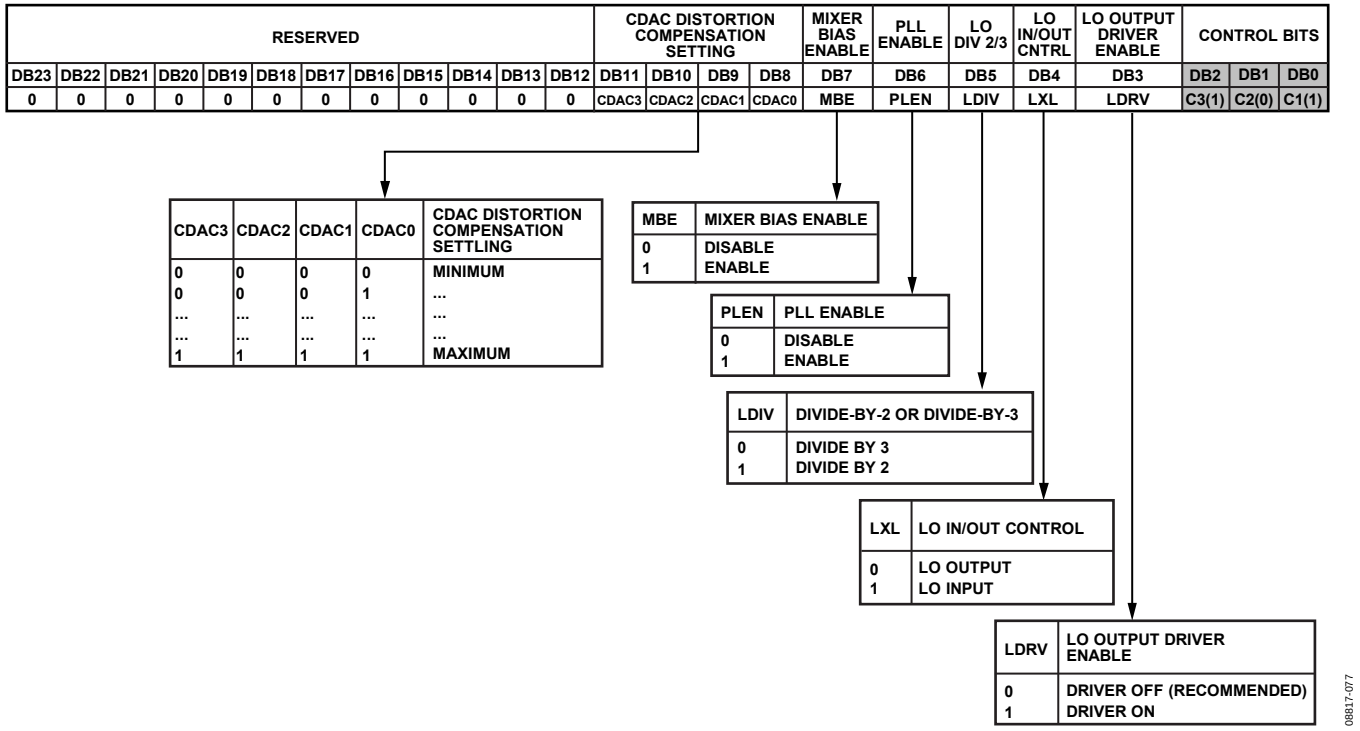


Figure 75. LO Path and Mixer Control Register (R5)

REGISTER 6—VCO CONTROL AND PLL ENABLES

With R6[2:0] set to 110, the VCO control and PLL enables register is programmed as shown in Figure 76.

The VCO tuning band is normally selected automatically by the band calibration algorithm, although the user can directly select the VCO band using Register 6.

The VCO BS SRC bit (DB9) determines whether the result of the calibration algorithm is used to select the VCO band, or if the band selected is based on the value in VCO band select (DB8 to DB3).

The VCO amplitude can be controlled through Register 6. The VCO amplitude setting can be controlled between 0 and 63.

The internal VCO can be disabled using Register 6. The internal VCO LDO can be disabled if an external clean 2.9 V supply is available to be applied to Pin 40. Additionally, the 3.3 V on-board LDO can be disabled through Register 6 and an external 3.3 V supply can be applied to Pin 2.

The internal charge pump can be disabled through Register 6. Normally, the charge pump is enabled.

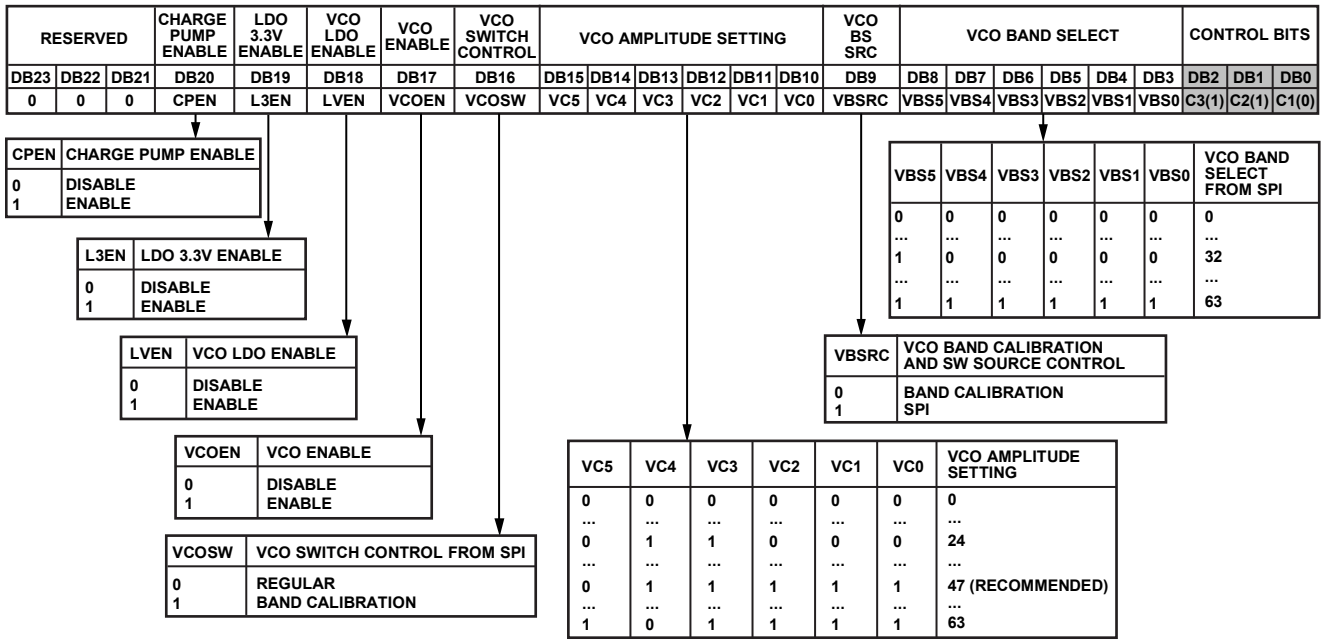


Figure 76. VCO Control and Enables Register (R6)

REGISTER 7—EXTERNAL VCO CONTROL

With R6[2:0] set to 111, the external VCO control register is programmed as shown in Figure 77.

The external VCO enable bit allows the use of an external VCO in the PLL instead of the internal VCO. This can be advantageous in cases where the internal VCO is not capable of providing the desired frequency, or where the internal phase noise of the VCO is higher than desired. By setting the external VCO enable bit (DB22) to 1, and setting Bit DB15 to Bit DB10 of Register 6 to 0, the internal VCO is disabled and the output of an external VCO can be fed into the part differentially on Pin 38 and Pin 37 (LOP and LON). Because the loop filter is already external, the output of the loop filter simply needs to be connected to the external, tuning voltage pin of the VCO. See the Using an External VCO section for more information.

RES	EXTERNAL VCO ENABLE	RESERVED																		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	XVCO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(1)	C1(1)

XVCO	EXTERNAL VCO ENABLE
0	INTERNAL VCO
1	EXTERNAL VCO

08817-079

Figure 77. External VCO Control Register (R7)

CHARACTERIZATION SETUPS

Figure 78 to Figure 80 show the general characterization bench setups used extensively for the ADRF6655. The setup shown in Figure 78 was used to do the bulk of the testing. An automated Agilent VEE program was used to control the equipment over the IEEE bus. This setup was used to measure gain, IP1dB, OP1dB, IIP2, IIP3, OIP2, OIP3, LO-to-IF and LO-to-RF leakage, LO amplitude, and supply current. The ADRF6655 was characterized on an upconversion and downconversion evaluation board configured for each conversion as described in the Input Matching section and the Output Matching and Biasing section. For all measurements of the ADRF6655, the loss of the RF input balun was de-embedded.

To do phase noise and reference spurs measurements, see the phase noise setup used in Figure 79. Phase noise measurements were done on a downconversion board looking at the output at different offsets.

Figure 80 shows the setup used to make the noise figure measurements with no blocker present, and Figure 81 shows the setup for making the noise figure measurements under blocking conditions. Note that attention must be given to the measurement setup. The RF blocker signal must be filtered through a band-pass filter to prevent noise (which increases when output power is increased) from contributing at the desired RF frequency. At least 30 dB attenuation is needed at the desired RF and image frequencies. For example, to generate a blocker signal at the IF output of 205 MHz, the blocker signal generator is set at 995 MHz, and the part is programmed to generate a LO frequency of 1200 MHz that results in an output signal of 205 MHz. This signal must be filtered out through a band reject filter on the output so that the noise figure can be measured at 200 MHz, which corresponds to the output frequency for LO = 1200 MHz and RF input = 1000 MHz.

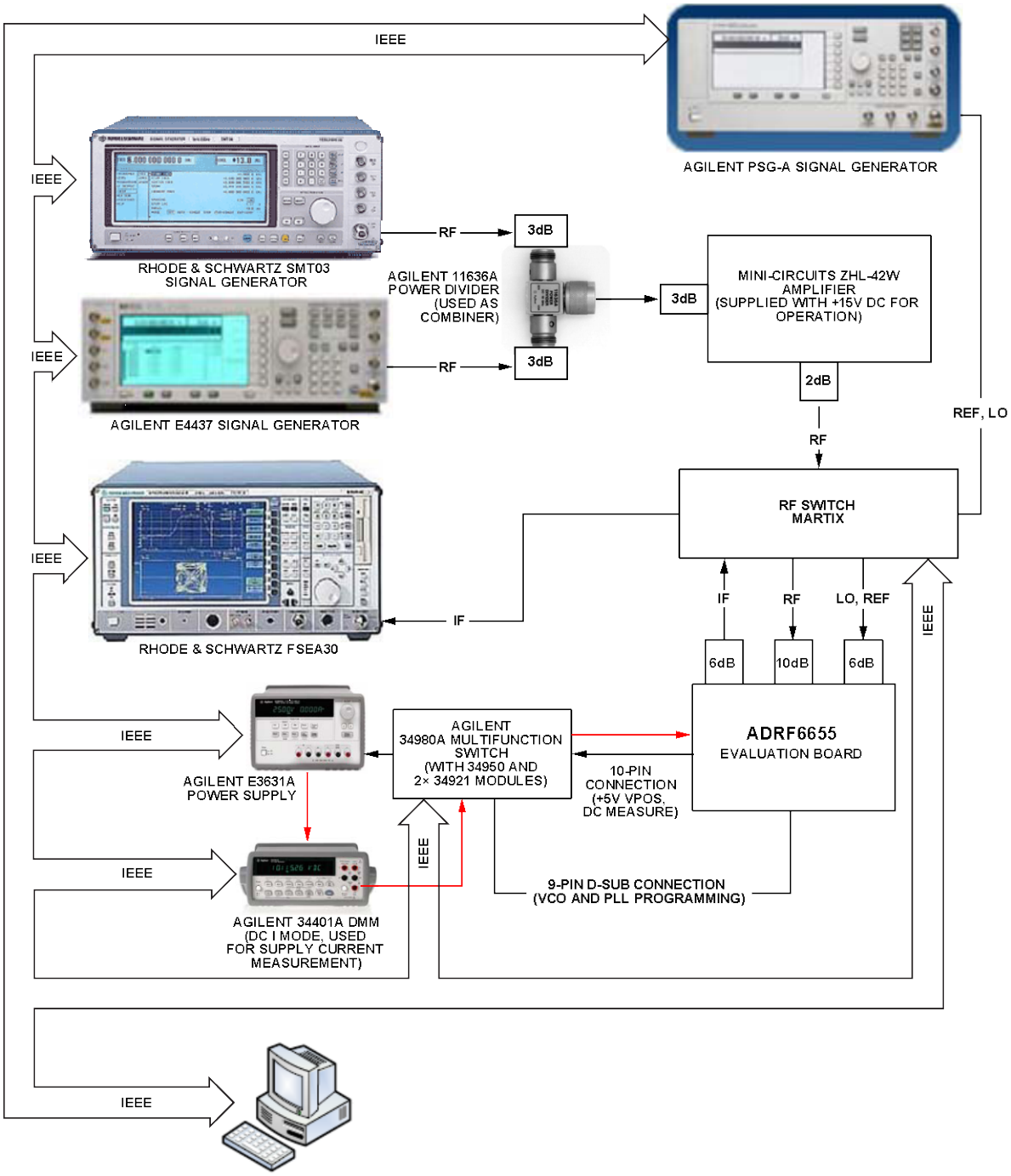


Figure 78. General Characterization Setup

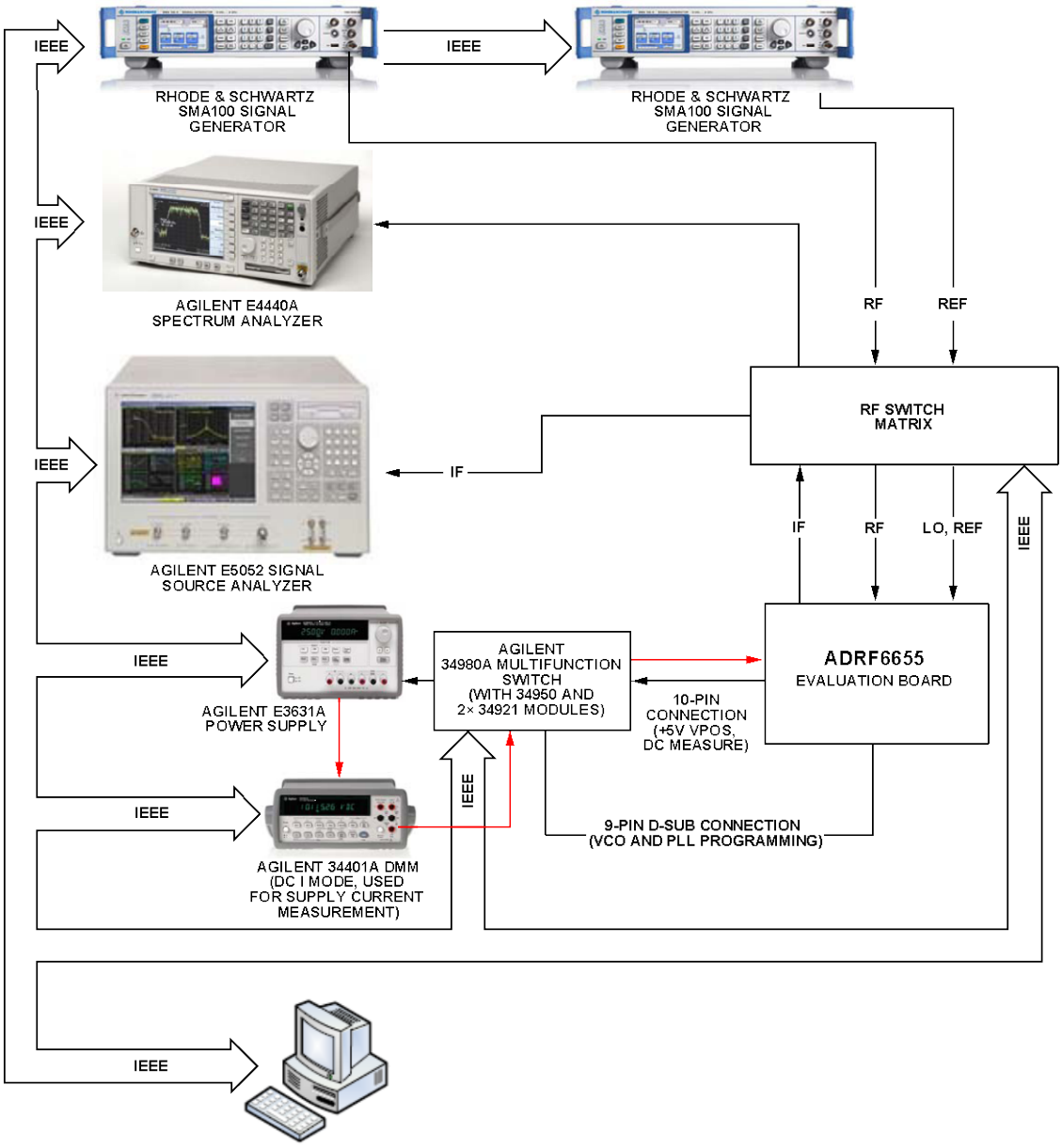


Figure 79. Phase Noise Setup

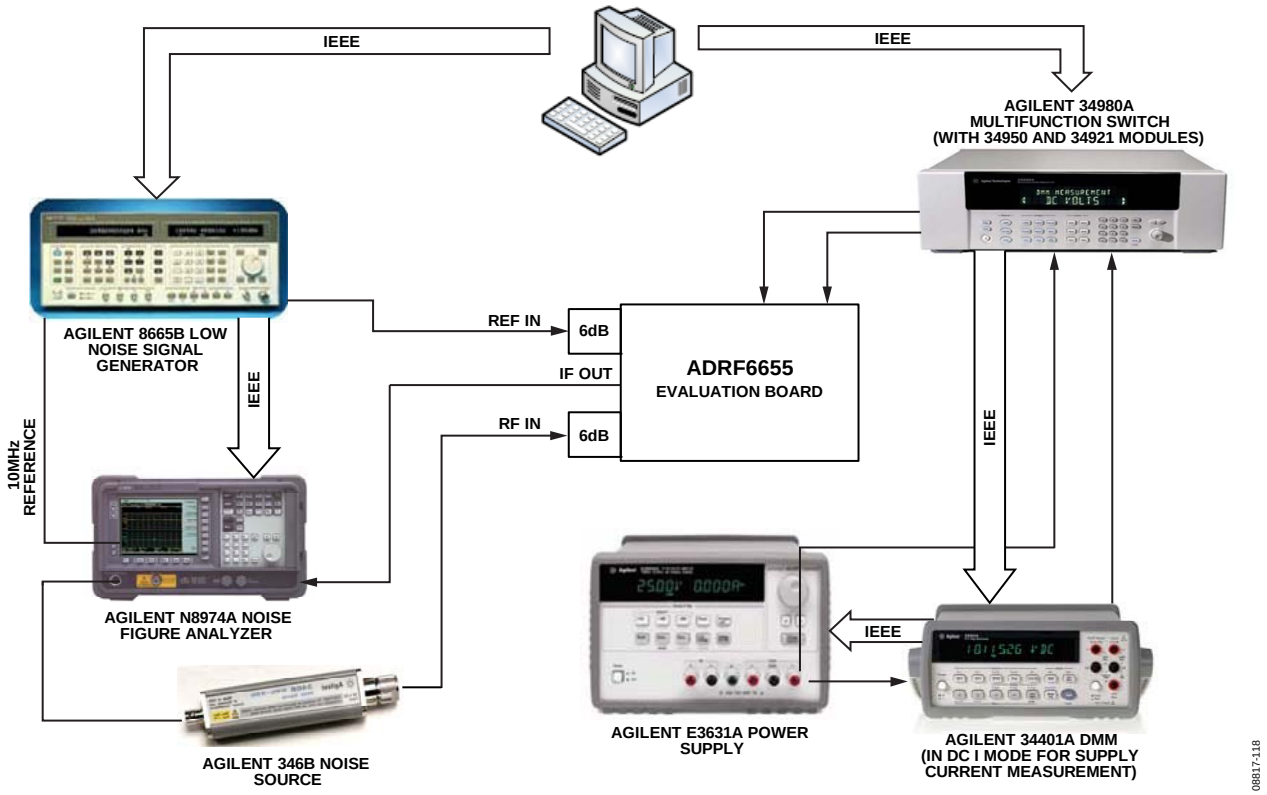


Figure 80. Noise Figure Setup

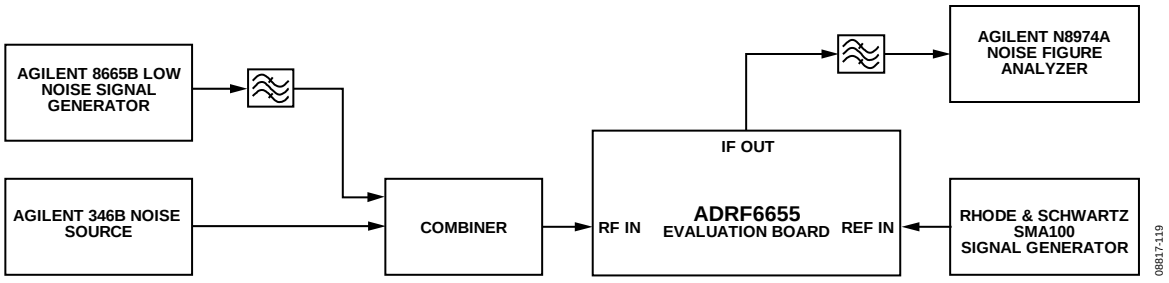


Figure 81. Noise Figure with Presence of Blocker Signal

EVALUATION BOARD LAYOUT AND THERMAL GROUNDING

An evaluation board is available for testing the ADRF6655. The standard evaluation is configured for downconversion applications. Table 5 provides the component values and suggestions for modifying component values for various modes of operation.

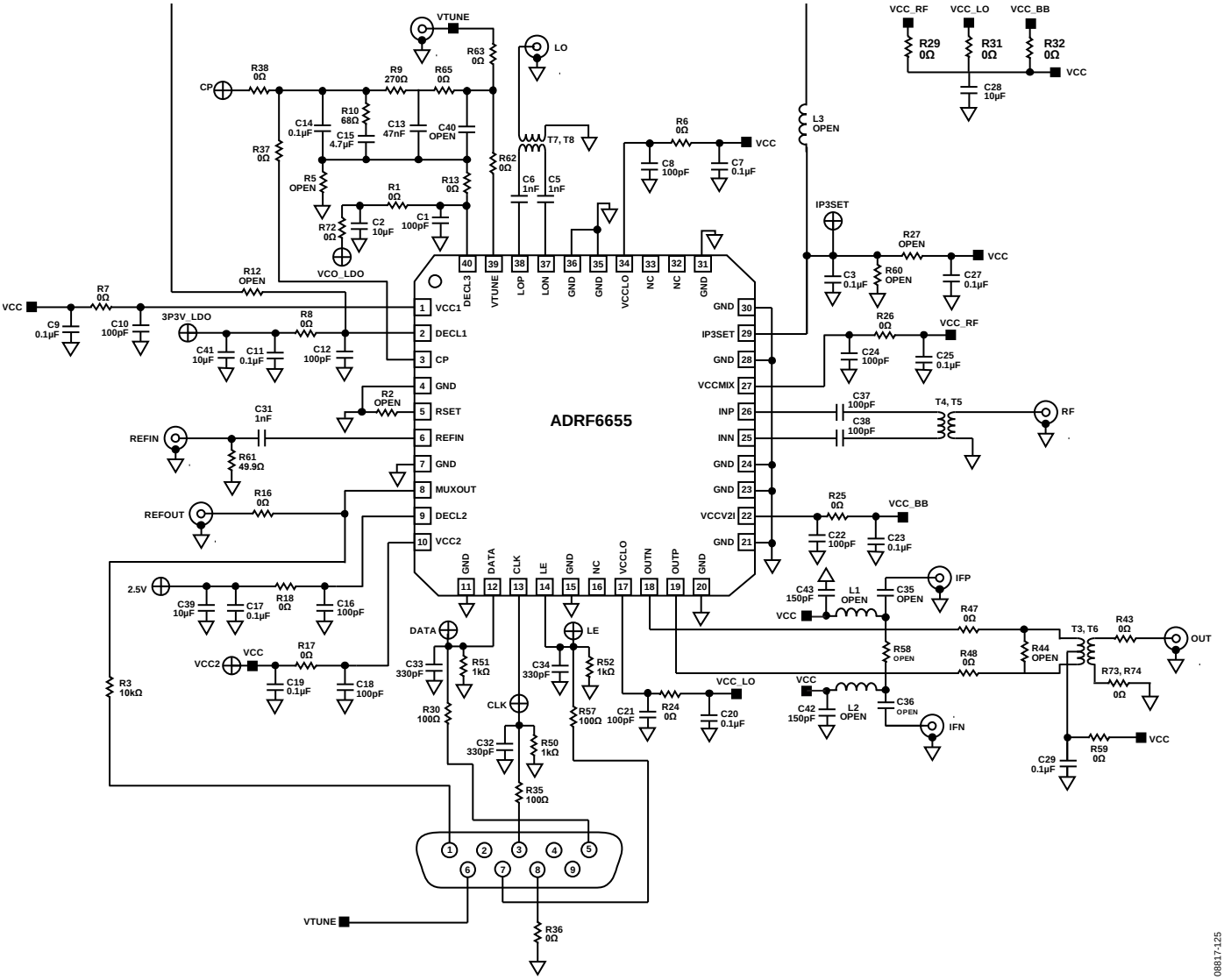


Figure 82. Evaluation Board Schematic

The package for the ADRF6655 features an exposed paddle on the underside that should be well soldered to a low thermal and electrical impedance ground plane. This paddle is typically soldered to an exposed opening in the solder mask on the evaluation board. Figure 83 illustrates the dimensions used in the layout of the ADRF6655 footprint on the ADRF6655 evaluation board (1 mil. = 0.0254 mm).

Notice the use of nine via holes on the exposed paddle. These ground vias should be connected to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Under these conditions, the thermal impedance of the ADRF6655 was measured to be approximately 29°C/W in still air.

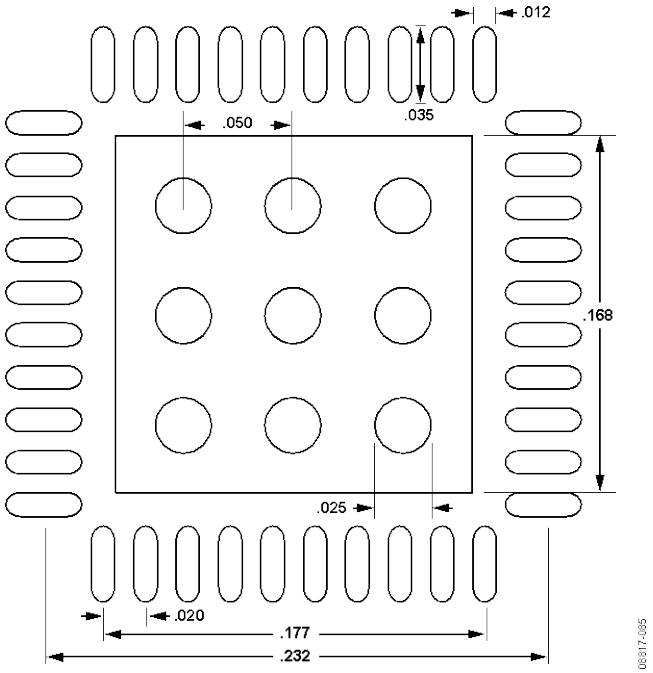


Figure 83. Evaluation Board Layout Dimensions for the ADRF6655 Package

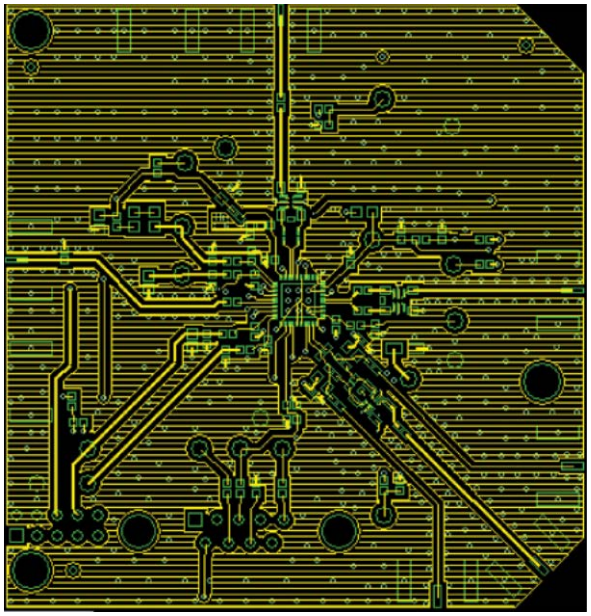


Figure 84. Evaluation Board Top Layer

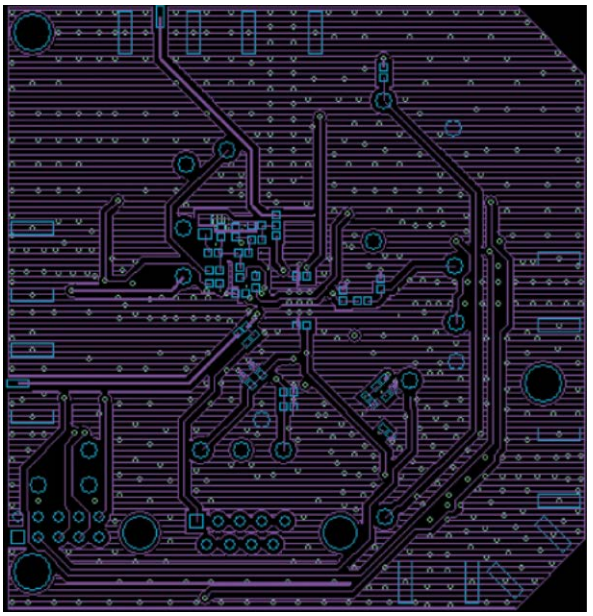


Figure 85. Evaluation Board Bottom Layer

Table 5. Evaluation Board Configuration Options

Component	Function	Default Condition
VCC, GND, IP3SET, CP, VCO_LDO, VCC_LO, VCC_RF, VCC_BB, LE, CLK, DATA	Power supply, ground, and other test points.	Not applicable
R1, R6, R7, R8, R17, R18, R24, R25, R26, R29, R31, R32, R36	Power supply decoupling. Shorts or power supply decoupling resistors.	R1, R6, R7, R8 = 0 Ω (0402), R17, R18 = 0 Ω (0402), R24, R25, R26 = 0 Ω (0402), R29, R31, R32 = 0 Ω (0402), R36 = 0 Ω (0402)
C1, C2, C7, C8, C9, C10, C11, C12, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C27, C28, C29, C39, C41, C42, C43	The capacitors provide the required decoupling of the supply-related pins.	C1, C8, C10 = 100 pF (0402), C2, C39, C41 = 10 µF (0603), C7, C9, C11 = 0.1 µF (0402), C12, C16, C18 = 100 pF (0402), C21, C22, C24 = 100 pF (0402), C17, C19, C20 = 0.1 µF (0402), C23, C25, C27 = 0.1 µF (0402), C28 = 10 µF (3216), C29 = 0.1 µF (0402), C42, C43 = 150 pF (0402)
C5, C6, T7, T8	External LO path. T7 and T8 provide different footprints for different LO path transformer selections. C5 and C6 provide the necessary ac coupling.	C5, C6 = 1 nF (0402), T7 = open (generic footprint), T8 = TC1-1-13M+ (Mini-Circuits)
R61, C31, R16	REFIN input path. R61 provides a broadband 50 Ω termination followed by C31, an ac coupling capacitor. R16 provides an external connectivity to the MUXOUT feature described in Register 4.	R61 = 49.9 Ω (0402), C31 = 1 nF (0402), R16 = 0 Ω (0402)
R2, R5, R9, R10, R13, R37, R38, R62, R63, R65, R72, C13, C14, C15, C40	Loop Filter Component Options. A variety of loop filter topologies are supported using component placements R9, R10, R13, R37, C13, C14, C15, R65, and C40. R2 provides resistor programmability of the charge pump current (see Register 4 description). R5, R38, R62, R63, and R72 provide connectivity options to numerous test points for engineering evaluation purposes.	R2 = R5 = open, R9 = 270 Ω (0402), R10 = 68 Ω (0402), R13 = 0 Ω (0402) C13 = 47nF, C14 = 0.1µF, C15 = 4.7µF (0805), C40 = open (0402), R37, R38, R62, R63, R65, R72 = 0 Ω (0402)
L1, L2, R43, R44, R47, R48, R58, R59, R73, R74, T3, T6, C35, C36	IF output path. This is the default configuration of the evaluation board for downconversion applications. R73 and R74 are populated for appropriate balun interface. The default values support a TC4-1W+ 4-to-1 impedance ratio transformer with center tap bias connection through R59. A differential IF output interface can be configured by populating C35 and C36 and omitting R47 and R48. When configuring for differential output operation or when using an ac-coupled transformer, it is important to use L1 and L2 to provide dc bias to the IF output pins. For additional information, see the Output Matching and Biasing section.	L1, L2 = open, R44, R58, = open, R43, R47, R48 = 0 Ω (0402), R59, R73, R74 = 0 Ω (0402), T3 = TC4-1W+ (Mini-Circuits), T6 = open, C35, C36 = open
C37, C38, T4, T5	RF input interface. T4 and T5 provide different footprints for different RF path transformer selections. C37 and C38 provide the necessary ac coupling. See the Input Matching section for additional information.	C37, C38 = 100 pF (0402), T4 = TC1-1-13M+ (Mini-Circuits), T5 = open
P1, R3, R30, R35, R50, R51, R52, R57, C32, C33, C34	Serial port interface. A 9-pin D-sub connector is provided for connecting to a host PC or control hardware. RC filter networks are provided on CLK, DATA, and LE lines to help clean up PC control signal wave shape. Test points are provided for control interface debug. R3 provides a connection to the MUXOUT for sensing lock detect through the P1 connector. See the Digital Interfaces section for additional information.	P1 = 9-pin D-sub male, R3 = 10 kΩ (0402), R30, R35, R57 = 100 Ω (0402), R50, R51, R52 = 1 kΩ (0402), C32, C33, C34 = 330 pF (0402)
C3, R12, R27, R60, L3	IP3SET linearization feature. R27 and R60 provision for a resistive divider network for providing nominal IP3SET voltage. Alternatively, the IP3SET pin can be externally driven via the test point or directly connected to the 3.3 V LDO (Pin 2, DECL1) using a 0 Ω resistor for R12 and a ferrite chip inductor for L3. For additional information regarding this feature, see the IP3SET Linearization Feature section.	C3 = 0.1 µF (0402), R12 = open, R27, R60 = open, L3 = open

OUTLINE DIMENSIONS

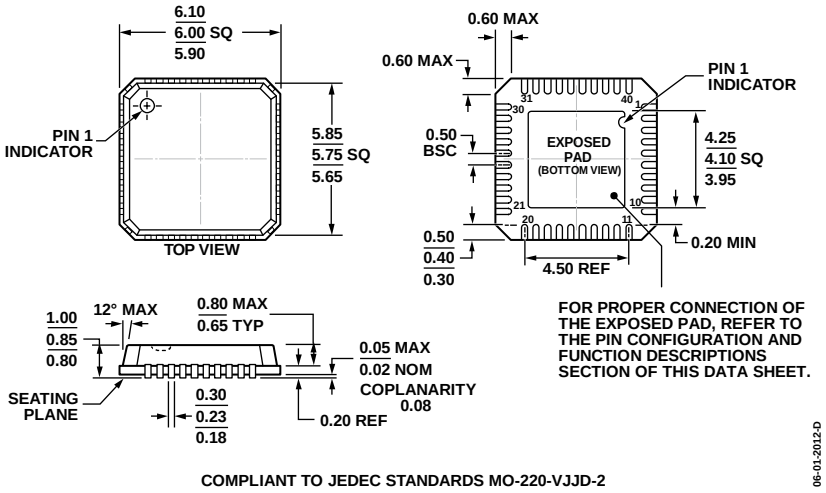


Figure 86. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	Package Description	Package Option	Quantity
ADRF6655ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1	750
ADRF6655-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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D08817-0-9/14(A)