700 MHz to 2700 MHz Rx Mixer with Integrated IF DGA, Fractional-N PLL, and VCO

Data Sheet

ADRF6620

FEATURES

- Integrated fractional-N phase-locked loop (PLL)
- RF input frequency range: 700 MHz to 2700 MHz
- Internal local oscillator (LO) frequency range: 350 MHz to 2850 MHz
- Input P1dB: 17 dBm
- Output IP3: 45 dBm
- Single-pole four-throw (SP4T) RF input switch
- Digital step attenuator (DSA) range: 0 dB to 15 dB
- Integrated RF tunable balun allowing single-ended 50 Ω input
- Multicore integrated voltage controlled oscillator (VCO)
- Digitally programmable variable gain amplifier (DGA)
  - −3 dB bandwidth: >600 MHz
- Balanced 150 Ω IF output impedance
- Programmable via 3-wire serial port interface (SPI)
- Single 5 V supply

APPLICATIONS

- Wireless receivers
- Digital predistortion (DPD) receivers

FUNCTIONAL BLOCK DIAGRAM

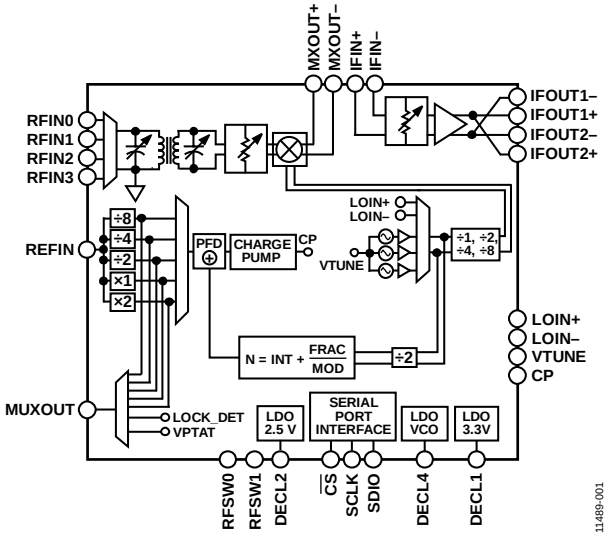

Figure 1.

GENERAL DESCRIPTION

The ADRF6620 is a highly integrated active mixer and synthesizer that is ideally suited for wireless receiver subsystems. The feature rich device consists of a high linearity broadband active mixer; an integrated fractional-N PLL; low phase noise, multicore VCO; and IF DGA. In addition, the ADRF6620 integrates a 4:1 RF switch, an on-chip tunable RF balun, programmable RF attenuator, and low dropout (LDO) regulators. This highly integrated device fits within a small 7 mm × 7 mm footprint.

The high isolation 4:1 RF switch and on-chip tunable RF balun enable the ADRF6620 to support four single-ended 50 Ω terminated RF inputs. A programmable attenuator ensures optimal RF input drive to the high linearity mixer core. The integrated DSA has an attenuation range of 0 dB to 15 dB with a step size of 1 dB.

The ADRF6620 offers two alternatives for generating the differential LO input signal: externally, via a high frequency, low phase noise LO signal, or internally, via the on-chip fractional-N PLL synthesizer. The integrated synthesizer enables continuous LO coverage from 350 MHz to 2850 MHz. The PLL reference input can support a wide frequency range because the divide and multiply blocks can be used to increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD).

The integrated high linearity DGA provides an additional gain range from 3 dB to 15 dB in steps of 0.5 dB for maximum flexibility in driving an analog-to-digital converter (ADC).

The ADRF6620 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 48-lead, RoHS-compliant, 7 mm × 7 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +85°C temperature range.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 Technical Support
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REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO INPUT					
Internal LO Frequency Range		350		2850	MHz
External LO Frequency Range	LO_DIV_A = 00	350		3200	MHz
LO Input Level		−6	0	+6	dBm
LO Input Impedance			50		Ω
RF INPUT					
Input Frequency		700		2700	MHz
Input Return Loss			12		dB
Input Impedance			50		Ω
RF DIGITAL STEP ATTENUATOR					
Attenuation Range	Step size = 1 dB	0		15	dB
POWER SUPPLY		4.75	5.0	5.25	V
Power Consumption	LO output buffer disabled				
	External LO + IF DGA enabled		1.3		W
	Internal LO + IF DGA enabled		1.7		W
	Only IF DGA enabled		0.6		W
Power-Down Current			6		mA

RF INPUT TO IF DGA OUTPUT SYSTEM SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, high-side LO injection, f_{IF} = 200 MHz, internal LO frequency, IF DGA output load = 150 Ω, and 2 V p-p differential output with third-order low-pass filter, unless otherwise noted. For mixer settings for maximum linearity, see Table 16. All losses from input and output traces and baluns are de-embedded from results

Table 2. RF Switch + Balun + RF Attenuator + Mixer + IF DGA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT f_{RF} = 900 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			12		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		43		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		78		dBm
Noise Figure	Noise figure optimized		16		dB
DYNAMIC PERFORMANCE AT f_{RF} = 1900 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			11		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		75		dBm
Noise Figure	Noise figure optimized		18.5		dB
DYNAMIC PERFORMANCE AT f_{RF} = 2100 MHz	f_{IF} = 200 MHz				dB
Voltage Conversion Gain			10.5		dBm
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		66		dBm
Noise Figure	Noise figure optimized		19		dB
DYNAMIC PERFORMANCE AT f_{RF} = 2700 MHz	f_{IF} = 200 MHz				
Voltage Conversion Gain			9		dB
Output P1dB			18		dBm
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		44		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		74		dBm
Noise Figure	Noise figure optimized		21		dB

SYNTHESIZER/PLL SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm, f_{PFD} = 38.4 MHz, and loop filter bandwidth = 120 kHz, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
PLL Reference Frequency		12		464	MHz
PLL Reference Level	For PLL lock condition	−15	+4	+14	dBm
PFD FREQUENCY		24		58	MHz
INTERNAL VCO RANGE		2800		5700	MHz
OPEN-LOOP VCO PHASE NOISE	VTUNE = 2 V, LO_DIV_A = 00				
f_{VCO2} = 3.4 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−81		dBc/Hz
	100 kHz offset		−103		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−155		dBc/Hz
	VCO sensitivity (K_V)		88		MHz/V
f_{VCO1} = 4.6 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−74		dBc/Hz
	100 kHz offset		−101		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−156		dBc/Hz
	VCO sensitivity (K_V)		89		MHz/V
f_{VCO0} = 5.5 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−69		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−121		dBc/Hz
	1 MHz offset		−124		dBc/Hz
	6 MHz offset		−142		dBc/Hz
	10 MHz offset		−146		dBc/Hz
	40 MHz offset		−155		dBc/Hz
	VCO sensitivity (K_V)		72		MHz/V
SYNTHESIZER SPECIFICATIONS	Measured at LO output, LO_DIV_A = 01				
f_{LO} = 1.710 GHz, f_{VCO2} = 3.420 GHz	f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz, 120 kHz loop filter				
f_{PFD} Spurs	$f_{PFD} \times 1$		−83		dBc
	$f_{PFD} \times 2$		−89		dBc
	$f_{PFD} \times 3$		−90		dBc
	$f_{PFD} \times 4$		−93		dBc
Closed-Loop Phase Noise	1 kHz offset		−97		dBc/Hz
	10 kHz offset		−110		dBc/Hz
	100 kHz offset		−107		dBc/Hz
	800 kHz offset		−128		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−152		dBc/Hz
	40 MHz offset		−158		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.21		° rms
Figure of Merit (FOM)[1]			−222		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{LO} = 2.305 GHz, f_{VCO1} = 4.610 GHz					
f_{PFD} Spurs	$f_{PFD} \times 1$		−84		dBc
	$f_{PFD} \times 2$		−87		dBc
	$f_{PFD} \times 3$		−91		dBc
	$f_{PFD} \times 4$		−92		dBc
Closed-Loop Phase Noise	1 kHz offset		−93		dBc/Hz
	10 kHz offset		105		dBc/Hz
	100 kHz offset		−103		dBc/Hz
	800 kHz offset		−116		dBc/Hz
	1 MHz offset		−130		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−152		dBc/Hz
	40 MHz offset		−156		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.3		° rms
Figure of Merit[1]			−222		dBc/Hz
f_{LO} = 2.75 GHz, f_{VCO2} = 5.5 GHz					
f_{PFD} Spurs	$f_{PFD} \times 1$		−82		dBc
	$f_{PFD} \times 2$		−88		dBc
	$f_{PFD} \times 3$		−93		dBc
	$f_{PFD} \times 4$		−96		dBc
Closed-Loop Phase Noise	1 kHz offset		−93		dBc/Hz
	10 kHz offset		−101		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−122		dBc/Hz
	1 MHz offset		−128		dBc/Hz
	6 MHz offset		−144		dBc/Hz
	10 MHz offset		−151		dBc/Hz
	40 MHz offset		−154		dBc/Hz
Integrated Phase Noise	10 kHz to 40 MHz integration bandwidth		0.38		° rms
Figure of Merit[1]			−222		dBc/Hz

[1] Figure of merit (FOM) is computed as phase noise (dBc/Hz) − 10 log 10(f_{PFD}) − 20 log 10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 160 MHz and f_{REF} power = 4 dBm (500 V/µs slew rate) with a 40 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

RF INPUT TO MIXER OUTPUT SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, high-side LO injection, f_{IF} = 200 MHz, external LO frequency, and RF attenuation = 0 dB, unless otherwise noted. Mixer settings configured for maximum linearity (see Table 16). All losses from input and output traces and baluns are de-embedded from results.

Table 4. RF Switch + Balun + RF Attenuator + Mixer

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE GAIN	Differential 255 Ω load		−4		dB
MIXER OUTPUT IMPEDANCE	Differential (see Figure 87)		255		Ω
DYNAMIC PERFORMANCE AT f_{RF}= 900 MHz					
Voltage Conversion Gain			−2		dB
Input P1dB			17		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		65		dBm
Noise Figure			15		dB
LO to RF Leakage			−70		dBm
RF to LO Leakage			−60		dBc
LO to IF Leakage			−32		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−45		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−52		dBc
DYNAMIC PERFORMANCE AT f_{RF} =1900 MHz					
Voltage Conversion Gain			−3		dB
Input P1dB			17		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		62		dBm
Noise Figure			17		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−50		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−43		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−47		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 2100 MHz					
Voltage Conversion Gain			−3.5		dB
Input P1dB			18		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		54.5		dBm
Noise Figure			18		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−40		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−40		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−45		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 2700 MHz					
Voltage Conversion Gain			−4.7		dB
Input P1dB			19		dBm
Input IP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
Input IP2	−5 dBm each input tone, 1 MHz tone spacing		56		dBm
Noise Figure			21		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−45		dBc
LO to IF Leakage			−40		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−42		dBc
Isolation[1]	Isolation between RFIN0 and RFIN3		−41		dBc

[1] Isolation between RF inputs. An input signal was applied to RFIN0 while RFIN1 to RFIN3 were terminated with 50 Ω. The IF signal amplitude was measured at the mixer output. The internal switch was then configured for RFIN3, and the feedthrough was measured as a delta from the fundamental.

IF DGA SPECIFICATIONS

VCCx = 5 V, T_A = 25°C, R_S = R_L = 150 Ω differential, f_{IF} = 200 MHz, 2 V p-p differential output,unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BANDWIDTH					
−1 dB Bandwidth	V_{OUT} = 2 V p-p		500		MHz
−3 dB Bandwidth	V_{OUT} = 2 V p-p		700		MHz
SLEW RATE			5.5		V/ns
INPUT STAGE					
Input P1dB	At minimum gain		17		dBm
Input Impedance			150		Ω
Common-Mode Input Voltage			1.5		V
Common-Mode Rejection Ratio (CMRR)			50		dB
GAIN					
Power/Voltage Gain, Step Size = 0.5 dB		3		15	dB
Gain Flatness	50 MHz < f_C < 200 MHz		0.2		dB
Gain Conformance Error			±0.1		dB
Gain Temperature Sensitivity			0.008		dB/C
Gain Step Response			15		ns
OUTPUT STAGE					
Output P1dB			18		dBm
Output Impedance	See Figure 88		150		Ω
NOISE/HARMONIC PERFORMANCE at 200 MHz					
Output IP3	1 V p-p each output tone, 1 MHz tone spacing		45		dBm
Output IP2	1 V p-p each output tone, 1 MHz tone spacing		63		dBm
HD2	V_{OUT} = 2 V p-p		−87		dBc
HD3	V_{OUT} = 2 V p-p		−84		dBc
Noise Figure			10		dB

DIGITAL LOGIC SPECIFICATIONS

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL PORT INTERFACE TIMING						
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.70	V
Output Voltage High	V_{OH}	I_{OH} = −100 µA	2.3			V
Output Voltage Low	V_{OL}	I_{OL} = +100 µA	0.2			V
Serial Clock Period	t_{SCLK}		38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}		8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}		8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	t_S		10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	t_H		10			ns
Minimum Period SCLK Can Be in Logic High State	t_{HIGH}		10			ns
Minimum Period SCLK Can Be in Logic Low State	t_{LOW}		10			ns
Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}				231	ns
Maximum Time Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	t_Z				5	ns

Timing Diagram

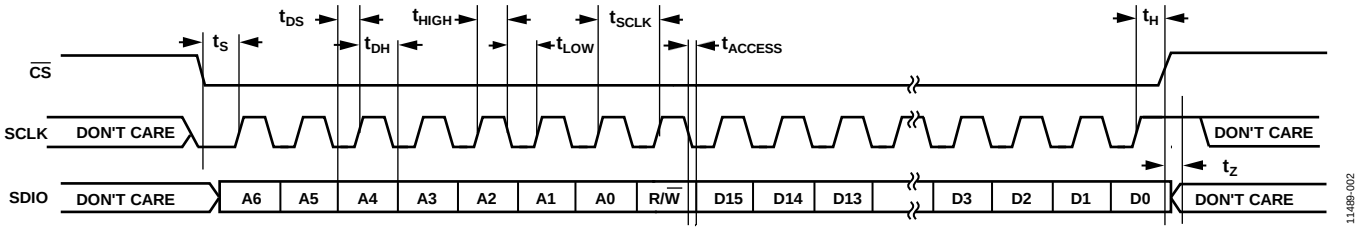

Figure 2. Serial Port Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCCx	−0.5 V to +5.5 V
RFSW0, RFSW1	−0.3 V to +3.6 V
RFIN0, RFIN1, RFIN2, RFIN3	20 dBm
LOIN−, LOIN+	16 dBm
REFIN	−0.3 V to +3.6 V
IFIN−, IFIN+	−1.2 V to +3.6 V
$\overline{CS}$, SCLK, SDIO	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JC}	Unit
48-Lead LFCSP	1.62	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

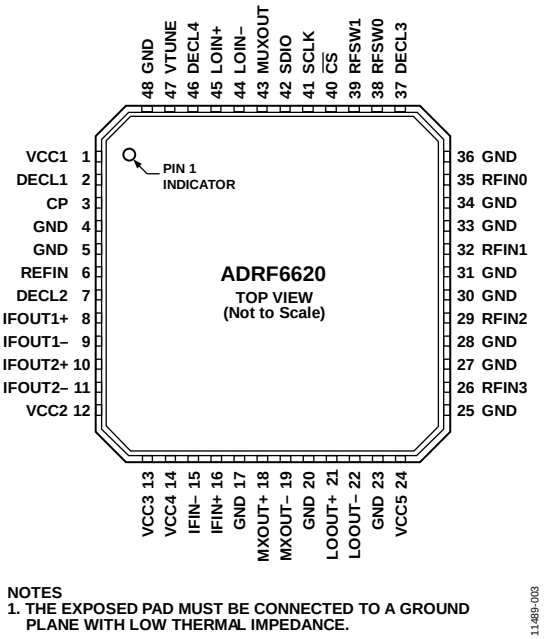

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1, 12, 13, 14, 24	VCC1, VCC2, VCC3, VCC4, VCC5	5 V Power Supplies. Decouple all power supply pins to ground, using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors near the pins.
2, 7, 37, 46	DECL1, DECL2, DECL3, DECL4	Decouple all DECLx pins to ground, using 100 pF, 0.1 µF, and 10 µF capacitors. Place the decoupling capacitors near the pins.
3	CP	Synthesizer Charge Pump Output. Connect this pin to the VTUNE pin through the loop filter.
4, 5, 17, 20, 23, 25, 27, 28, 30, 31, 33, 34, 36, 48	GND	Ground.
6	REFIN	Synthesizer Reference Frequency Input.
8 to 11	IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−	IF DGA Outputs. Connect the positive pins such that IFOUT1+ and IFOUT2+ are tied together. Similarly, connect the negative pins such that IFOUT1− and IFOUT2− are tied together. Refer to the Layout section for a recommended layout that minimizes parasitic capacitance and optimizes performance.
15, 16	IFIN−, IFIN+	Differential IF DGA Inputs. AC couple the mixer outputs to the IF DGA inputs.
18, 19	MXOUT+, MXOUT−	Differential Mixer Outputs. AC couple the mixer outputs to the IF DGA inputs.
21, 22	LOOUT+, LOOUT−	Differential LO Outputs. The differential output impedance is 50 Ω.
26, 29, 32, 35	RFIN3, RFIN2, RFIN1, RFIN0	RF Inputs. These single-ended RF inputs have a 50 Ω input impedance and must be ac-coupled.
38, 39	RFSW0, RFSW1	External Pin Control of RF Input Switches. For logic high, connect these pins to 2.5 V logic.
40	$\overline{CS}$	SPI Chip Select, Active Low. 3.3 V tolerant logic levels.
41	SCLK	SPI Clock. 3.3 V tolerant logic levels.
42	SDIO	SPI Data Input or Output. 3.3 V tolerant logic levels.
43	MUXOUT	Multiplexer Output. This output pin provides the PLL reference signal or the PLL lock detect signal.
44, 45	LOIN−, LOIN+	Differential Local Oscillator Inputs. The differential input impedance is 50 Ω.
47	VTUNE	VCO Tuning Voltage. Connect this pin to the CP pin through the loop filter.
49	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

[1] For more connection information about these pins, see Table 14.

TYPICAL PERFORMANCE CHARACTERISTICS

RF INPUT TO DGA OUTPUT SYSTEM PERFORMANCE

VCCx = 5 V, T_A = 25°C, RFDSA_SEL = 00 (0 dB), RFSW_SEL = 00 (RFIN0), BAL_CIN and BAL_COUT optimized for maximum gain; MIXER_BIAS, MIXER_RDAC, and MIXER_CDAC optimized for highest linearity, DGA at maximum gain; third-order low-pass filter between the mixer output and IF DGA input; high-side LO, internal LO frequency, IF frequency = 200 MHz, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

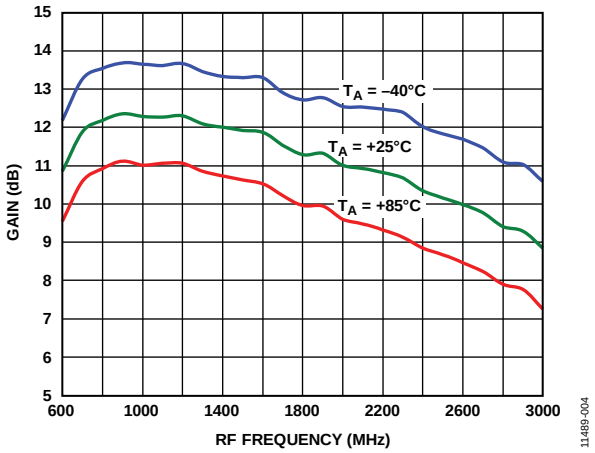

Figure 4. Gain vs. RF Frequency; IF Frequency = 200 MHz

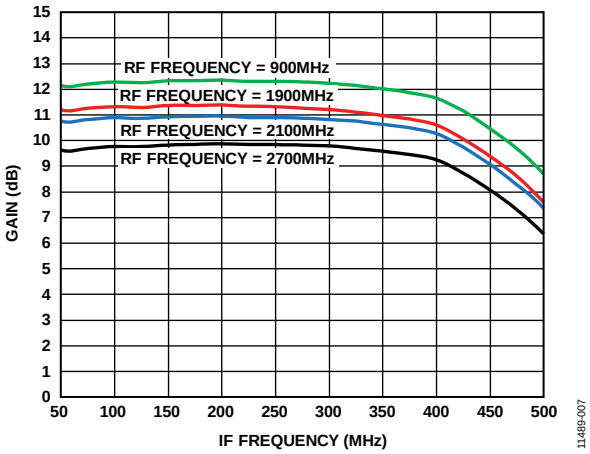

Figure 6. Gain vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

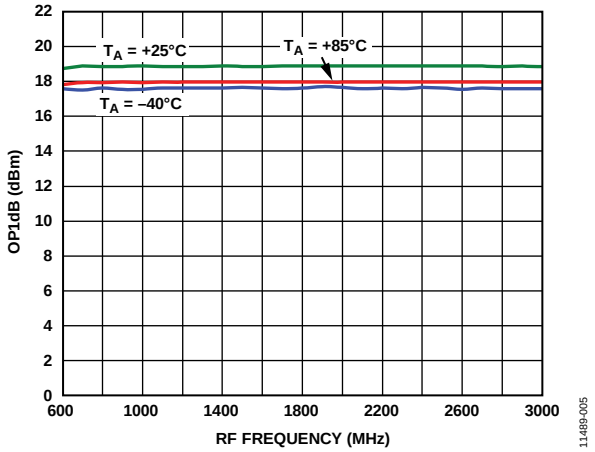

Figure 5. OP1dB vs. RF Frequency

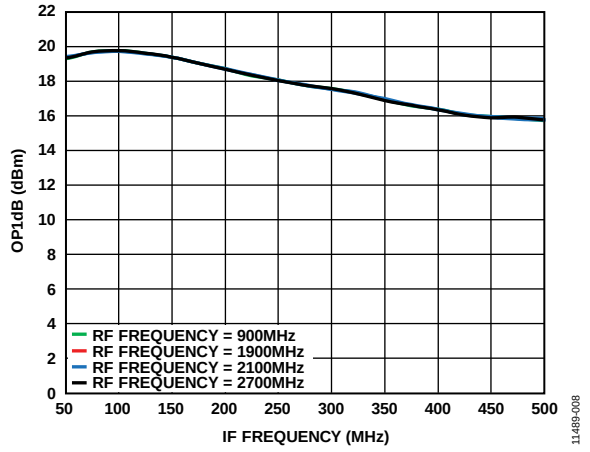

Figure 7. OP1dB vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

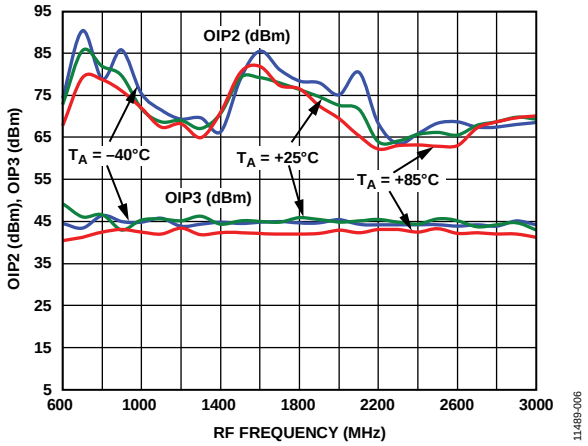

Figure 8. OIP2/OIP3 vs. RF Frequency; Measured on 1 V p-p on Each Tone at DGA Output

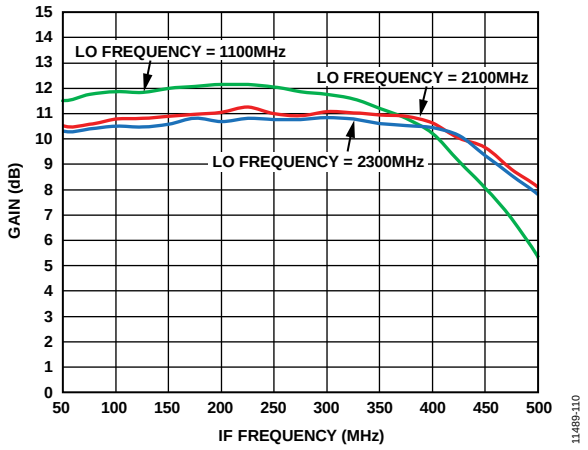

Figure 9. Gain vs. IF Frequency; RF Sweep with Fixed LO; IF and RF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

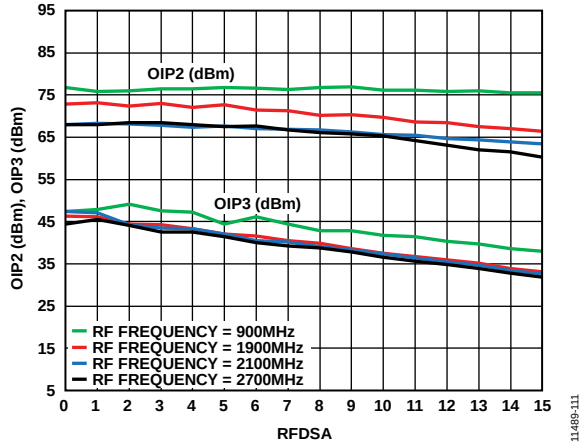

Figure 10. OIP2/OIP3 vs. RFDSA; Measured on 1 V p-p on Each Tone at DGA Output

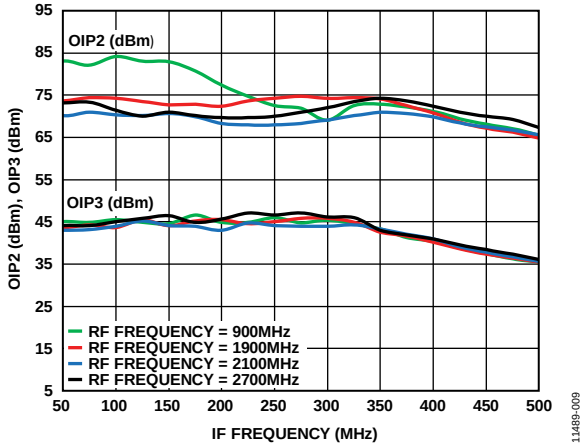

Figure 11. OIP2/OIP3 vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

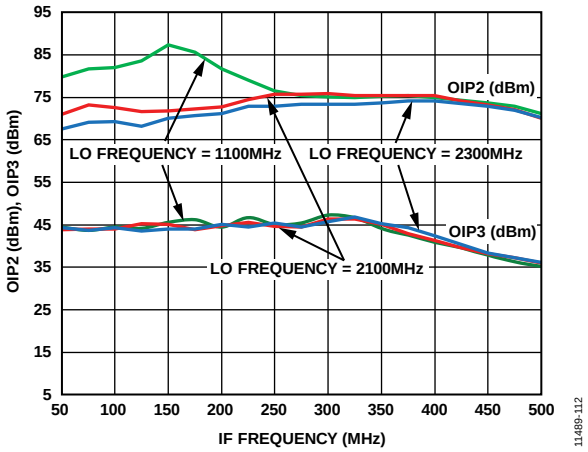

Figure 12. OIP2/OIP3 vs. IF Frequency; RF Sweep with Fixed LO; IF and RF Roll-Off; Measured on 1 V p-p on Each Tone at DGA Output

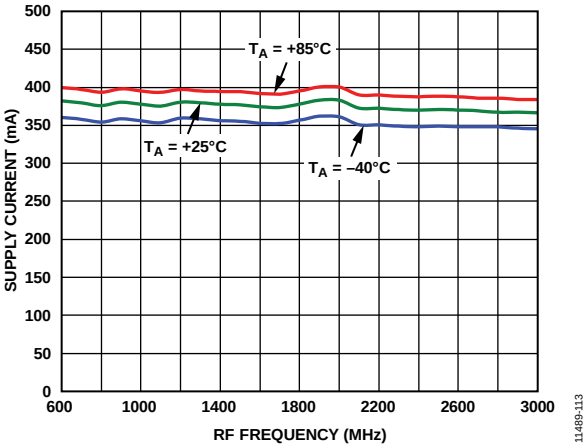

Figure 13. Supply Current vs. RF Frequency

PHASE-LOCKED LOOP (PLL)

VCCx = 5 V, T_A = 25°C, 120 kHz loop filter, f_{REF} = 153.6 MHz, PLL reference amplitude = 4 dBm, f_{PFD} = 38.4 MHz, measured at LO output, unless otherwise noted.

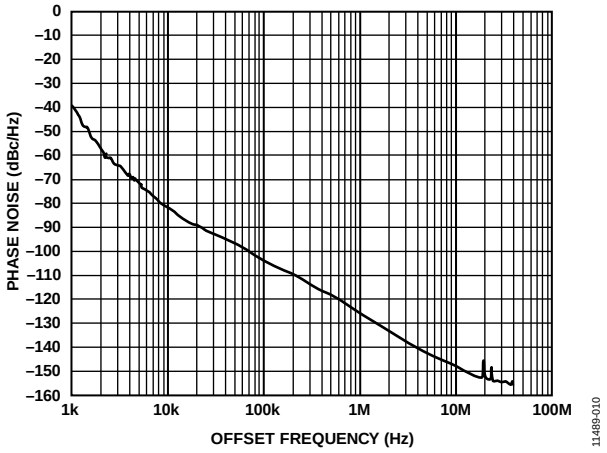

Figure 14. VCO2 Open-Loop VCO Phase Noise vs. Offset Frequency; f_{VCO2} = 3.4 GHz, LO_DIV_A = 00, VTUNE = 2 V

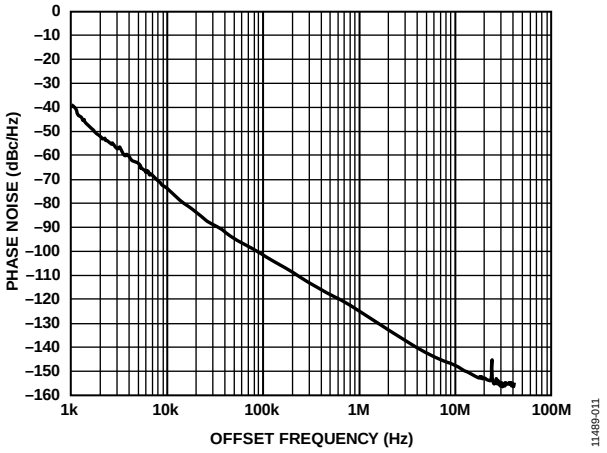

Figure 15. VCO1 Open-Loop Phase Noise vs. Offset Frequency; f_{VCO1} = 4.6 GHz, LO_DIV_A = 00, VTUNE = 2 V

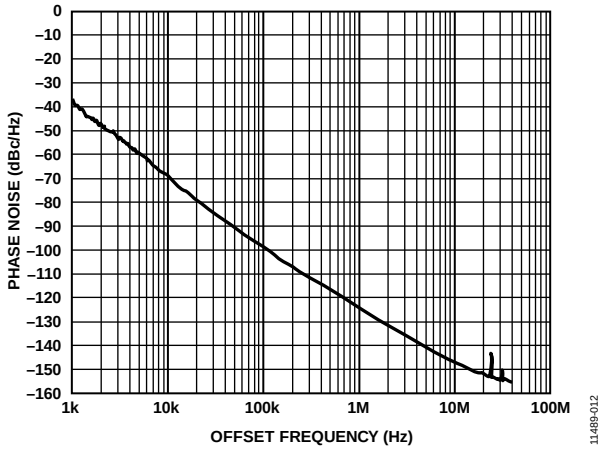

Figure 16. VCO0 Open-Loop Phase Noise vs. Offset Frequency; f_{VCO0} = 5.5 GHz, LO_DIV_A = 00, VTUNE = 2 V

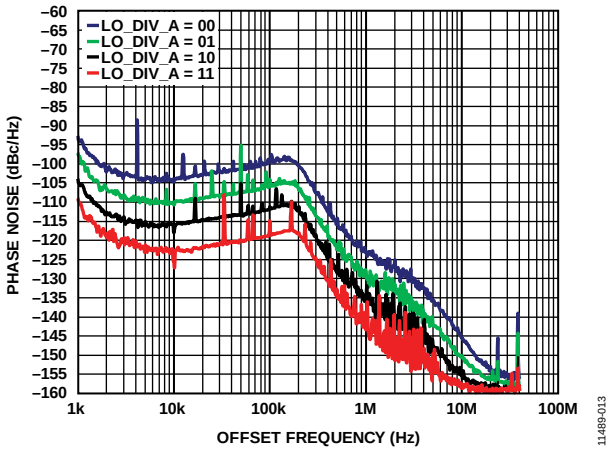

Figure 17. VCO2 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO2} = 3.4 GHz

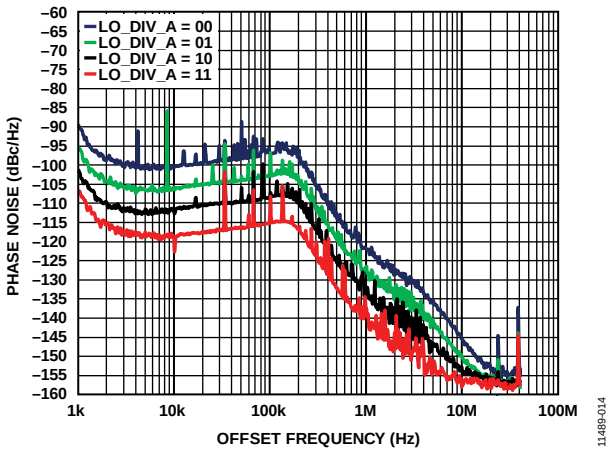

Figure 18. VCO1 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO1} = 4.6 GHz

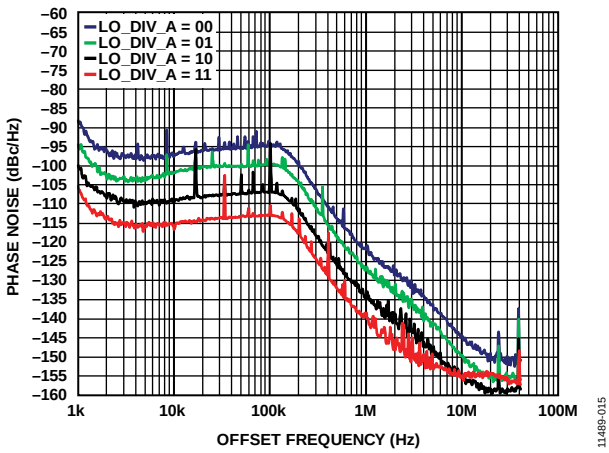

Figure 19. VCO0 Closed-Loop Phase Noise for Various LO_DIV_A Dividers vs. Offset Frequency; f_{VCO0} = 5.532 GHz

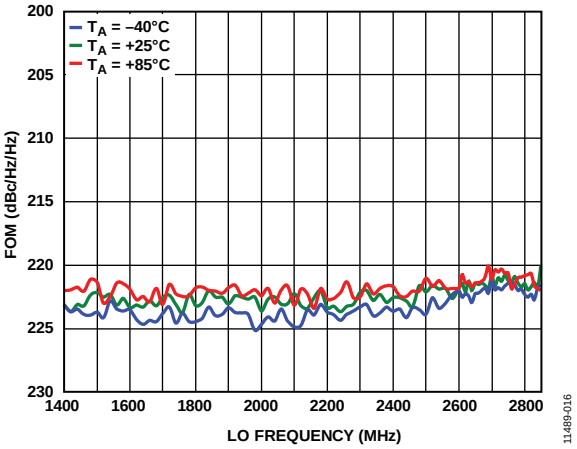

Figure 20. PLL Figure of Merit (FOM) vs. LO Frequency

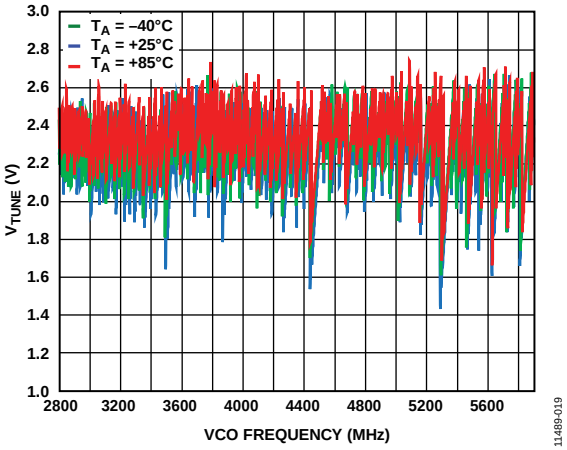

Figure 23. V_{TUNE} vs. VCO Frequency

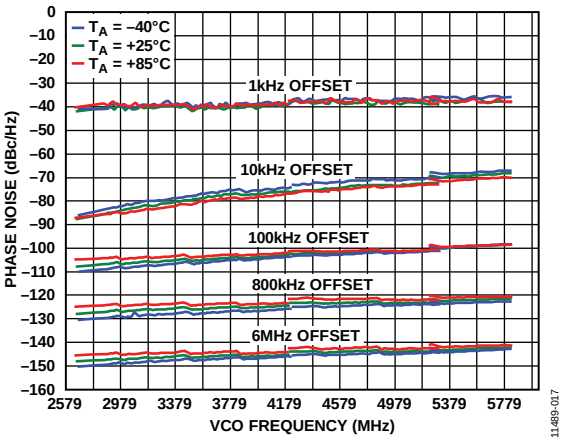

Figure 21. Open-Loop Phase Noise vs. VCO Frequency; LO_DIV_A = 00

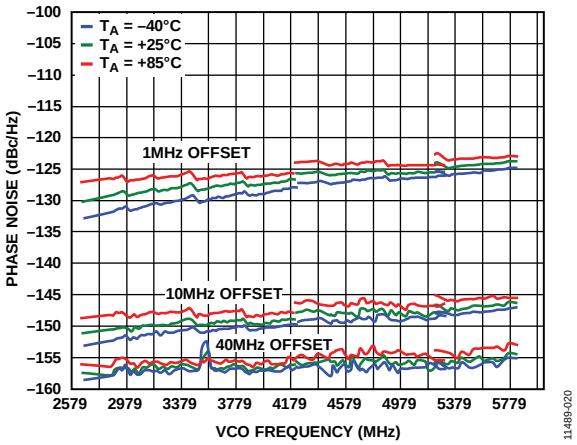

Figure 24. Open-Loop Phase Noise vs. VCO Frequency; LO_DIV_A = 00

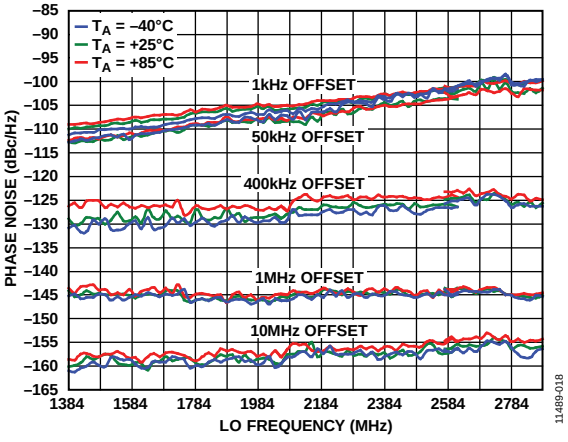

Figure 22. 120 kHz Bandwidth Loop Phase Noise, LO_DIV_A = 01; Offset = 1 kHz, 50 kHz, 400 kHz, 1 MHz, and 10 MHz

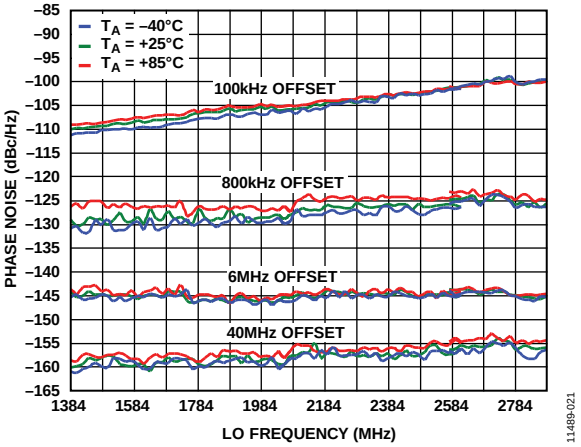

Figure 25. 120 kHz Bandwidth Loop Phase Noise, LO_DIV_A = 01; Offset = 100 kHz, 800 kHz, 6 MHz, and 40 MHz

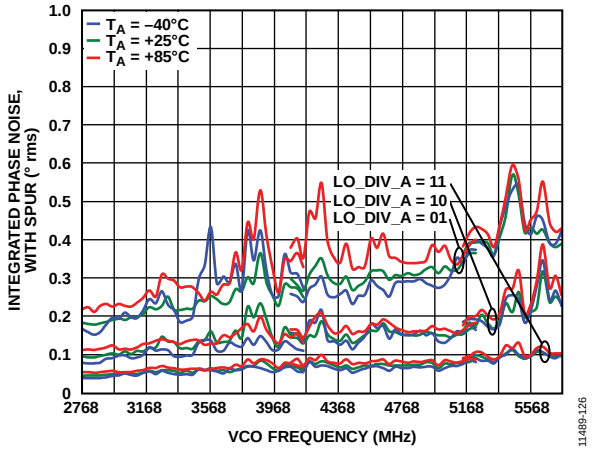

Figure 26. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency; LO_DIV_A = 01, 10, and 11, Including Spurs, for Various LO Divider Ratios

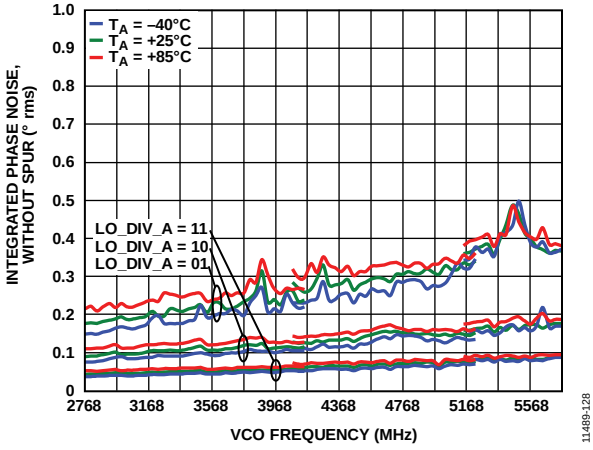

Figure 29. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency; LO_DIV_A = 01, 10, and 11, Excluding Spurs, for Various LO Divider Ratios

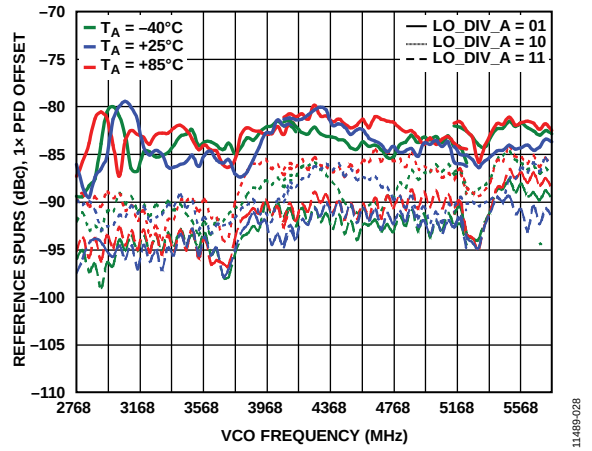

Figure 27. f_{PFD} Spurs vs. VCO Frequency; 1× PFD Offset; Measured at LO Output

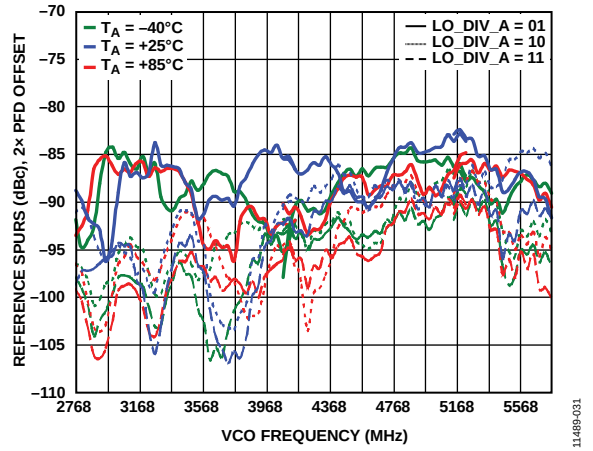

Figure 30. f_{PFD} Spurs vs. VCO Frequency; 2× PFD Offset; Measured at LO Output

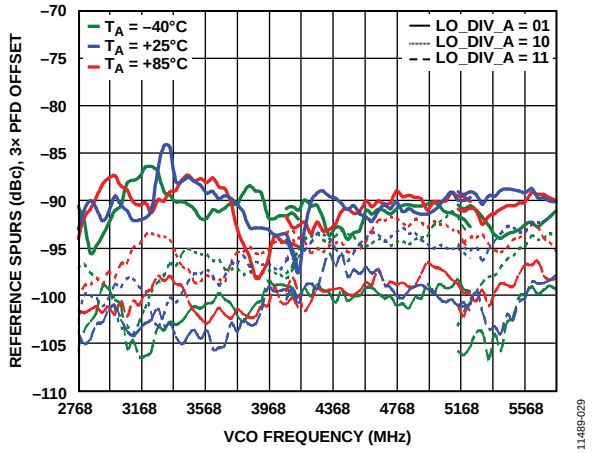

Figure 28. f_{PFD} Spurs vs. VCO Frequency; 3× PFD Offset; Measured at LO Output

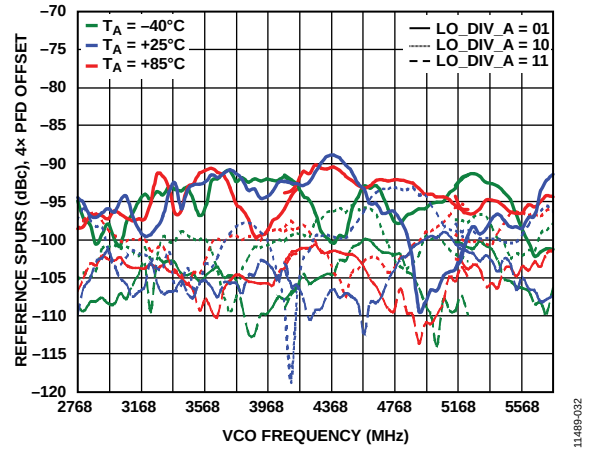

Figure 31. f_{PFD} Spurs vs. VCO Frequency; 4× PFD Offset; Measured at LO Output

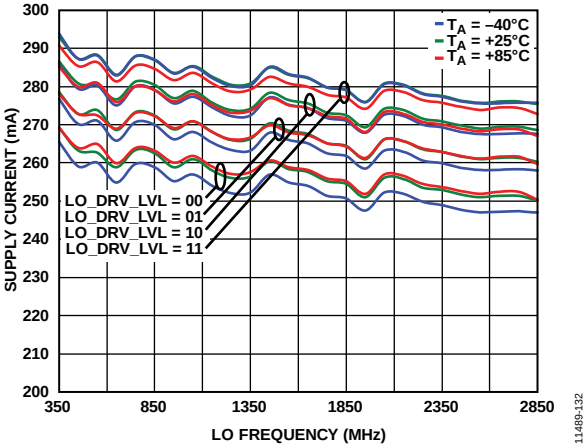

Figure 32. Supply Current vs. LO Frequency; LO_DRV_LVL = 00, 01, 10, and 11

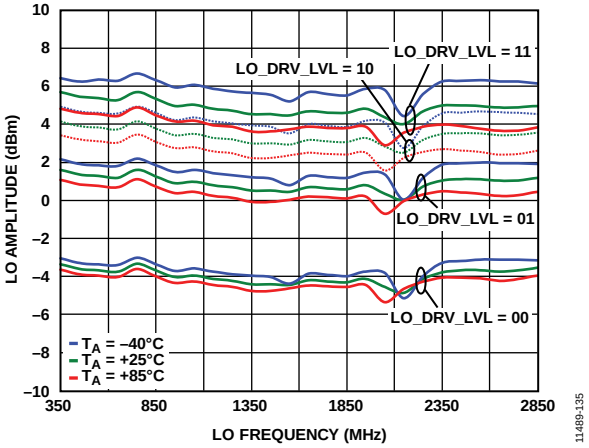

Figure 35. LO Amplitude vs. LO Frequency; LO_DRV_LVL = 00, 01, 10, and 11

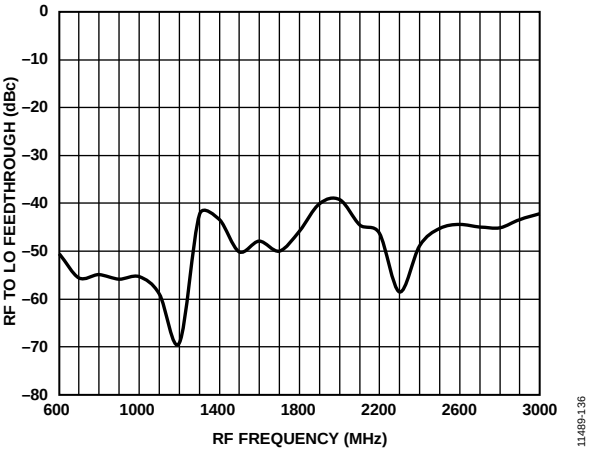

Figure 33. RF to LO Output Feedthrough, LO_DRV_LVL = 00

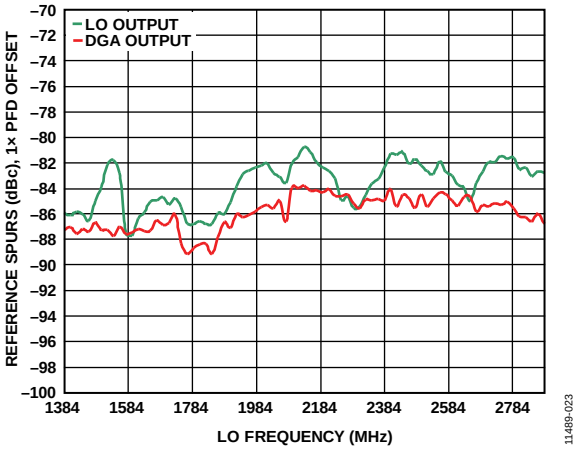

Figure 36. f_{PFD} Spurs, LO_DIV_A = 01, 1× PFD Offset; Measured on LO Output and DGA Output

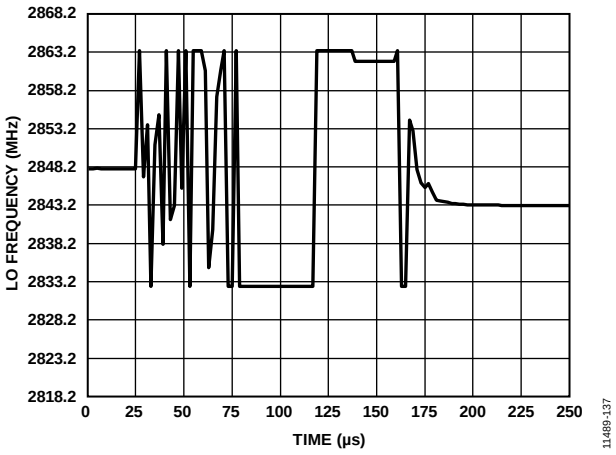

Figure 34. LO Frequency Settling Time, Loop Filter Bandwidth = 120 kHz

RF INPUT TO MIXER OUTPUT PERFORMANCE

VCCx = 5 V, T_A = 25°C, R_L = 250 Ω, external LO, P_{LO} = 0 dBm, RFDSA_SEL = 00 (0 dB), RFSW_SEL = 00 (RFIN0), BAL_CIN and BAL_COUT optimized, MIXER_BIAS, MIXER_RDAC, and MIXER_CDAC optimized for highest linearity, DGA and LO output disabled, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

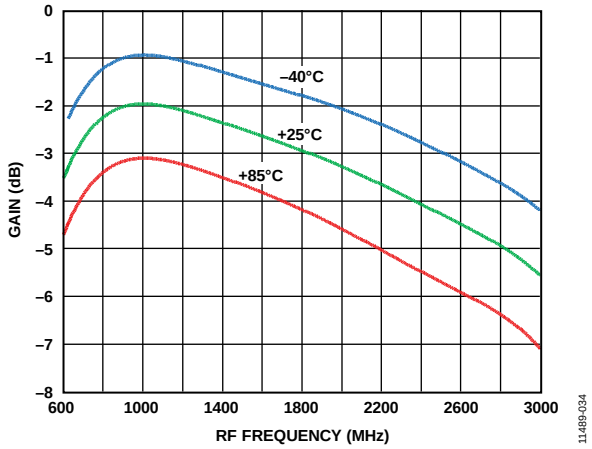

Figure 37. Mixer Gain vs. RF Frequency

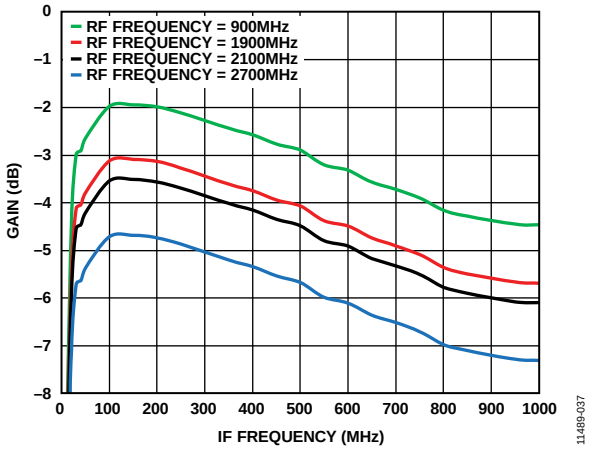

Figure 40. Mixer Gain vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

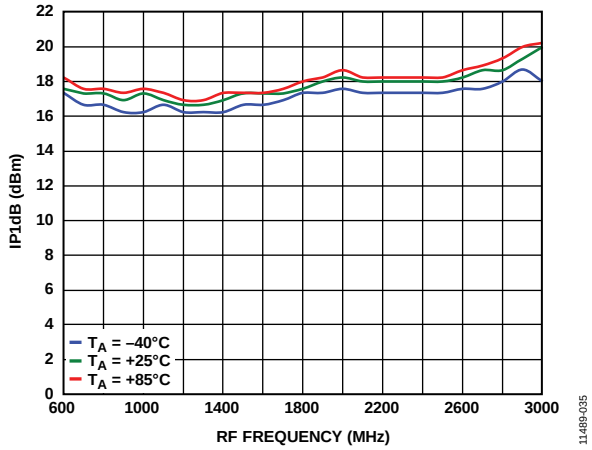

Figure 38. Mixer IP1dB vs. RF Frequency

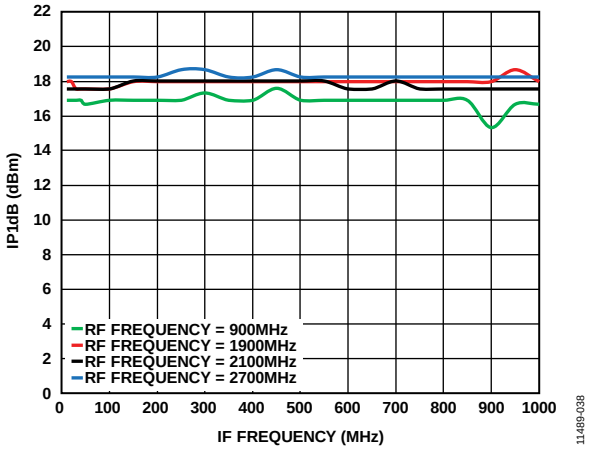

Figure 41. Mixer IP1dB vs. IF Frequency; LO Sweep with Fixed RF, IF Roll-Off

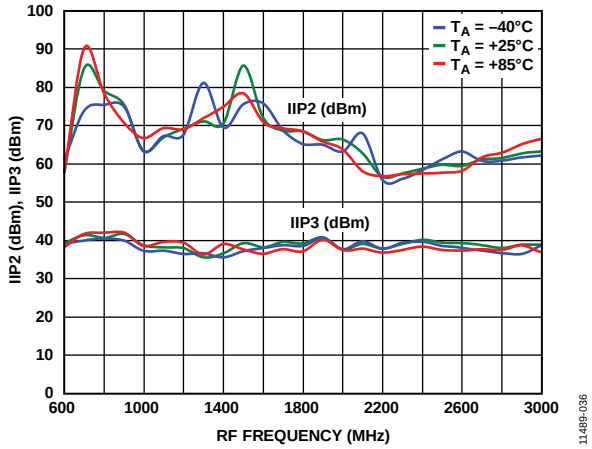

Figure 39. Mixer IIP2/IIP3 vs. RF Frequency; P_{IN} = –5 dBm/Tone, 1 MHz Spacing

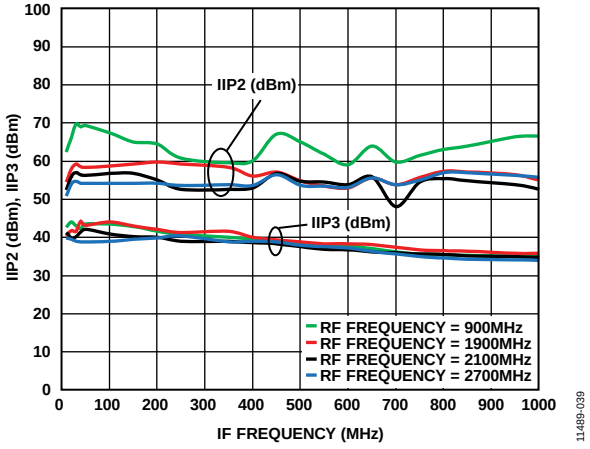

Figure 42. Mixer IIP2/IIP3 vs. IF Frequency; P_{IN} = –5 dBm/Tone, 1 MHz Spacing, LO Sweep with Fixed RF, IF Roll-Off

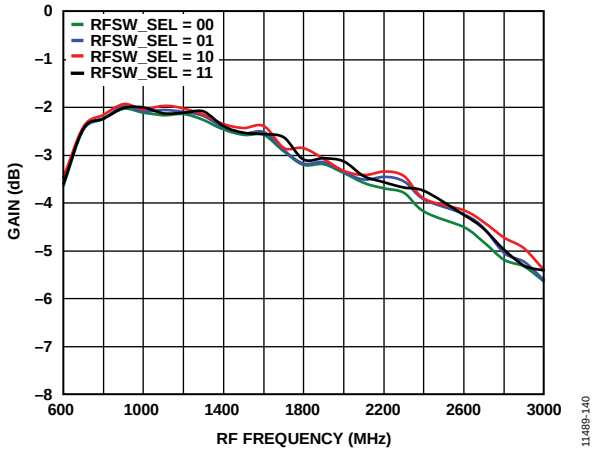

Figure 43. Mixer Gain vs. RF Frequency; RFSW_SEL = 00, 01, 10, and 11

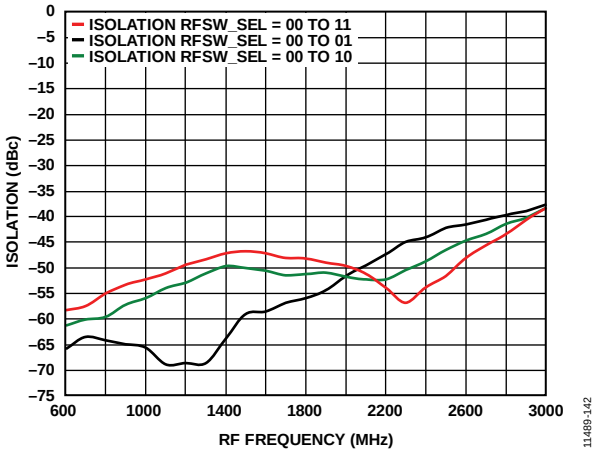

Figure 44. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 00 Driven

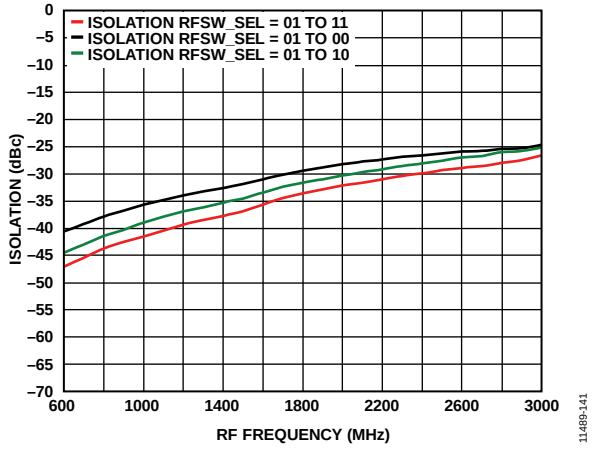

Figure 45. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 01 Driven

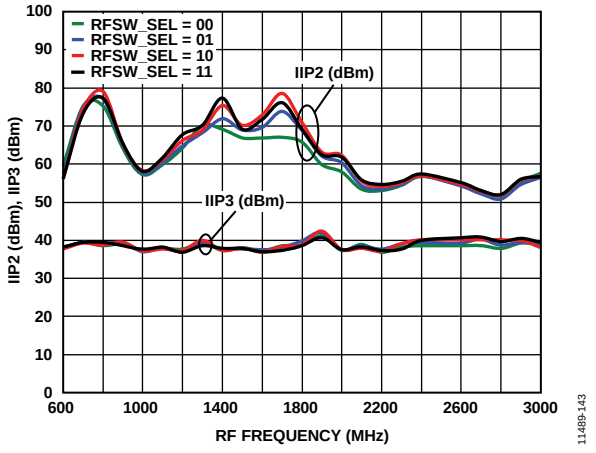

Figure 46. Mixer IIP2/IIP3 vs. RF Frequency; RFSW_SEL = 00, 01, 10, and 11

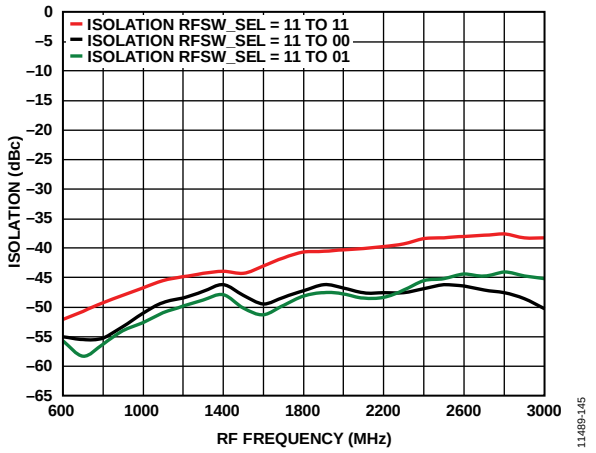

Figure 47. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 11 Driven

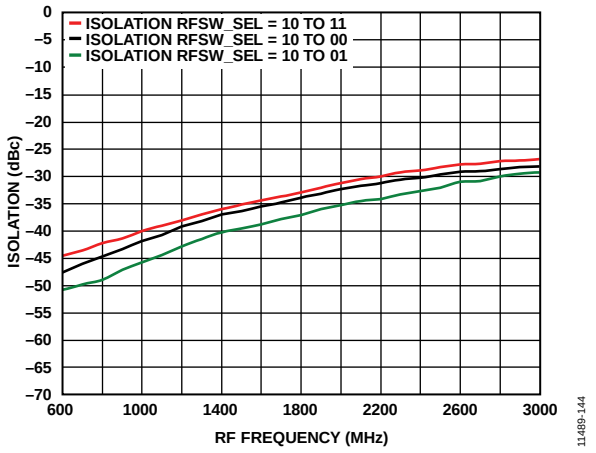

Figure 48. Mixer Input to Mixer Output Isolation vs. RF Frequency; RFSW_SEL = 10 Driven

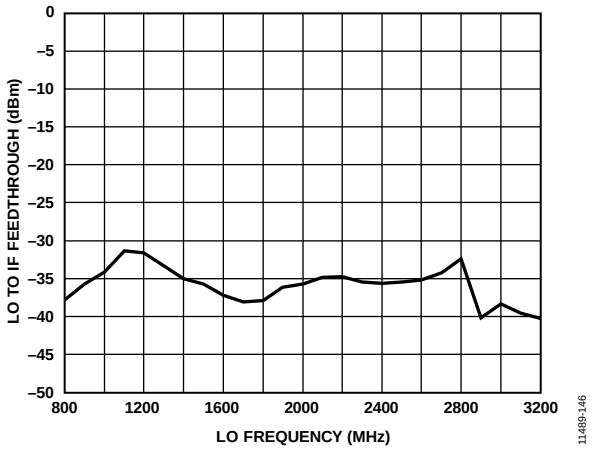

Figure 49. LO to IF Feedthrough at Mixer Output Without Filtering

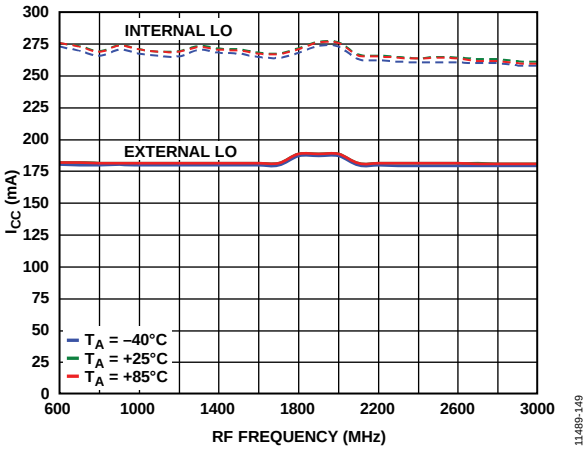

Figure 52. I_{CC} vs. RF Frequency; DGA and LO Output Disabled

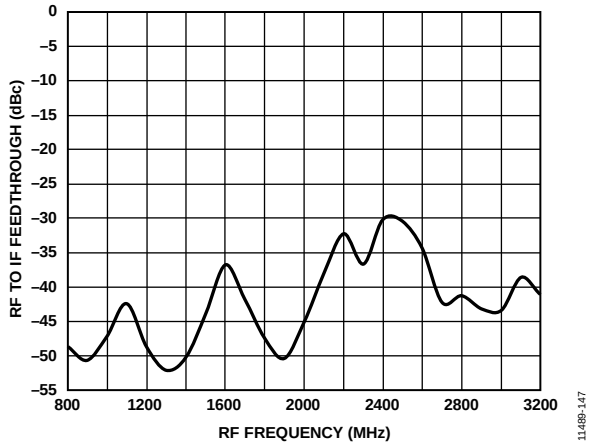

Figure 50. RF to IF Feedthrough at Mixer Output Without Filtering; Mixer Input Power = 0 dBm

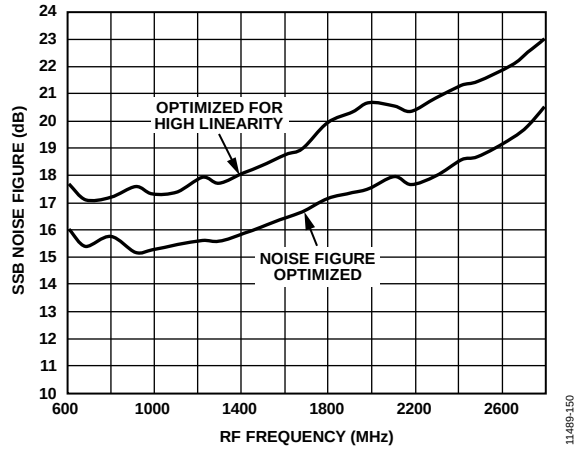

Figure 53. SSB Noise Figure vs. RF Frequency (see Table 16)

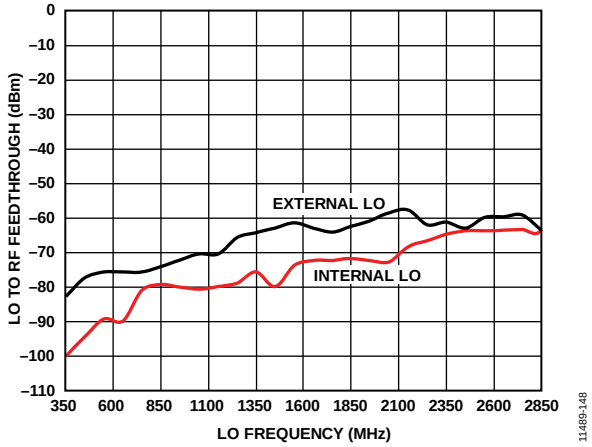

Figure 51. LO to RF Feedthrough; P_{LO} = 0 dBm

IF DGA

VCCx = 5 V, T_A = 25°C, R_S = R_L = 150 Ω, IF = 200 MHz, 2 V p-p differential output, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

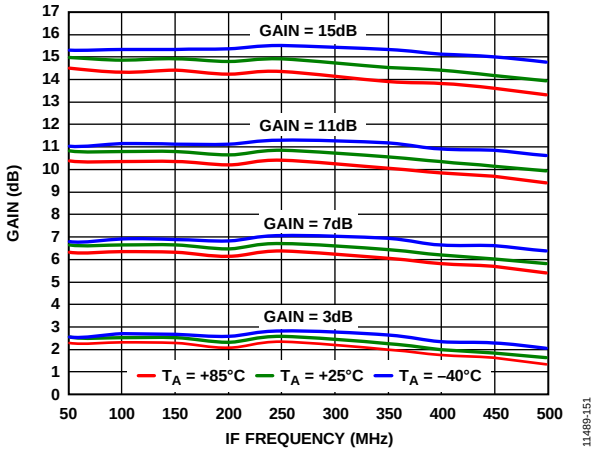

Figure 54. DGA Gain vs. IF Frequency and Temperature

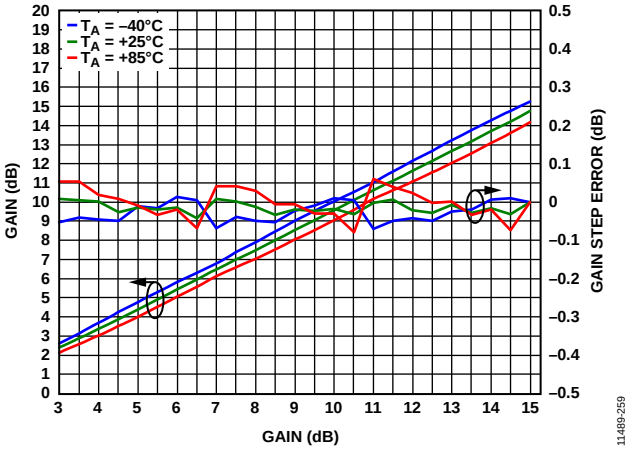

Figure 57. DGA Gain and Gain Step Error vs. Gain Setting and Temperature

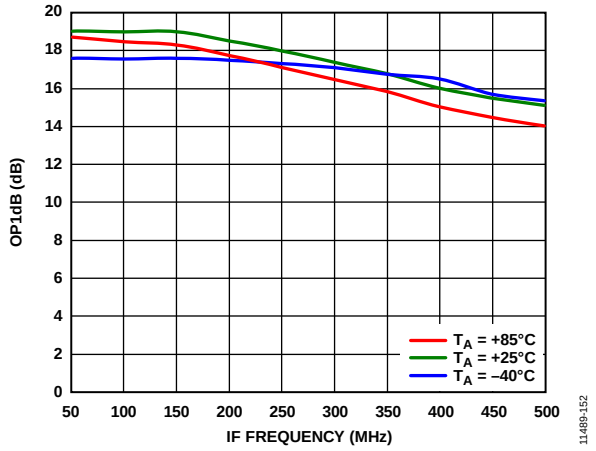

Figure 55. DGA OP1dB vs. Frequency and Temperature; Maximum Gain

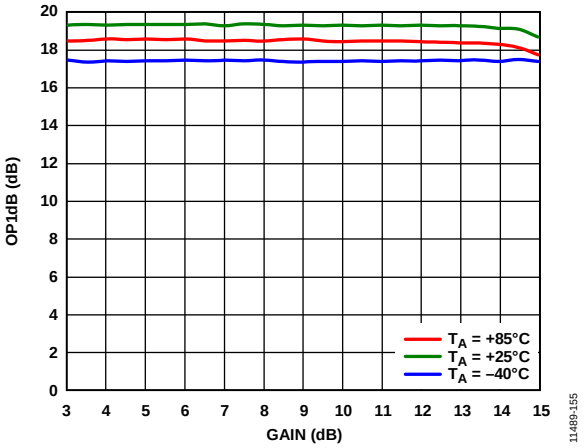

Figure 58. DGA OP1dB vs. Gain Setting and Temperature

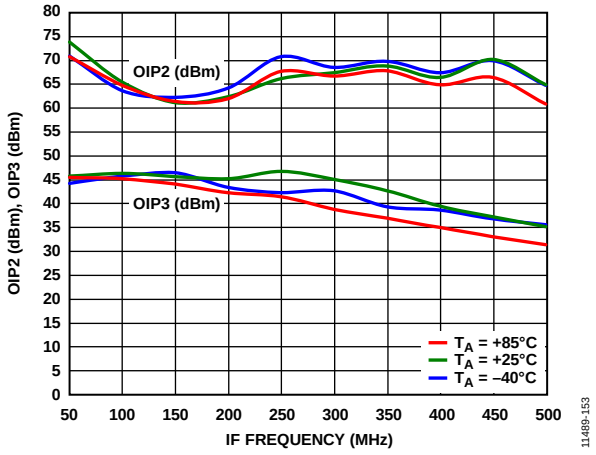

Figure 56. DGA OIP2/OIP3 vs. IF Frequency and Temperature; Maximum Gain

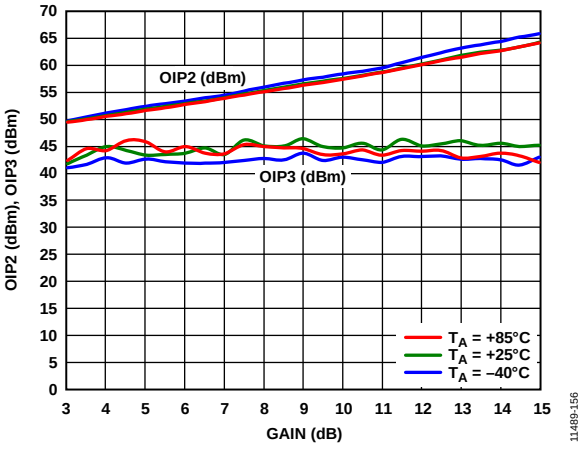

Figure 59. DGA OIP2/OIP3 vs. Gain Setting and Temperature

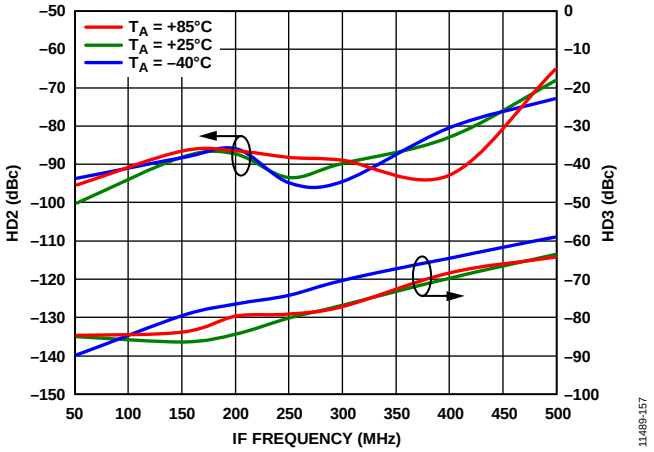

Figure 60. DGA HD2/HD3 vs. IF Frequency and Temperature; Maximum Gain

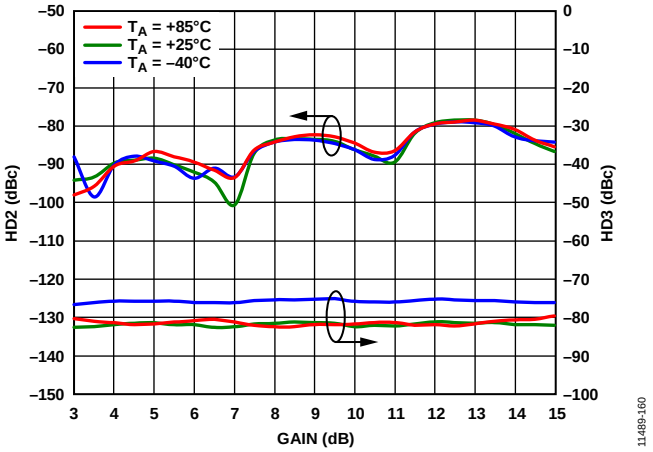

Figure 63. DGA HD2/HD3 vs. Gain Setting and Temperature

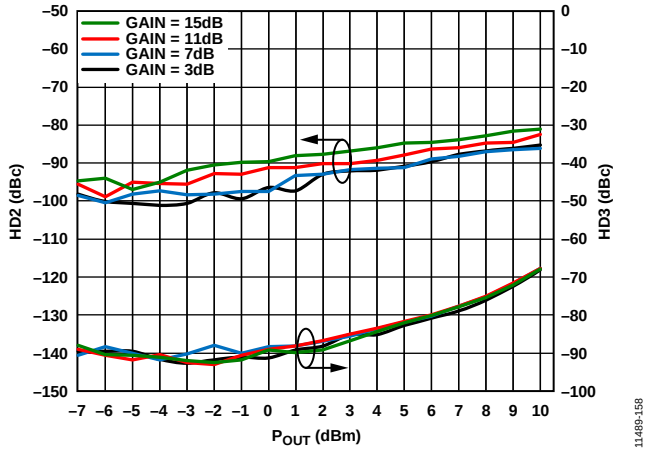

Figure 61. DGA HD2/HD3 vs. Output Power (P_{OUT}) and Gain Setting

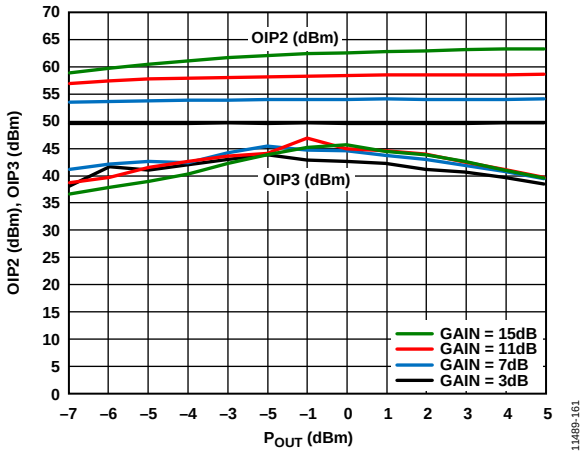

Figure 64. DGA OIP2/OIP3 vs. Output Power (P_{OUT}) and Gain Setting

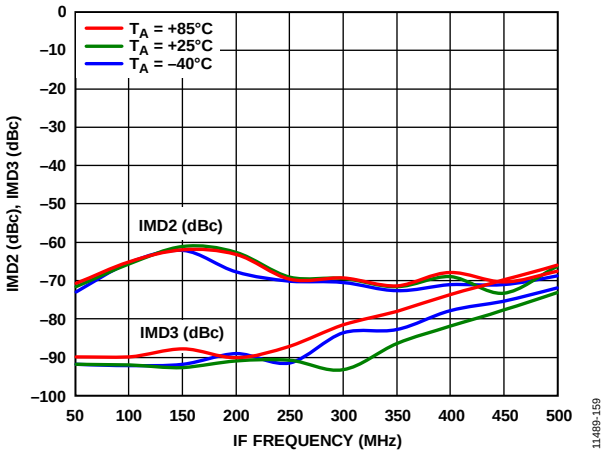

Figure 62. DGA IMD2/IMD3 vs. IF Frequency and Temperature; Maximum Gain

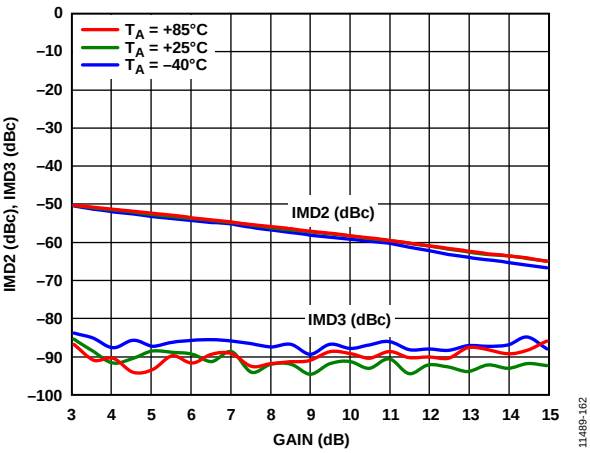

Figure 65. DGA IMD2/IMD3 vs. Gain Setting

SPURIOUS PERFORMANCE

$(N \times f_{RF}) - (M \times f_{LO})$ spur measurements were made using the standard evaluation board. Mixer spurious products were measured in decibels (dB) relative to the carrier (dBc) from the IF output power level. Data is shown for all spurious components greater than −115 dBc and frequencies of less than 3 GHz.

915 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 914 MHz, f_{LO} = 1114 MHz

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−34	−35				
	1	−43	0	−52	−16			
	2	−72	−60	−72	−67	−74		
	3	−102	−73	−103	−78	<−115	−80	
	4		−102	<−115	<−115	<−115	<−115	
	5			<−115	−105	<−115	<−115	<−115
	6				<−115	<−115	<−115	<−115

1910 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 1910 MHz, f_{LO} = 2110 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−38.208					
	1	−40.462	−0.001	−50.9				
	2		−59.208	−69.655	−62.35			
	3			−106.741	−74.322	−106.429		
	4				<−115	<−115	<−115	
	5				<−115	<−115	−110.954	
	6						<−115	<−115

2140 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 2140 MHz, f_{LO} = 2340 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−40					
	1	−36	0	−45				
	2		−58	−67	−59			
	3			<−115	−74	<−115		
	4				<−115	<−115	<−115	
	5					<−115	<−115	<−115
	6						<−115	<−115

2700 MHz Performance

VCCx = 5 V, T_A = 25°C, RF power = 0 dBm, internal LO, f_{RF} = 2700 MHz, f_{LO} = 2500 MHz.

		M						
		0	**1**	**2**	**3**	**4**	**5**	**6**
N	**0**		−38.613					
	1	−40.126	−0.001	−43.84				
	2		−58.299	−67.06	−62.116			
	3				−73.603	<−115		
	4					<−115	<−115	
	5						<−115	<−115
	6							<−115

THEORY OF OPERATION

The ADRF6620 integrates the essential elements of a multi-channel loopback receiver that is typically used in digital predistortion systems. The main features of the ADRF6620 include a single-pole four throw (SP4T) RF input switch with tunable balun, variable attenuation, a wideband active mixer, and digitally programmable variable gain amplifier (DGA). In addition, the ADRF6620 integrates a local oscillator (LO) generation block consisting of a synthesizer and a multicore voltage controlled oscillator (VCO) with an octave range and low phase noise. The synthesizer uses a fractional-N phase-locked loop (PLL) to enable continuous LO coverage from 350 MHz to 2850 MHz.

Putting all the building blocks of the ADRF6620 together, the signal path through the device starts at the RF input, where one of four single-ended RF inputs is selected by the input mux and converted to a differential signal via a tunable balun. The differential RF signal is attenuated to an optimal input level via the digital step attenuator with 15 dB of attenuation range in steps of 1 dB. The RF signal is then mixed via a Gilbert cell mixer with the LO signal down to an IF frequency. The 255 Ω terminated differential output of the mixer is brought off chip to a pair of inductors and passed through an IF filter. The output of the IF filter is ac-coupled off chip and fed to an on-chip digital attenuator and IF DGA. The output of the IF DGA is then passed to an off-chip analog-to-digital converter (ADC).

RF INPUT SWITCHES

The ADRF6620 integrates a SP4T switch where one of four RF inputs is selected. The desired RF input can be selected using either pin control or register writes via the SPI. Compared to the serial write approach, pin control allows faster control over the switch. When the RFSW0 pin (Pin 38) and the RFSW1 pin (Pin 39) are used, the RF switches can switch at speeds of up to 100 ns. When serial port control is used, the switch time is 100 ns, plus the latency of the SPI programming.

The RFSW_MUX bit (Register 0x23, Bit 11) selects whether the RF input switch is controlled via the external pins or the SPI port. By default at power-up, the device is configured for serial control. Writing to the RFSW_SEL bits (Register 0x23, Bits[10:9]) allows selection of one of the four RF inputs. Alternatively, by setting the RFSW_MUX bit high, the RFSW0 and RFSW1 pins can be used to select the RF input. Table 10 summarizes the different control options for the RF inputs.

To maintain good channel-to-channel isolation, ensure that unused RF inputs are properly terminated. The RFINx ports are internally terminated with 50 Ω resistors and have a dc bias level of 2.5 V. To avoid disrupting the dc level, the recommended termination is a dc blocking capacitor to GND. Figure 66 shows the recommended configuration when only RFIN0 is used, and the other RF input ports are properly terminated.

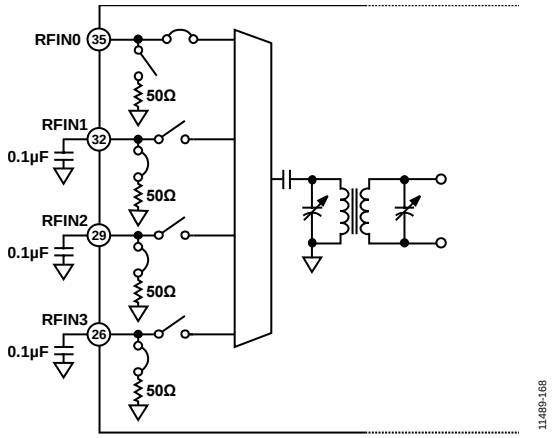

Figure 66. Terminating Unused RF Input Ports

Table 10. RF Input Selection Table

RFSW_MUX (Register Address 0x23[11])	SPI Control, RFSW_SEL (Register Address 0x23[10:9])		Pin Control		
Bit 11	**Bit 10**	**Bit 9**	**RFSW1, Pin 39**	**RFSW0, Pin 38**	**RF Input**
0	0	0	X[1]	X[1]	RFIN0
0	0	1	X[1]	X[1]	RFIN1
0	1	0	X[1]	X[1]	RFIN2
0	1	1	X[1]	X[1]	RFIN3
1	X[1]	X[1]	0	0	RFIN0
1	X[1]	X[1]	0	1	RFIN1
1	X[1]	X[1]	1	0	RFIN2
1	X[1]	X[1]	1	1	RFIN3

[1] X = don't care.

TUNABLE BALUN

The ADRF6620 integrates a programmable balun operating over a frequency range from 700 MHz to 2700 MHz. The tunable balun offers the benefit of ease of drivability from a single-ended 50 Ω RF input, and the single-ended-to-differential conversion of the balun optimizes common-mode rejection.

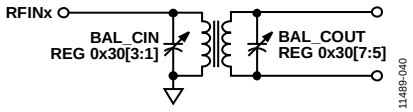

Figure 67. Integrated Tunable Balun

The RF balun is tuned by switching parallel capacitances on the primary and secondary sides by writing to Register 0x30. The added capacitance, in parallel with the inductive windings of the balun, changes the resonant frequency of the inductive capacitive (LC) tank. Therefore, selecting the proper combination of BAL_CIN (Register 0x30, Bits[3:1]) and BAL_COUT (Register 0x30, Bits[7:5]) sets the desired frequency and minimizes the insertion loss of the balun. Under most circumstances, the input and output can be tuned together; however, sometimes for matching reasons, it may be advantageous to tune them separately. See the RF Input Balun Insertion Loss Optimization section for the recommended BAL_CIN and BAL_COUT settings.

RF DIGITAL STEP ATTENUATOR (DSA)

The RF DSA follows the tunable balun. The attenuation range is 0 dB to 15 dB with a step size of 1 dB. DSA attenuation is set using the RFDSA_SEL bits (Register 0x23, Bits[8:5]).

ACTIVE MIXER

The double balanced mixer uses high performance SiGe NPN transistors. This mixer is based on the Gilbert cell design of four cross-connected transistors.

The mixer output has a 255 Ω differential output resistance. Bias the mixer outputs using either a pair of supply referenced RF chokes or an output transformer with the center tap connected to the positive supply.

DIGITALLY PROGRAMMABLE VARIABLE GAIN AMPLIFIER (DGA)

The ADRF6620 integrates a differential IF DGA consisting of a 150 Ω digitally controlled passive attenuator followed by a highly linear transconductance amplifier with feedback. The attenuation range is 12 dB, and the transconductor amplifier has a fixed gain of 15 dB. Therefore, at minimum attenuation, the gain of the IF DGA is 15 dB; at maximum attenuation, the gain is 3 dB. The attenuation is controlled by addressing the IF_ATTN bits in Register 0x23, Bits[4:0]. The attenuation step size is 0.5 dB.

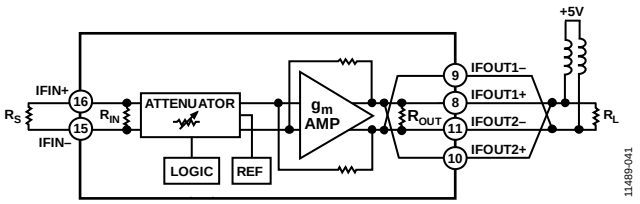

Figure 68. Simplified IF DGA Schematic

An independent internal voltage reference circuit sets the dc voltage level at the input of the amplifier to approximately 1.5 V. This reference is not accessible and cannot be adjusted.

The IF DGA consumes 35 mA through the VCC2 pin (Pin 12) and 75 mA through the two output choke inductors. The IF DGA can be powered down by disabling the IF_AMP_EN bit (Register 0x01, Bit 11). In its power-down state, the IF DGA current reduces to 6 mA. The dc bias level at the input remains at approximately 1.5 V when the DGA is disabled.

At minimum attenuation, the gain of the IF DGA is 15 dB when driving a 150 Ω load. The source and load resistance of the amplifier is set to 150 Ω in a matched condition. If the load or the source resistance is not equal to 150 Ω, the following equations can be used to determine the resulting gain and input/output resistances.

$$Voltage\ Gain = A_V = 0.044 \times (1000||R_L)$$

$$R_{IN} = (1000 + R_L)/(1 + 0.044 \times R_L)$$

$$S21\ (Gain) = 2 \times R_{IN}/(R_{IN} + R_S) \times A_V$$

$$R_{OUT} = (1000 + R_S)/(1 + 0.044 \times R_S)$$

The dc current to the outputs of each amplifier is supplied through two external choke inductors. The inductance of the chokes and the resistance of the load, in parallel with the output resistance of the device, add a low frequency pole to the response. The parasitic capacitance of the chokes adds to the output capacitance of the part. This total capacitance, in parallel with the load and output resistance, sets the high frequency pole of the device. In general, the larger the inductance of the choke, the higher the parasitic capacitance. Therefore, this trade-off must be considered when the value and type of the choke are selected.

For each polarity, the amplifier has two output pins that are oriented in an alternating fashion: IFOUT1+ (Pin 8), IFOUT1– (Pin 9), IFOUT2+ (Pin 10), and IFOUT2– (Pin 11). When designing the board, minimize the parasitic capacitance caused by routing the corresponding outputs together. See the Layout section for the recommended printed circuit board (PCB) layout.

LO GENERATION BLOCK

The ADRF6620 offers two modes for sourcing the LO signal to the mixer. The first mode uses the on-chip PLL and VCO. This mode of operation provides a high quality LO that meets the performance requirements of most applications. Using the on-chip synthesizer and VCO removes the burden of generating and distributing a high frequency LO signal.

The second mode bypasses the integrated LO generation block and allows the LO to be supplied externally. This second mode can provide a very high quality signal directly to the mixer core. Sourcing the LO signal externally may be necessary in demanding applications that require the lowest possible phase noise performance.

External LO Mode

External or internal LO mode can be selected via the VCO_SEL bits (Register 0x22, Bits[2:0]). To configure for external LO mode, set Register 0x22, Bits[2:0] to 011 and apply the differential LO signals to Pin 44 (LOIN−) and Pin 45 (LOIN+). The external LO frequency range is 350 MHz to 3.2 GHz. The ADRF6620 offers the flexibility of using a higher LO frequency signal and dividing it down before it drives the mixer. The LO divider can be found in the LO_DIV_A bits (Register 0x22, Bits[4:3]), where options include ÷1, ÷2, ÷4, or ÷8.

The external LO input pins present a broadband differential 50 Ω input impedance. The LOIN+ and LOIN− input pins must be ac-coupled. When not in use, LOIN+ and LOIN− can be left unconnected.

Internal LO Mode

The ADRF6620 includes an on-chip VCO and PLL for LO synthesis. The PLL, shown in Figure 69, consists of a reference input, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and divides it down by a factor of 1, 2, 4, or 8 or multiplies it by a factor of 2 before passing it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends an up/down signal to the charge pump if the VCO signal is slow/fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (VTUNE).

The ADRF6620 integrates three VCO cores that cover an octave range from 2.8 GHz to 5.7 GHz. Table 11 summarizes the frequency range for each VCO. The desired VCO can be selected by addressing the VCO_SEL bits (Register 0x22, Bits[2:0]).

Table 11. VCO Range

VCO_SEL (Register 0x22, Bits[2:0])	Frequency Range (GHz)
000	5.2 to 5.7
001	4.1 to 5.2
010	2.8 to 4.1
011	External LO

The N-divider divides down the differential VCO signal to the PFD frequency. The N-divider can be configured for fractional mode or integer mode by addressing the DIV_MODE bit (Register 0x02, Bit 11). The default configuration is set for fractional mode.

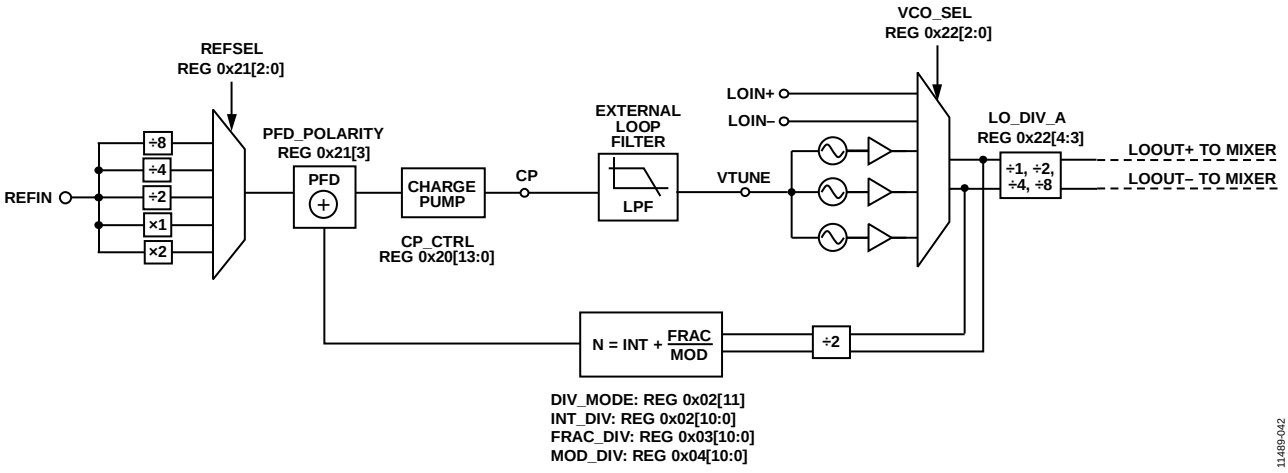

Figure 69. LO Generation Block Diagram

The following equations can be used to determine the N value and PLL frequency:

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{f_{PFD} \times 2 \times N}{LO_DIVIDER}$$

where:
f_{PFD} is the phase frequency detector frequency.
f_{VCO} is the voltage controlled oscillator frequency.
N is the fractional divide ratio (INT + FRAC/MOD)
INT is the integer divide ratio programmed in Register 0x02.
FRAC is the fractional divider programmed in Register 0x03.
MOD is the modulus divide ratio programmed in Register 0x04.
f_{LO} is the LO frequency going to the mixer core when the loop is locked.
LO_DIVIDER is the final divider block that divides the VCO frequency down by 1, 2, 4, or 8 before it reaches the mixer (see Table 12). This control is located in the LO_DIV_A bits (Register 0x22, Bits[4:3]).

Table 12. LO Divider

LO_DIV_A (Register 0x22, Bits[4:3])	LO_DIVIDER
00	1
01	2
10	4
11	8

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin; a logic high indicates that the loop is locked. The MUXOUT pin is controlled by the REF_MUX_SEL bits (Register 0x21, Bits[6:4]); the PLL lock detect signal is the default configuration.

To ensure that the PLL locks to the desired frequency, follow the proper write sequence of the PLL registers. The PLL registers must be configured accordingly to achieve the desired frequency, and the last writes must be to Register 0x02 (INT_DIV), Register 0x03 (FRAC_DIV), or Register 0x04 (MOD_DIV). When one of these registers is programmed, an internal VCO calibration is initiated, which is the last step in locking the PLL.

The time it takes to lock the PLL after the last register is written can be broken down into two parts: VCO band calibration and loop settling.

After the last register is written, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration takes approximately 5120 PFD cycles. For a 40 MHz f_{PFD}, this corresponds to 128 µs. After calibration is complete, the feedback action of the PLL causes the VCO to eventually lock to the correct frequency. The speed with which this locking occurs depends on the nonlinear cycle-slipping behavior, as well as the small-signal settling of the loop. For an accurate estimation of the lock time, download the ADIsimPLL tool, which correctly captures these effects. In general, higher bandwidth loops tend to lock more quickly than lower bandwidth loops.

Additional LO Controls

To access the LO signal going to the mixer core through the LOOUT+ and LOOUT− pins (Pin 21 and Pin 22), enable the LO_DRV_EN bit in Register 0x01, Bit 7. This setting offers direct monitoring of the LO signal to the mixer for debug purposes; or the LO signal can be used to daisy-chain many devices synchronously. One ADRF6620 can serve as the master where the LO signal is sourced, and the subsequent slave devices share the same LO signal from the master. This flexibility substantially eases the LO requirements of a system with multiple LOs.

The LO output drive level is controlled by the LO_DRV_LVL bits (Register 0x22, Bits[8:7]). Table 13 shows the available drive levels.

Table 13. LO Drive Level

LO_DRV_LVL (Register 0x22, Bits[8:7])	Amplitude (dBm)
00	−4
01	0.5
10	3
11	4.5

SERIAL PORT INTERFACE (SPI)

The SPI port of the ADRF6620 allows the user to configure the device through a structured register space provided inside the chip. Registers are accessed via the serial port interface and can be written to or read from via the serial port interface.

The serial port interface consists of three control lines: SCLK, SDIO, and $\overline{CS}$. SCLK (serial clock) is the serial shift clock. The SCLK signal clocks data on its rising edge. SDIO (serial data input/output) is an input or output depending on the instruction being sent and the relative position in the timing frame. $\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the frame. All SCLK and SDIO activity is ignored when $\overline{CS}$ is high. Table 6 and Figure 2 show the serial timing and its definitions.

The ADRF6620 protocol consists of seven register address bits, followed by a read/write indicator and 16 data bits. Both the address and data fields are organized from MSB to LSB.

On a write cycle, up to 16 bits of serial write data are shifted in, MSB to LSB. If the rising edge of $\overline{CS}$ occurs before the LSB of the serial data is latched, only the bits that were clocked in are written to the device. If more than 16 data bits are shifted in, the 16 most recent bits are written to the device. The ADRF6620 input logic level for the write cycle supports a logic level as low as 1.8 V.

On a read cycle, up to 16 bits of serial read data are shifted out, MSB to LSB. Data shifted out beyond 16 bits is undefined. It is not necessary for readback content at a given register address to correspond with the write data of the same address. The output logic level for a read cycle is 2.5 V.

BASIC CONNECTIONS

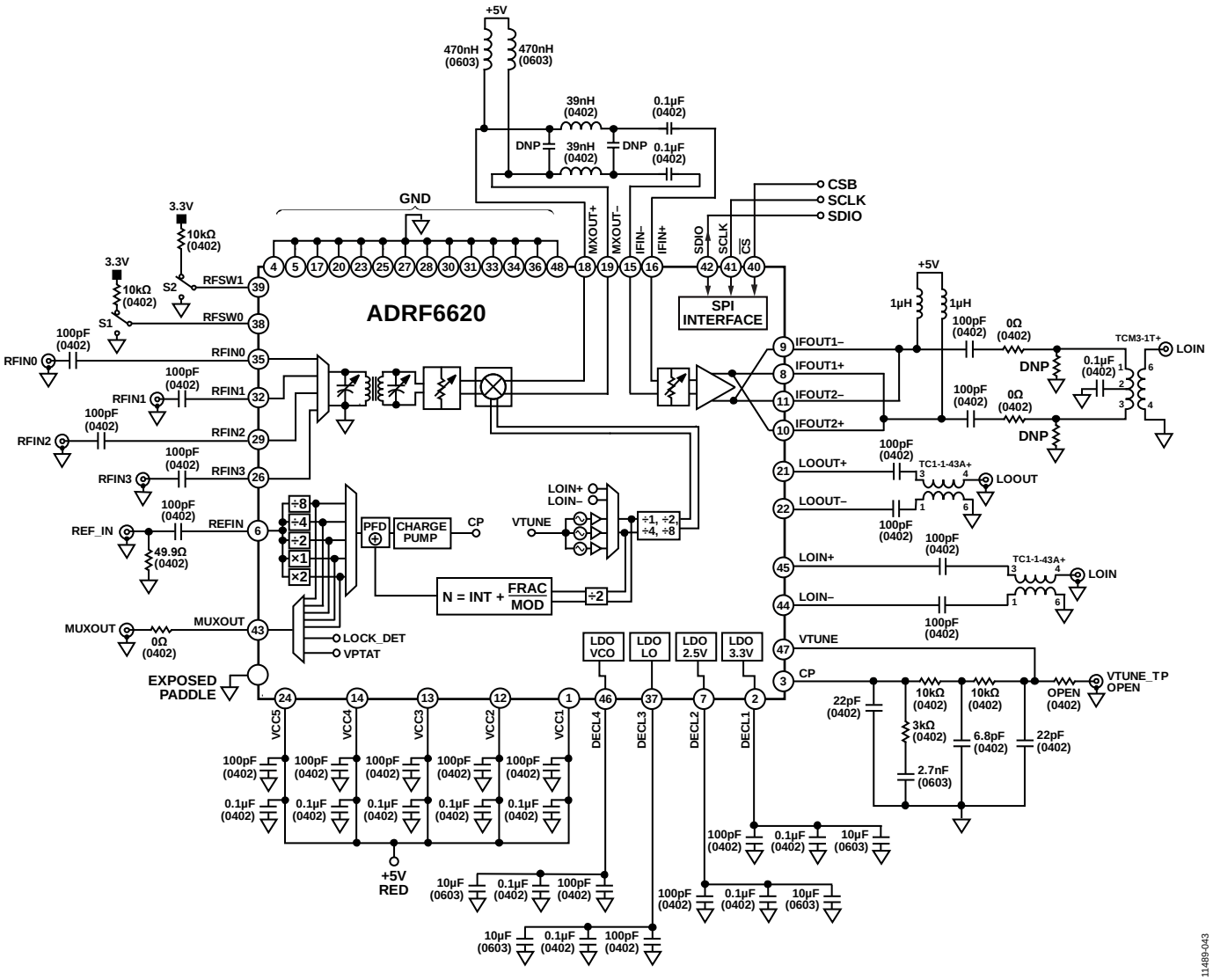

Figure 70. Basic Connection Diagram

Table 14. Basic Connections

Pin No.	Mnemonic	Description	Basic Connection
5 V Power			
1	VCC1	LO, VCO, mixer power supply	Decouple all power supply pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins.
12	VCC2	IF DGA power supply	
13	VCC3	Factory calibration pin	
14	VCC4	Factory calibration pin	
24	VCC5	RF front-end power supply	
PLL/VCO			
3	CP	Synthesizer charge pump output	Connect this pin to the VTUNE pin through the loop filter.
6	REFIN	Synthesizer reference frequency input	The nominal input level of this pin is 1 V p-p. The input range is 12 MHz to 464 MHz. This pin is internally biased and must be ac-coupled and terminated externally with a 50 Ω resistor. Place the ac coupling capacitor between the pin and the resistor. When driven from an 50 Ω RF signal generator, the recommended input level is 4 dBm.
21, 22	LOOUT+, LOOUT–	Differential LO outputs	The differential output impedance of these pins is 50 Ω. The pins

Pin No.	Mnemonic	Description	Basic Connection
			are internally biased to 2.5 V and must be ac-coupled.
44, 45	LOIN−, LOIN+	Differential LO inputs	The differential input impedance of these pins is 50 Ω. The pins are internally biased to 2.5 V and must be ac-coupled.
43	MUXOUT	PLL multiplex output	This output pin provides the PLL reference signal or the PLL lock detect signal.
47	VTUNE	VCO tuning voltage	This pin is driven by the output of the loop filter; its nominal input voltage range is 1.5 V to 2.5 V.
RF Inputs			
26, 29, 32, 35	RFIN3, RFIN2 RFIN1, RFIN0	RF inputs	The single-ended RF inputs have a 50 Ω input impedance and are internally biased to 2.5 V. These pins must be ac-coupled. Terminate unused RF inputs with a dc blocking capacitor to GND to improve isolation. Refer to the Layout section for the recommended PCB layout for optimized channel-to-channel isolation.
38, 39	RFSW0, RFSW1	Pin control of the RF inputs	See Table 10 for the pin settings for RF input pin control. For logic high, connect these pins to 2.5 V logic.
IF DGA			
8, 9, 10, 11	IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−	IF DGA outputs	The differential IF DGA outputs have two output pins for each polarity. They are oriented in alternating fashion: IFOUT1+ (Pin 8), IFOUT1− (Pin 9), IFOUT2+ (Pin 10), and IFOUT2− (Pin 11). Connect the positive pins such that IFOUT1+ and IFOUT2+ are tied together. Similarly, connect the negative pins such that IFOUT1− and IFOUT2− are tied together. Refer to the Layout section for a recommended layout that minimizes parasitic capacitance and optimizes on performance. The output stage of the IF DAG is an open-collector configuration that requires a dc bias of 5 V. Use bias choke inductors to achieve this configuration. Choose the bias choke inductors such that they can handle a maximum current of 50 mA on each side. By design, the IF DGA is optimized for linearity when the source and load are terminated with 150 Ω.
15, 16	IFIN−, IFIN+	IF DGA inputs	AC couple the mixer outputs to the IF DGA inputs. See the Interstage Filtering Requirements section for the recommended filter designs.
Mixer Outputs			
18, 19	MXOUT+, MXOUT−	Differential mixer outputs	The output stage of the mixer is an open collector configuration that requires a dc bias of 5 V. Use bias choke inductors to achieve this configuration. Carefully choose the bias choke inductors such that they can handle a maximum current of 50 mA on each side. The differential output impedance of the mixer is 255 Ω.
Serial Port Interface			
40	$\overline{CS}$	SPI chip select	Active low. 3.3 V logic levels.
41	SCLK	SPI clock	3.3 V tolerant logic levels.
42	SDIO	SPI data input and output	3.3 V tolerant logic levels.
LDO Decoupling			
2	DECL1	3.3 V LDO decoupling	Decouple all DECLx pins to ground using 100 pF, 0.1 µF, and 10 µF capacitors. Place the decoupling capacitors close to the pin.
7	DECL2	2.5 V LDO decoupling	
37	DECL3	LO LDO decoupling	
46	DECL4	VCO LDO decoupling	
GND			
4, 5, 17, 20, 23, 25, 27, 28, 30, 31, 33, 34, 36, 48	GND	Ground	Connect these pins to the GND of the PCB.
49 (EPAD)		Exposed pad (EPAD)	The exposed thermal pad is on the bottom of the package. The exposed pad must be soldered to ground.

RF INPUT BALUN INSERTION LOSS OPTIMIZATION

As shown in Figure 71 to Figure 74, the gain of the ADRF6620 mixer has been characterized for every combination of BAL_CIN and BAL_COUT (Register 0x30). As shown, a range of BAL_CIN and BAL_COUT values can be used to optimize the gain of the ADRF6620. The optimized values do not change with temperature. After the values are chosen, the absolute gain changes over temperature; however, the signature of the BAL_CIN and BAL_COUT values is fixed.

At lower input frequencies, more capacitance is needed. This increase is achieved by programming higher codes into BAL_CIN and BAL_COUT. At high frequencies, less capacitance is required; therefore, lower BAL_CIN and BAL_COUT codes are appropriate. Table 16 provides a list of recomended BAL_CIN and BAL_COUT codes for popular radio frequencies. Use Figure 71 to Figure 74 and Table 16 only as guides; do not interpret them in the absolute sense because every application and PCB design varies. Additional fine-tuning may be necessary to achieve the maximum gain.

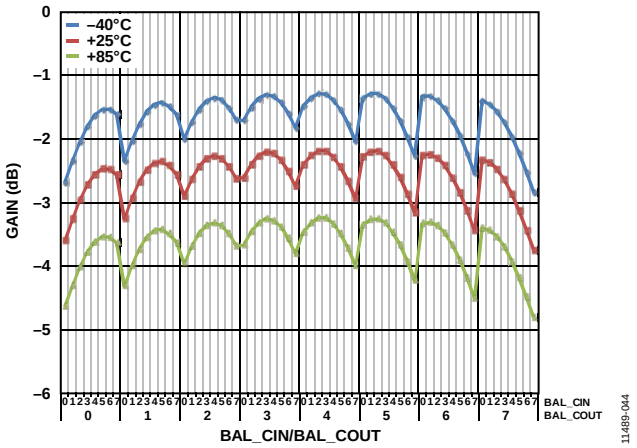

Figure 71. Gain vs. BAL_CIN and BAL_COUT at RF = 900 MHz

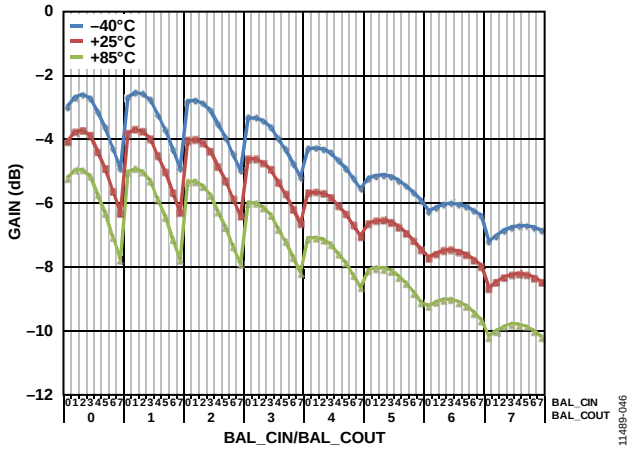

Figure 72. Gain vs. BAL_CIN and BAL_COUT at RF = 2100 MHz

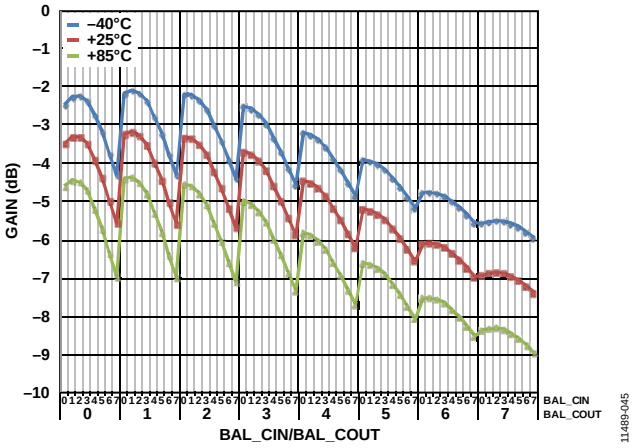

Figure 73. Gain vs. BAL_CIN and BAL_COUT at RF = 1900 MHz

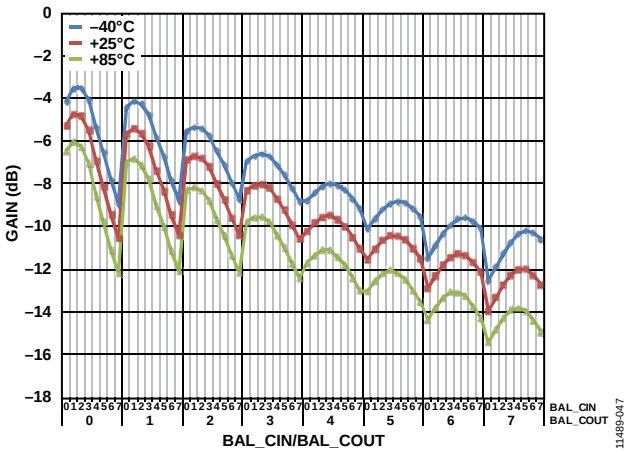

Figure 74. Gain vs. BAL_CIN and BAL_COUT at RF = 2700 MHz

IP3 AND NOISE FIGURE OPTIMIZATION

The ADRF6620 can be configured for either improved performance or reduced power consumption. In applications where performance is critical, the ADRF6620 offers IP3 or noise figure optimization. However, if power consumption is the priority, the mixer bias current can be reduced to save on the overall power at the expense of degraded performance. Whatever the application specific needs are, the ADRF6620 offers configurability that balances performance and power consumption.

Adjustments to the mixer bias setting have the most impact on performance and power. For this reason, mixer bias should be the first adjustment. The active mixer core of the ADRF6620 is a linearized transconductor. With increased bias current, the transconductor becomes more linear, resulting in higher IP3. The improved IP3, however, is at the expense of degraded noise figure and increased power consumption (see Figure 75). For a 1-bit change of the mixer bias (MIXER_BIAS, Register 0x31, Bits[11:9]), the current increases by 7.71 mA.

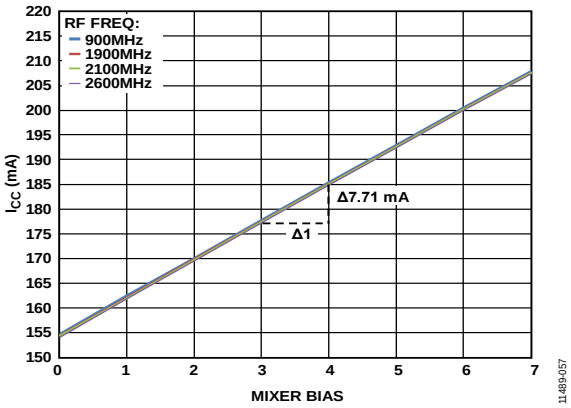

Figure 75. Change in Current Consumption vs. MIXER_BIAS

Inevitably, there is a limit on how much the bias current can increase before the improvement in linearity no longer justifies the increase in power and noise. The mixer core reaches a saturation point where further increases in bias current do not translate to improved performance. When that point is reached, it is best to decrease the bias current to a level where the desired performance is achieved. Depending on the system specifications of the customer, a balance between linearity, noise figure, and power can be attained.

In addition to bias optimization, the ADRF6620 also has configurable distortion cancellation circuitry. The linearized transconductor input of the ADRF6620 is made up of a main path and a secondary path. Through adjustments of the amplitude and phase of the secondary path, the distortion generated by the main path can be canceled, resulting in improved IPd3 performance. The amplitude and phase adjustments are located in the following serial interface bits: MIXER_RDAC (Register 0x31, Bits[8:5]) and MIXER_CDAC (Register 0x31, Bits[4:0]).

Figure 76 to Figure 83 show the IIP3 and noise figure sweeps for all MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS combinations. The IIP3 vs. MIXER_RDAC and MIXER_CDAC figures show both a surface and a contour plot in one figure. The contour plot is located directly underneath the surface plot. The best approach for reading the figure is to localize the peaks on the surface plot, which indicate maximum IIP3, and to follow the same color pattern to the contour plot to determine the optimized MIXER_RDAC and MIXER_CDAC values. The overall shape of the IIP3 plot does not vary with the MIXER_BIAS setting; therefore, only MIXER_BIAS = 011 is displayed.

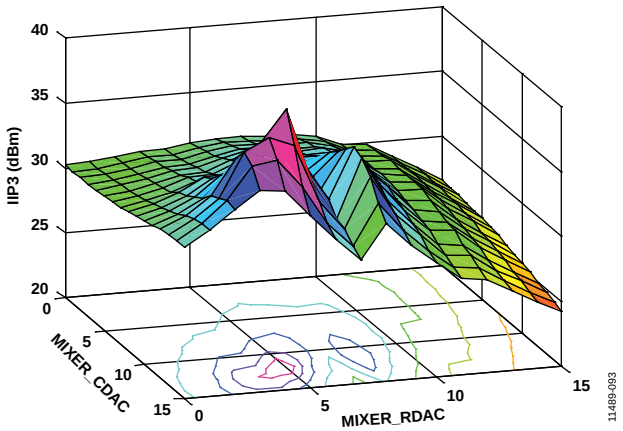

Figure 76. IIP3 vs. MIXER_RDAC, MIXER_CDAC; MIXER_BIAS = 011 at RF Frequency = 900 MHz

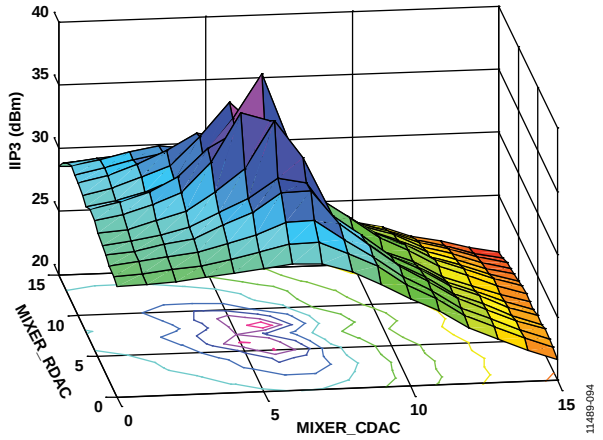

Figure 77. IIP3 vs. MIXER_RDAC, MIXER_CDAC; MIXER_BIAS = 011 at RF Frequency = 1900 MHz

The data shows that MIXER_BIAS has the largest impact on performance. As previously mentioned and evident in the data, IIP3 improves with increased MIXER_BIAS, and noise figure is optimized at the lowest bias setting. Taking a more detailed look at the data, the different MIXER_RDAC and MIXER_CDAC combinations can result in a ~5 dB to +10 dB change in IIP3, but the noise figure changes by only ~0.5 dB. These trends become very important in deciding the trade-offs between IP3, noise figure, and power consumption. The total current consumption of the ADRF6620 does not change with MIXER_RDAC and MIXER_CDAC and varies only with the mixer bias settings (see Figure 75).

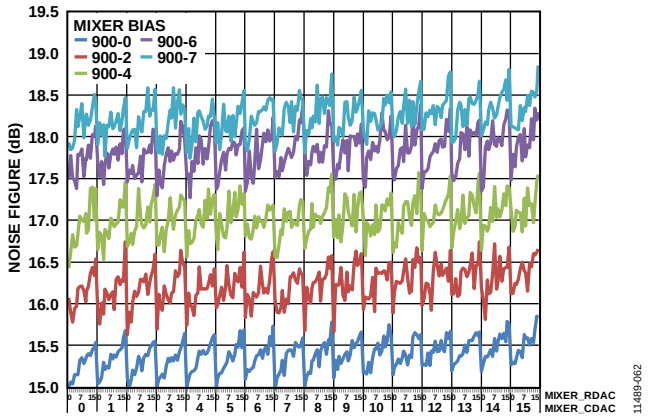

Figure 78. Noise Figure vs. MIXER_RDAC, MIXER_CDAC, and Various MIXER_BIAS Values at RF Frequency = 900 MHz

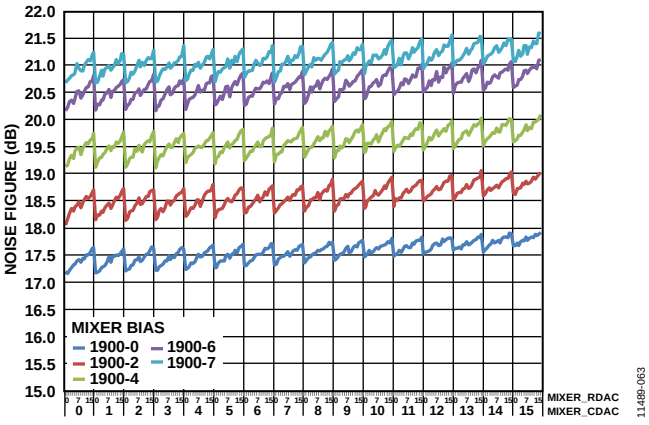

Figure 79. Noise Figure vs. MIXER_RDAC, MIXER_CDAC, and Various MIXER_BIAS Values at RF Frequency = 1900 MHz

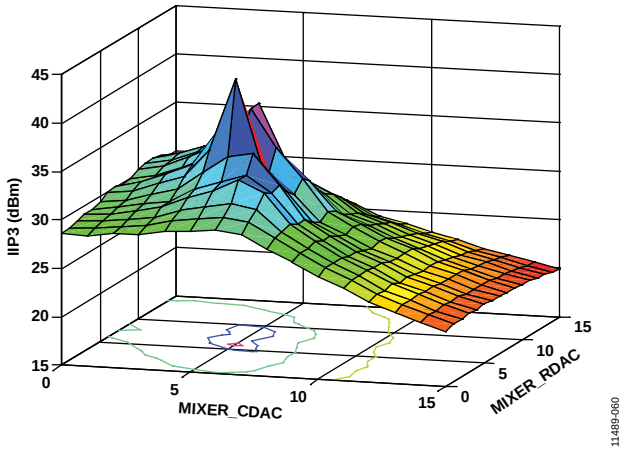

Figure 80. IIP3 vs. MIXER_RDAC, MIXER_CDAC; MIXER_BIAS = 011 at RF Frequency = 2100 MHz

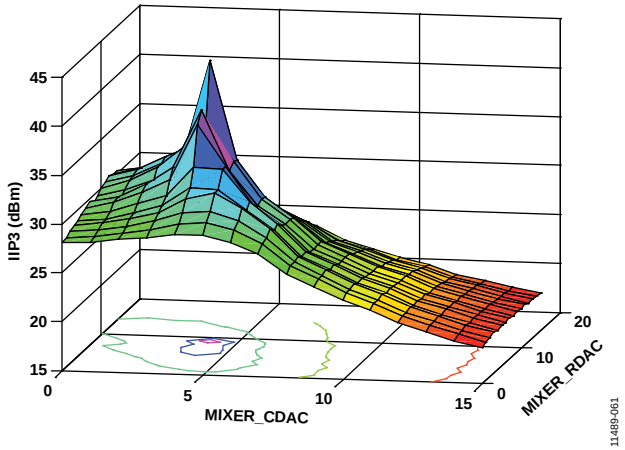

Figure 81. IIP3 vs. MIXER_RDAC, MIXER_CDAC; MIXER_BIAS = 011 at RF Frequency = 2700 MHz

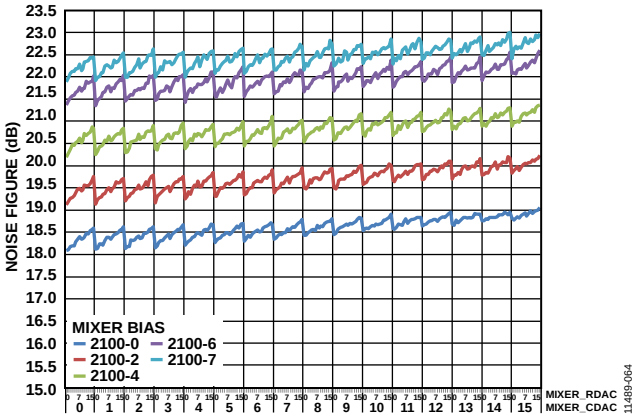

Figure 82. Noise Figure vs. MIXER_RDAC, MIXER_CDAC, and Various MIXER_BIAS Values at RF Frequency = 2100 MHz

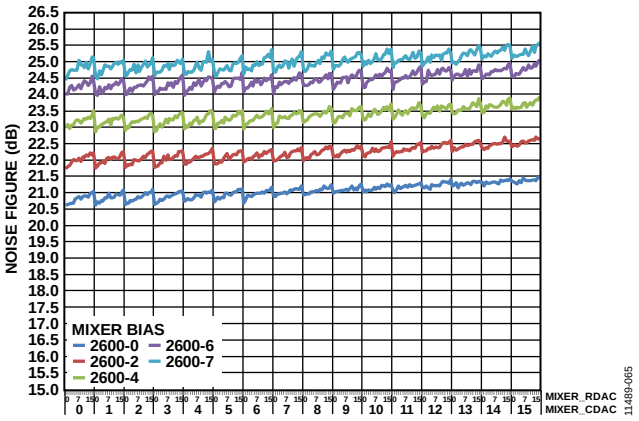

Figure 83. Noise Figure vs. MIXER_RDAC, MIXER_CDAC, and Various MIXER_BIAS Values at RF Frequency = 2700 MHz

As an example, the MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS settings of the ADRF6620 were carefully selected, based on three individual goals that resulted in three sets of MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS values. The first goal was for optimized IIP3. To achieve the most optimal IIP3 performance, the MIXER_BIAS was set to a higher current setting, and MIXER_RDAC and MIXER_CDAC were selected at the peaks. This configuration allowed for the most optimal IIP3 performance. However, it also consumed the most power, and the noise figure was degraded. The second goal was to achieve a balance among IIP3, the noise figure, and power consumption. Finally, the third goal was for an optimized noise figure. This configuration resulted in the lowest power consumption while IIP3 was not optimized. Table 15 summarizes the test conditions; Table 16 shows the corresponding MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS values. The resulting IIP3 and noise figure performance for the specific MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS settings are shown in Figure 84.

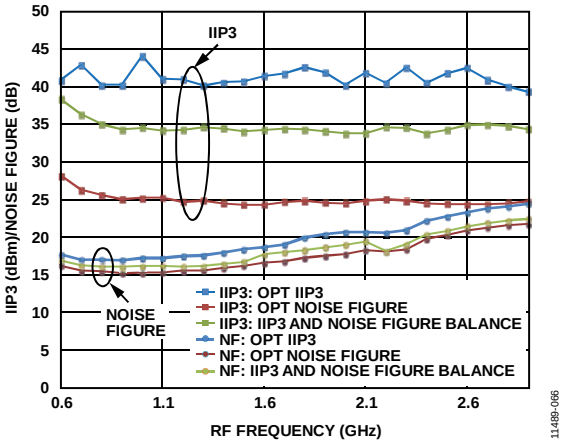

Figure 84. Example IIP3 and Noise Figure Optimization

Table 15. Mixer Optimization Summary

Parameter	Test Conditions/Comments
Optimized IIP3	MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS were configured for optimized IIP3 performance.
Noise Figure, IIP3, and Power Consumption Balance	MIXER_BIAS was limited to 0, 1, or 2 decimal for improved noise figure while allowing IIP3 to degrade. MIXER_RDAC and MIXER_CDAC were chosen for optimized IIP3 because MIXER_RDAC and MIXER_CDAC have a larger impact on IIP3 than on noise figure.
Optimized Noise Figure	MIXER_BIAS was set to 0 decimal for the best noise figure. MIXER_RDAC and MIXER_CDAC were chosen for optimized IIP3 because they have a larger impact on IIP3 than on noise figure.

Table 16. Recommended BAL_CIN, BAL_COUT, MIXER_RDAC, MIXER_CDAC, and MIXER_BIAS Settings (in Decimal)

RF Frequency (MHz)			Optimized IIP3			IIP3 and Noise Figure Balance			Optimized Noise Figure		
	BAL_CIN	BAL_COUT	RDAC	CDAC	BIAS	RDAC	CDAC	BIAS	RDAC	CDAC	BIAS
600	7	7	6	10	4	4	15	2	4	15	0
700	7	7	5	14	4	4	15	2	4	15	0
800	5	5	3	13	3	3	14	2	2	15	0
900	3	4	0	15	0	3	13	2	2	14	0
940	3	3	5	12	4	5	11	2	2	13	0
1000	2	3	5	11	4	4	10	2	3	11	0
1100	1	2	5	10	4	3	10	1	2	11	0
1200	1	2	5	9	4	3	9	1	2	10	0
1300	0	2	8	8	4	3	9	1	2	10	0
1400	0	2	6	7	4	4	8	1	2	9	0
1500	0	2	6	7	4	5	7	2	3	8	0
1600	0	2	8	7	4	5	7	2	2	8	0
1700	0	1	6	6	4	5	6	2	4	7	0
1800	0	1	9	6	4	5	6	2	4	7	0
1840	0	1	9	6	5	5	6	2	3	7	0
1900	0	1	9	6	5	6	5	2	3	7	0
2000	0	1	7	5	5	3	6	0	3	6	0
2100	1	1	9	5	5	5	5	1	3	6	0
2140	1	1	9	5	4	5	5	1	3	6	0
2200	2	0	7	4	4	5	5	1	3	6	0
2300	2	0	7	4	4	5	5	1	3	6	0
2400	1	0	7	4	4	5	5	1	3	6	0
2500	1	0	7	4	4	5	5	1	3	6	0
2600	1	0	7	4	4	5	5	1	3	6	0
2700	1	0	7	4	4	5	5	1	3	6	0
2800	1	0	7	4	4	4	15	2	4	15	0
2900	1	0	7	4	4	4	15	2	4	15	0
3000	0	0	7	4	4	3	14	2	2	15	0

INTERSTAGE FILTERING REQUIREMENTS

Filtering at the mixer output may be necessary for improved linearity performance. For applications where the frequency plan requires low RF frequency inputs and IF outputs, the resulting sum term at the mixer outputs, $f_{RF} + f_{LO}$, may fall within the band of interest. The unwanted sum term may cause the IF DGA to operate in its nonlinear region because of the unnecessary presence of additional signal power. As a result, the linearity performance degrades where OIP3 and OIP2 decrease substantially. For this reason, a low-pass filter is necessary to attenuate the unwanted signal while maintaining the integrity of the wanted signal within the band of interest. In addition, the low-pass filter serves to suppress the LO feedthrough. Because of the absence of blockers in a typical DPD receive application, a lower order filter, such as a third-order Chebyshev, is typically adequate.

The low-pass filter resides between the mixer outputs and the IF DGA inputs, as shown in Figure 85. The signal flow starts with the differential outputs of the mixer being dc biased to positive supply (5 V) via a pair of pull-up inductors, L1 and L2. The inductor value is determined by the low frequency cutoff of the signal band of interest. Next, the third-order low-pass filter attenuates the high frequency sum term. The combination of the pull-up inductors and the low-pass filter results in a band-pass filter profile. The outputs of the filter are then ac-coupled through series capacitors and routed to the on-chip IF DGA via the IFIN+ and IFIN− pins.

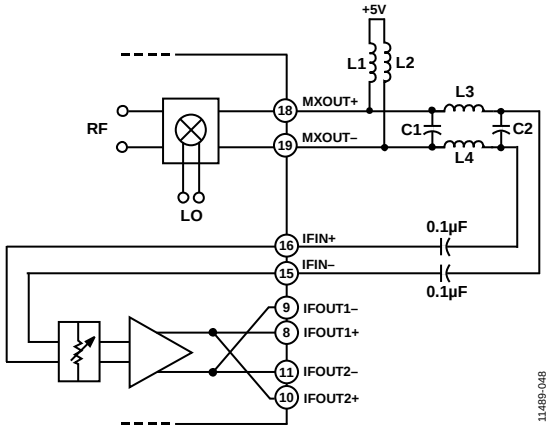

Figure 85. Low-Pass IF Filter

When designing the low-pass filter, it is important to consider the output impedance of the mixer and the input impedance of the IF DGA. The output impedance of the mixer has both a real and reactive component, and its equivalent model is shown in Figure 86. Correspondingly, Figure 87 shows the impedance vs. frequency for the mixer output.

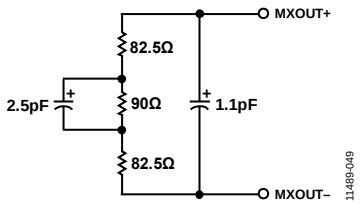

Figure 86. Equivalent Model of the Mixer Output Impedance

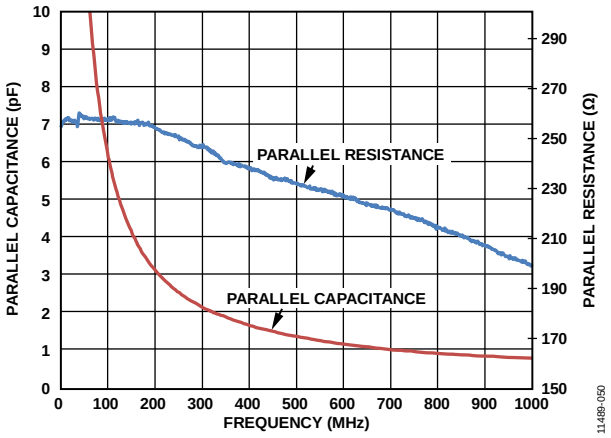

Figure 87. Mixer Output Impedance vs. Frequency

Likewise, Figure 88 shows the impedance vs. frequency for the IF DGA. The four-port S parameter files for the IF DGA and mixer are available on analog.com and can serve as a useful tool to accurately capture the input and output impedance when designing the interstage filter. As a first-order approximation at low frequencies, the mixer output has a fixed impedance of approximately 255 Ω, and the input impedance of the IF DAG is approximately 150 Ω. Therefore, design the low-pass filter to have an input impedance of 255 Ω and an output impedance of 150 Ω.

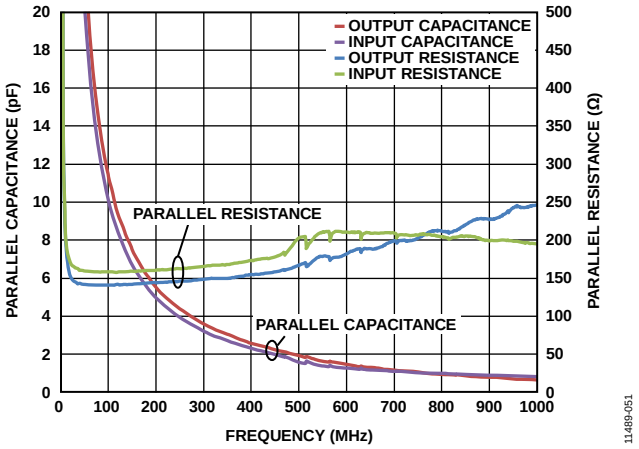

Figure 88. IF DGA Input/Output Impedance vs. Frequency

Most important, the low-pass interstage filter must attenuate the sum term ($f_{RF} + f_{LO}$) and LO feedthrough to prevent unnecessary overdrive of the DGA. The level of attenuation that is required to achieve optimal OIP3 performance is shown in Figure 89, where OIP3 vs. ($f_{RF} + f_{LO}$) amplitude is plotted. To maintain performance, attenuate the amplitude of the sum term to at least −16 dBm (see Figure 89). Beyond this point, the OIP3 degrades decibel per decibel for increased amplitudes.

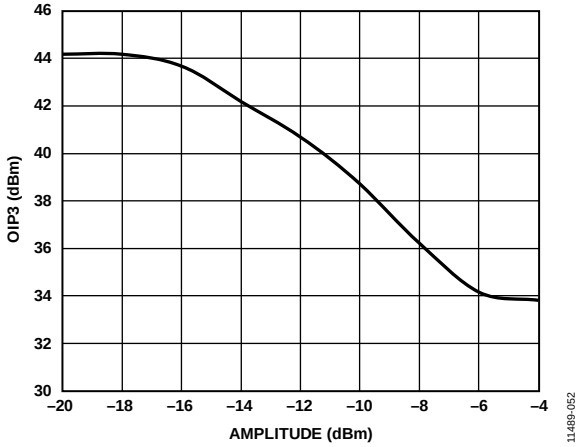

Figure 89. OIP3 vs. ($f_{RF} + f_{LO}$) Amplitude

The ADRF6620 is optimized for use in digital predistortion (DPD) receivers. An example filter design for DPD is shown in Figure 91. Table 17 lists the interstage filter design targets. In most DPD systems for cellular transmission, the pass band is between 50 MHz and 500 MHz. For this reason, the pull-up inductors have a low frequency cutoff of 50 MHz, and the pass-band edge of the interstage low-pass filter is 500 MHz. This results in a band-pass filter profile with a maximally flat pass band from 50 MHz to 500 MHz. The stop-band attenuation at 1400 MHz is 20 dB, which typically provides the necessary attenuation of the mixer sum term with some margin.

Table 17. Example Filter Design

Parameter	Value
R_S	255 Ω
R_L	150 Ω
Pass-Band Edge	500 MHz
Attenuation at Pass-Band Edge	0.5 dB
Stop-Band Edge	1400 MHz
Attenuation at Stop-Band Edge	20 dB
Filter Type	Third-order Chebyshev

Using filter equations from a textbook or filter design software, a third-order Chebyshev filter can be designed to satisfy all the specifications in Table 17, as shown in Figure 91. The mixer output capacitance of 1.1 pF can be absorbed into the filter, resulting in a reduction in C1 from 2 pF to 0.8 pF. In addition, depending on the PCB board stack-up, C2 can be further reduced, or eliminated, because the capacitance of the PCB board can be used as the third pole of the filter. The components used in the simulation were the Coilcraft 0805CS inductors and Murata GRM15 series capacitors. Figure 90 shows the filter profile that satisfies all the filter specifications in Table 17.

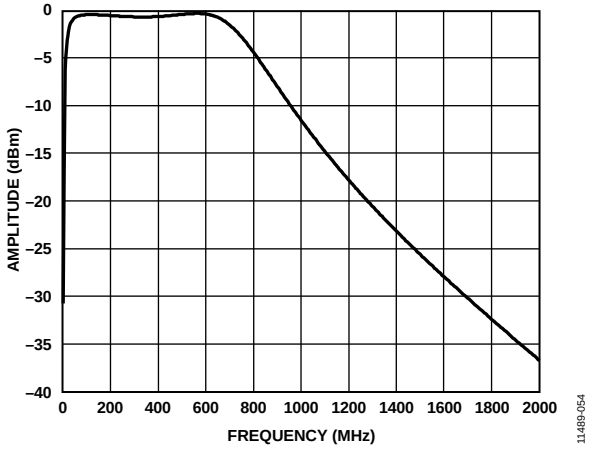

Figure 90. Third-Order Chebyshev Filter Profile

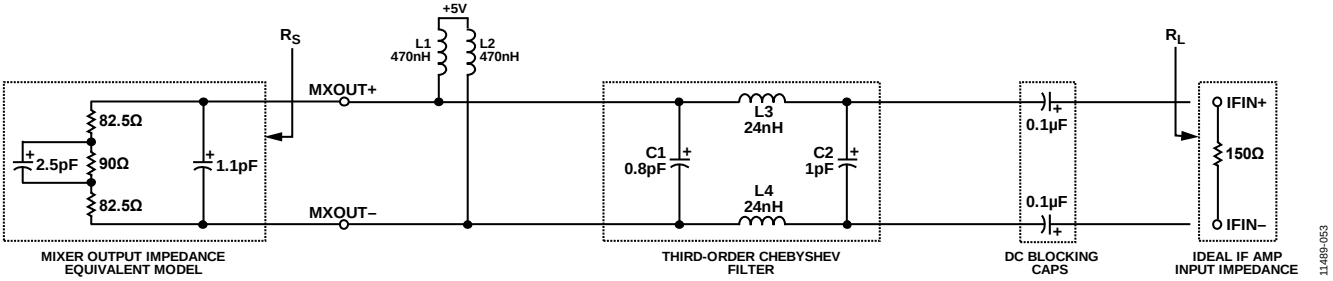

Figure 91. Low-Pass Interstage Filter Design

Maintaining the same third-order Chebyshev filter design shown in Figure 91, the component values can be tuned to optimize performance with some trade-offs. To achieve maximally flat pass-band response, the trade-off is signal bandwidth (see Figure 92). The L3 and L4 inductors are replaced with 47 nH, and the capacitors are not populated. This configuration results in the flattest pass-band ripple; however, the signal bandwidth starts to roll off at 300 MHz. A narrower bandwidth translates to more attenuation of the mixer sum and LO leakage, which is a desirable effect if the wider signal bandwidth is not a requirement. Use the results shown in Figure 92 only as a guide, and design the interstage filter to the specific PCB board conditions. The plots in Figure 92 were measured using the ADRF6620 evaluation board.

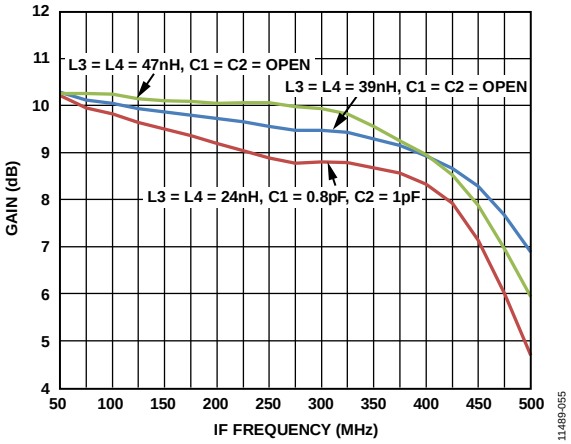

Figure 92. Interstage Filter Design Trade-Offs

Because the capacitance of the ADRF6620 evaluation board closely approximates the C1 and C2 capacitors, they can be removed from the design. However, this may not be the case for every PCB design with different stack-ups.

Figure 93 compares the OIP3 and OIP2 performance of the ADRF6620 with and without filtering at the mixer output.

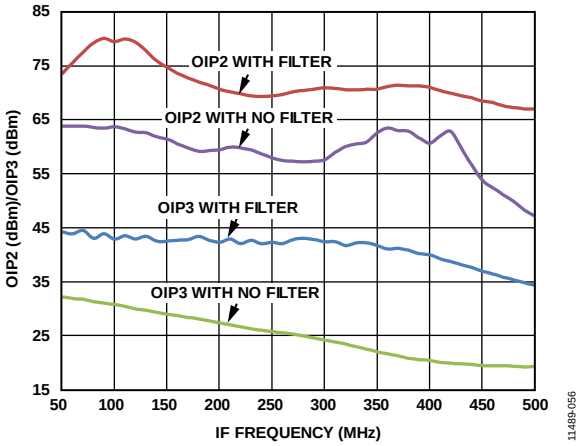

Figure 93. OIP2/OIP3 Performance With and Without Filtering at the DGA Output; RF Frequency = 900 MHz; High-Side LO Injection, LO Sweep

IF DGA VS. LOAD

By design, the IF DGA is optimized for performance in a matched condition where the source and load resistances are both 150 Ω. If the load or the source resistance is not equal to 150 Ω (see the Digitally Programmable Variable Gain Amplifier (DGA) section), use the following equations to determine the resulting gain and input/output resistances:

$$Voltage\ Gain = A_V = 0.044 \times (1000||R_L)$$

$$R_{IN} = (1000 + R_L)/(1 + 0.044 \times R_L)$$

$$S21\ (Gain) = 2 \times R_{IN}/(R_{IN} + R_S) \times A_V$$

$$R_{OUT} = (1000 + R_S)/(1 + 0.044 \times R_S)$$

In a configuration where the mixer outputs of the ADRF6620 are routed to the IF DGA inputs, the matched condition is no longer satisfied because the source impedance, as seen by the IF DGA, is the 255 Ω output impedance of the mixer outputs. As a result, the gain and output resistance of the amplifier vary from the expected 15 dB (see Figure 94).

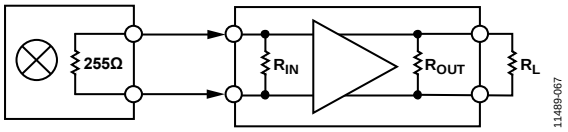

Figure 94. Mixer Loading of the IF DGA

The ideal load is 150 Ω for the matched condition; however, this may not be the most readily available load impedance. As a result, load vs. performance trade-offs must be considered. In the matched condition, the IF DGA is optimized for linearity; therefore, the third-order intermodulation product degrades with load. Table 18 shows some common output loads, and Figure 95, Figure 96, and Figure 97 show the effects of loading on gain, IMD2, and IMD3.

As the equations in this section indicate, the manner in which the IF DGA is loaded affects the input resistance, R_{IN}, of the amplifier. R_{IN}, in turn, determines the load resistance of the interstage filter between the mixer outputs and the IF DGA inputs. The interstage filter has a source impedance of 255 Ω from the mixer outputs and a load impedance of R_{IN} for the particular R_L load (see Table 18). As a result of the impedance mismatch, the insertion loss of the interstage filter must be included in the level planning calculations.

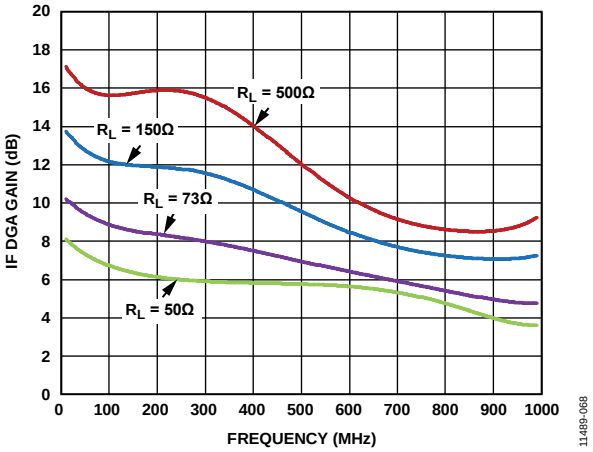

Figure 95. IF DGA Gain vs. Frequency for Different Loads

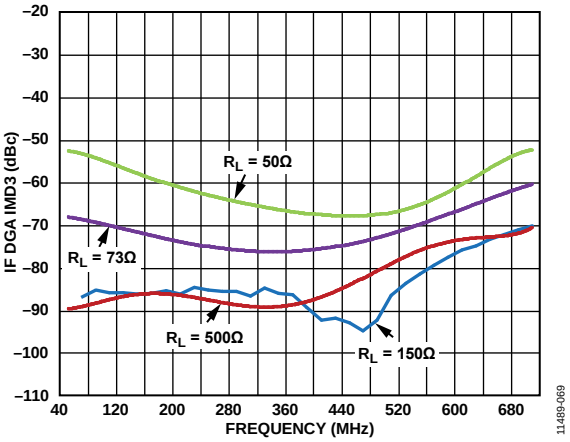

Figure 96. IF DGA IMD3 vs. Frequency for Different Loads

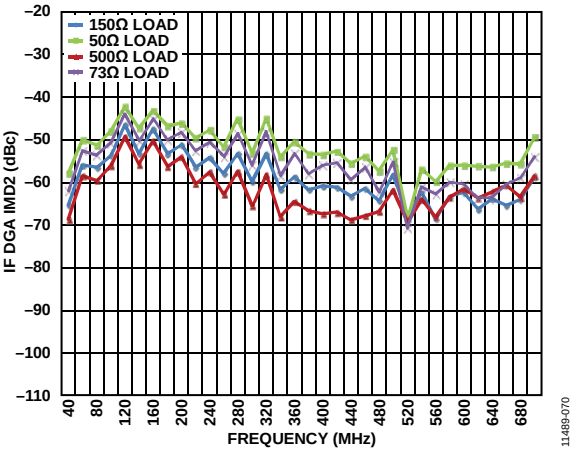

Figure 97. IF DGA IMD2 vs. Frequency for Different Loads

Table 18. Common Output Loads

R_S (Ω)	R_{IN} (Ω)	A_V (Linear)	A_V (dB)	S21 (Linear)	S21 (dB)	R_{OUT} (Ω)	R_L (Ω)
255	65	14.7	23.3	6	15.5	102.7	500
255	151	5.7	15.2	4.3	12.6	102.7	150
255	255	3	9.5	3	9.5	102.7	73
255	328	2.1	6.4	2.4	7.5	102.7	50

ADC INTERFACING

The integrated IF DGA of the ADRF6620 provides variable and sufficient drive capability for both buffered and unbuffered ADCs. It also provides isolation between the sampling edges of the ADC and the mixer core. As result, only an antialiasing filter is required when interfacing with an ADC.

The ADRF6620 is optimized for use in cellular base station digital predistortion (DPD) systems. Predistortion is used to improve the linearity of transmitter power amplifiers (PA). Because the input signal to the DPD path is the known transmitted signal, the hardware specifications are not typically as stringent as the main receive path. The signal-to-noise ratio (SNR) of the ADC is not paramount, due to the autocorrelation with the known transmitted signal. For this reason, lower resolution ADCs are usually adequate, and 11-bit to 14-bit resolution typically suffices. A more critical consideration is the analog bandwidth of the converter. Traditional DPD systems require 3× to 5× the transmit bandwidth. Therefore, for a 100 MHz Tx bandwidth, the DPD bandwidth must be at least 500 MHz for fifth-order correction.

The AD9434 complements the ADRF6620 very well in a DPD design. The AD9434 is a 12-bit, 370 MSPS/500 MSPS buffered ADC. Its full power analog bandwidth is 1 GHz, making it wide enough for fifth-order correction with substantial margin. The sampling rate of the AD9434 is insufficient in satisfying the sampling theorem; however, this may be acceptable in DPD applications where undersampling is often permissible. Because the receive signal in the DPD path is the known transmitted signal, the desired signal and its aliases are clearly distinguished.

The antialiasing filter resides between the ADRF6620 and the AD9434. Because aliasing is common practice in a DPD receive chain, the antialiasing filter requirements can be relaxed. A second-order or third-order filter is sufficient in reducing the high frequency noise from folding back into the band of interest. When designing the antialiasing filter, it is important to consider the output impedance of the IF DGA of the ADRF6620 and the input impedance of the AD9434. The differential resistance of the AD9434 is 1 kΩ, and the parallel capacitance is 1.3 pF. For the matched load condition, where the IF DGA is optimized for gain and linearity, load the IF DGA with 150 Ω. To do this, place a 176 Ω resistor in parallel with the input of the ADC.

The parallel combination of the 176 Ω with the 1 kΩ of the ADC input impedance results in an equivalent 150 Ω differential output load as seen by the IF DGA of the ADRF6620. In addition, the input capacitance of the AD9434 can be used as the fourth pole of the antialiasing filter. The final schematic design is shown in Figure 99. The antialiasing filter is maximally flat, with a pass-band bandwidth of 500 MHz. Table 19 shows the component values for the antialiasing filter design for DPD. Figure 98 shows the simulated antialiasing filter design.

Table 19. Component Values for 500 MHz Antialiasing Filter Design

Parameter	Value	Type	Manufacturer
L1 = L2	470 nH	0805CS	Coilcraft
C1	DNP	GRM15	Murata
L3 = L4	39 nH	0805CS	Coilcraft
C2	DNP	GRM15	Murata
L5 = L6	1 µH	0805LS	Coilcraft
L7 = L8	15 nH	0805CS	Coilcraft
C3	2.7 pF	GRM15	Murata
L9 = L10	27 nH	0805CS	Coilcraft

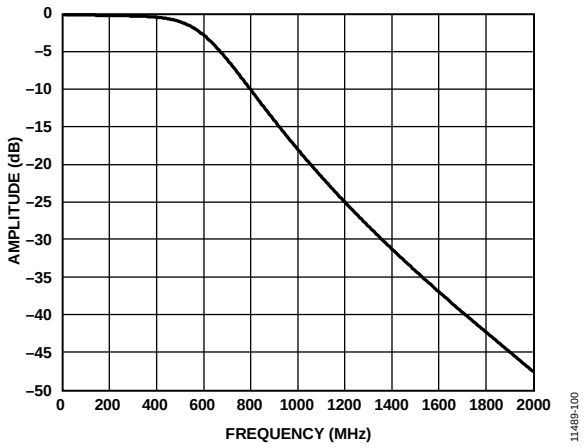

Figure 98. Simulated Antialiasing Filter Design

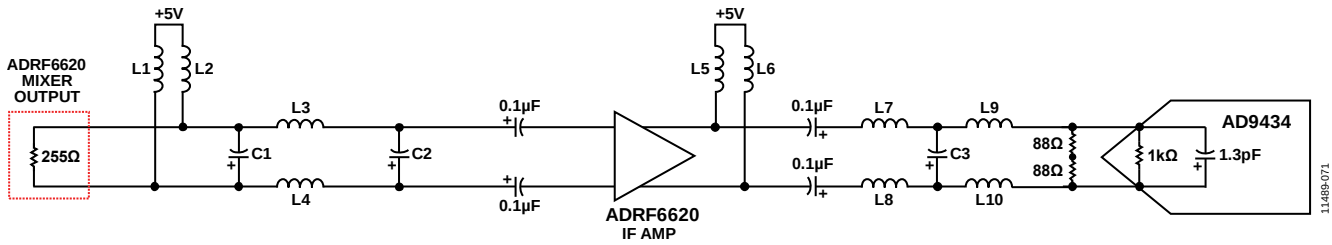

Figure 99. ADRF6620 Interface to the AD9434

POWER MODES

The ADRF6620 has many building blocks, and these blocks can be independently powered off by writing to Register 0x01 (see Table 23).

External LO Mode

In external LO mode, the internal PLL and VCO are disabled, which reduces the current consumption by approximately 100 mA. Table 20 lists the register settings that are required to configure external LO mode.

Table 20. Serial Port Configuration for External LO Mode

Bit Name	State	Register
LDO_3P3_EN	On	0x01 = 0x8B53
VCO_LDO_EN	On	0x01 = 0x8B53
CP_EN	Off	0x01 = 0x8B53
DIV_EN	Off	0x01 = 0x8B53
VCO_EN	On	0x01 = 0x8B53
REF_BUF_EN	Off	0x01 = 0x8B53
LO_DRV_EN	Off	0x01 = 0x8B53
LO_PATH_EN	On	0x01 = 0x8B53
MIX_EN	On	0x01 = 0x8B53
IF_AMP_EN	On	0x01 = 0x8B53
LO_LDO_EN	On	0x01 = 0x8B53
VCO_SEL	External LO	0x22, Bits[2:0] = 011

IF DGA Disable Mode

In applications where the IF DGA is not used, it can be powered down. Power-down is achieved by disabling the IF_AMP_EN bit (Register 0x01, Bit 11 = 0). By disabling the amplifier, the current consumption of the ADRF6620 decreases by approximately 25 mA, along with a 35 mA to 50 mA current savings through each bias inductor at the output of the amplifier. When the IF DGA is disabled, its input and output impedance is high-Z. For this reason, the input and output pins can be left open. If the preference is not to leave the nodes open, the alternative option is to terminate the pins to ground via a 1 kΩ resistor.

LAYOUT

Careful layout of the ADRF6620 is necessary for optimizing performance and minimizing stray parasitics. Because the ADRF6620 supports four RF inputs, the layout of the RF section is critical in achieving isolation between each channel. Figure 100 shows the recommended layout for the RF inputs. Each RF input, RFIN0 to RFIN3, is isolated between ground pins, and the best layout approach is to keep the traces short and direct. To achieve this layout, connect the pins directly to the center ground pad of the exposed pad of the ADRF6620. This approach minimizes the trace inductance and promotes better isolation between the channels. In additional, for improved isolation, do not route the RFIN0 to RFIN3 traces in parallel to each other; instead, spread the traces immediately after each one leaves the pins. Keep the traces as far away from each other as possible (and at an angle, if possible) to prevent cross coupling.

The input impedance of the RF inputs is 50 Ω, and the traces leading to the pin must also have a 50 Ω characteristic impedance. Terminate unused RF inputs with a dc blocking capacitor to ground.

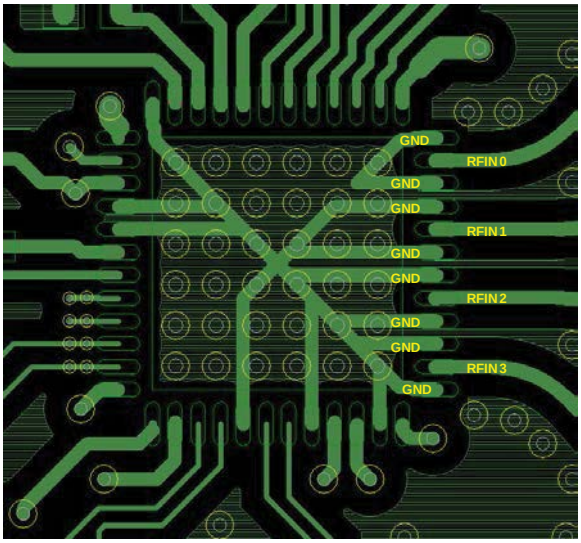

Figure 100. Recommended Layout for the RF Inputs

The IF DGA outputs on the ADRF6620 have two output pins for each polarity, and they are oriented in an alternating fashion, as follows: IFOUT1+ (Pin 8), IFOUT1− (Pin 9), IFOUT2+ (Pin 10), and IFOUT2− (Pin 11). When designing the board, minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance. Figure 101 shows the recommended layout. The IF DGA output pins with the same polarity are tied together on the bottom of the board with the blue traces and vias.

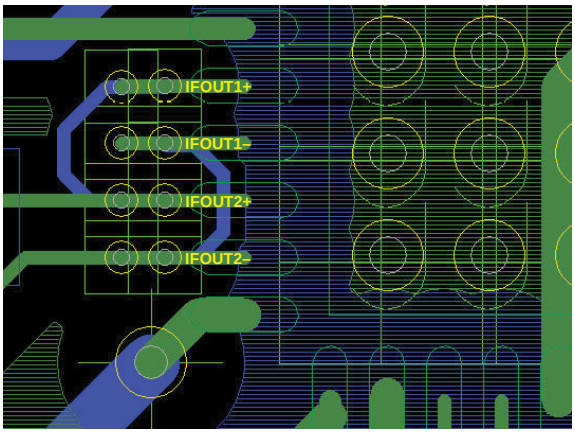

Figure 101. Recommended Layout for the IF DGA Outputs (Green traces are routings on top of the board, and blue traces are routings on the bottom of the board.)

REGISTER MAP

Table 21. Register Map Summary Table

Reg	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x00	SOFT_RESET	[15:8]	RESERVED								0x00000	W
		[7:0]	RESERVED							SOFT_RESET		
0x01	Enables	[15:8]	LO_LDO_EN	RESERVED	RESERVED	RESERVED	IF_AMP_EN	RESERVED	MIX_EN	LO_PATH_EN	0x8B7F	RW
		[7:0]	LO_DRV_EN	RESERVED	REF_BUF_EN	VCO_EN	DIV_EN	CP_EN	VCO_LDO_EN	LDO_3P3_EN		
0x02	INT_DIV	[15:8]	RESERVED				DIV_MODE	INT_DIV[10:8]			0x0058	RW
		[7:0]	INT_DIV[7:0]									
0x03	FRAC_DIV	[15:8]	RESERVED					FRAC_DIV[10:8]			0x0250	RW
		[7:0]	FRAC_DIV[7:0]									
0x04	MOD_DIV	[15:8]	RESERVED					MOD_DIV[10:8]			0x0600	RW
		[7:0]	MOD_DIV[7:0]									
0x20	CP_CTL	[15:8]	RESERVED	RESERVED	CSCALE				RESERVED		0x0C26	RW
		[7:0]	RESERVED		BLEED_DIR	BLEED						
0x21	PFD_CTL	[15:8]	RESERVED								0x0003	RW
		[7:0]	RESERVED	REF_MUX_SEL			PFD_POLARITY	REFSEL				
0x22	FLO_CTL	[15:8]	RESERVED							LO_DRV_LVL[1]	0x000A	RW
		[7:0]	LO_DRV_LVL[0]	RESERVED		LO_DIV_A		VCO_SEL				
0x23	DGA_CTL	[15:8]	RESERVED				RFSW_MUX	RFSW_SEL		RFDSA_SEL[3]	0x0000	RW
		[7:0]	RFDSA_SEL[2:0]			IF_ATTN						
0x30	BALUN_CTL	[15:8]	RESERVED								0x00000	RW
		[7:0]	BAL_COUT			RESERVED	BAL_CIN			RESERVED		
0x31	MIXER_CTL	[15:8]	RESERVED				MIXER_BIAS			MIXER_RDAC[3]	0x08EF	RW
		[7:0]	MIXER_RDAC[2:0]			RESERVED	MIXER_CDAC					
0x40	PFD_CTL2	[15:8]	RESERVED								0x0010	RW
		[7:0]	RESERVED	ABLDLY		CPCTRL			CLKEDGE			
0x42	DITH_CTL1	[15:8]	RESERVED								0x000E	RW
		[7:0]	RESERVED				DITH_EN	DITH_MAG		DITH_VAL		
0x43	DITH_CTL2	[15:8]	DITH_VAL[15:8]								0x0001	RW
		[7:0]	DITH_VAL[7:0]									

REGISTER ADDRESS DESCRIPTIONS

REGISTER 0x00, RESET: 0x00000, NAME: SOFT_RESET

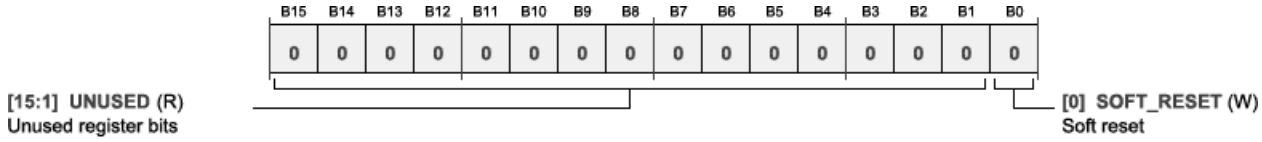

Table 22. Bit Descriptions for SOFT_RESET

Bit	Bit Name	Settings	Description	Reset	Access
0	SOFT_RESET		Soft reset	0x0000	W

REGISTER 0x01, RESET: 0x8B7F, NAME: ENABLES

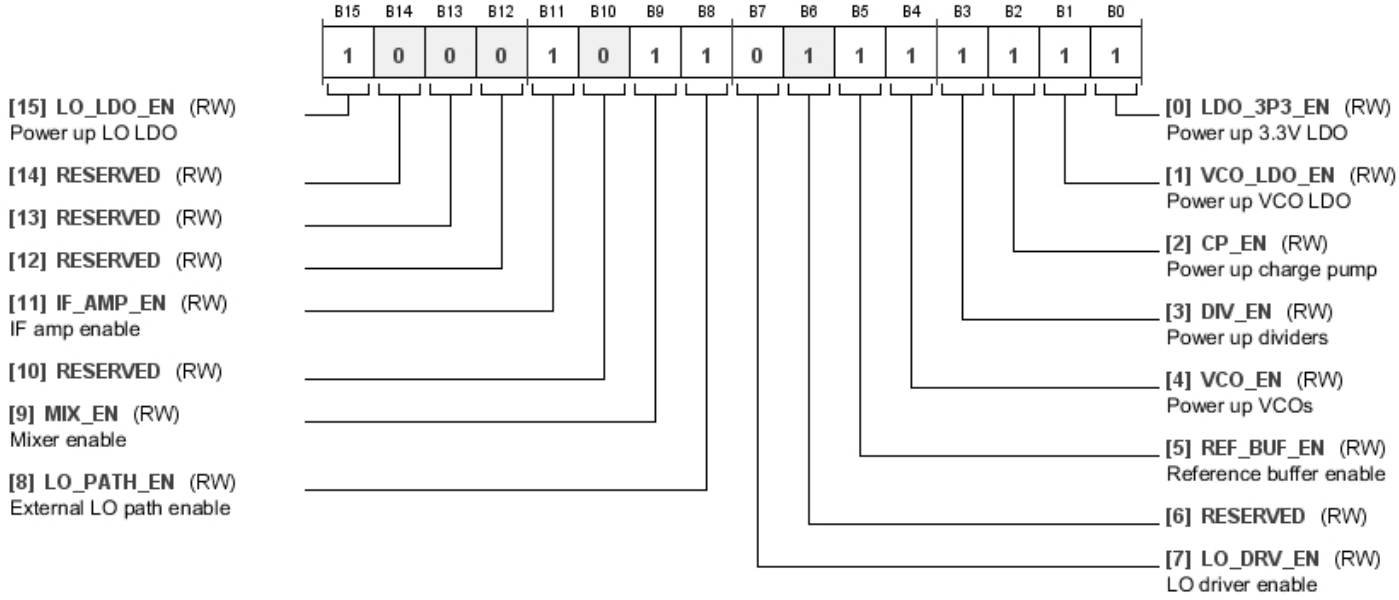

Table 23. Bit Descriptions for Enables

Bits	Bit Name	Settings	Description	Reset	Access
15	LO_LDO_EN		Power up LO LDO	0x1	RW
11	IF_AMP_EN		IF DGA enable	0x1	RW
9	MIX_EN		Mixer enable	0x1	RW
8	LO_PATH_EN		External LO path enable	0x1	RW
7	LO_DRV_EN		LO driver enable	0x0	RW
5	REF_BUF_EN		Reference buffer enable	0x1	RW
4	VCO_EN		Power up VCOs	0x1	RW
3	DIV_EN		Power up dividers	0x1	RW
2	CP_EN		Power up charge pump	0x1	RW
1	VCO_LDO_EN		Power up VCO LDO	0x1	RW
0	LDO_3P3_EN		Power up 3.3 V LDO	0x1	RW

REGISTER 0x02, RESET: 0x0058, NAME: INT_DIV

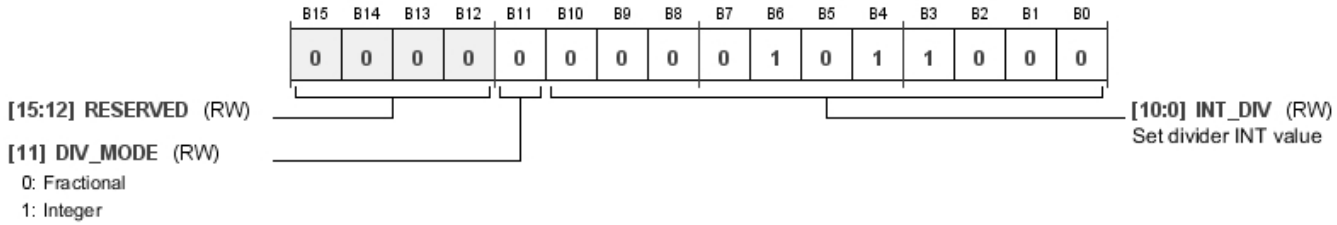

Table 24. Bit Descriptions for INT_DIV

Bits	Bit Name	Settings	Description	Reset	Access
11	DIV_MODE			0x0	RW
		0	Fractional		
		1	Integer		
[10:0]	INT_DIV		Set divider INT value	0x58	RW

REGISTER 0x03, RESET: 0x0250, NAME: FRAC_DIV

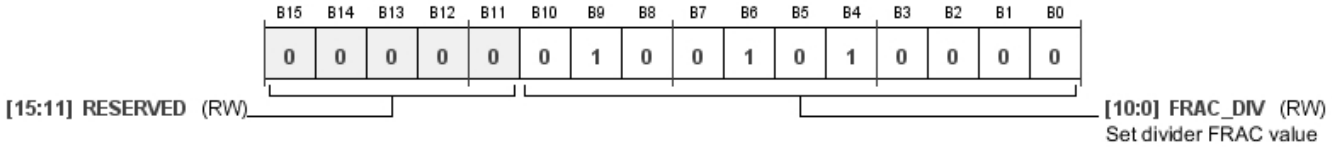

Table 25. Bit Descriptions for FRAC_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[10:0]	FRAC_DIV		Set divider FRAC value	0x250	RW

REGISTER 0x04, RESET: 0x0600, NAME: MOD_DIV

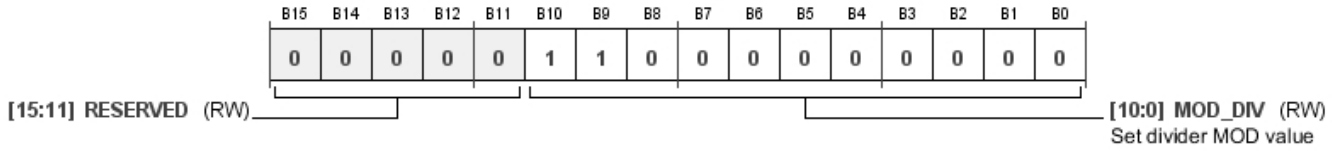

Table 26. Bit Descriptions for MOD_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[10:0]	MOD_DIV		Set divider MOD value	0x600	RW

REGISTER 0x20, RESET: 0x0C26, NAME: CP_CTL

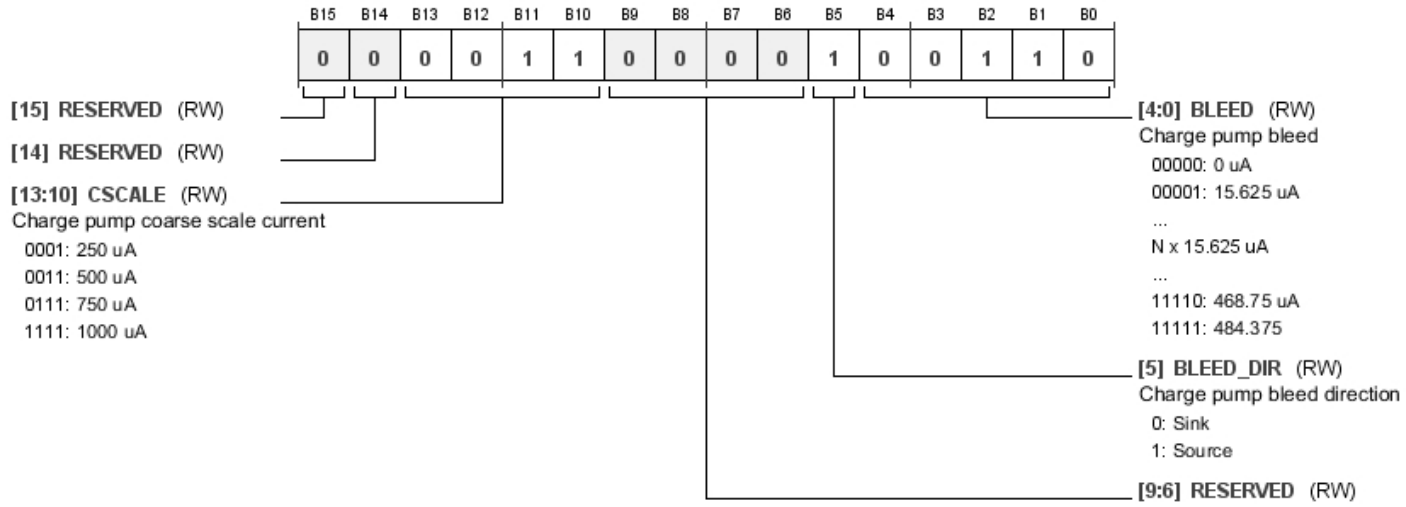

Table 27. Bit Descriptions for CP_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[13:10]	CSCALE		Charge pump current	0x3	RW
		0001	250 µA		
		0011	500 µA		
		0111	750 µA		
		1111	1000 µA		
5	BLEED_DIR		Charge pump bleed direction	0x1	RW
		0	Sink		
		1	Source		
[4:0]	BLEED		Charge pump bleed	0x06	RW
		00000	0 µA		
		00001	15.625 µA		
		…			
		…	N × 15.625 µA		
		…			
		11110	468.75 µA		
		11111	484.375 µA		

REGISTER 0x21, RESET: 0x0003, NAME: PFD_CTL

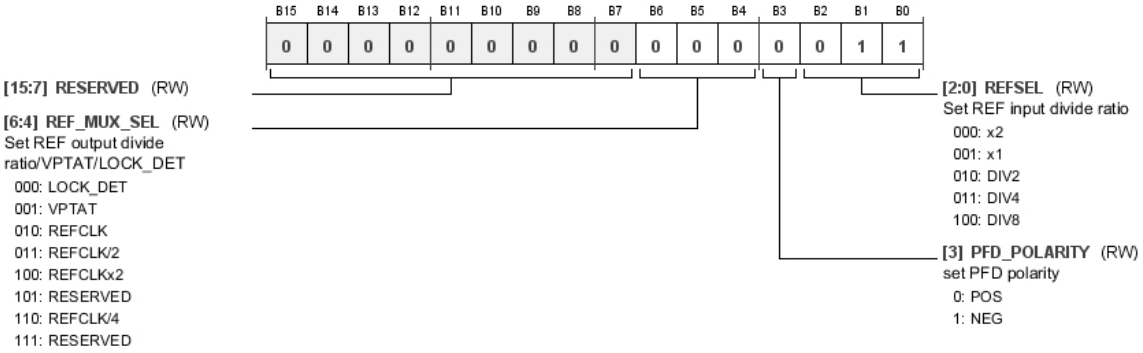

Table 28. Bit Descriptions for PFD_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	REF_MUX_SEL		Set REF output divide ratio/VPTAT/LOCK_DET	0x0	RW
		000	LOCK_DET		
		001	VPTAT		
		010	REFCLK		
		011	REFCLK/2		
		100	REFCLK × 2		
		101	RESERVED		
		110	REFCLK/4		
		111	RESERVED		
3	PFD_POLARITY		Set PFD polarity	0x0	RW
		0	Positive K_V VCO		
		1	Negative K_V VCO		
[2:0]	REFSEL		Set REF input divide ratio	0x3	RW
		000	×2		
		001	×1		
		010	DIV2		
		011	DIV4		
		100	DIV8		

REGISTER 0x22, RESET: 0x000A, NAME: FLO_CTL

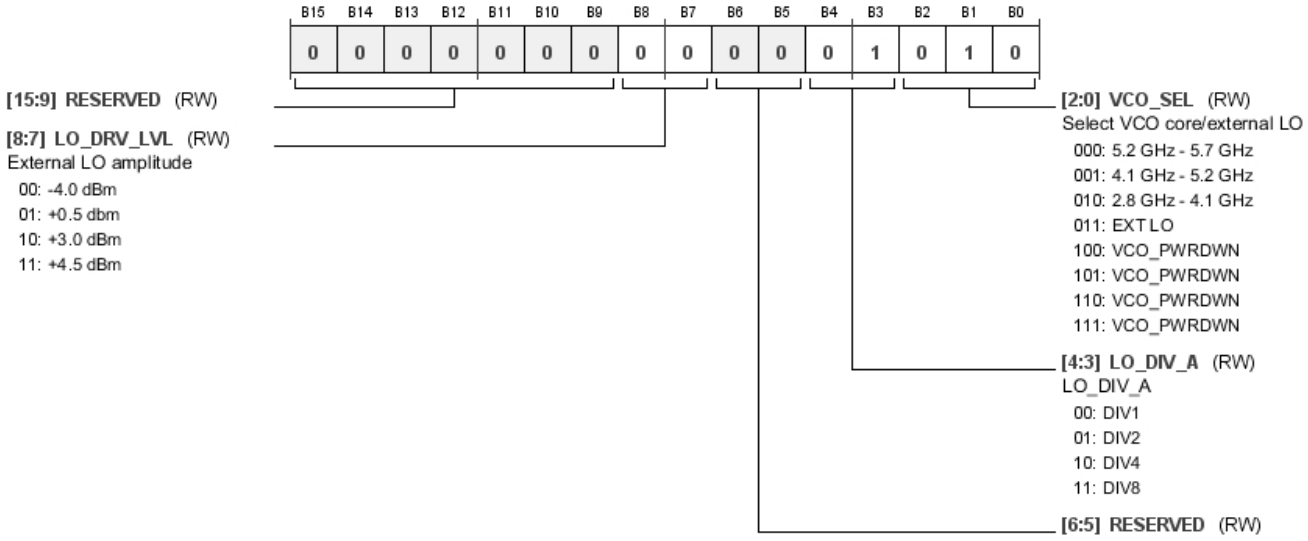

Table 29. Bit Descriptions for FLO_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[8:7]	LO_DRV_LVL		LO amplitude	0x0	RW
		00	−4 dBm		
		01	0.5 dBm		
		10	+3 dBm		
		11	+4.5 dBm		
[4:3]	LO_DIV_A		LO_DIV_A	0x1	RW
		00	DIV1		
		01	DIV2		
		10	DIV4		
		11	DIV8		
[2:0]	VCO_SEL		Select VCO core/external LO	0x2	RW
		000	5.2 GHz to 5.7 GHz		
		001	4.1 GHz to 5.2 GHz		
		010	2.8 GHz to 4.1 GHz		
		011	EXT LO		
		100	VCO_PWRDWN		
		101	VCO_PWRDWN		
		110	VCO_PWRDWN		
		111	VCO_PWRDWN		

REGISTER 0x23, RESET: 0x0000, NAME: DGA_CTL

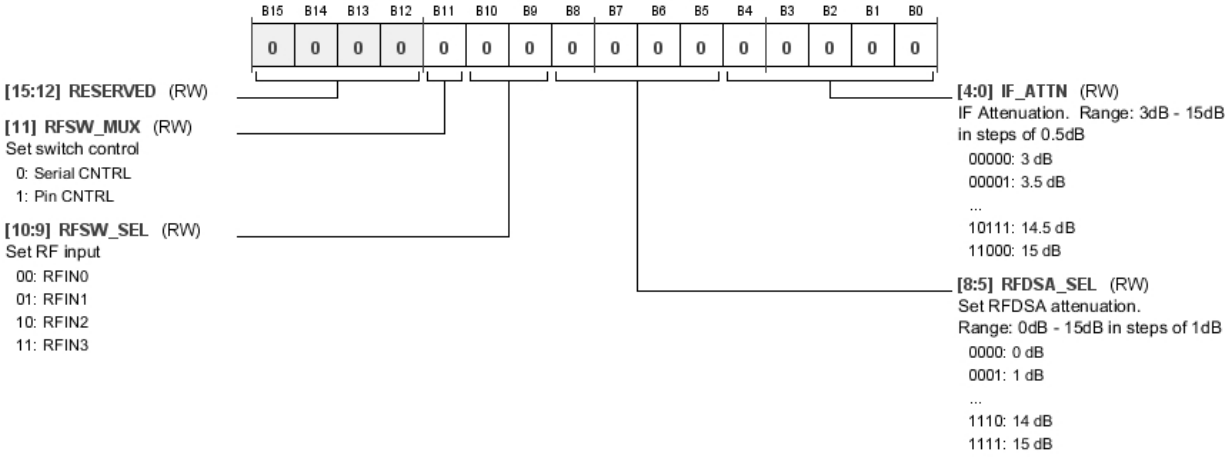

Table 30. Bit Descriptions for DGA_CTL

Bits	Bit Name	Settings	Description	Reset	Access
11	RFSW_MUX		Set switch control.	0x0	RW
		0	Serial CNTRL		
		1	Pin CNTRL		
[10:9]	RFSW_SEL		Set RF input.	0x0	RW
		00	RFIN0		
		01	RFIN1		
		10	RFIN2		
		11	RFIN3		
[8:5]	RFDSA_SEL		Set RFDSA attenuation. Range: 0 dB to 15 dB in steps of 1 dB.	0x0	RW
		0000	0 dB		
		0001	1 dB		
		...			
		1110	14 dB		
		1111	15 dB		
[4:0]	IF_ATTN		IF Attenuation. Range: 3 dB to 15 dB in steps of 0.5 dB.	0x0	RW
		00000	3 dB		
		00001	3.5 dB		
		...			
		10111	14.5 dB		
		11000	15 dB		

REGISTER 0x30, RESET: 0x00000, NAME: BALUN_CTL

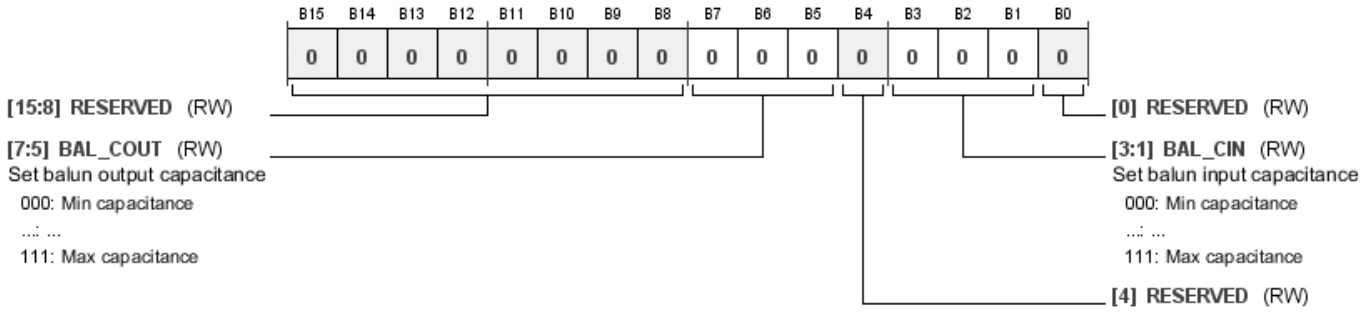

Table 31. Bit Descriptions for BALUN_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	BAL_COUT		Set balun output capacitance	0x0	RW
		000	Minimum capacitance		
		...	...		
		111	Maximum capacitance		
[3:1]	BAL_CIN		Set balun input capacitance	0x0	RW
		000	Minimum capacitance		
		...	...		
		111	Maximum capacitance		

REGISTER 0x31, RESET: 0x08EF, NAME: MIXER_CTL

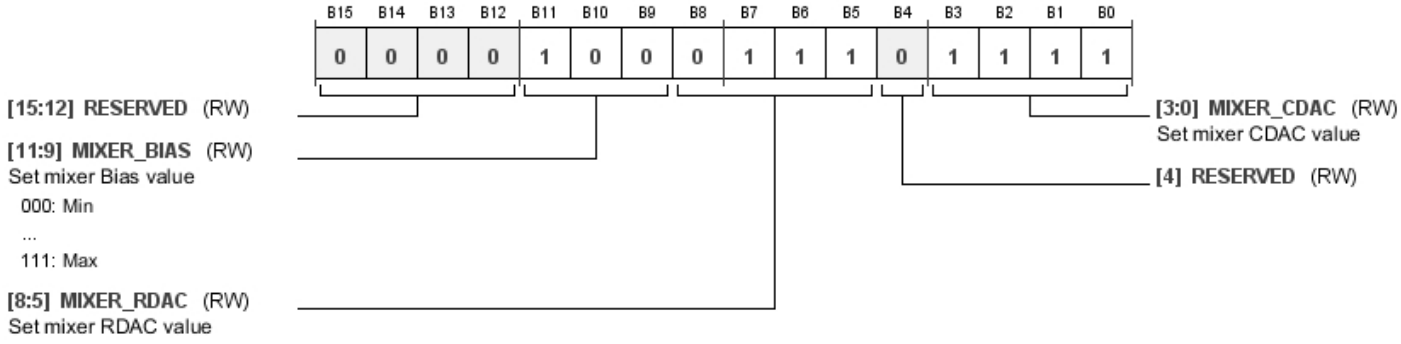

Table 32. Bit Descriptions for MIXER_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[11:9]	MIXER_BIAS		Set mixer bias value	0x4	RW
		000	Minimum		
		...			
		111	Maximum		
[8:5]	MIXER_RDAC		Set mixer RDAC value	0x7	RW
[3:0]	MIXER_CDAC		Set mixer CDAC value	0xF	RW

REGISTER 0x40, RESET: 0x0010, NAME: PFD_CTL2

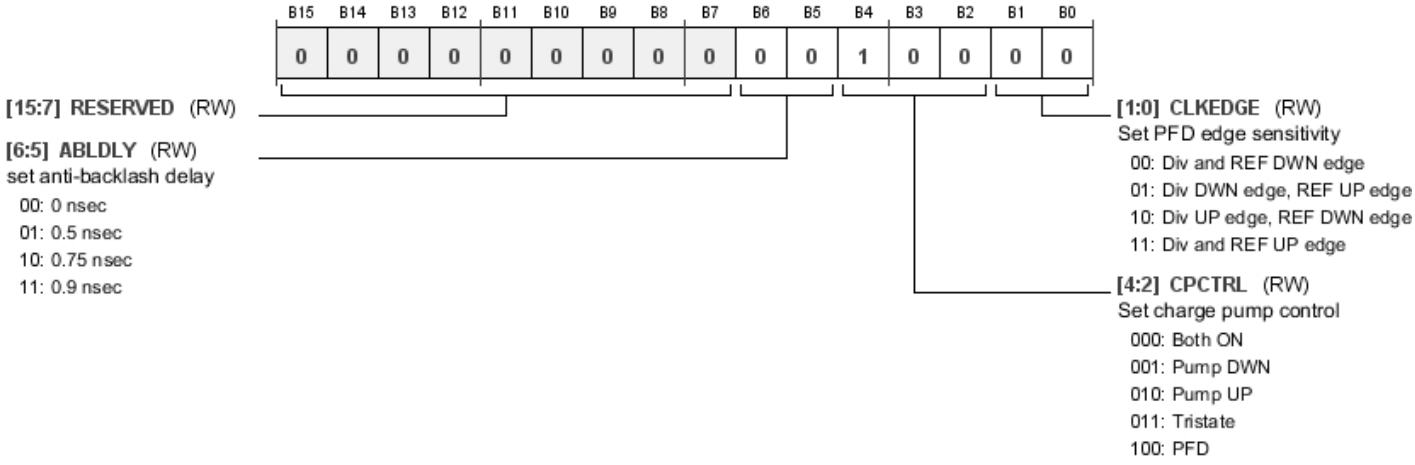

Table 33. Bit Descriptions for PFD_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[6:5]	ABLDLY		Set antibacklash delay	0x0	RW
		00	0 ns		
		01	0.5 ns		
		10	0.75 ns		
		11	0.9 ns		
[4:2]	CPCTRL		Set charge pump control.	0x4	RW
		000	Both on		
		001	Pump down		
		010	Pump up		
		011	Tristate		
		100	PFD		
[1:0]	CLKEDGE		Set PFD edge sensitivity	0x0	RW
		00	Div and REF down edge		
		01	Div down edge, REF up edge		
		10	Div up edge, REF down edge		
		11	Div and REF up edge		

REGISTER 0x42, RESET: 0x000E, NAME: DITH_CTL1

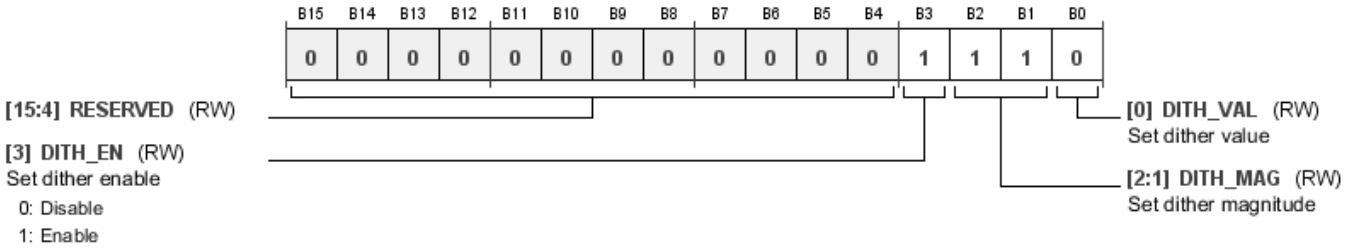

Table 34. Bit Descriptions for DITH_CTL1

Bits	Bit Name	Settings	Description	Reset	Access
3	DITH_EN		Set dither enable	0x1	RW
		0	Disable		
		1	Enable		
[2:1]	DITH_MAG		Set dither magnitude	0x3	RW
0	DITH_VAL		Set dither value	0x0	RW

REGISTER 0x43, RESET: 0x0001, NAME: DITH_CTL2

Table 35. Bit Descriptions for DITH_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DITH_VAL		Set dither value	0x1	RW

OUTLINE DIMENSIONS

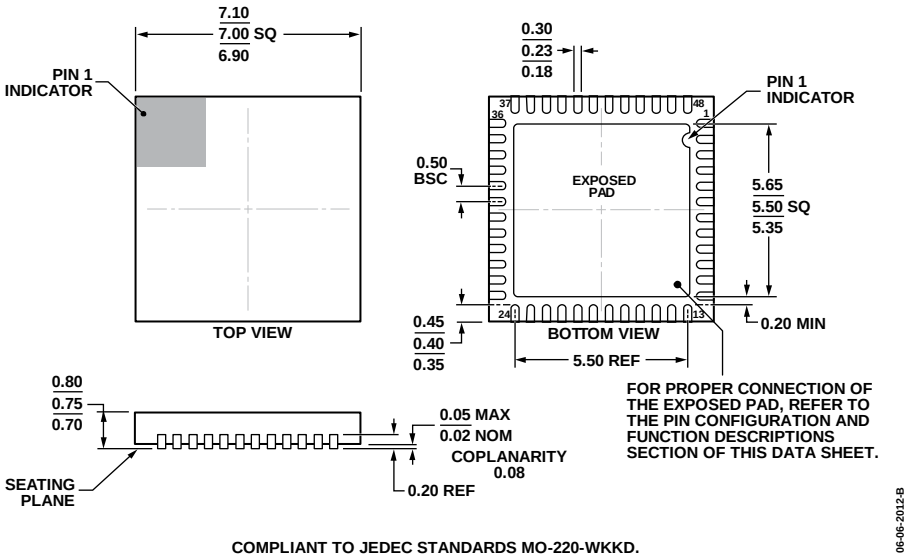

Figure 102. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6620ACPZ-R7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-9
ADRF6620-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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