ANALOG DEVICES

ADRF6520-EVALZ User Guide
UG-1045

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Evaluating the ADRF6520 Dual-Channel, Programmable Low-Pass Filters and VGAs, for 2 GHz Channel Spacing for Microwave Radios

FEATURES

Standard single-ended interfacing
Differential interfacing available
Supply voltage easily applied to test loops
Analog gain control applied to test loops
VRMS output via SMA or 2-pin header
SPI signals available via the P3 header

EVALUATION KIT CONTENTS

ADRF6520-EVALZ evaluation board

EQUIPMENT NEEDED

6 GHz signal generator
6 GHz spectrum analyzer
3-channel power supply that can supply 600 mA on at least 1 channel
SDP-S controller board
PC
DMM/voltmeter
VNA

DOCUMENTS NEEDED

ADRF6520 data sheet

SOFTWARE NEEDED

ADRF6520 Evaluation Software

GENERAL DESCRIPTION

This user guide describes the ADRF6520-EVALZ evaluation board kit for the ADRF6520 dual-channel, programmable, low-pass filters and variable gain amplifiers (VGAs) and how to configure the evaluation board to evaluate the ADRF6520 in a single-ended or differential configuration.

The ADRF6520 features a filter bypass mode that extends the bandwidth greater than 1 GHz. The ADRF6520-EVALZ evaluation board allows the user to test all the functions and features offered by the ADRF6520 including low-pass filtering, analog gain control, and the on-chip rms detectors. Signal path traces are matched and are intuitively laid out on the left and right side of the evaluation board, providing easy interfacing with other evaluation boards.

The ADRF6520-EVALZ uses an SDP-S controller board to program its signal peripheral interface (SPI) port using the ADRF6520 Evaluation Software.

A full description and complete specifications for the ADRF6520 are provided in the ADRF6520 data sheet and should be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

4/2017—Revision 0: Initial Version

EVALUATION BOARD LAYOUT

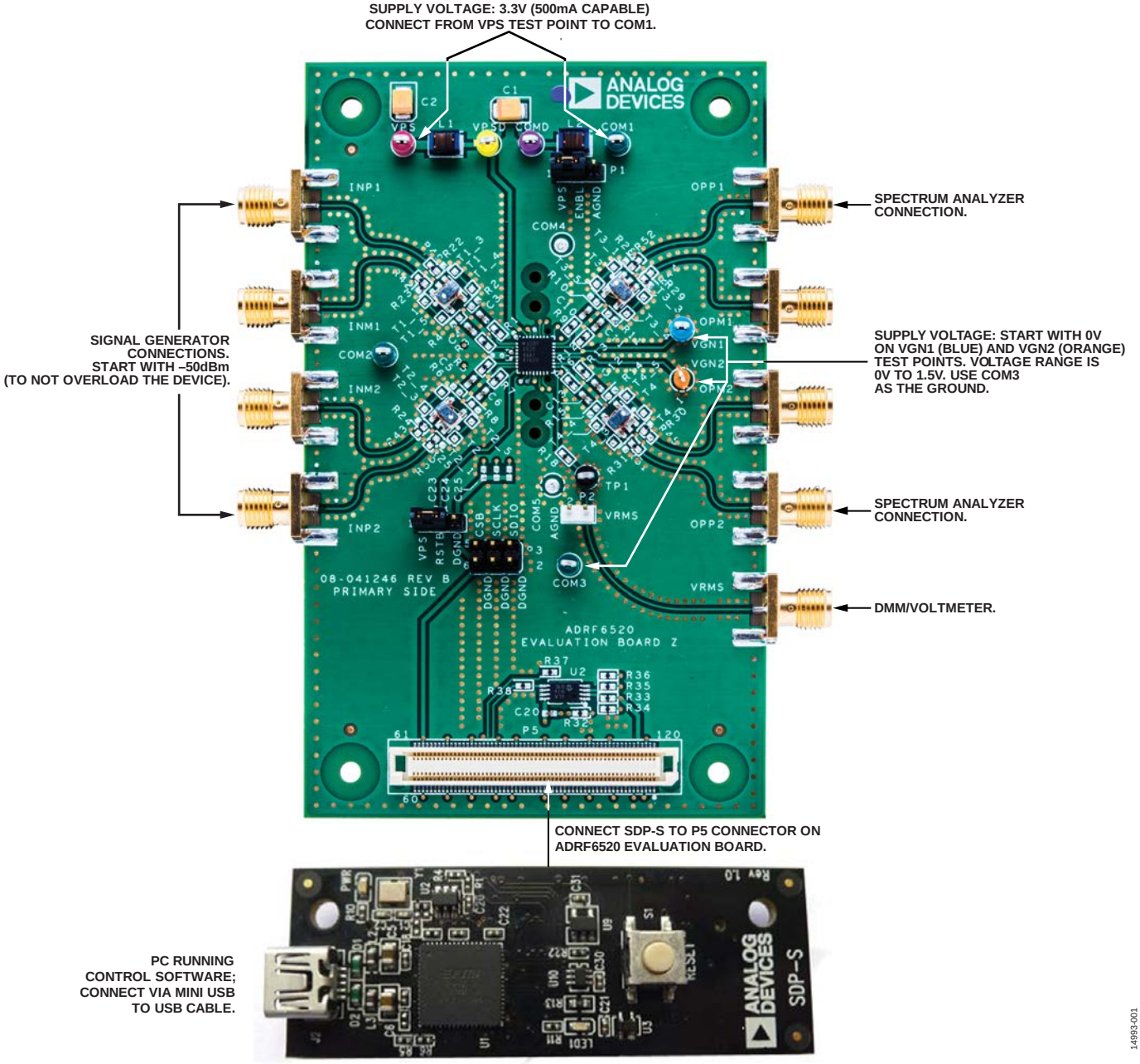


Figure 1. Layout of the ADRF6520-EVALZ Evaluation Board and the SDP-S Controller Board

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

Setting up the ADRF6520-EVALZ evaluation board includes the following steps:

1. Connect a signal generator or vector network analyzer (VNA) to the INP1 (for the Channel 1 input) or INP2 (for the Channel 2 input) connectors.
2. Connect a spectrum analyzer or VNA to the OPP1 (for the Channel 1 output) or OPP2 (for the Channel 2 output) connectors.
3. Connect a 3.3 V power supply capable of 600 mA to the red VPS test point.
4. Apply 0 V (minimum gain) to the VGN1 and VGN2 test points.
5. Check that the evaluation board has solid connections at all subminiture A (SMA) and test point locations before using the ADRF6520-EVALZ.

Power Up and Enable

The ADRF6520-EVALZ has several test points that can power up the evaluation board, which are an analog supply, an analog ground, a digital supply, and a digital ground. The analog supply, the red VPS test point, is dc-coupled via the L1 chip inductor to the yellow VPSD test point (digital supply). Similarly, the green COM1, COM2, and COM3 analog ground test points are dc-coupled to the purple COMD test point (digital ground), via the L2 chip inductor.

Apply one 3.3 V between the red VPS test point and one of the analog grounds to power up the ADRF6520; the COM1, COM2, and COM3 analog ground test points are shorted together.

The P1 header enables and disables the ADRF6520. Pin 1 of the P1 header is connected to the analog voltage supply, VPS, Pin 2 is connected to the ENBL pin on the ADRF6520, and Pin 3 is connected to analog ground. Short Pin 1 and Pin 2 to enable the ADRF6520 and short Pin 2 and Pin 3 to disable the ADRF6520.

If the ADRF6520-EVALZ is connected and working properly, upon power-up, the evaluation board draws approximately 395 mA of bias current from the analog supply voltage. By default on power-up, the ADRF6520 is in filter bypass mode. When in filter mode, the ADRF6520-EVALZ draws approximately 425 mA.

Upon power-up, the default configuration of the ADRF6520 is

- Filter bypass mode
- Chip enabled
- DC offset correction loop enabled

More information on this can be found in the ADRF6520 data sheet.

Inputs and Outputs

The ADRF6520-EVALZ is set up in a single-ended configuration for easy evaluation and testing with 50 Ω test equipment. For use of Channel 1 on the ADRF6520, use the INP1 SMA connector for the input and the OPP1 SMA connector for the output. On Channel 2 on the ADRF6520, use INP2 and OPP2.

The evaluation board can convert to a differential configuration for convenient interfacing to differential I/Q demodulators and analog-to-digital converters (ADCs), on the ADRF6520 inputs and outputs, respectively; see the Evaluation Board Setup Options section for more information.

Gain Control

The ADRF6520 has only analog gain control, achieved by applying voltages between 0 V (minimum gain) and 1.5 V (maximum gain) to the blue VGN1 and orange VGN2 test points. VGN1 controls the first variable gain amplifier and VGN2 controls the second variable gain amplifier for both Channel 1 and Channel 2.

Programming the SPI Port

To program the SPI port on the ADRF6520 while using the ADRF6520-EVALZ board, connect an SDP-S controller board to the 120-pin P5 connector, then connect the SDP-S board to a PC via a USB cable, which runs the ADRF6520 Evaluation Software; for more information, see Evaluation Board Software Quick Start Procedures section.

The ADRF6520 Evaluation Software controls the filter corner, filter bypass, dc offset correction loop enable, and chip enable by writing to Register 0x0010 (hexadecimal value). Click the **Filter Corner** dropdown list box (see Figure 2) to select the desired filter corner or filter bypass mode. Click the **Chip Enable** check box to enable or disable the ADRF6520 chip enable and the **DC offset correction** check box to enable or disable the dc offset correction loop.

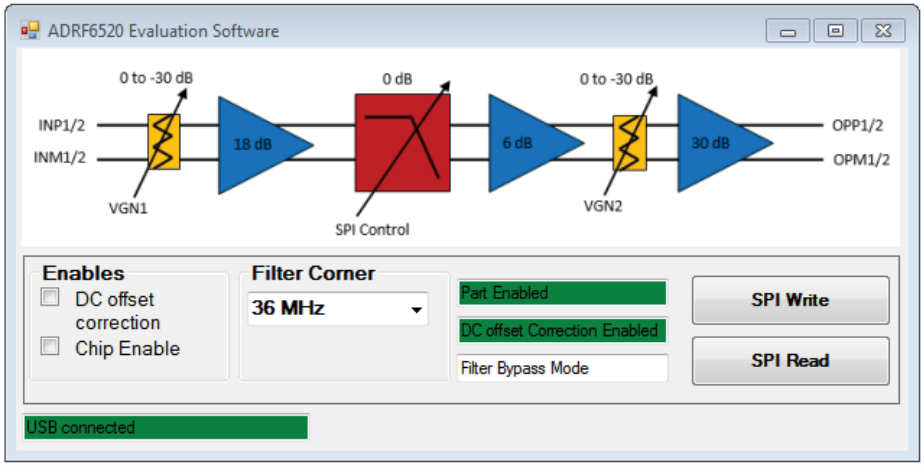


Figure 2. ADRF6520 Evaluation Software Graphical User Interface (GUI)

Users can also access the three SPI pins (SDIO, SCLK, and $\overline{CS}$) and the traces associated with each pin with the P3 3 × 2 pin header. Pin 1, Pin 3, and Pin 5 of P3 are connected to SDIO, SCLK, and $\overline{CS}$, respectively. Pin 2, Pin 4, and Pin 6 are connected to the COMD test point. With the access that P3 provides to the SPI lines, users can easily program the SPI port with a personal microcontroller and software if desired.

Resetting the SPI Register 0x010

Register 0x010 can be reset to its default value of 0x97 (hexadecimal value) by pulling the $\overline{RST}$ pin to analog or digital ground; $\overline{RST}$ is an active low pin. This can be accomplished with the P4 header by shorting Pin 2 and Pin 3. Shorting the pins can be accomplished by the provided black 0.100 mil socket that is attached to the ADRF6520-EVALZ. Keep Pin 1 and Pin 2 of P4 shorted with the provided blue socket when not resetting the SPI port ($\overline{RST}$ pulled to 3.3 V).

RMS Detector

Access the output of the rms detectors by either the VRMS SMA connector or the P2, 2-pin header. P2 allows an easy connection to a high impedance field effect transistor (FET) probe if the user needs a transient response from the rms detector with minimal parasitic loading.

The video bandwidth (BW) of the rms detectors is set with the 10 nF C7 and C8 capacitors. This sets a video BW of approximately 70 kHz. For more information on the BW of the rms detectors, see the Evaluation Board Setup Options section.

DC Offset Correction Loop

The ADRF6520 has a dc offset correction loop that can be enabled or disabled via the SPI port. This loop superimposes a high-pass response onto the signal paths. This high-pass corner of this response is controlled with the C9 and C19 capacitors. Both capacitors are populated with 1 µF capacitors, creating a high-pass corner of 500 Hz. For more information on the high-pass corner of the dc offset corner loops, see the Evaluation Board Setup Options section.

EVALUATION BOARD SETUP OPTIONS

Differential Signal Path Setup

The ADRF6520-EVALZ is configured as single-ended. The ADRF6520-EVALZ allows users to operate the ADRF6520 with differential inputs and/or outputs.

To make the Channel 1 input differential, depopulate the T1 balun and the R23 shunt, populate the R42 resistor with a 0 Ω value resistor (see Figure 3). There are two pairs of pads, each pair connected to each other via a short trace, that surround T1, but are normally electrically open. The user must also populate 0 Ω resistors from these open pads to the pads (footprint) on to which the T1 balun previously was installed. Install 0 Ω resistors in the following locations of the T1 balun footprint:

- Pad 1 of T1 to the T1_1 pad
- Pad 3 of T1 to the T1_3 pad
- Pad 4 of T1 to the T1_4 pad
- Pad 5 of T1 to the T1_5 pad

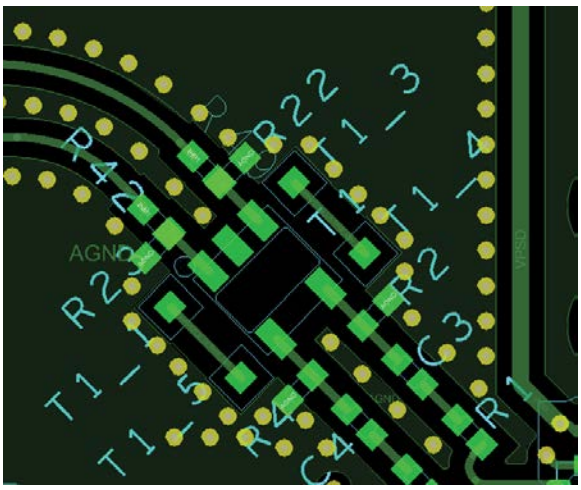


Figure 3. Layout of Channel 1 Input Showing Pad Locations For Differential Operation

To make the Channel 1 output differential, depopulate T3 and R29 and populate R44 with a 0 Ω resistor. The user must also populate 0 Ω resistors in the following locations of the T3 balun:

- Pad 1 of T3 to the T3_1 pad
- Pad 3 of T3 to the T3_3 pad
- Pad 4 of T3 to the T3_4 pad
- Pad 5 of T3 to the T3_5 pad

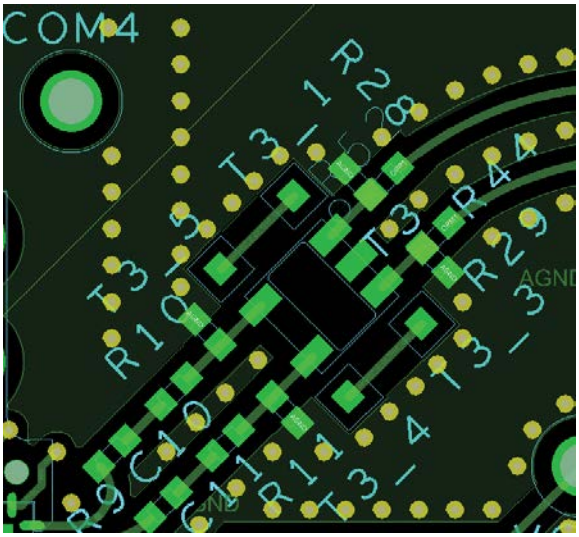


Figure 4. Layout of Channel 1 Output Showing Pad Locations For Differential Operation

A similar process can be followed to make the Channel 2 input and/or output differential. Refer to the Evaluation Board Schematics and Artwork section when making these changes.

RMS Video Bandwidth

The ADRF6520-EVALZ has factory installed C7 and C8 capacitors, placed from the CFLT1 and CFLT2 pins, respectively, to the analog voltage supply, VPS, to set the video BW of each rms detector. Each capacitor has a value of 0.01 µF, which sets the video BW to approximately 70 kHz. The relationship between the BW and CFLT1 and CFLT2 is described as follows:

$$Video\ BW_{RMS}\ (\text{Hz}) = 0.0007/(130\ \text{pF} + CFLTx)$$

where *CFLTx* is the value of either CFLT1 or CFLT2.

To decrease the video BW, increase the value of C7 and C8, which also increases the response time of the rms detectors. Decreasing the value decreases the response time and increases the video BW. Depopulating CFLT1 or CFLT2, sets the video BW to approximately 5.4 MHz.

If using the detectors in an automatic gain control (AGC) loop that levels certain modulated signals, there is a tradeoff between response time and error vector magnitude (EVM). The AGC loop must level the rms value of the signal and must not affect the voltage peaks of the signal. If the response time is too fast, the EVM degrades because the AGC loop tries to level each voltage peak, which corrupts the symbols of the modulated signal.

DC Offset Correction Loop High-Pass Corner

The ADRF6520 has dc offset correction loops on each channel. These loops can be enabled or disabled via the GUI or by setting Bit 5 of the 24-bit SPI Register 0x010 (refer to ADRF6520 data sheet for more information). The loops null out the dc offsets that appear and can become large at high gains. The loops null any signal below their low-pass frequency corner, which is set by the C9 and C16 1 µF capacitors to ground on the CHP1 and CHP2 pins of ADRF6520.

Although the dc offset correction loops have a low-pass response, the signal paths show a high-pass response because the loops null any low frequency signal below their low-pass corner. The following equation shows the relationship between the high-pass corner observed on the signal paths and the value of the C9 or C16 capacitors:

$$f_{HP}\ (\text{Hz}) = 16.1 \times VGA2\ Linear\ Voltage\ Gain/C_{OFS}\ (\mu\text{F})$$

where:
VGA2 Linear Voltage Gain is expressed in linear terms, not in decibels (dB), and is the gain following the offset correction amplifier, which excludes the all prior gain.
C_{OFS} is either the value for C9 or C16.

For example, the high-pass corner at the maximum VGA2 gain, 30 dB, and with C_{OFS} = 1 µF, is calculated as

$$f_{HP}(\text{Hz}) = 16.1\frac{10^{30/20}}{1} = 509.1\ \text{Hz}$$

Loss and Gain of the Input and Output Networks

The ADRF6520-EVALZ has 1:1 baluns (T1 and T2) on the inputs signal paths. Ideally,because the baluns are a 1:1 ratio, the signal level must be the same on either side of the balun.

However, the baluns have approximately a 1 dB of voltage gain associated with them, when measured from the INP1 or INP2 SMA connectors to the respective input pins of the ADRF6520.

The output signal paths have 1:1 baluns and 25 Ω series resistors: T3, T4, R9, R12, R13, and R16. The series resistors are lossy: from the output pins of the ADRF6520 to the OPP1 or OPP2 SMA connectors, the voltage and power of the signal attenuates by approximately 7 dB and 4 dB, respectively.

Users must account for the losses of the input and output networks when applying signals on the input SMAs (INP1 and INP2) and measuring signals on the output SMAs (OPP1 and OPP2).

DC Coupling

It is not recommend to dc couple the inputs and outputs signal paths of the ADRF6520. In most situations, ac coupling is suitable. The high-pass corner caused by the ac coupling capacitors can be set low enough in frequency so the information lost at and near dc is negligible. However, if the user must dc couple the input and/or output signal paths, take care that the common-mode voltage of previous or subsequent devices to which the ADRF6520 is interfacing is the same as the common-mode voltage of the ADRF6520 (1.375 V for its inputs and 1.65 V for its outputs).

There is no mechanism built into the ADRF6520 to change these common-mode voltages. For example, in a typical signal chain, the ADRF6520 input is driven by a quadrature demodulator and its output drives a dual, high speed ADC. If dc coupling, the quadrature demodulator output common-mode voltage must equal 1.375 V and the ADC input common-mode voltage must equal 1.65 V. If different common-mode voltages are needed on the ADRF6520 inputs or outputs and users must dc couple, the user must implement a common-mode translator circuit.

Input Networks

The ADRF6520-EVALZ comes from the factory with the ADRF6520 input impedance mismatched to a 50 Ω source impedance presented by the signal generator or VNA. The T1 and T2 baluns present a 50 Ω impedance to the 100 Ω input impedance of the ADRF6520.

If users want to match the input so the ADRF6520 is presented with 100 Ω, and the test equipment is presented with 50 Ω, the following change can be made: populate R1 through R8 with 35 Ω resistors.

Installing these values of resistors in the input network creates approximately 4.6 dB of voltage loss and 7.6 dB of power loss between the INP1 and INP2 SMA connectors and the respective input pins of the ADRF6520.

Output Networks

The ADRF6520-EVALZ comes from the factory with the input loaded with 100 Ω differential, which is mismatched from the low 20 Ω output impedance of the ADRF6520 output buffers. This loading is achieved with the T3 and T4 baluns as well as the 25 Ω series resistors, R9, R12, R13, and R16.

If users want to match the output so the ADRF6520 is presented with 100 Ω, and the test equipment is presented with 50 Ω, the following changes can be made:

- Populate R10, R11, R14, and R15 with 55 Ω resistors
- Populate R9, R12, R13, and R16 with 33 Ω resistors

Installing these values of resistors in the output network creates approximately 9 dB of voltage loss and 6 dB of power loss between the output pins of the ADRF6520 and the OPP1 or OPP2 SMA connectors.

Balun Termination

The ADRF6520-EVALZ is configured in a single-ended configuration with SMA connector inputs, labeled INP1 and INP2, and the SMA connector outputs, labeled OPP1 and OPP2.

Users can change the inputs and outputs to the INM1 and INM2 inputs and OPM1 and OPM2 outputs with a simple evaluation board modification. On the first input, for example, R23 is populated with a 0 Ω resistor and R42 is not installed, while R49 is 0 Ω and R22 is not installed. If users want to change the first input (single-ended) to the INM1 SMA connector, modify the evaluation board by depopulating R23 and R49, and installing 0 Ω resistors for R22 and R42. Similar changes can be made on the second input and both outputs if the user desires.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

The following procedures detail how to begin using the ADRF6520 Evaluation Software.

1. Install the SDP drivers that are provided on the ADRF6520 webpage.
2. Connect the SDP-S controller board to the ADRF6520 via the P5 connector on the ADRF6520-EVALZ evaluation board.
3. Plug the USB miniconnector of the USB cable (provided with the SDP-S board) into the SDP-S board and the USB connector into the PC.
4. Connect a supply cable from the red VPS test point to the green COM1 test point. Set Channel 1 of the power supply to 3.3 V (600 mA capable). Do not turn on the power supply at this point.
5. Connect the second channel of the power supply to the blue VGN1 test point and set it to 0 V. Set the current limit to 1 mA; the current draw must be within the µA range.
6. Connect Channel 3 of the power supply to the orange VGN2 test point and set the channel to 0 V. Set the current limit to 1 mA; the current draw must be in the µA range.
7. Connect the signal generator to the INP1 SMA connector and the spectrum analyzer to the OPP1 SMA connector. Connect the VRMS SMA connector to a digital multimeter (DMM) or voltmeter to read the output voltage of the on-chip rms detectors.
8. Turn on the power supply. The device must have about 395 mA (±5%) of the supply current upon power-up.
9. Turn on the radio frequency (RF) output of the signal generator.
10. Run the ADRF6520 Evaluation Software to launch the GUI. If the PC is connected to the SDP-S board via the USB cable and the SDP-S board is connected to the ADRF6520-EVALZ board, the status bar reads **USB Connected** (see Figure 5).
11. In the GUI, click both of the enable check boxes and select **720 MHz** in the **Filter Corner** dropdown menu. Then click the **SPI Write** button (see Figure 6).
12. The supply current increases to approximately 425 mA (±5%).

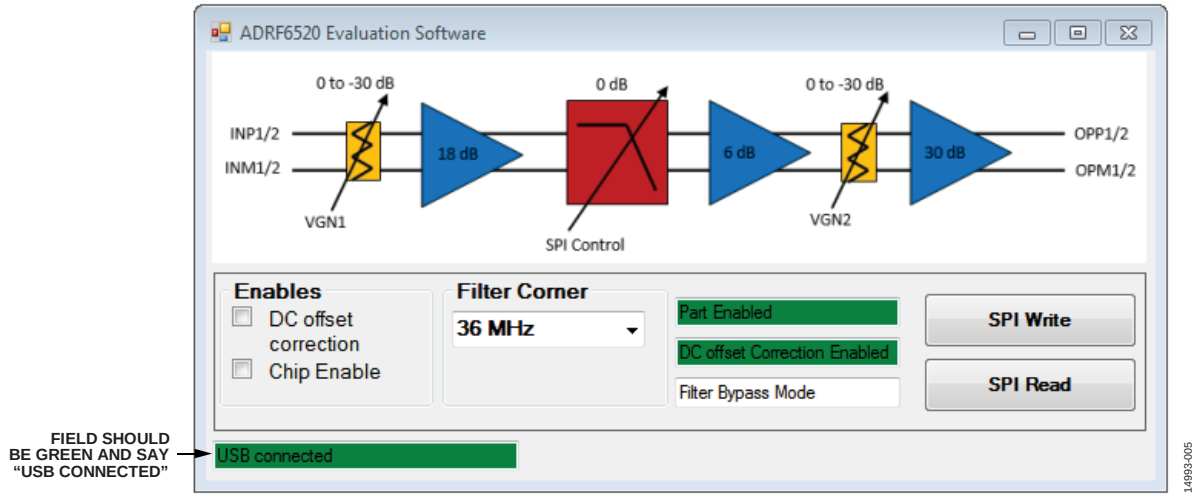


Figure 5. Status Bar in the ADRF6520 Evaluation Software GUI

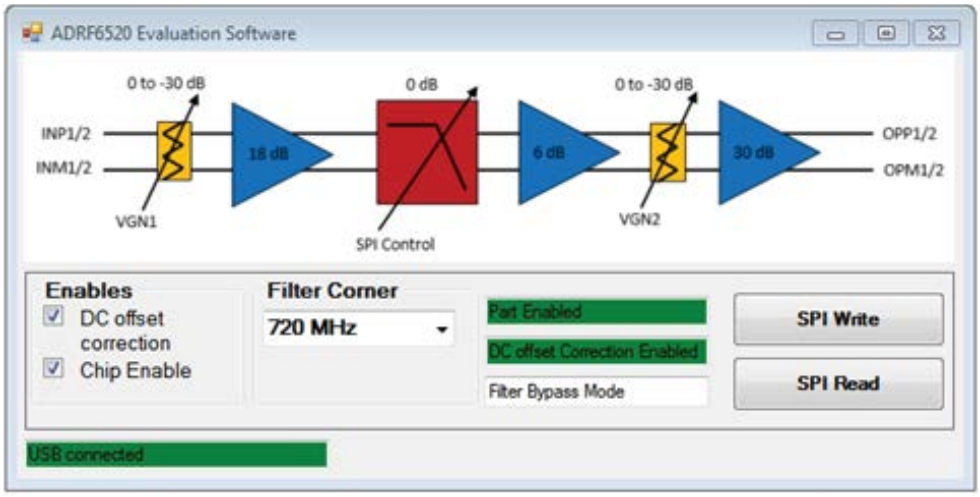


*Figure 6. Setting the **Filter Corner** Option*

EVALUATION BOARD SCHEMATICS AND ARTWORK

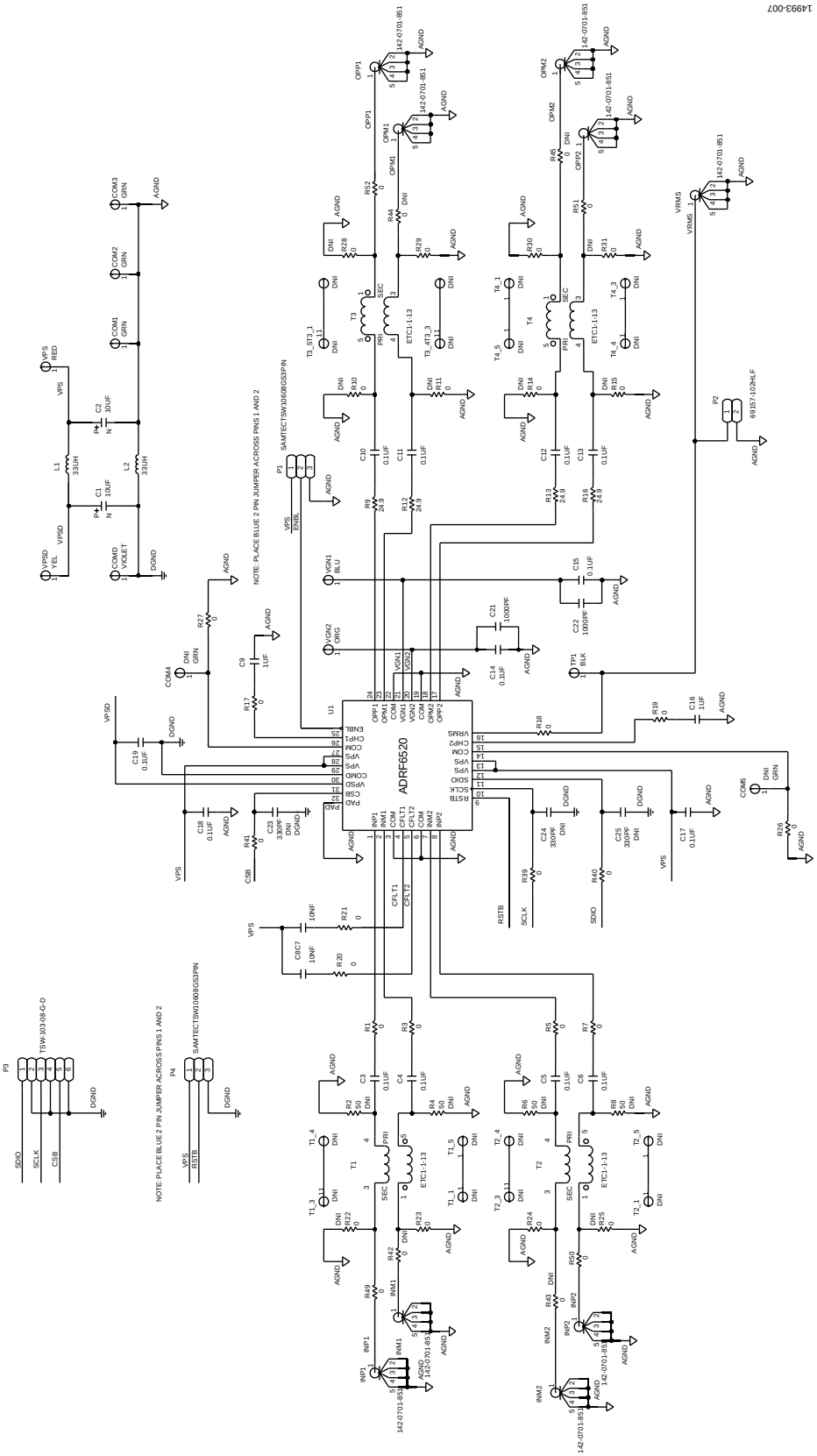


Figure 7. ADRF6520-EVALZ Main Schematic

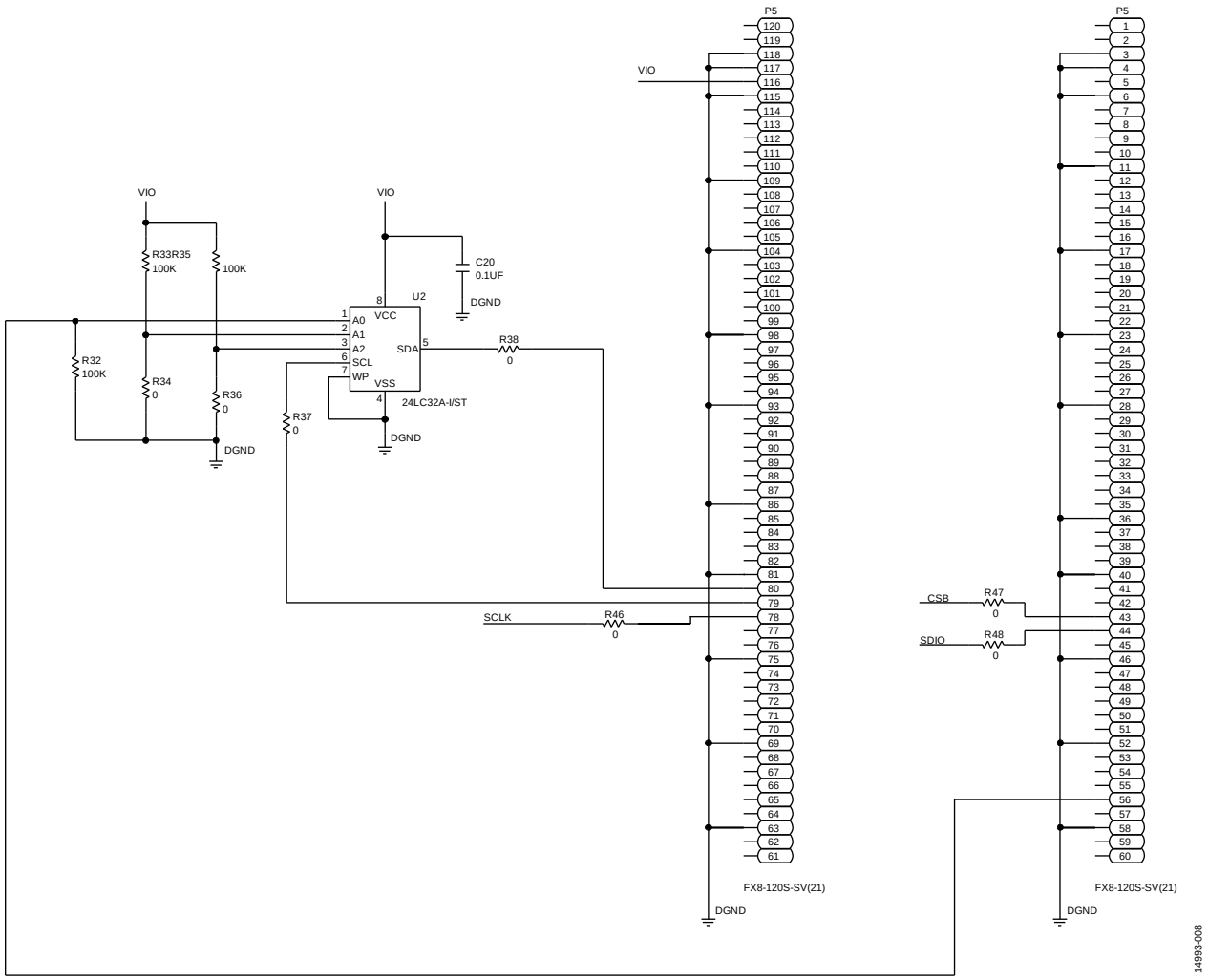


Figure 8. ADRF6520-EVALZ Schematic of Components Required for Use with SDP-S Controller Board

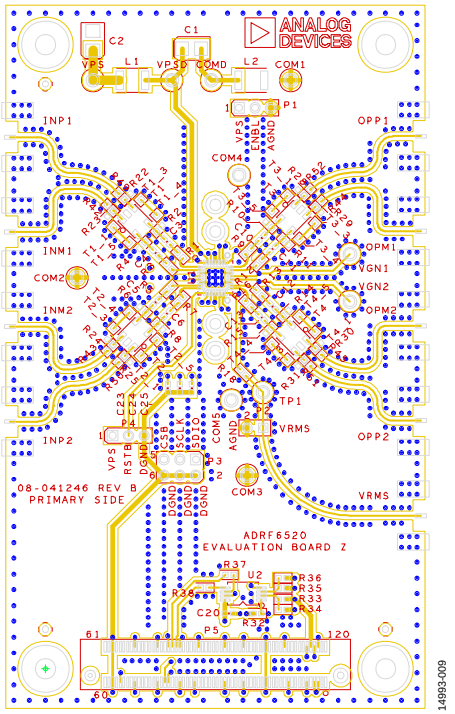


Figure 9. ADRF6520-EVALZ Silkscreen, Top View

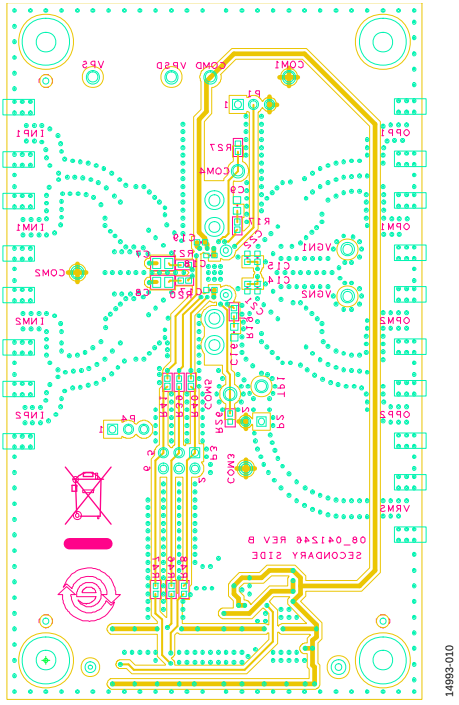


Figure 10. ADRF6520-EVALZ Silkscreen, Bottom View

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. ADRF6520-EVALZ Evaluation Board Bill of Materials (Installed)

Reference Designator	Description	Part Number	Manufacturer
U1	Integrated circuit (IC), dual-programmable filters and VGAs	ADRF6520-ACPZ	Analog Devices, Inc.
U2	IC, 32 kB serial EEPROM	24LC32A-I/ST	Microchip Technology
C1, C2	Capacitors, standard tantalum, Case B, 10 µF	TAJB106K016RNJ	AVX
C3 to C6, C10 to C15, C17 to C20	Ceramic capacitors, X7R, 0402, 10 µF	GRM155R71C104KA88D	Murata
C9, C16	Monoceramic capacitors, X5R, 1 µF	GRM188R61E105KA12D	Murata
C21, C22	Ceramic capacitors, X7R, 1000 pF	CC0402KRX7R7BB102	Yageo
C7, C8	Ceramic capacitors, X7R, high voltage, 10 nF	C0805C103KCRACTU	Kemet
R1, R3, R5, R7, R17 to R21, R23, R24, R26, R27, R29, R30, R34, R36 to R41, R46 to R52	Resistor chips, SMD jumper, 0 Ω	ERJ-2GE0R00X	Panasonic
R9, R12, R13, R16	Resistors, precision thick film chip, R0402, 24.9 Ω	ERJ-2RKF24R9X	Panasonic
R32, R33, R35	Resistors, precision thick film chip, R0402,100 kΩ	ERJ-2RKF1003X	Panasonic
L1, L2	Inductor chips, 1812, 33 µH	1812CS-333XJLB	Coilcraft
P1, P4	3-position header connector, male, 0.100"	TSW-103-08-G-S	Samtec
P2	2-position header connector, male, 0.100"	69157-102HLF	FCI
P3	6-positions header connector, 0.100"	TSW-103-08-G-D	Samtec
P5	120-pin connector, PCB, board to board receptacle, 0.6 mm pitch	FX8-120S-SV(21)	Hirose Electric Co.
T1 to T4	RF balun, 4.5 MHz to 3 GHz, 1:1	ETC1-1-13	Macom
INP1, INP2, INM1, INM2, OPP1, OPP2, OPM1, OPM2, VRMS	SMA connector jack, 50 Ω, end launch, female receptacle	142-0701-851	Cinch
VPS	CONN-PCB test point, red	TP-104-01-02	Components Corporation
VPSD	CONN-PCB test point, yellow	TP-104-01-04	Components Corporation
VGN1	CONN-PCB test point, blue	TP104-01-06	Components Corporation
VGN2	CONN-PCB test point, orange	TP-105-40-03	Components Corporation
COM1 to COM3	CONN-PCB test point, green	TP104-01-05	Components Corporation
COMD	CONN-PCB test point, violet	TP104-01-07	Components Corporation
Installed on P1 and P4	Socket, two-position, 0.100" pitch, connector shunt	SNT-100-BK-G	Samtec

Table 4. ADRF6520-EVALZ Evaluation Board Bill of Materials (Not Installed)

Reference Designator	Description	Part Number	Manufacturer
C23 to C25	Monoceramic capacitors, 330 pF	GRM1555C1H331JA01D	Murata
R10, R11, R14, R15, R22, R25, R28, R31, R42 to R45	Resistor chips, SMD jumper, 0 Ω	ERJ-2GE0R00X	Panasonic
R2, R4, R6, R8	High frequency resistor chip, 0402, 50 Ω	FC0402E50R0FST1	Vishay Precision Group

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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