High Power, 20 W Peak, Silicon SPDT, Reflective Switch, 0.7 GHz to 5.0 GHz

Data Sheet **ADRF5132**

FEATURES

- Reflective, 50 Ω design
- Low insertion loss: 0.6 dB typical at 2.7 GHz
- High power handling at T_{CASE} = 105°C
  - Long-term (>10 years operation)
    - Peak power: 43 dBm
    - CW power: 38 dBm
    - LTE power average (8 dB PAR): 35 dBm
- Single event (<10 sec operation)
  - LTE power average (8 dB PAR): 41 dBm
- High linearity
  - P0.1dB: 42.5 dBm typical
  - IP3: 65 dBm typical at 2.0 GHz to 4.0 GHz
- ESD ratings
  - HBM: 2 kV, Class 2
  - CDM: 1.25 kV
- Single positive supply: 5 V
- Positive control, CMOS/TTL compatible
- 16-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

- Cellular/4G infrastructure
- Wireless infrastructure
- Military and high reliability applications
- Test equipment
- Pin diode replacement

FUNCTIONAL BLOCK DIAGRAM

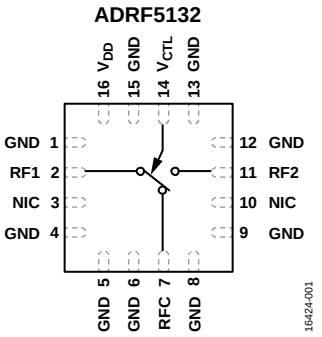


Figure 1.

GENERAL DESCRIPTION

The ADRF5132 is a high power, reflective, 0.7 GHz to 5.0 GHz, silicon, single-pole, double-throw (SPDT) reflective switch in a leadless, surface-mount package. The switch is ideal for high power and cellular infrastructure applications, like long-term evolution (LTE) base stations. The ADRF5132 has high power handling of 35 dBm LTE (average typical at 105°C), a low insertion loss of 0.6 dB at 2.7 GHz, input third-order intercept of 65 dBm (typical), and 0.1 dB compression (P0.1dB) of 42.5 dBm.

The on-chip circuitry operates at a single, positive supply voltage of 5 V and a typical supply current of 1.1 mA typical, making the ADRF5132 an ideal alternative to pin diode-based switches.

The device is in a RoHS compliant, compact, 16-lead, 3 mm × 3 mm LFCSP package.

Rev. B
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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REVISION HISTORY

8/2019—Rev. A to Rev. B

Changes to Figure 11 and Figure 12 7
Updated Outline Dimensions 12

4/2018—Rev. 0 to Rev. A

Changes to Figure 1 1
Changes to Figure 2 and Table 2 5
Changes to Figure 17 11

12/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V, V_{CTL} = 0 V or V_{DD}, T_A = 25°C, and 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.7		5.0	GHz
INSERTION LOSS	0.9 GHz		0.5		dB
	2.7 GHz		0.6		dB
	3.8 GHz		0.65		dB
	5.0 GHz		0.9		dB
ISOLATION					
RFC to RF1/RF2 (Worst Case)	0.7 GHz to 2.0 GHz		50		dB
	2.0 GHz to 5.0 GHz		45		dB
RF1 to RF2 (Worst Case)	0.7 GHz to 2.0 GHz		50		dB
	2.0 GHz to 5.0 GHz		35		dB
RETURN LOSS					
RFC	0.7 GHz to 4.0 GHz		25		dB
	4.0 GHz to 5.0 GHz		15		dB
RFC to RF1/RF2	0.7 GHz to 4.0 GHz		25		dB
	4.0 GHz to 5.0 GHz		15		dB
SWITCHING SPEED					
Rise and Fall Time (t_{RISE}, t_{FALL})	90% to 10% of radio frequency (RF) output		140		ns
On and Off Time (t_{ON}, t_{OFF})	50% V_{CTL} to 10% to 90% of RF output		550		ns
INPUT POWER					
0.1 dB Compression (P0.1dB)			42.5		dB
INPUT THIRD-ORDER INTERCEPT (IP3)	Two-tone input power = 30 dBm per tone at 10 MHz tone spacing				
	0.7 GHz to 2.0 GHz		68		dBm
	2.0 GHz to 4.0 GHz		65		dBm
	4.0 GHz to 5.0 GHz		62		dBm
RECOMMENDED OPERATING CONDITIONS	0.7 GHz to 4.0 GHz				
Bias Voltage Range (V_{DD})		4.5		5.4	V
Control Voltage Range (V_{CTL})		0		V_{DD}	V
Maximum RF Input Power					
T_{CASE} = 105°C[1]	Continuous wave (CW)			38	dBm
	8 dB peak average ratio (PAR), long-term (>10 years operation), average			35	dBm
	8 dB PAR LTE, single event (<10 sec), average			41	dBm
T_{CASE} = 85°C	CW			40	dBm
	8 dB PAR LTE, long-term (>10 years operation), average			35	dBm
	8 dB PAR LTE, single event (<10 sec), average			41	dBm
T_{CASE} = 25°C	CW			43	dBm
	8 dB PAR LTE, long-term (>10 years operation), average			35	dBm
	8 dB PAR LTE, single event (<10 sec), average			41	dBm
Case Temperature Range (T_{CASE})		−40		+105	°C
DIGITAL INPUT CONTROL VOLTAGE	V_{DD} = 4.5 V to 5.4 V, T_{CASE} = −40°C to +105°C, at <1 µA typical				
Low (V_{IL})		0		0.8	V
High (V_{IH})		1.3		5.0	V
SUPPLY CURRENT (I_{DD})	V_{DD} = 5 V		1.1		mA

[1] Peak power is 43 dBm, corresponding to PAR of 8 dB at LTE long-term.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Bias Voltage Range (V_{DD})	−0.3 V to +5.5 V
Control Voltage Range (V_{CTL})	−0.3 V to V_{DD}
RF Input Power[1]	43 dBm
Channel Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +105°C
Peak Reflow Temperature (MSL3)	260°C
ESD Sensitivity	
Human Body Model (HBM)	2 kV (Class 2)
Charged Device Model (CDM)	1.25 kV

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-16-35	17	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

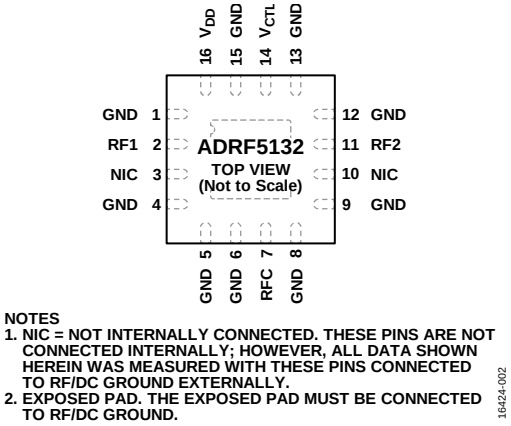


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 5, 6, 8, 9, 12, 13, 15	GND	Ground. See Figure 3 for the GND interface schematic.
2	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
3, 10	NIC	Not Internally Connected. These pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/dc ground externally.
7	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
11	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
14	V_{CTL}	Control Input. See Figure 4 for the V_{CTL} interface schematic. Refer to Table 5 and the recommended digital input control voltage range in Table 1.
16	V_{DD}	Supply Voltage.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

Table 5. Truth Table

	Signal Path State	
Control Input, V_{CTL} State	**RFC to RF1**	**RFC to RF2**
High	Off	On
Low	On	Off

INTERFACE SCHEMATICS



Figure 3. Ground Interface

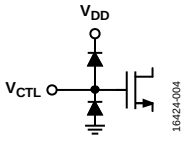


Figure 4. Control Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, RETURN LOSS, THIRD-ORDER INTERCEPT, AND POWER COMPRESSION

V_{DD} = 5 V, V_{CTL} = 0 V or V_{DD}, T_A = 25°C, and 50 Ω system, unless otherwise noted.

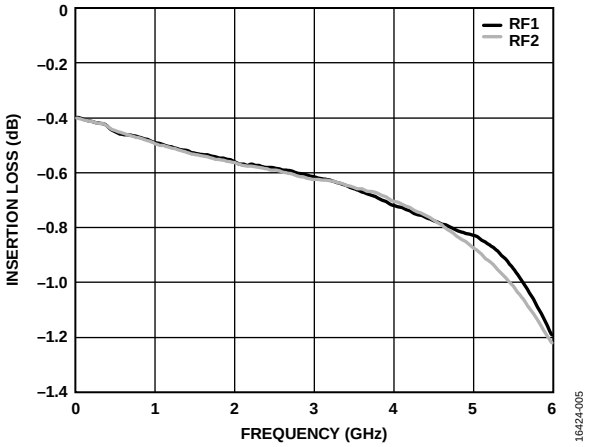


Figure 5. Insertion Loss of RF1 and RF2 vs. Frequency at V_{DD} = 5 V

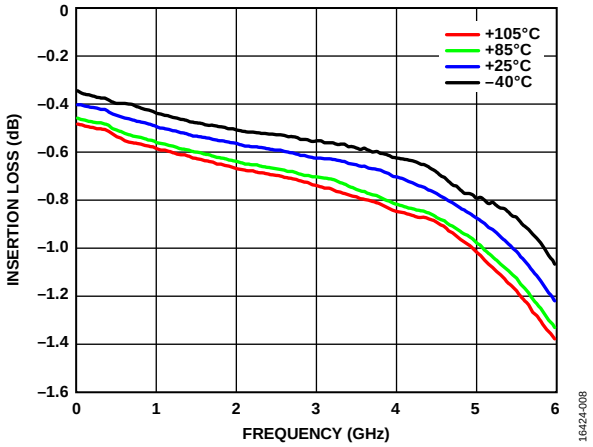


Figure 8. Insertion Loss vs. Frequency over Temperature, V_{DD} = 5 V

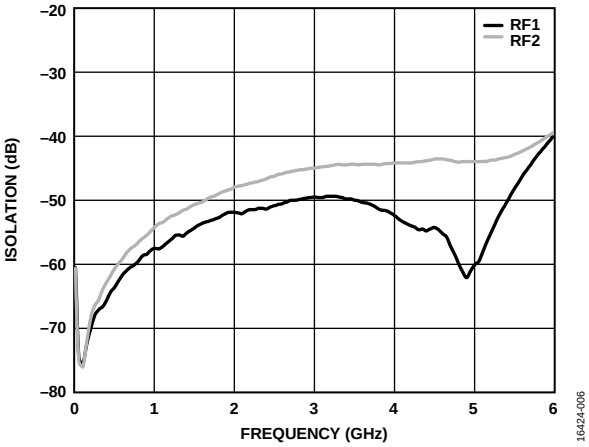


Figure 6. Isolation Between RFC and RF1/RF2 vs. Frequency at V_{DD} = 5 V

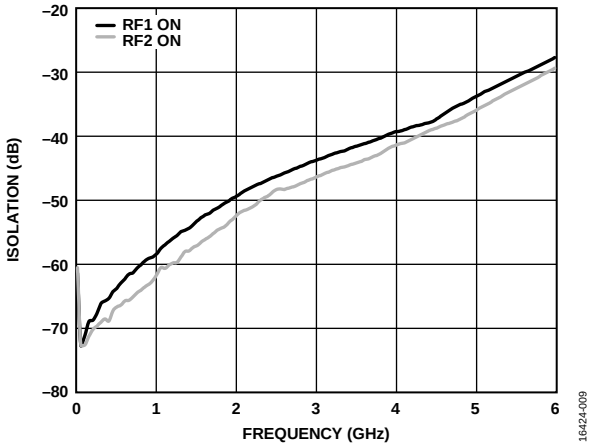


Figure 9. Isolation Between RF1 and RF2 vs. Frequency at V_{DD} = 5 V, Switch Mode On

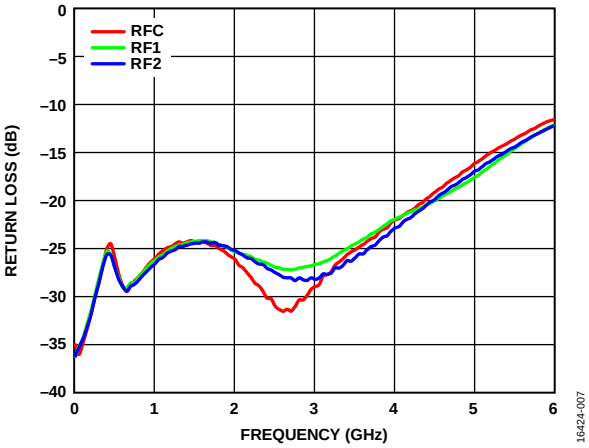


Figure 7. Return Loss vs. Frequency at V_{DD} = 5 V

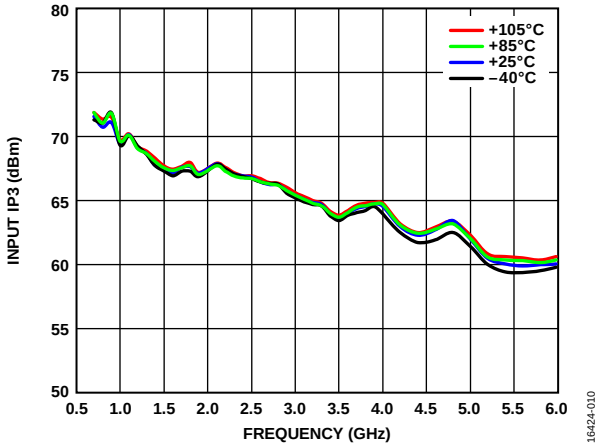


Figure 10. Input IP3 vs. Frequency over Temperature, V_{DD} = 5 V

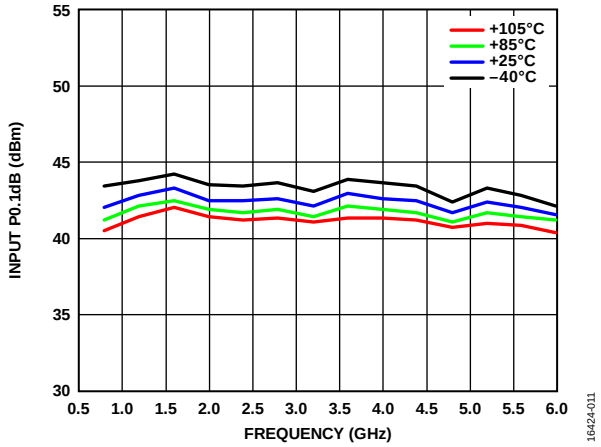


Figure 11. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature, V_{DD} = 5 V

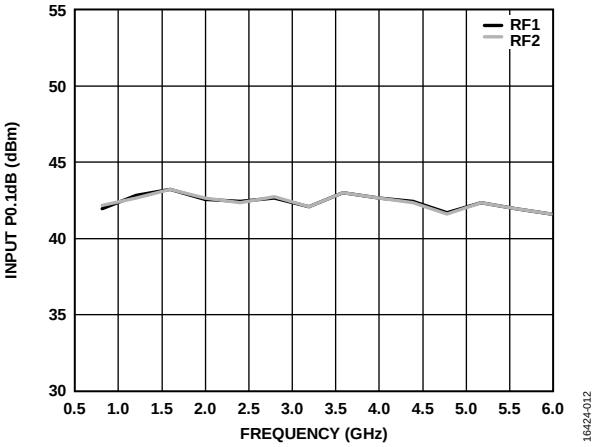


Figure 12. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency, V_{DD} = 5 V

THEORY OF OPERATION

The ADRF5132 requires a single-supply voltage applied to the V_{DD} pin. Bypass capacitors are recommended on the supply line to minimize RF coupling.

The ADRF5132 is controlled via a digital control voltage applied to the V_{CTL} pin. A small bypassing capacitor is recommended on the V_{CTL} signal line to improve the RF signal isolation.

The ADRF5132 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RFx (RFC, RF1, and RF2) pins are dc-coupled, and dc blocking capacitors are required on the RFx lines. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Connect the device to ground.
2. Power up V_{DD}.
3. Power up the digital control input. Powering the digital control input before the V_{DD} supply can inadvertently forward bias and damage ESD protection structures.
4. Power up the RF input. Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from RFC to the output, while the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from RFC.

Table 6. Switch Operation Mode

Digital Control Input, V_{CTL}	Switch Mode	
	RFC to RF1	**RFC to RF2**
1	Off mode: the RF1 port is isolated from RFC and is reflective.	On mode: a low insertion loss path from RFC to the RF2 port.
0	On mode: a low insertion loss path from RFC to the RF1 port.	Off mode: the RF2 port is isolated from RFC and is reflective.

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADRF5132-EVALZ can handle high power levels and temperatures at which the device operates.

The ADRF5132-EVALZ evaluation board is constructed with eight metal layers and dielectrics between each layer as shown in Figure 13. Each metal layer has 1 oz (1.3 mil) copper thickness, whereas the external layers are 1.5 oz copper.

The top dielectric material is 10 mil Rogers RO4350, which exhibits a very low thermal coefficient, offering control over the thermal rise of the board. The dielectrics between the other metal layers are FR4. The total board thickness achieved is 60 mil.

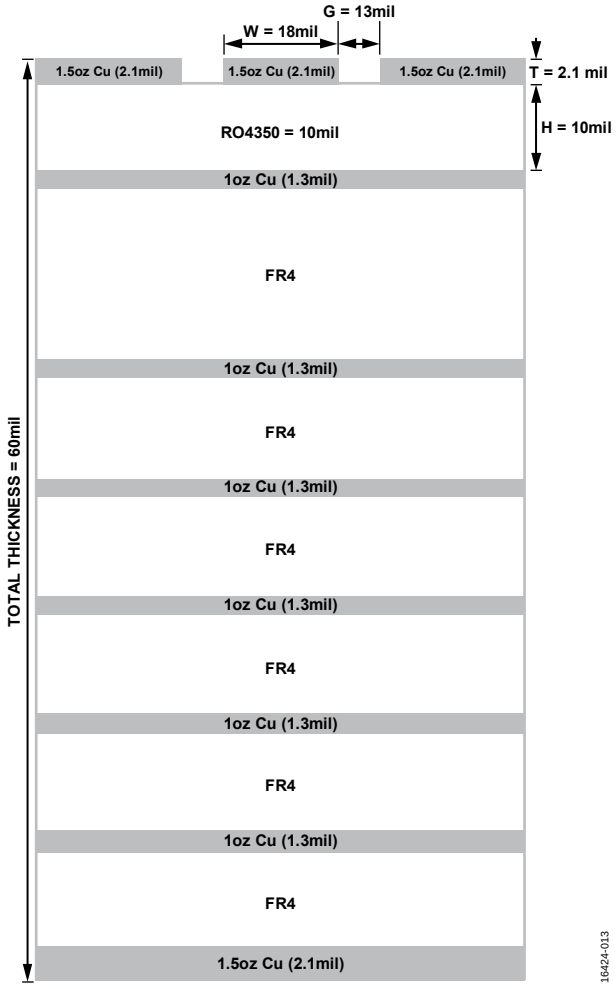


Figure 13. ADRF5132-EVALZ Evaluation Board Cross Sectional View

The top copper layer has all RF and dc traces, whereas the other seven layers provide sufficient ground and help to handle the thermal rise on the ADRF5132-EVALZ. In addition, via holes are provided around transmission lines and under the exposed pad of package, as shown in Figure 15, for proper thermal grounding. RF transmission lines on the evaluation board are coplanar wave guide design with a width of 18 mil and ground spacing of 13 mil.

To ensure maximum heat dissipation and reduce thermal rise on the evaluation board, some application considerations are essential. Attach the ADRF5132-EVALZ to a copper support plate at the bottom of the evaluation board. The ADRF5132-EVALZ comes with this support plate attachment. Attach the ADRF5132-EVALZ with its support plate to a big heat sink using thermal grease during all high power operations. Figure 14 shows the evaluation board temperature vs. RF power input tested with the preceding conditions and precautions (evaluation board and support plate attached to a big heat sink). The temperature rise is less than 5°C up to 43 dBm RF power input, which provides the required thermal dissipation when operated at high power levels.

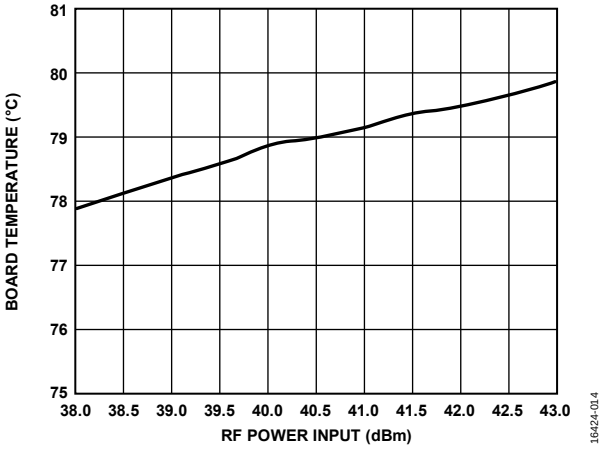


Figure 14. ADRF5132-EVALZ Evaluation Board Temperature Rise (Oven Temperature Set to 75°C)

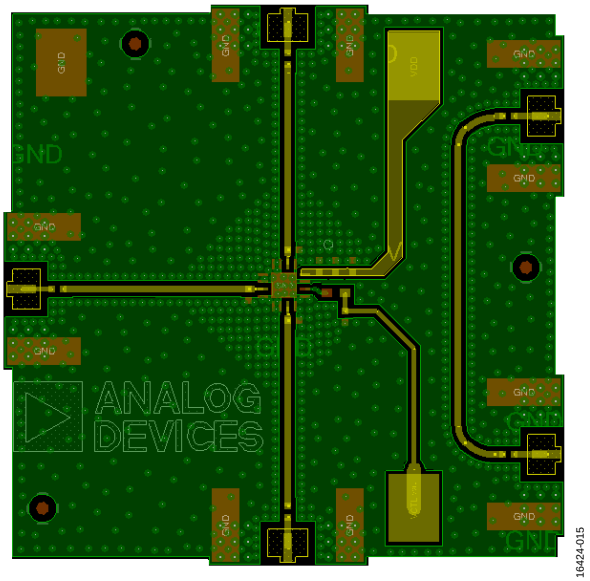


Figure 15. ADRF5132-EVALZ Evaluation Board Layout

APPLICATION CIRCUIT

Generate the evaluation printed circuit board (PCB) used in the application circuit shown in Figure 17 with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and backside ground slug must connect directly to the ground plane. The evaluation board shown in Figure 16 is available from Analog Devices, Inc., upon request.

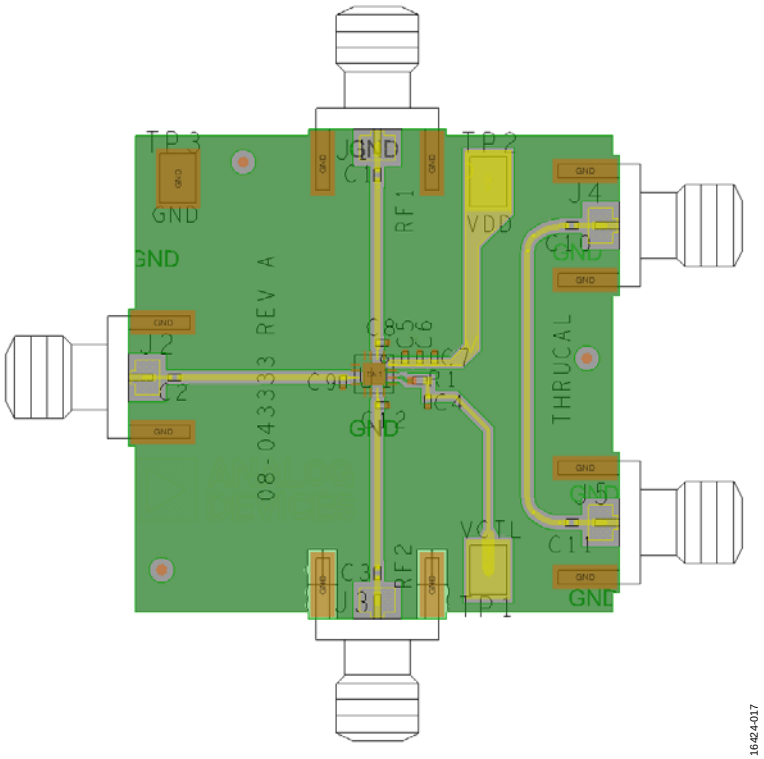


Figure 16. ADRF5132-EVALZ Evaluation Board Component Placement

Table 7. Bill of Materials for ADRF5132-EVALZ Evaluation Board

Reference Designator	Description
J1 to J3	PCB mount SMA connector
C1 to C5	100 pF, 250 V capacitor, 0402 package
C6	1000 pF capacitor, 0402 package
C7	1 µF capacitor, 0402 package
C8, C9, C12	Do not insert
R1	0 Ω resistor, 0402 package
U1	ADRF5132 SPDT switch
PCB[1]	ADRF5132-EVALZ[2] evaluation PCB

[1] Circuit board material: Roger 4350 or Arlon 25FR.
[2] Reference this evaluation board number when ordering the complete evaluation board.

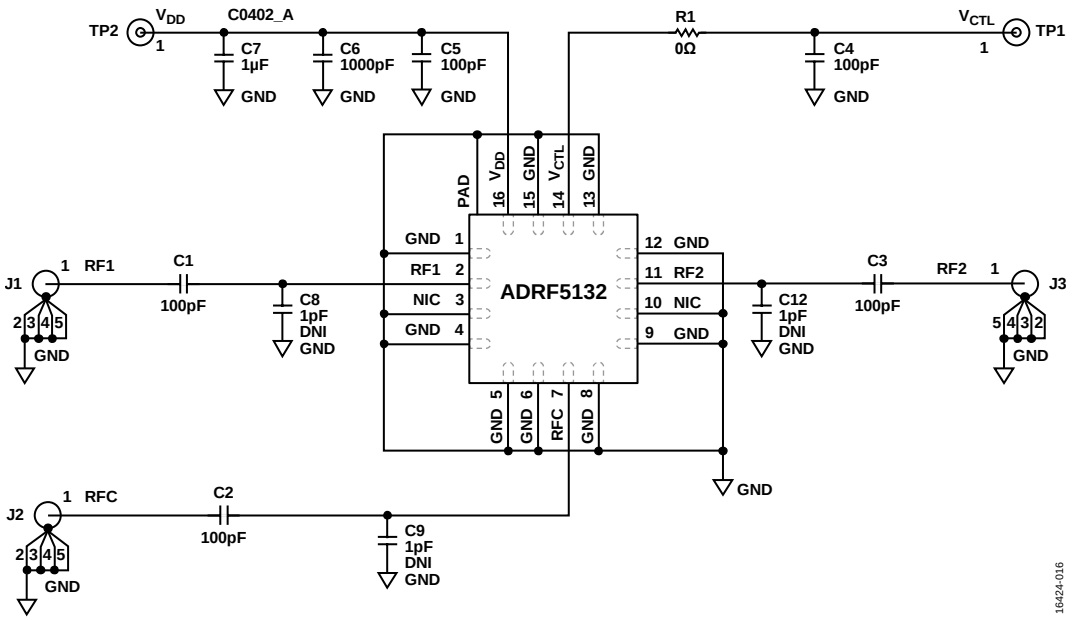


Figure 17. Application Circuit

OUTLINE DIMENSIONS

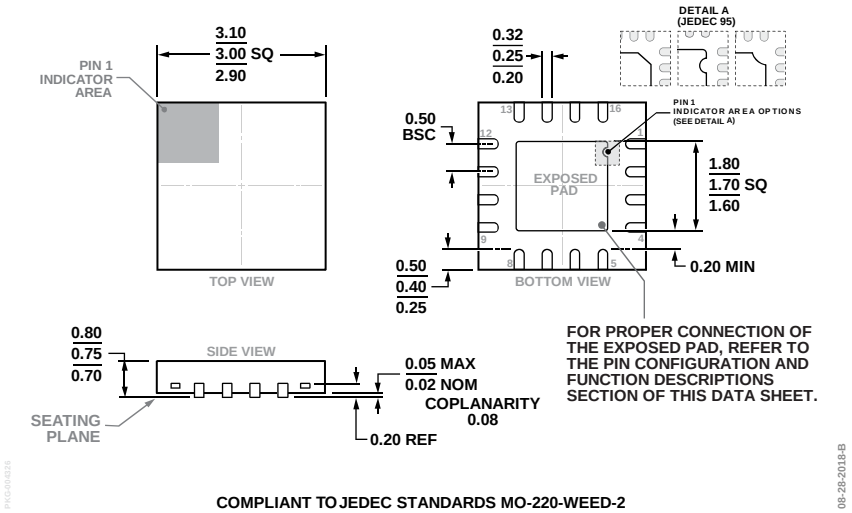


Figure 18. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-35)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5132BCPZN	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-35
ADRF5132BCPZN-R7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-35
ADRF5132-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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