100 MHz to 30 GHz, Silicon SPDT Switch

Data Sheet **ADRF5020**

FEATURES

- Ultrawideband frequency range: 100 MHz to 30 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 2.0 dB to 30 GHz
- High isolation: 60 dB to 30 GHz
- High input linearity
  - 1 dB power compression (P1dB): 28 dBm typical
  - Third-order intercept (IP3): 52 dBm typical
- High power handling
  - 24 dBm through path
  - 24 dBm terminated path
- ESD sensitivity: Class 1, 1 kV human body model (HBM)
- 20-terminal, 3 mm × 3 mm, land grid array package
- No low frequency spurious
- Radio frequency (RF) settling time (to 0.1 dB of final RF output): 15 ns

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

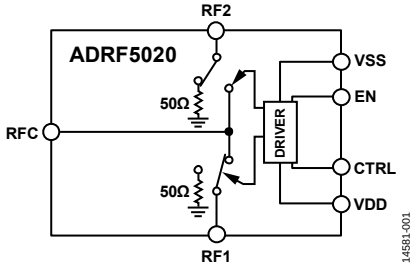


Figure 1.

GENERAL DESCRIPTION

The ADRF5020 is a general-purpose, single-pole, double-throw (SPDT) switch manufactured using a silicon process. It comes in a 3 mm × 3 mm, 20-terminal land grid array (LGA) package and provides high isolation and low insertion loss from 100 MHz to 30 GHz.

This broadband switch requires dual supply voltages, +3.3 V and −2.5 V, and provides CMOS/LVTTL logic-compatible control.

Rev. B
Document Feedback

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REVISION HISTORY

4/2020—Rev. A to Rev. B

Changes to Table 2 5
Changes to Theory of Operation Section 9

2/2017—Rev. 0 to Rev. A

Changed V_{EN} = 3.3 V to 5 V to V_{EN} = 0 V or 3.3 V to 5 V 3

7/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V to 5 V, V_{SS} = −2.5 V, V_{CTRL} = 0 V or 3.3 V to 5 V, V_{EN} = 0 V or 3.3 V to 5 V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		30,000	MHz
INSERTION LOSS						
Between RFC and RF1/RF2		100 MHz to 10 GHz		1.2		dB
		10 GHz to 20 GHz		1.5		dB
		20 GHz to 30 GHz		2.0		dB
ISOLATION						
Between RFC and RF1/RF2		100 MHz to 10 GHz		65		dB
		10 GHz to 20 GHz		60		dB
		20 GHz to 30 GHz		60		dB
Between RF1 and RF2		100 MHz to 10 GHz		70		dB
		10 GHz to 20 GHz		65		dB
		20 GHz to 30 GHz		65		dB
RETURN LOSS						
RFC and RF1/RF2 (On)		100 MHz to 10 GHz		22		dB
		10 GHz to 20 GHz		16		dB
		20 GHz to 30 GHz		13		dB
RF1/RF2 (Off)		100 MHz to 10 GHz		28		dB
		10 GHz to 20 GHz		20		dB
		20 GHz to 30 GHz		10		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		2		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		10		ns
RF Settling Time						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		15		ns
0.05 dB		50% V_{CTL} to 0.05 dB of final RF output		20		ns
INPUT LINEARITY[1]		600 MHz to 30 GHz				
Power Compression						
0.1 dB	P0.1dB			26		dBm
1 dB	P1dB			28		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, Δf = 1 MHz		52		dBm
SUPPLY CURRENT		VDD, VSS pins				
Positive	I_{DD}	V_{DD} = 3.3 V		80	300	µA
		V_{DD} = 5 V		100	600	µA
Negative	I_{SS}	V_{SS} = −2.5 V		<1	10	µA
DIGITAL CONTROL INPUTS		CTRL, EN pins				
Voltage						
Low	V_{INL}	V_{DD} = 3.3 V	0		0.8	V
		V_{DD} = 5 V			0.9	V
High	V_{INH}	V_{DD} = 3.3 V	1.2		3.3	V
		V_{DD} = 5 V	1.7		5.0	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.0		5.4	V
Negative	V_{SS}		−2.75		−2.25	V
Digital Control Voltage	V_{CTL}		0		V_{DD}	V
RF Input Power[2]	P_{IN}	f = 600 MHz to 30 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or through connected RF1/RF2			24	dBm
Terminated Path		RF signal is applied to terminated RF1/RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			18	dBm
Case Temperature	T_{CASE}		−40		+85	°C

[1] For input linearity performance at frequencies less than 600 MHz, see Figure 15 to Figure 17.
[2] For power derating at frequencies less than 600 MHz, see Figure 2 to Figure 4.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +5.5 V
Negative	−2.75 V to +0.3 V
Digital Control Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 3.3 mA, whichever occurs first
RF Input Power[2] (f = 600 MHz to 30 GHz, T_{CASE}) = 85°C)	
Through Path	27 dBm
Terminated Path	25 dBm
Hot Switching	21 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow (MSL3 Rating)[3]	260°C
Junction to Case Thermal Resistance (θ_{JC})	
Through Path	420°C/W
Terminated Path	160°C/W
ESD Sensitivity	
HBM	1 kV (Class 1)

[1] Overvoltages at digital control inputs are clamped by internal diodes. The current must be limited to the maximum rating.
[2] For power derating at frequencies less than 600 MHz, see Figure 2 to Figure 4.
[3] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

POWER DERATING CURVES

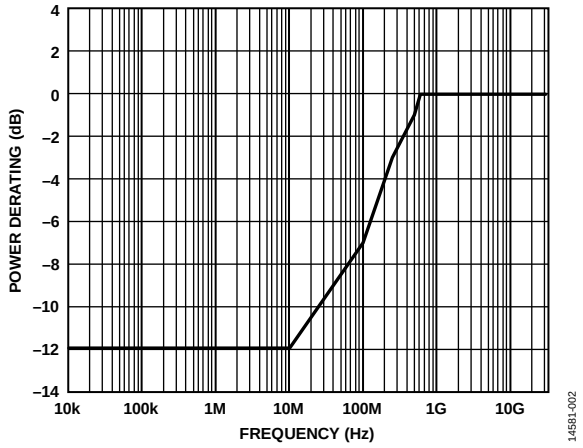


Figure 2. Power Derating for Through Path vs. Frequency, T_{CASE} = 85°C

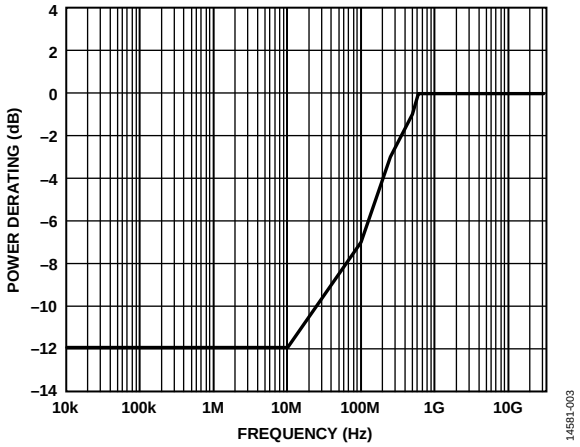


Figure 3. Power Derating for Terminated Path vs. Frequency, T_{CASE} = 85°C

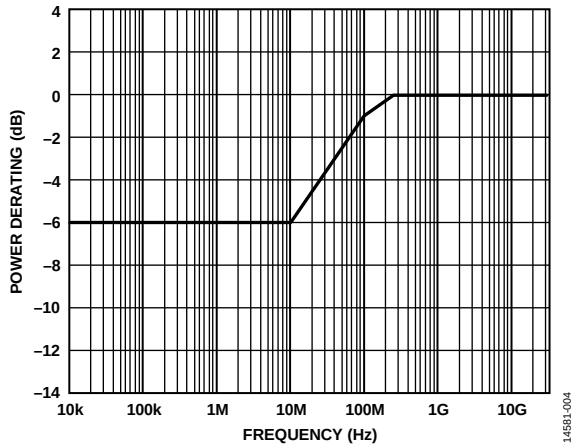


Figure 4. Power Derating for Hot Switching vs. Frequency, T_{CASE} = 85°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

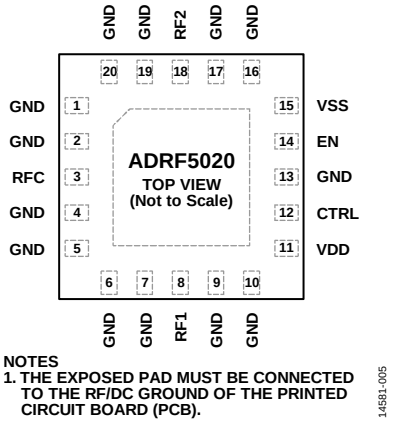


Figure 5. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
8	RF1	RF1 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
11	VDD	Positive Supply Voltage.
12	CTRL	Control Input. See Figure 7 for the interface schematic.
14	EN	Enable Input. See Figure 7 for the interface schematic.
15	VSS	Negative Supply Voltage.
18	RF2	RF2 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

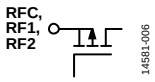


Figure 6. RFC, RF1, and RF2 Pins Interface Schematic

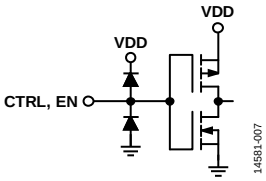


Figure 7. Digital Pins (CTRL and EN) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

Insertion loss and return loss measured on the probe matrix board using the ground, signal, ground (GSG) probes close to the RF pins; isolation measured on an evaluation board because signal coupling between the probes limits the isolation performance of the ADRF5020 on the probe matrix board (see the Applications Information section for details of evaluation and probe matrix boards).

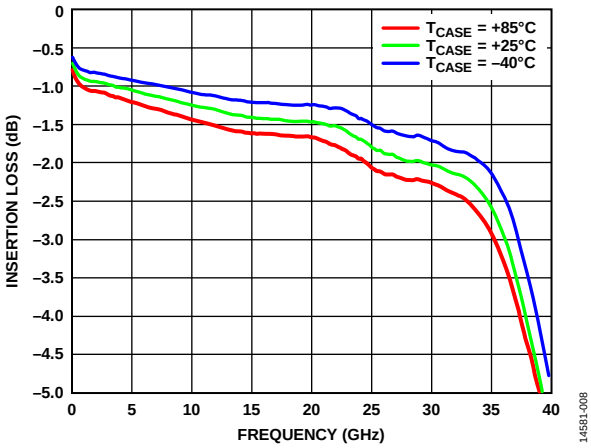


Figure 8. Insertion Loss Between RFC and RF1/RF2 vs. Frequency over Temperature

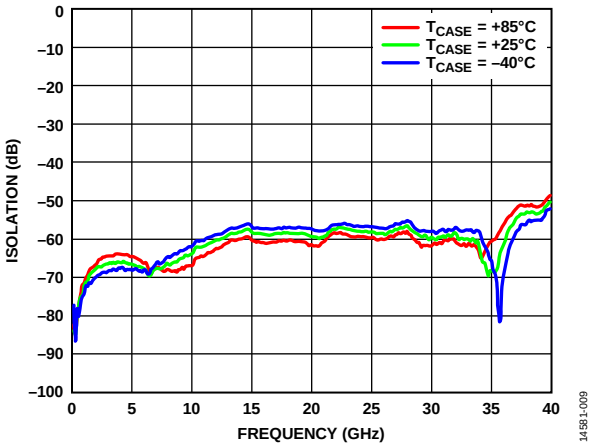


Figure 9. Isolation Between RFC and RF1/RF2 vs. Frequency over Temperature

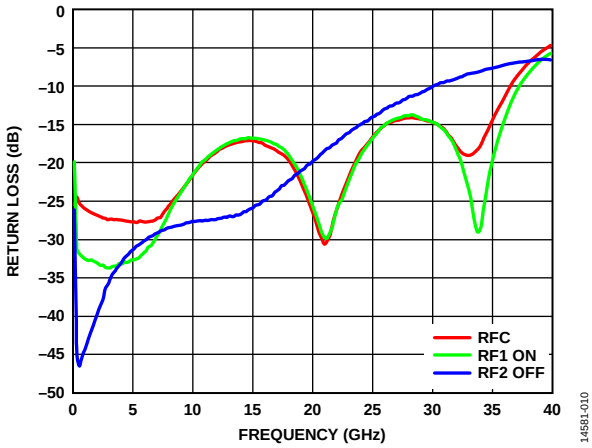


Figure 10. Return Loss vs. Frequency for RFC, RF1 On, and RF2 Off

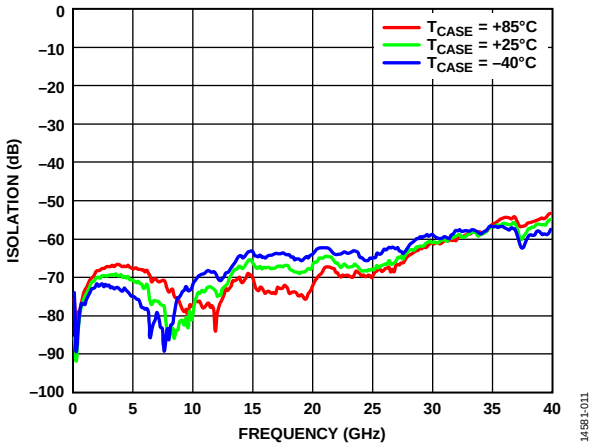


Figure 11. Isolation Between RF1 and RF2 vs. Frequency over Temperature

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT (IP3)

All large signal performance parameters were measured on the evaluation board.

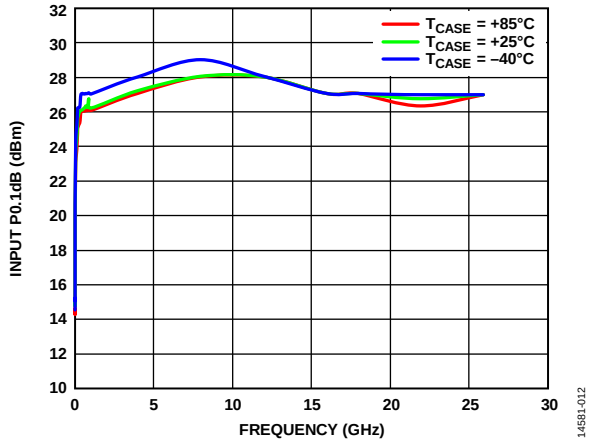


Figure 12. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature

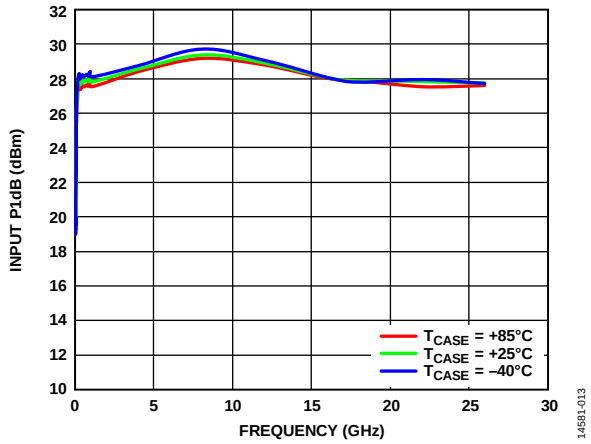


Figure 13. Input 1 dB Power Compression (P1dB) vs. Frequency over Temperature

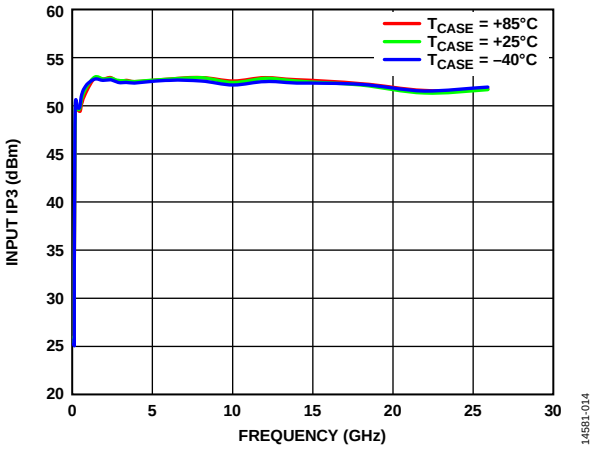


Figure 14. Input IP3 vs. Frequency over Temperature

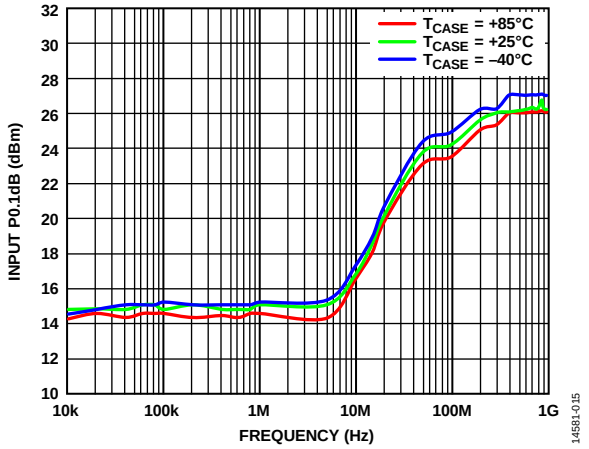


Figure 15. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature (Low Frequency Detail)

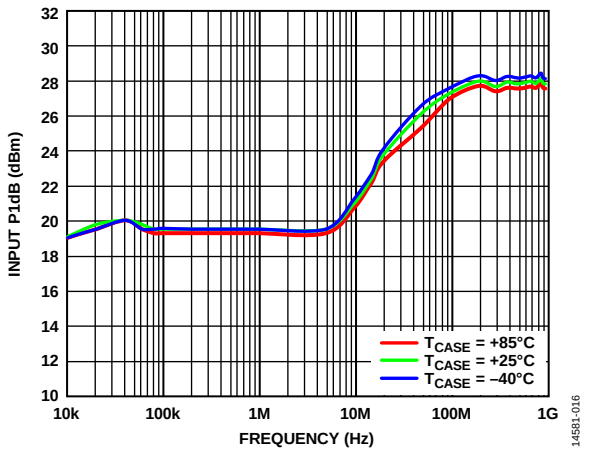


Figure 16. Input 1 dB Power Compression (P1dB) vs. Frequency over Temperature (Low Frequency Detail)

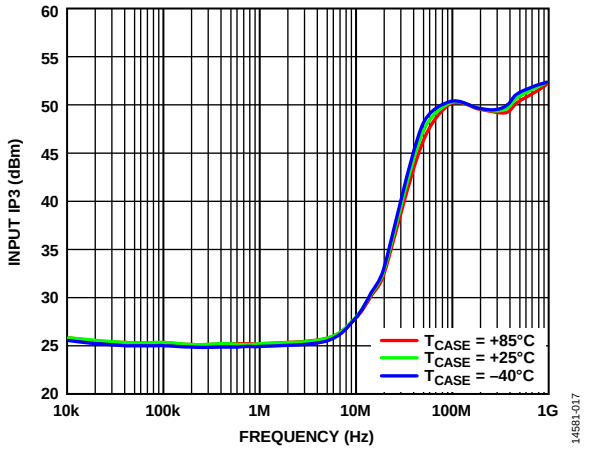


Figure 17. Input IP3 vs. Frequency over Temperature (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5020 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ADRF5020 is internally matched to 50 Ω at the RF common port (RFC) and the RF throw ports (RF1 and RF2); therefore, no external matching components are required. All of the RF ports are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The design is bidirectional; the RF input signal can be applied to the RFC port while the RF throw port (RF1 or RF2) is output or vice versa.

The ADRF5020 incorporates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features two digital control input pins, CTRL and EN.

When the EN pin is logic low, the RF1 to RFC path is in an insertion loss state, and the RF2 to RFC path is in an isolation state, or vice versa, depending on the logic level applied to the CTRL pin. The insertion loss path (for example, RF1 to RFC) conducts the RF signal equally well in both directions between its throw port (for example, RF1) and common port (RFC). The isolation path (for example, RF2 to RFC) provides high loss between the insertion loss path and its throw port (for example, RF2) terminated to an internal 50 Ω resistor.

When the EN pin is logic high, both the RF1 to RFC path and the RF2 to RFC path are in an isolation state regardless of the logic state of CTRL. RF1 and RF2 ports are terminated to internal 50 Ω resistors, and RFC becomes open reflective.

The ideal power-up sequence is as follows:

1. Connect EPAD and GND pins to ground reference.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.
3. Apply the digital control inputs CTRL and EN. Applying digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. A series 1.5 kΩ resistor can be used to limit the current flowing into the control pin in this case. If the control pins are not driven to a valid logic state (for example, the controller output is in high impedance state) after VDD is powered up, it is recommended to use pull up/down resistors.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

EVALUATION BOARD

Figure 18 and Figure 19 show the top and cross sectional views of the evaluation board, which uses 4-layer construction with a copper thickness of 0.5 oz (0.7 mil) and dielectric materials between each copper layer.

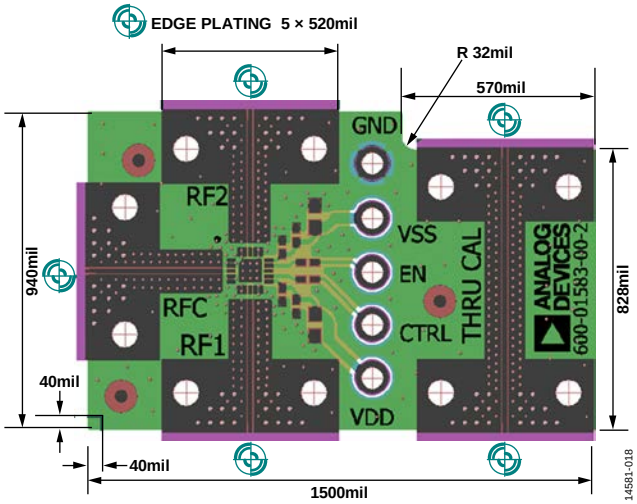


Figure 18. Evaluation Board Layout (Top View)

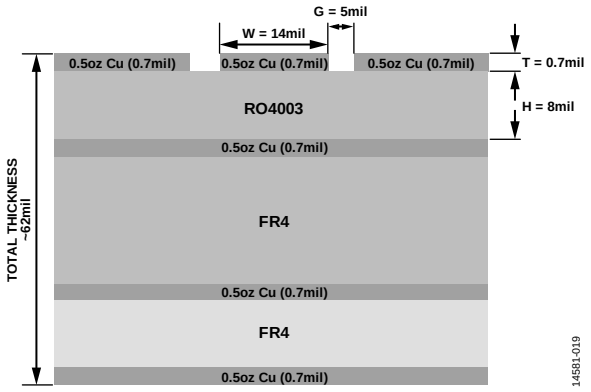


Figure 19. Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. Top dielectric material is 8 mil Rogers RO4003, offering good high frequency performance. The middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 5 mil to have a characteristic impedance of 50 Ω. For good RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 20 shows the actual ADRF5020 evaluation board with component placement. Two power supply ports are connected to the VDD and VSS test points, TP5 and TP2, and the ground reference is connected to the GND test point, TP1. On each supply trace, a 100 pF bypass capacitor is used, and unpopulated components positions are available for applying extra bypass capacitors.

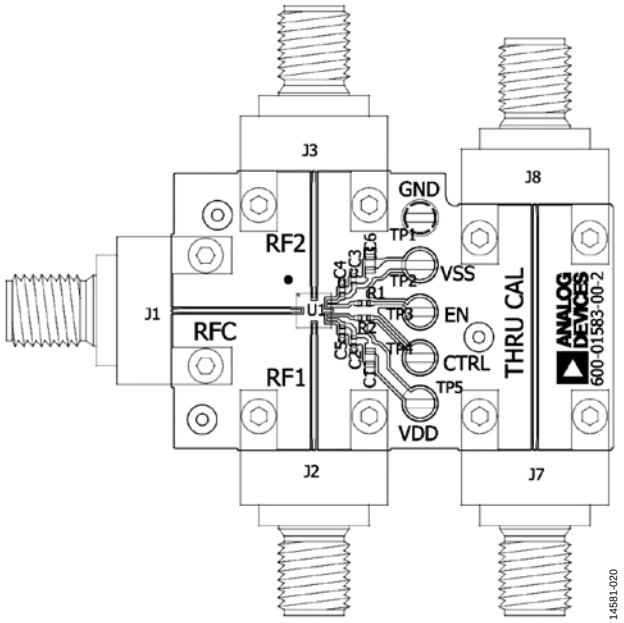


Figure 20. Populated Evaluation Board

Two control ports are connected to the EN and CTRL test points, TP3 and TP4. On each control trace, a resistor position is available to improve the isolation between the RF and control signals. The RF ports are connected to the RFC, RF1, and RF2 connectors (J1, J2, and J3) that are end launch 2.4 mm RF connectors. A through transmission line that connects unpopulated RF connectors (J7 and J8) is also available to measure the loss of the PCB. Figure 21 and Table 5 are the evaluation board schematic and bill of materials, respectively.

The evaluation board shown in Figure 20 is available from Analog Devices, Inc., upon request.

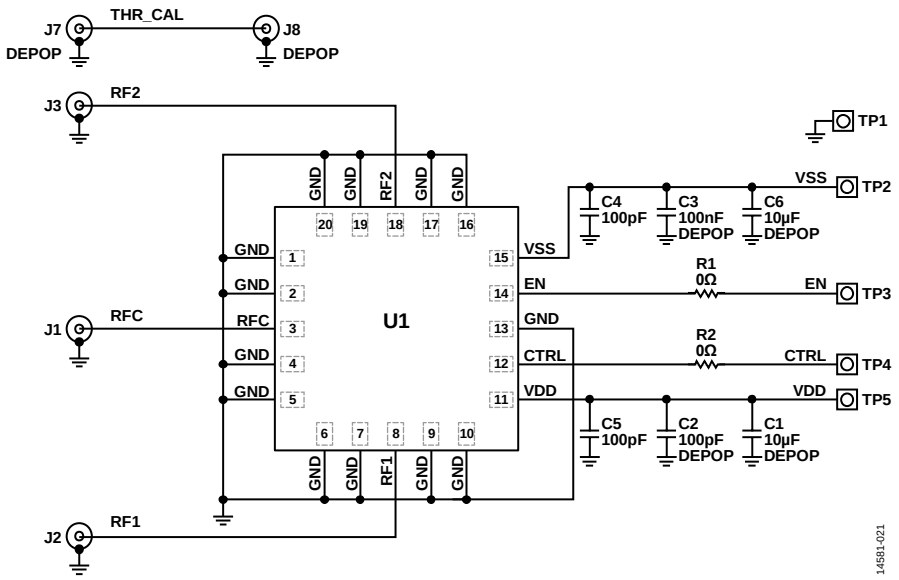


Figure 21. Evaluation Board Schematic

Table 5. Bill of Materials, Evaluation Board Components

Component	Description
J1, J2, J3	End launch connectors, 2.4 mm
J7, J8	Unpopulated end launch connectors, 2.4 mm
TP1 to TP5	Through hole mount test points
C4, C5	100 pF capacitors, 0402 package
C2, C3	Unpopulated capacitors, 0402 package
C1, C6	Unpopulated capacitors, 0603 package
R1, R2	0 Ω resistors, 0402 package
U1	ADRF5020 SPDT switch
PCB	600-01583-00-1 evaluation PCB

PROBE MATRIX BOARD

Figure 22 and Figure 23 show the top and cross sectional views of the probe matrix board that measures the s-parameters of the ADRF5020 at close proximity to the RF pins using the GSG probes. The actual board duplicates the same layout in matrix form to assemble multiple devices and uses RF traces for through, reflect, and line (TRL) calibration.

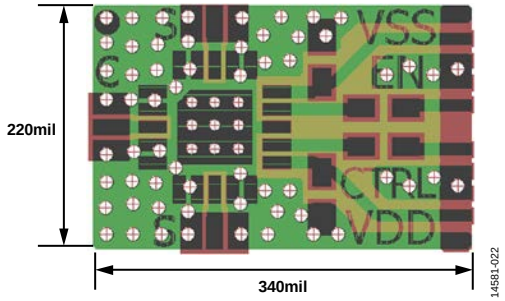


Figure 22. Probe Board Layout (Top View)

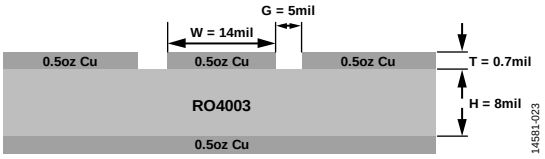


Figure 23. Probe Matrix Board (Cross Sectional View)

OUTLINE DIMENSIONS

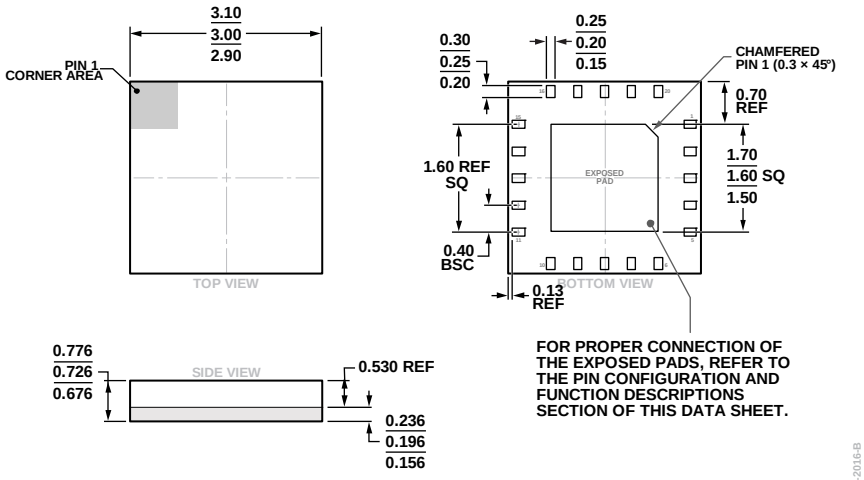


Figure 24. 20-Terminal Land Grid Array [LGA]
3 mm × 3 mm Body and 0.72 mm Package Height
(CC-20-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Marking Code[3]
ADRF5020BCCZN	−40°C to +85°C	MSL3	20-Terminal Land Grid Array [LGA]	CC-20-3	020 XXXX
ADRF5020BCCZN-R7	−40°C to +85°C	MSL3	20-Terminal Land Grid Array [LGA]	CC-20-3	020 XXXX
ADRF5020-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section.
[3] XXXX is the 4-digit lot number.

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