Ultralow Noise, LDO, XFET, Voltage Reference with Current Sink and Source

Data Sheet

ADR441ACHIPS

FEATURES

- Ultralow voltage noise (0.1 Hz to 10 Hz): 1.2 µV p-p
- Low temperature drift: 10 ppm/°C maximum
- Low dropout operation (supply voltage headroom): 500 mV
- Supply voltage operating range: 3 V to 18 V
- Output sourcing and sinking current capacity: +10 mA typical and −5 mA typical, respectively
- Wide temperature range: −40°C to +125°C

APPLICATIONS

- Precision data acquisition systems
- High resolution data converters
- Battery-powered instrumentation
- Portable medical instruments
- Industrial process control systems
- Precision instruments
- Optical control circuits

METAL MASK DIE IMAGE

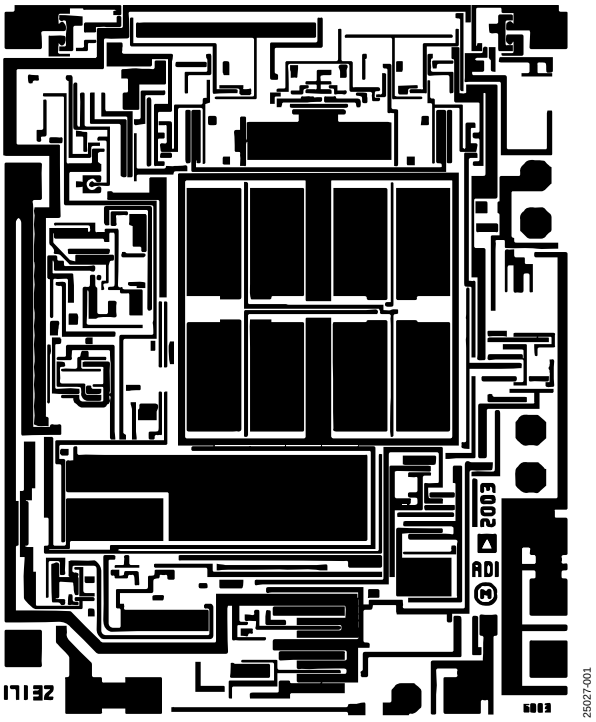

Figure 1.

GENERAL DESCRIPTION

The ADR441ACHIPS[1] is an extra implanted junction FET (XFET®) voltage reference that features ultralow noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., temperature drift curvature correction and XFET technology, voltage change vs. temperature nonlinearity in the ADR441ACHIPS is greatly minimized.

This XFET reference offers better noise performance (ultralow voltage noise of 1.2 µV p-p and voltage noise density at 1 kHz of 48 nV/√Hz) than buried Zener references and operates off a low supply voltage headroom (500 mV). This combination of features makes the ADR441ACHIPS ideally suited for precision signal conversion applications in high end data acquisition systems, optical networks, and medical applications.

The ADR441ACHIPS has the capability to source up to +10 mA of output current and sink up to −5 mA of output current. The device also comes with a TRIM terminal to adjust the output voltage over a 0.5% range without compromising performance.

Additional application and technical information can be found in the ADR441 data sheet.

[1] Protected by U.S. Patent Number 5,838,192.

Rev. 0 Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2020 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features 1
Applications 1
Metal Mask Die Image 1
General Description 1
Revision History 2
Specifications 3
Absolute Maximum Ratings 4
ESD Caution 4
Pin Configuration and Function Descriptions 5
Outline Dimensions 6
Ordering Guide 6

REVISION HISTORY

10/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3 V to 18 V, T_A = 25°C, input capacitance (C_{IN}) = 0.1 µF, and output capacitance (C_{OUT}) = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		2.497	2.500	2.503	V
INITIAL ACCURACY	V_{OERR}				±3	mV
					0.12	%
TEMPERATURE DRIFT	TCV_{OUT}			2	10	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$			10	20	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$					
Sourcing		Load current (I_{LOAD}) = 0 mA to 10 mA, V_{IN} = 4 V	−50		+50	ppm/mA
Sinking		I_{LOAD} = 0 mA to −5 mA, V_{IN} = 4 V	−50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	I_{LOAD}					
Sourcing				10		mA
Sinking				−5		mA
QUIESCENT CURRENT	I_{IN}	No load		3	3.75	mA
VOLTAGE NOISE						
0.1 Hz to 10 Hz	e_N p-p			1.2		µV p-p
Density	e_N	1 kHz		48		nV/√Hz
TURN-ON SETTLING TIME	t_R			10		µs
LONG-TERM STABILITY[1]	ΔV_{OUT}	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{OUT_HYS}			70		ppm
RIPPLE REJECTION RATIO		Input frequency (f_{IN}) = 1 kHz		−80		dB
SHORT CIRCUIT TO GND	I_{SC}			27		mA
SUPPLY VOLTAGE						
Operating Range	V_{IN}		3		18	V
Headroom	$V_{IN} - V_{OUT}$		500			mV

[1] The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Temperature Range	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

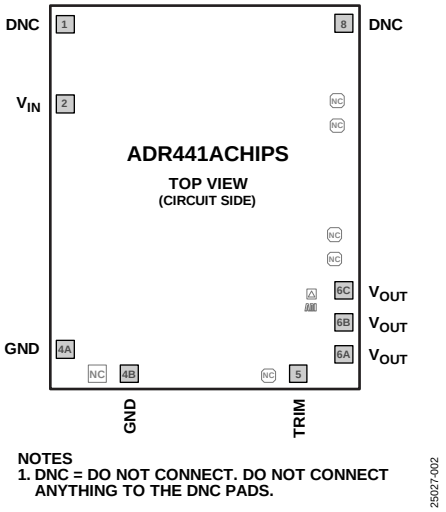

Figure 2. Pad Configuration

Table 3. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−731	+905	DNC	Do Not Connect. Do not connect anything to the DNC pads.
2	−731	+489	V_{IN}	Input Voltage Connection.
4A	−731	−798	GND	Ground. Connect to other GND pad.
4B	−396	−926	GND	Ground. Connect to other GND pad.
5	+491	−926	TRIM	Output Voltage Trim. Use the TRIM pad to finely adjust the output voltage.
6A	+731	−825	V_{OUT}	Output Voltage. Connect to other V_{OUT} pads.
6B	+731	−657	V_{OUT}	Output Voltage. Connect to other V_{OUT} pads.
6C	+731	−489	V_{OUT}	Output Voltage. Connect to other V_{OUT} pads.
8	+731	+905	DNC	Do Not Connect. Do not connect anything to the DNC pads.

OUTLINE DIMENSIONS

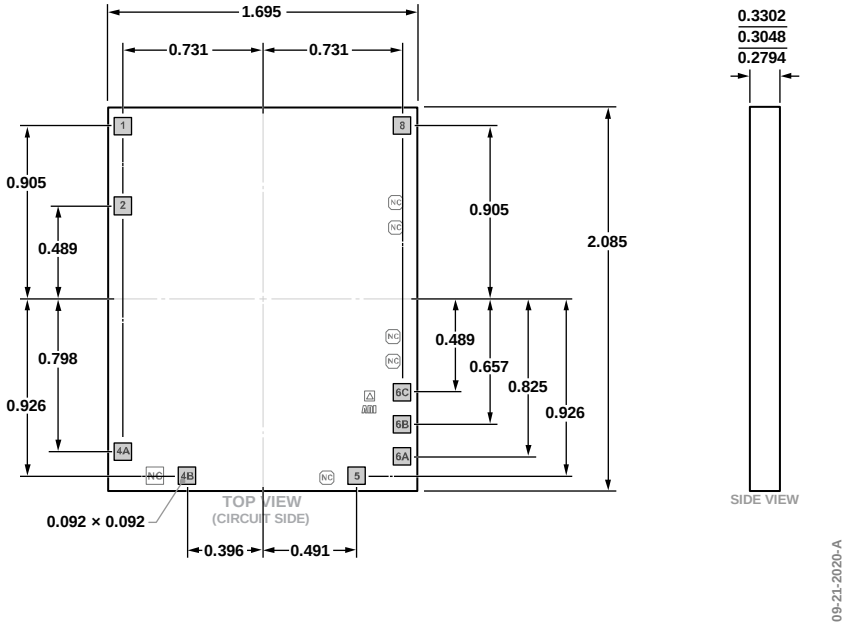

Figure 3. 9-Pad Bare Die [CHIP]
(C-9-3)
Dimensions shown in millimeters

Table 4. Die Specifications

Parameter	Value	Unit
Chip Size	1620 × 2010	µm
Scribe Line Width	75	µm
Die Size	1695 × 2085	µm
Thickness	12 ± 1	mils
Bond Pads (Minimum)	92 × 92	µm
Bond Pad Composition	Aluminum copper (AlCu), 0.5	%
Passivation	Doped-oxide/silicon nitride (SiN)	Not applicable
Polyimide	5	µm
Die Marker	1713	Not applicable
Backside	Not applicable (left floating)	Not applicable

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	LOCTITE® ABLESTIK 84-1LMISR4 conductive
Bonding Method	Forward bond
Bonding Sequence	Lead to bond first = 1

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADR441ACHIPS	−40°C to +125°C	9-Pad Bare Die [CHIP]	C-9-3

[1] The ADR441ACHIPS is a RoHS compliant part.

©2020 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D25027-10/20(0)