



Low Noise XFET Voltage References with Current Sink and Source Capability

Data Sheet

ADR431-EP/ADR434-EP/ADR435-EP

FEATURES

Low noise (0.1 Hz to 10.0 Hz): 3.5 μV p-p at 2.5 V_o typical
([ADR431-EP](#))

No external capacitor required

Low temperature coefficient

5 ppm/ $^{\circ}\text{C}$ maximum ([ADR431-EP](#))

3 ppm/ $^{\circ}\text{C}$ maximum ([ADR434-EP/ADR435-EP](#))

Load regulation: 15 ppm/mA maximum

Line regulation: 20 ppm/V maximum

Wide supply voltage operating range: 4.5 V to 18 V
([ADR431-EP](#))

High output source and sink current: +10 mA and –10 mA

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications, aerospace
qualified electronic component (AQEC) standard

Military temperature range: -55°C to $+125^{\circ}\text{C}$

Controlled manufacturing baseline

One assembly and test site

One fabrication site

Enhanced product change notification

Qualification data available on request

APPLICATIONS

Precision data acquisition systems

High resolution data converters

Optical control circuits

Precision instruments

GENERAL DESCRIPTION

The [ADR431-EP/ADR434-EP/ADR435-EP](#) are XFET[®] voltage references featuring low noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., patented temperature drift curvature correction and eXtra implanted junction FET (XFET) technology, voltage change vs. temperature nonlinearity in the [ADR431-EP/ADR434-EP/ADR435-EP](#) is minimized.

The XFET references operate at lower current (800 μA) and lower supply voltage headroom (2 V) than buried Zener references. Buried Zener references require more than 5 V headroom for operation. The [ADR431-EP/ADR434-EP/ADR435-EP](#) XFET references are optimal low noise solutions for 5 V systems.

PIN CONFIGURATION



NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1. 8-Lead SOIC_N (R-8)

The [ADR431-EP/ADR434-EP/ADR435-EP](#) have the capability to source up to +10 mA of output current and sink up to –10 mA. They also come with a trim terminal to adjust the output voltage over a 0.5% range without compromising performance.

The [ADR431-EP/ADR434-EP/ADR435-EP](#) are available in an 8-lead narrow SOIC package and are specified over the military temperature range of -55°C to $+125^{\circ}\text{C}$.

Additional application and technical information can be found in the [ADR430/ADR431/ADR433/ADR434/ADR435](#) data sheet.

Table 1. Selection Guide

Model	Output Voltage (V)	Accuracy (mV)	Temperature Coefficient (ppm/ $^{\circ}\text{C}$)
ADR431T-EP	2.500	± 1.0	5
ADR434T-EP	4.096	± 1.5	3
ADR435T-EP	5.000	± 2.0	3

Rev. B

[Document Feedback](#)

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TABLE OF CONTENTS

Features	1	ADR431-EP Electrical Characteristics	5
Enhanced Product Features	1	Absolute Maximum Ratings	6
Applications.....	1	Thermal Resistance.....	6
Pin Configuration.....	1	ESD Caution.....	6
General Description	1	Pin Configuration and Function Descriptions.....	7
Revision History	2	Typical Performance Characteristics	8
Specifications.....	3	Outline Dimensions	9
ADR431-EP Electrical Characteristics	3	Ordering Guide	9
ADR434-EP Electrical Characteristics	4		

REVISION HISTORY

5/2017—Rev. A to Rev. B

Deleted ADR439	Throughout
Added Pin Configuration and Function Descriptions Section, Figure 2; Renumbered Sequentially, and Table 7	7
Changes to Typical Performance Characteristics Section.....	8

8/2010—Rev. 0 to Rev. A

Added ADR431-EP.....	Throughout
Added ADR435-EP.....	Throughout
Changes to Ordering Guide	8

7/2010—Revision 0: Initial Version

SPECIFICATIONS

ADR431-EP ELECTRICAL CHARACTERISTICS

$V_{IN} = 4.5\text{ V}$ to 18 V , $I_L = 0\text{ mA}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O		2.499	2.500	2.501	V
INITIAL ACCURACY	V_{OERR}				± 1.0 ± 0.04	mV %
TEMPERATURE COEFFICIENT	TCV_O	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	5	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O / \Delta V_{IN}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		5	20	ppm/V
LOAD REGULATION	$\Delta V_O / \Delta I_L$	$I_L = 0\text{ mA}$ to 10 mA , $V_{IN} = 5\text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$ $I_L = -10\text{ mA}$ to 0 mA , $V_{IN} = 5\text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$			15 15	ppm/mA ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		580	800	μA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.5		μV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		80		nV/ $\sqrt{\text{Hz}}$
TURN ON SETTLING TIME	t_R	$C_L = 0\text{ }\mu\text{F}$		10		μs
LONG-TERM STABILITY ¹	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		-70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

¹ The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR434-EP ELECTRICAL CHARACTERISTICS

$V_{IN} = 6.1 \text{ V}$ to 18 V , $I_L = 0 \text{ mA}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O		4.0945	4.096	4.0975	V
INITIAL ACCURACY	V_{OERR}				± 1.5 ± 0.04	mV %
TEMPERATURE COEFFICIENT	TCV_O	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O / \Delta V_{IN}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		5	20	ppm/V
LOAD REGULATION	$\Delta V_O / \Delta I_L$	$I_L = 0 \text{ mA}$ to 10 mA , $V_{IN} = 7 \text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$ $I_L = -10 \text{ mA}$ to 0 mA , $V_{IN} = 7 \text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$			15 15	ppm/mA ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		595	800	μA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		6.25		μV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		100		nV/ $\sqrt{\text{Hz}}$
TURN ON SETTLING TIME	t_R	$C_L = 0 \mu\text{F}$		10		μs
LONG-TERM STABILITY ¹	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1 \text{ kHz}$		-70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		6.1		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

¹ The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR435-EP ELECTRICAL CHARACTERISTICS

$V_{IN} = 7.0\text{ V}$ to 18 V , $I_L = 0\text{ mA}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O		4.998	5.000	5.002	V
INITIAL ACCURACY	V_{OERR}				± 2.0 ± 0.04	mV %
TEMPERATURE COEFFICIENT	TCV_O	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_O / \Delta V_{IN}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		5	20	ppm/V
LOAD REGULATION	$\Delta V_O / \Delta I_L$	$I_L = 0\text{ mA}$ to 10 mA , $V_{IN} = 8\text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$ $I_L = -10\text{ mA}$ to 0 mA , $V_{IN} = 8\text{ V}$, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$			15 15	ppm/mA ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		620	800	μA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		8		μV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		115		nV/ $\sqrt{\text{Hz}}$
TURN ON SETTLING TIME	t_R	$C_L = 0\text{ }\mu\text{F}$		10		μs
LONG-TERM STABILITY ¹	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		-70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		7.0		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

¹ The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	130	43	$^\circ\text{C}/\text{W}$

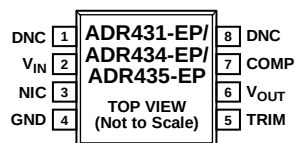
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

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Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	DNC	Do Not Connect. Do not connect to this pin.
2	V _{IN}	Input Voltage Connection.
3	NIC	Not Internally Connected. This pin is not connected internally.
4	GND	Ground.
5	TRIM	Output Voltage Trim.
6	V _{OUT}	Output Voltage.
7	COMP	Compensation Input. Connect a series resistor capacitor network from COMP to V _{OUT} to reduce overall noise.

TYPICAL PERFORMANCE CHARACTERISTICS

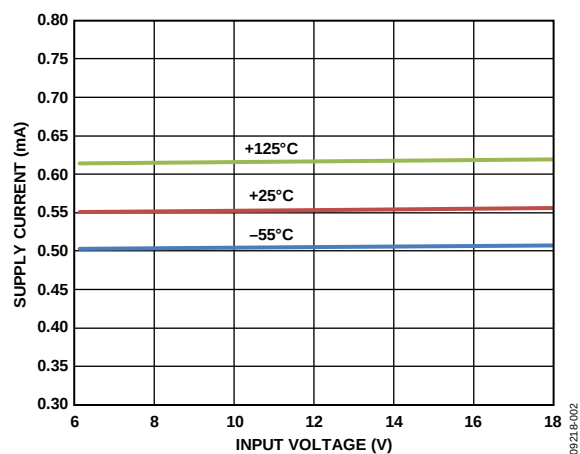
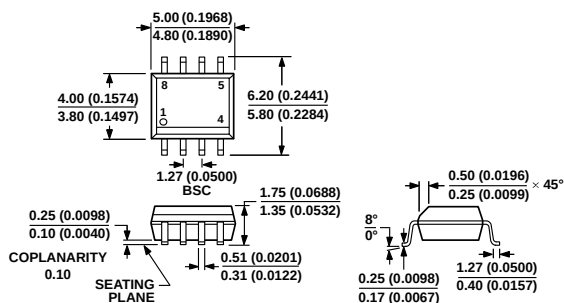


Figure 3. Supply Current vs. Input Voltage at Various Temperatures

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 4. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Output Voltage (V)	Initial Accuracy, ±		Temperature Coefficient Package (ppm/°C)	Temperature Range	Package Description	Package Option	Ordering Quantity
		(mV)	(%)					
ADR431TRZ-EP	2.500	1.0	0.04	5	−55°C to +125°C	8-Lead SOIC_N	R-8	98
ADR431TRZ-EP-R7	2.500	1.0	0.04	5	−55°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR434TRZ-EP	4.096	1.5	0.04	3	−55°C to +125°C	8-Lead SOIC_N	R-8	98
ADR434TRZ-EP-R7	4.096	1.5	0.04	3	−55°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR435TRZ-EP	5.000	2.0	0.04	3	−55°C to +125°C	8-Lead SOIC_N	R-8	98
ADR435TRZ-EP-R7	5.000	2.0	0.04	3	−55°C to +125°C	8-Lead SOIC_N	R-8	1,000

¹ Z = RoHS Compliant Part.