Photometric Front End

Data Sheet

ADPD103

FEATURES

- Multifunction photometric front end
- Fully integrated AFE, ADC, LED drivers, and timing core
- Usable in a broad range of optical measurement applications, including photoplethysmography
- Enables best-in-class ambient light rejection capability without the need for photodiode optical filters
- Three 8 mA to 250 mA LED drivers
- Separate data registers for each LED/photodiode combination
- 1 to 8 optical inputs
- Flexible, multiple, short LED pulses per optical sample
- 20-bit burst accumulator enabling 20 bits per sample period
- On-board sample to sample accumulator, enabling up to 27 bits per data read
- Low power operation
- I^2C interface and 1.8 V analog/digital core
- Flexible sampling frequency ranging from 0.122 Hz to 3.820 kHz
- FIFO data operation

APPLICATIONS

- Body worn health and fitness monitors, for example, heart rate monitoring
- Clinical measurements, for example, SpO_2
- Industrial monitoring
- Background light measurements

GENERAL DESCRIPTION

The ADPD103 is a highly efficient photometric front end with an integrated 14-bit analog-to-digital converter (ADC) and a 20-bit burst accumulator that works in concert with flexible light emitting diode (LED) drivers. It is designed to stimulate an LED and measure the corresponding optical return signal. The data output and functional configuration occur over a 1.8 V I^2C interface. The control circuitry includes flexible LED signaling and synchronous detection.

The analog front end (AFE) features best-in-class rejection of signal offset and corruption due to modulated interference commonly caused by ambient light.

Couple the ADPD103 with a low capacitance photodiode of <100 pF for optimal performance. The ADPD103 can be used with any LED.

Rev. B
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REVISION HISTORY

2/16—Revision B: Initial Version

FUNCTIONAL BLOCK DIAGRAM

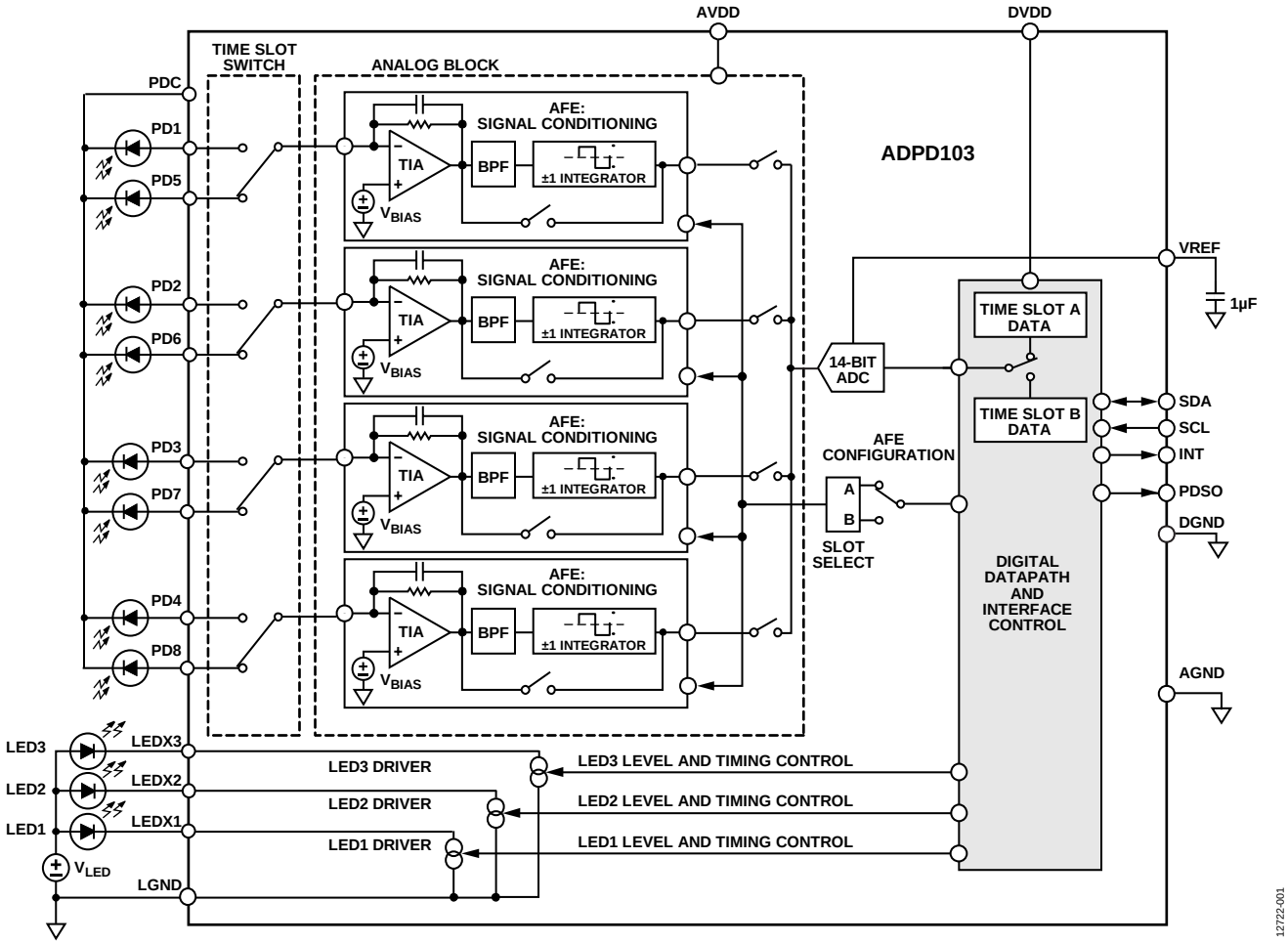

Figure 1. Typical Functional Block Diagram

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Operating Conditions

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating Range		−40		+85	°C
Storage Range		−65		+150	°C
POWER SUPPLY VOLTAGES					
V_{DD}	Applied at the AVDD and DVDD pins	1.7	1.8	1.9	V

AVDD = DVDD = 1.8 V, ambient temperature, unless otherwise noted.

Table 2. Current Consumption[1, 2]

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (V_{DD}) CURRENT						
V_{DD} Supply Current		LED_OFFSET = 25 µs; LED_PERIOD = 19 µs; LED peak current = 25 mA, 4 channels active				
1 Pulse		100 Hz data rate; Time Slot A only		106		µA
		100 Hz data rate; Time Slot B only		94		µA
		100 Hz data rate; both Time Slot A and Time Slot B		151		µA
10 Pulses		100 Hz data rate; Time Slot A only		258		µA
		100 Hz data rate; Time Slot B only		246		µA
		100 Hz data rate; both Time Slot A and Time Slot B		455		µA
Peak V_{DD} Supply Current (1.8 V)	IV_{DD_PEAK}					
4-Channel Operation				9.3		mA
1-Channel Operation				2.3		mA
Standby Mode Current	$IV_{DD_STANDBY}$			3.5		µA
V_{LEDA} AND V_{LEDB} SUPPLY CURRENT						
Average Supply Current						
V_{LEDA} or V_{LEDB}		Peak LED current = 100 mA; LED_PULSE width = 3 µs				
1 Pulse		50 Hz data rate		15		µA
		100 Hz data rate		30		µA
		200 Hz data rate		60		µA
10 Pulses		50 Hz data rate		150		µA
		100 Hz data rate		300		µA
		200 Hz data rate		600		µA

[1] LEDA or LEDB is one of LED1, LED2, or LED3. V_{LEDA} or V_{LEDB} is one of V_{LED1}, V_{LED2}, or V_{LED3}.
[2] V_{DD} is the voltage applied at the AVDD and DVDD pins.

PERFORMANCE SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DATA AQUISITION					
Resolution	Single pulse		14		Bits
Resolution/Sample	64 to 255 pulses		20		Bits
Resolution/Data Read	64 to 255 pulses and sample average = 128		27		Bits
LED DRIVER					
LED Current Slew Rate[1]					
Rise	Slew rate control setting = 0; T_A = 25°C; I_{LED} = 70 mA		240		mA/µs
	Slew rate control setting = 7; T_A = 25°C; I_{LED} = 70 mA		1400		mA/µs
Fall	Slew rate control setting = 0, 1, 2; T_A = 25°C; I_{LED} = 70 mA		3200		mA/µs
	Slew rate control setting = 6, 7; T_A = 25°C; I_{LED} = 70 mA		4500		mA/µs
LED Peak Current	LED pulse enabled	8		250	mA
Driver Compliance Voltage	Voltage above ground required for LED driver operation	0.2			V
LED PERIOD	AFE width = 4 µs	19			µs
	AFE width = 3 µs	17			µs
Sampling Frequency[2]	Time Slot A only; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		3230	Hz
	Time Slot B only; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		3820	Hz
	Both time slots; normal mode; 1 pulse; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		1750	Hz
	Time Slot A only; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		2257	Hz
	Time Slot B only; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		2531	Hz
	Both time slots; normal mode; 8 pulses; OFFSET_LEDA = 23 µs; PERIOD_LEDA = 19 µs	0.122		1193	Hz
CATHODE PIN (PDC) VOLTAGE					
During All Sampling Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1[3]		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
During Slot A Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x0[3]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[9:8] = 0x3[4]		0		V
During Slot B Sampling	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x0[3]		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[11:10] = 0x3[4]		0		V
During Sleep Periods	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 1		1.8		V
	Register 0x54, Bit 7 = 0x0; Register 0x3C, Bit 9 = 0		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54, Bits[13:12] = 0x0		1.8		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x1		1.3		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x2		1.55		V
	Register 0x54, Bit 7 = 0x1; Register 0x54[13:12] = 0x3		0		V
PHOTODIODE INPUT PINS/ ANODE VOLTAGE					
During All Sampling Periods			1.3		V
During Sleep Periods			Cathode voltage		V

[1] LED inductance is negligible for these values. The effective slew rate slows with increased inductance.

[2] The maximum values in this specification are the internal ADC sampling rates in normal mode. The I²C read rates in some configurations may limit the actual output data rate of the device

[3] This mode may induce additional noise and is not recommended unless absolutely necessary. The 1.8 V setting uses V_{DD}, which contains greater amounts of differential voltage noise with respect to the anode voltage. A differential voltage between the anode and cathode injects a differential current across the capacitance of the photodiode of the magnitude C × dV/dt.

[4] This setting is not recommended for photodiodes because it causes a 1.3 V forward bias of the photodiode.

ANALOG SPECIFICATIONS

AVDD = DVDD = 1.8 V, T_A = full operating temperature range, unless otherwise noted. Compensation of the AFE offset is explained in the AFE Operation section.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CAPACITANCE				100	pF
PULSED SIGNAL CONVERSIONS, 3 µs WIDE LED PULSE[1]	4 µs wide AFE integration; normal operation, Register 0x43 (Time Slot A) and Register 0x45 (Time Slot B) = 0xADA5				
ADC Resolution[2]	Transimpedance amplifier (TIA) feedback resistor				
	25 kΩ		1.64		nA/LSB
	50 kΩ		0.82		nA/LSB
	100 kΩ		0.41		nA/LSB
	200 kΩ		0.2		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		13.4		µA
	50 kΩ		6.7		µA
	100 kΩ		3.35		µA
	200 kΩ		1.67		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		37		µA
	50 kΩ		18.5		µA
	100 kΩ		9.25		µA
	200 kΩ		4.63		µA
PULSED SIGNAL CONVERSIONS, 2 µs WIDE LED PULSE[1]	3 µs wide AFE integration; normal operation, Register 0x43 (Time Slot A) and Register 0x45 (Time Slot B) = 0xADA5				
ADC Resolution[2]	TIA feedback resistor				
	25 kΩ		2.31		nA/LSB
	50 kΩ		1.15		nA/LSB
	100 kΩ		0.58		nA/LSB
	200 kΩ		0.29		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	25 kΩ		18.9		µA
	50 kΩ		9.46		µA
	100 kΩ		4.73		µA
	200 kΩ		2.37		µA
Ambient Signal Headroom on Pulsed Signal	TIA feedback resistor				
	25 kΩ		31.5		µA
	50 kΩ		15.7		µA
	100 kΩ		7.87		µA
	200 kΩ		3.93		µA
FULL SIGNAL CONVERSIONS[3]					
TIA Saturation Level of Pulsed Signal and Ambient Level	TIA feedback resistor				
	25 kΩ		50.4		µA
	50 kΩ		25.2		µA
	100 kΩ		12.6		µA
	200 kΩ		6.3		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Total Output Noise Floor	Normal mode; per pulse; per channel; no LED; C_{PD} = 70 pF				
	25 kΩ; referred to ADC input		2.0		LSB rms
	25 kΩ; referred to peak input signal for 2 µs LED pulse		4.6		nA rms
	25 kΩ; referred to peak input signal for 3 µs LED pulse		3.3		nA rms
	25 kΩ; saturation signal-to-noise ratio (SNR) per pulse per channel[4]		72.3		dB
	50 kΩ; referred to ADC input		2.4		LSB rms
	50 kΩ; referred to peak input signal for 2 µs LED pulse		2.8		nA rms
	50 kΩ; referred to peak input signal for 3 µs LED pulse		2.0		nA rms
	50 kΩ; saturation SNR per pulse per channel[4]		70.6		dB
	100 kΩ; referred to ADC input		3.4		LSB rms
	100 kΩ; referred to peak input signal for 2 µs LED pulse		1.9		nA rms
	100 kΩ; referred to peak input signal for 3 µs LED pulse		1.4		nA rms
	100 kΩ; saturation SNR per pulse per channel[4]		67.6		dB
	200 kΩ; referred to ADC input		5.5		LSB rms
	200 kΩ; referred to peak input signal for 2 µs LED pulse		1.6		nA rms
	200 kΩ; referred to peak input signal for 3 µs LED pulse		1.1		nA rms
	200 kΩ; saturation SNR per pulse per channel[4]		63.5		dB
DC Power Supply Rejection Ratio (DC PSRR)			−37		dB

[1] This saturation level applies to the ADC only and, therefore, includes only the pulsed signal. Any nonpulsatile signal is removed prior to the ADC stage.
[2] ADC resolution is listed per pulse when the AFE offset is correctly compensated per the AFE Operation section. If using multiple pulses, divide by the number of pulses.
[3] This saturation level applies to the full signal path and, therefore, includes both the ambient signal and the pulsed signal.
[4] The noise term of the saturation SNR value refers to the receive noise only and does not include photon shot noise or any noise on the LED signal itself.

DIGITAL SPECIFICATIONS

DVDD = 1.7 V to 1.9 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (SCL, SDA)						
Input Voltage Level						
High	V_{IH}		0.7 × DVDD		3.6	V
Low	V_{IL}				0.3 × DVDD	V
Input Current Level						
High	I_{IH}		−10		+10	µA
Low	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
INT Output Voltage Level						
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
PDSO Output Voltage Level						
High	V_{OH}	2 mA high level output current	DVDD − 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
SDA Output Voltage Level						
Low	V_{OL1}	2 mA low level output current			0.2 × DVDD	V
SDA Output Current Level						
Low	I_{OL}	V_{OL1} = 0.6 V	6			mA

TIMING SPECIFICATIONS

Table 6. I²C Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
I²C PORT[1]		See Figure 2				
SCL						
Frequency				400		kHz
Minimum Pulse Width						
High	t_1		600			ns
Low	t_2		1300			ns
Start Condition						
Hold Time	t_3		600			ns
Setup Time	t_4		600			ns
SDA Setup Time	t_5		100			ns
SCL and SDA						
Rise Time	t_6				1000	ns
Fall Time	t_7				300	ns
Stop Condition						
Setup Time	t_8		600			ns

[1] Guaranteed by design.

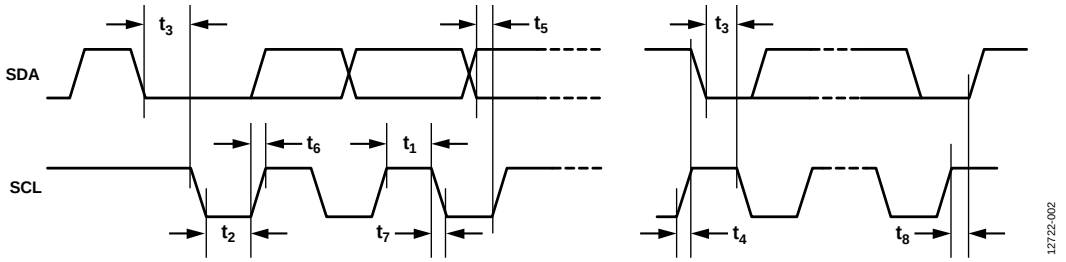

Figure 2. I²C Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
DVDD to DGND	−0.3 V to +2.2 V
INT to DGND	−0.3 V to +2.2 V
PDSO to DGND	−0.3 V to +2.2 V
LEDXx to LGND	−0.3 V to +3.6 V
SCL to DGND	−0.3 V to +3.9 V
SDA to DGND	−0.3 V to +3.9 V
Junction Temperature	150°C
ESD	
28-Lead LFCSP	
Human Body Model (HBM)	1500 V
Charge Device Model (CDM)	1250 V
Machine Model (MM)	100 V
16-Ball WLCSP	
Human Body Model (HBM)	1500 V
Charge Device Model (CDM)	500 V
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
28-Lead LFCSP_WQ	54.9	°C/W
16-Ball WLCSP	60	°C/W

RECOMMENDED SOLDERING PROFILE

Figure 3 and Table 9 provide details about the recommended soldering profile.

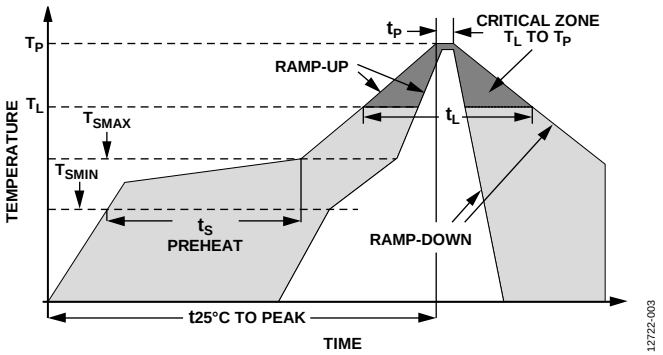

Figure 3. Recommended Soldering Profile

Table 9. Recommended Soldering Profile

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature	8 minutes maximum

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

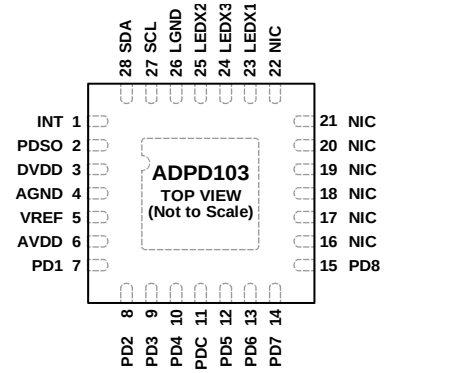

Figure 4. 28-Lead LFCSP Pin Configuration

Table 10. 28-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	INT	DO	Interrupt Output.
2	PDSO	DO	Power-Down Status Output.
3	DVDD	S	1.8 V Digital Supply.
4	AGND	S	Analog Ground.
5	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
6	AVDD	S	1.8 V Analog Supply.
7	PD1	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
8	PD2	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
9	PD3	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
10	PD4	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
11	PDC	AO	Photodiode Common Cathode Bias.
12	PD5	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
13	PD6	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
14	PD7	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
15	PD8	AI	Photodiode Current Input (Anode). If not in use, leave this pin floating.
16 to 22	NIC	R	Not Internally Connected (Nonbonded Pad). This pin can be grounded.
23	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
24	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
25	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
26	LGND	S	LED Driver Ground.
27	SCL	DI	I^2C Clock Input.
28	SDA	DIO	I^2C Data Input/Output.
	EPAD (DGND)	S	Exposed Pad (Digital Ground). Connect the exposed pad to ground.

[1] DO means digital output, S means supply, REF means voltage reference, AI means analog input, AO means analog output, R means reserved, DI means digital input, and DIO means digital input/output.

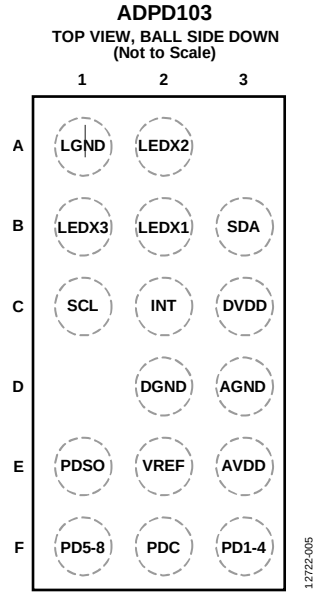

Figure 5. 16-Ball WLCSP Pin Configuration

Table 11. 16-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	LGND	S	LED Driver Ground.
A2	LEDX2	AO	LED Driver 2 Current Sink. If not in use, leave this pin floating.
B1	LEDX3	AO	LED Driver 3 Current Sink. If not in use, leave this pin floating.
B2	LEDX1	AO	LED Driver 1 Current Sink. If not in use, leave this pin floating.
B3	SDA	DIO	I^2C Data Input/Output.
C1	SCL	S	I^2C Clock Input.
C2	INT	DO	Interrupt Output.
C3	DVDD	S	1.8 V Digital Supply.
D2	DGND	S	Digital Ground.
D3	AGND	S	Analog Ground.
E1	PDSO	DO	Power-Down Status Output.
E2	VREF	REF	Internally Generated ADC Voltage Reference. Buffer this pin with a 1 µF capacitor to AGND.
E3	AVDD	S	1.8 V Analog Supply.
F1	PD5-8	AI	Photodiode Combined Current Input of PD5 to PD8. If not in use, leave this pin floating.
F2	PDC	AO	Photodiode Common Cathode Bias.
F3	PD1-4	AI	Photodiode Combined Current Input of PD1 to PD4. If not in use, leave this pin floating.

[1] S means supply, AO means analog output, DIO means digital input/output, DO means digital output, REF means voltage reference, and AI means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

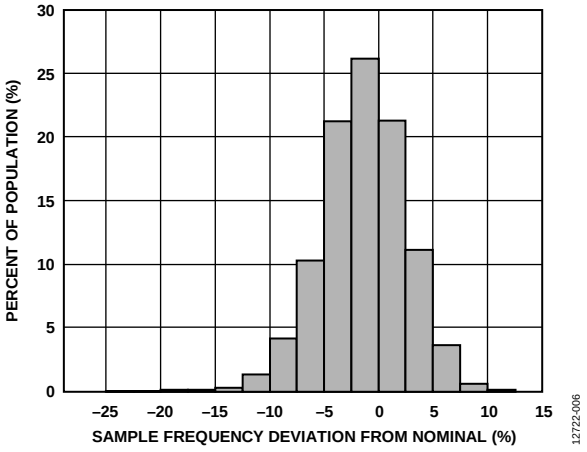

Figure 6. 32 kHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4B = 0x2612)

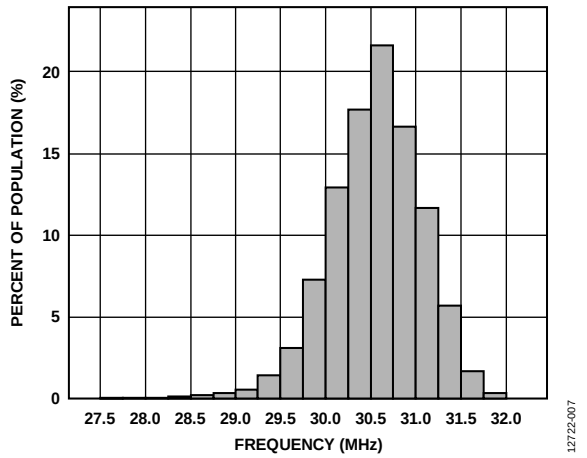

Figure 7. 32 MHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4D = 0x425E)

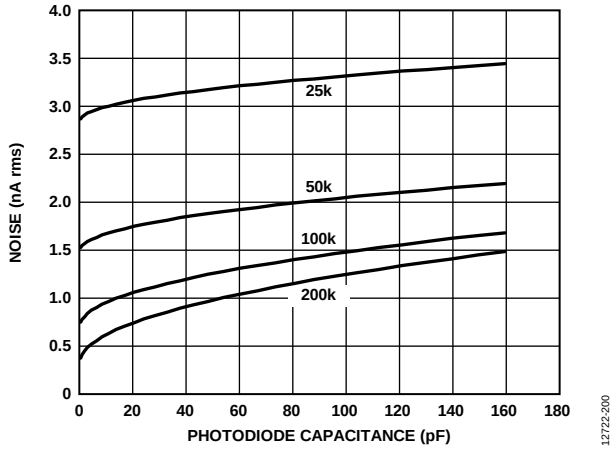

Figure 8. Input Referred Noise vs. Photodiode Capacitance,
LED Pulse Width = 3 µs

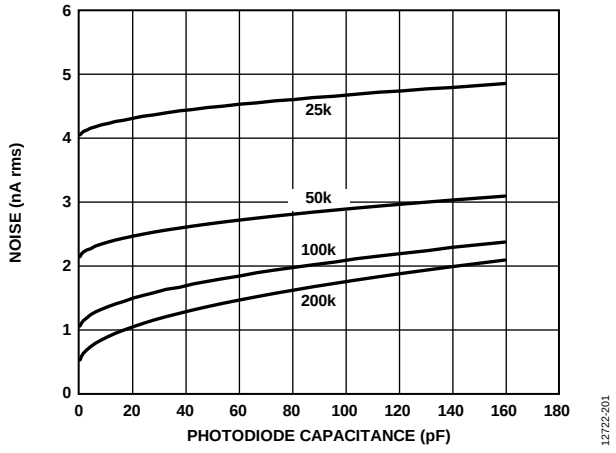

Figure 9. Input Referred Noise vs. Photodiode Capacitance,
LED Pulse Width = 2 µs

THEORY OF OPERATION

INTRODUCTION

The ADPD103 operates as a complete optical transceiver stimulating up to three LEDs and measuring the return signal on up to eight separate current inputs. The core consists of a photometric front end coupled with an ADC, digital block, and three independent LED drivers. The core circuitry stimulates the LEDs and measures the return in the analog block through one to eight photodiode inputs, storing the results in discrete data locations. The eight inputs are broken into two blocks of four simultaneous input channels. Data can be read directly by a register, or through a FIFO. This highly integrated system includes an analog signal processing block, digital signal processing block, I²C communication interface, and programmable pulsed LED current sources.

The LED driver is a current sink and is agnostic to LED supply voltage and LED type. The photodiode (PDx) inputs can accommodate any photodiode with an input capacitance of less than 100 pF. The ADPD103 is purposefully designed to produce a high SNR for relatively low LED power while greatly reducing the effect of ambient light on the measured signal.

DUAL TIME SLOT OPERATION

The ADPD103 operates in two independent time slots, Time Slot A and Time Slot B, which are carried out sequentially. The entire signal path from LED stimulation to data capture and processing is executed during each time slot. Each time slot has a separate datapath that uses independent settings for the LED driver, AFE setup, and the resulting data. Time Slot A and Time Slot B operate in sequence for every sampling period, as shown in Figure 10.

The timing parameters are defined as follows:

$$t_A\ (\mu s) = SLOTA_LED_OFFSET + n_A \times SLOTA_LED_PERIOD$$

where n_A is the number of pulses for Time Slot A (Register 0x31, Bits[15:8]).

$$t_B\ (\mu s) = SLOTB_LED_OFFSET + n_B \times SLOTB_LED_PERIOD$$

where n_B is the number of pulses for Time Slot B (Register 0x36, Bits[15:8]).

Calculate the LED period using the following equation:

$$LED_PERIOD,\ minimum = 2 \times AFE_WIDTH + 11$$

t_1 and t_2 are fixed and based on the computation time for each slot. If a slot is not in use, these times do not add to the total active time. Table 12 defines the values for these LED and sampling time parameters.

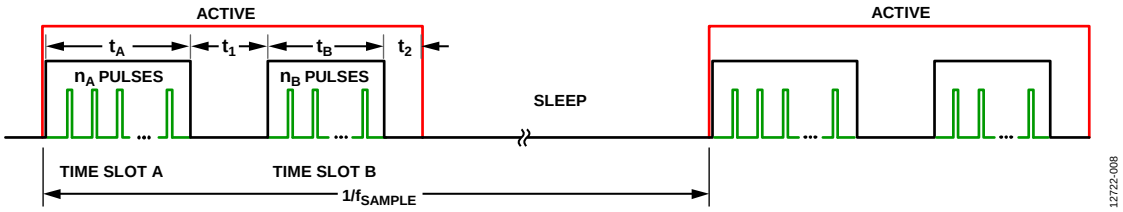

Figure 10. Time Slot Timing Diagram

Table 12. LED Timing and Sample Timing Parameters

Parameter	Register	Bits	Test Conditions/Comments	Min	Typ	Max	Unit
SLOTA_LED_OFFSET[1]	0x30	[7:0]	Delay from power-up to LEDA rising edge	23		63	µs
SLOTB_LED_OFFSET[1]	0x35	[7:0]	Delay from power-up to LEDB rising edge	23		63	µs
SLOTA_LED_PERIOD[2]	0x31	[7:0]	Time between LED pulses in Time Slot A; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
SLOTB_LED_PERIOD[2]	0x36	[7:0]	Time between LED pulses in Time Slot B; SLOTx_AFE_WIDTH = 4 µs	19		63	µs
t_1			Compute time for Time Slot A		68		µs
t_2			Compute time for Time Slot B		20		µs
t_{SLEEP}			Sleep time between sample periods	222			µs

[1] Setting the SLOTx_LED_OFFSET below the specified minimum value may cause failure of ambient light rejection for large photodiodes.
[2] Setting the SLOTx_LED_PERIOD below the specified minimum value can cause invalid data captures.

TIME SLOT SWITCH

Up to eight photodiodes (PD1 to PD8) can be connected to the ADPD103. The photodiode anodes are connected to the PD1 to PD8 input pins; the photodiode cathodes are connected to the cathode pin, PDC. The anodes are assigned in three different configurations depending on the settings of Register 0x14 (see Figure 11, Figure 12, and Figure 13).

A switch sets which photodiode group is connected during Time Slot A and Time Slot B. See Table 13 for the time slot switch registers. When using less than eight photodiodes, it is important to leave the unused inputs floating for proper operation of the device. The photodiode inputs are current inputs and as such, these pins are also considered to be voltage outputs. Tying these inputs to a voltage may saturate the analog block.

Register 0x14, PD1 to PD8 Input Configurations

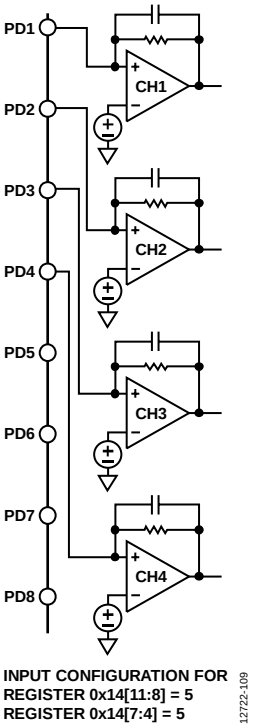

Figure 11. PD1 to PD4 Connection

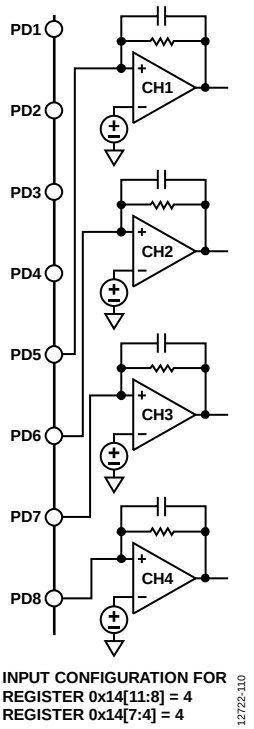

Figure 12. PD5 to PD8 Connection

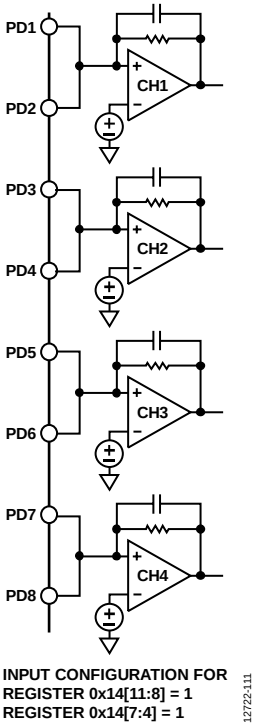

Figure 13. 2-to-1 PD Current Summation

Table 13. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	Selects connection of photodiode for Time Slot B as shown in Figure 11, Figure 12, and Figure 13. 0x0: inputs are floating in Time Slot B. 0x1: all PDx pins (PD1 to PD8) are connected during Time Slot B. 0x4: PD5 to PD8 are connected during Time Slot B. 0x5: PD1 to PD4 are connected during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	Selects connection of photodiode for Time Slot A as shown in Figure 11, Figure 12, and Figure 13. 0x0: inputs are floating in Time Slot A. 0x1: All PDx pins (PD1 to PD8) are connected during Time Slot A. 0x4: PD5 to PD8 are connected during Time Slot A. 0x5: PD1 to PD4 are connected during Time Slot A. Other: reserved.

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 controls the sampling frequency setting of the ADPD103 and Register 0x4B, Bits[5:0] further tunes this clock for greater accuracy. The sampling frequency is governed by an internal 32 kHz sample rate clock that also drives the transition of the internal state machine. The maximum sampling frequencies for some sample conditions are listed in Table 3. The maximum sample frequency for all conditions is determined by the following equation:

$$f_{SAMPLE,\ MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP,\ MIN})$$

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period and the new maximum sampling frequency is calculated as follows:

$$f_{SAMPLE,\ MAX} = 1/(\ t_B + t_2 + t_{SLEEP,\ MIN})$$

where $t_{SLEEP,\ MIN}$ is the minimum sleep time required between samples. See the Dual Time Slot Operation section for the definitions of t_A, t_1, t_B, and t_2.

External Sync for Sampling

The ADPD103 provides an option to use an external sync signal to trigger the sampling periods. This external sample sync signal can be provided either on the INT pin or the PDSO pin. This functionality is controlled by Register 0x4F, Bits[3:2]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same as if the normal sample timer provided the trigger. To enable the external sync signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write the appropriate value to Register 0x4F, Bits[3:2] to select whether the INT pin or the PDSO pin specifies when the next sample cycle occurs. Also, enable the appropriate input buffer using Register 0x4F, Bit 1, for the INT pin, or Register 0x4F, Bit 5, for the PDSO pin.
3. Write b1 to EXT_SYNC_ENA, Register 0x38, Bit 14 to enable the external sampling trigger.
4. Write 0x2 to Register 0x10 to start the sampling operations.
5. Apply the external sync signal on the selected pin at the desired rate; sampling occurs at that rate. As with normal sampling operations, read the data using the FIFO or the data registers.

The maximum frequency constraints also apply in this case.

Providing an External 32kHz Clock

The ADPD103 has an option for the user to provide an external 32 kHz clock to the device for system synchronization or for situations where a clock with better accuracy than the internal 32 kHz clock is required. The external 32 kHz clock is provided on the PDSO pin. To enable the 32 kHz external clock, use the following procedure at startup:

1. Drive the PDSO pin to a valid logic level or with the desired 32 kHz clock prior to enabling the PDSO pin as an input. Do not leave the pin floating prior to enabling it.
2. Write b1 to Register 0x4F, Bit 5 to enable the PDSO pin as an input.
3. Write b11 to register 0x4B, Bit 7 and Bit 8 (CLK32K_EN and CLK32K_BYP, respectively) to configure the device to use an external 32 kHz clock.
4. Write 0x1 to Register 0x10 to enter program mode.
5. Write additional control registers in any order while the device is in program mode to configure the device as required.
6. Write 0x2 to Register 0x10 to start the normal sampling operation.

STATE MACHINE OPERATION

During each time slot, the ADPD103 operates according to a state machine. The state machine operates in the following sequence, shown in Figure 14.

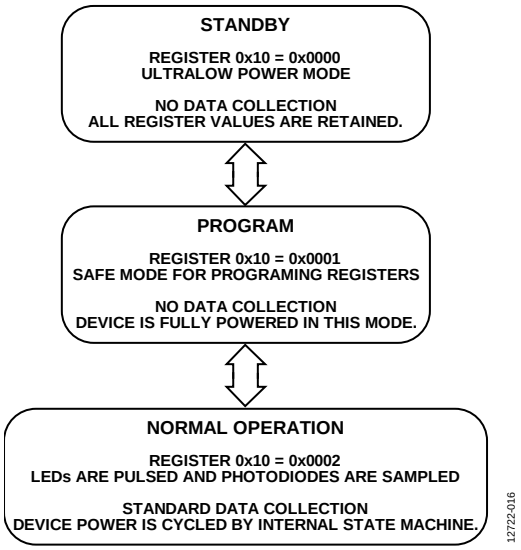

Figure 14. State Machine Operation Flowchart

The ADPD103 operates in one of three modes: standby, program, and normal sampling mode.

Standby mode is a power saving mode in which no data collection occurs. All register values are retained in this mode. To place the device in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The device powers up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD103 through program mode when writing registers or changing modes. Because no power cycling occurs in this mode, the device may consume higher current in program mode than in normal operation. To place the device in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation, the ADPD103 pulses light and collects data. Power consumption in this mode depends on the pulse count and data rate. To place the device in normal sampling mode, write 0x2 to Register 0x10, Bits[1:0].

NORMAL MODE OPERATION AND DATA FLOW

In normal mode, the ADPD103 follows a specific pattern set up by the state machine. This pattern is shown in the corresponding data flow in Figure 15. The pattern is as follows:

1. LED pulse and sample.The ADPD103 pulses external LEDs. The response of a photodiode or photodiodes to the reflected light is measured by the ADPD103. Each data sample is constructed from the sum of n individual pulses, where n is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average n samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

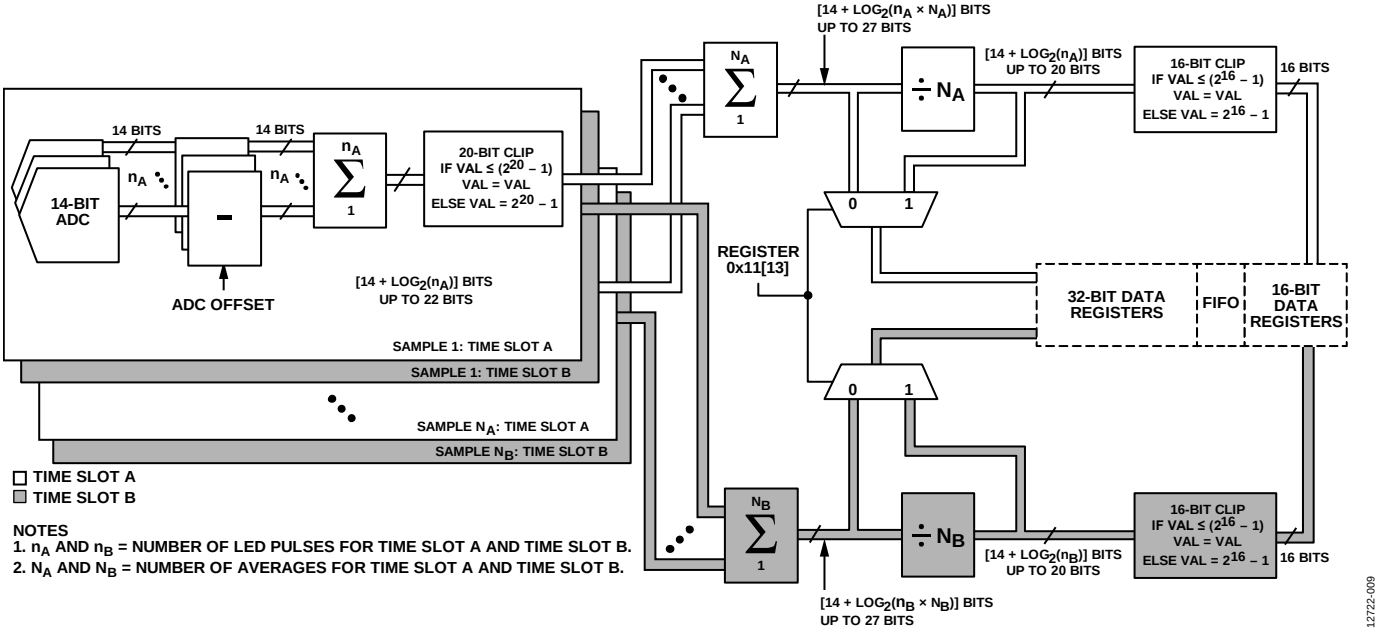

Figure 15. ADPD103 Datapath

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses, as shown in Figure 16. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period so that the sensed value represents the total charge acquired on the photodiode in response to only the corresponding LED pulse. Charge, such as ambient light, that does not correspond to the LED pulse is rejected.

After each LED pulse, the photodiode output relating the pulsed LED signal is sampled and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a sampling period is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual sampling period. There is a 20-bit maximum range for each sampling period.

Averaging

The ADPD103 offers sample accumulation and averaging functionality to increase signal resolution.

Within a sampling period, the AFE can sum up to 256 sequential pulses. As shown in Figure 15, samples acquired by the AFE are clipped to 20 bits at the output of the AFE. Additional resolution, up to 27 bits, can be achieved by averaging between sampling periods. This accumulated data of N samples is stored as 27-bit values and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration.

When using the averaging feature set up by the register, subsequent pulses can be averaged by powers of 2. The user can select from 2, 4, 8 … up to 128 samples to be averaged. Pulse data is still acquired by the AFE at the sampling frequency, f_{SAMPLE} (Register 0x12), but new data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. This new data consists of the sum of the previous N samples. The full 32-bit sum is stored in the 32-bit registers. However, before sending this data to the FIFO, a divide by N operation occurs. This divide operation maintains bit depth to prevent clipping on the FIFO.

Use this between sample averaging to lower the noise while maintaining 16-bit resolution. If the pulse count registers are kept to 8 or less, the 16-bit width is never exceeded. Therefore, when using Register 0x15 to average subsequent pulses, many pulses can be accumulated without exceeding the 16-bit word width. This can reduce the number of FIFO reads required by the host processor.

Data Read

The host processor reads output data from the ADPD103, via the I²C protocol, from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If they are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO; data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

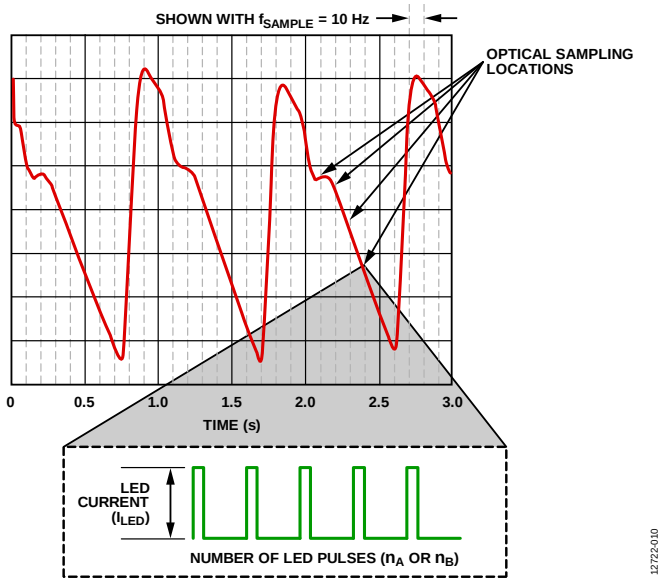

Figure 16. Example of a Photoplethysmography (PPG) Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

AFE OPERATION

The timing within each pulse burst is important for optimizing the operation of the ADPD103. Figure 17 shows the timing waveforms for a single time slot as an LED pulse response propagates through the analog block of the AFE. The first graph, shown in green, shows the ideal LED pulsed output. The filtered LED response, shown in blue, shows the output of the analog integrator. The third graph, shown in orange, illustrates an optimally placed integration window. When programmed to the optimized value, the full signal of the filtered LED response can be integrated. The AFE integration window is then applied to the output of the band-pass filter (BPF) and the result is sent to the ADC and summed for N pulses. If the AFE window is not correctly sized or located, all of the receive signal is not properly reported and system performance is not optimal; therefore, it is important to verify proper AFE position for every new hardware design or the LED width.

AFE INTEGRATION OFFSET ADJUSTMENT

The AFE integration width must be equal or larger than the LED width. As AFE width increases, the output noise increases and the ability to suppress high frequency content from the environment decreases. It is therefore desirable to keep the AFE integration width small. However, if the AFE width is too small, the LED signal is attenuated. With most hardware selections, the AFE width produces the optimal SNR at 1 µs more than the LED width. After setting LED width, LED offset, and AFE width, the ADC offset can then be optimized. The AFE offset must be manually set such that the falling edge of the first segment of the integration window matches the zero crossing of the filtered LED response.

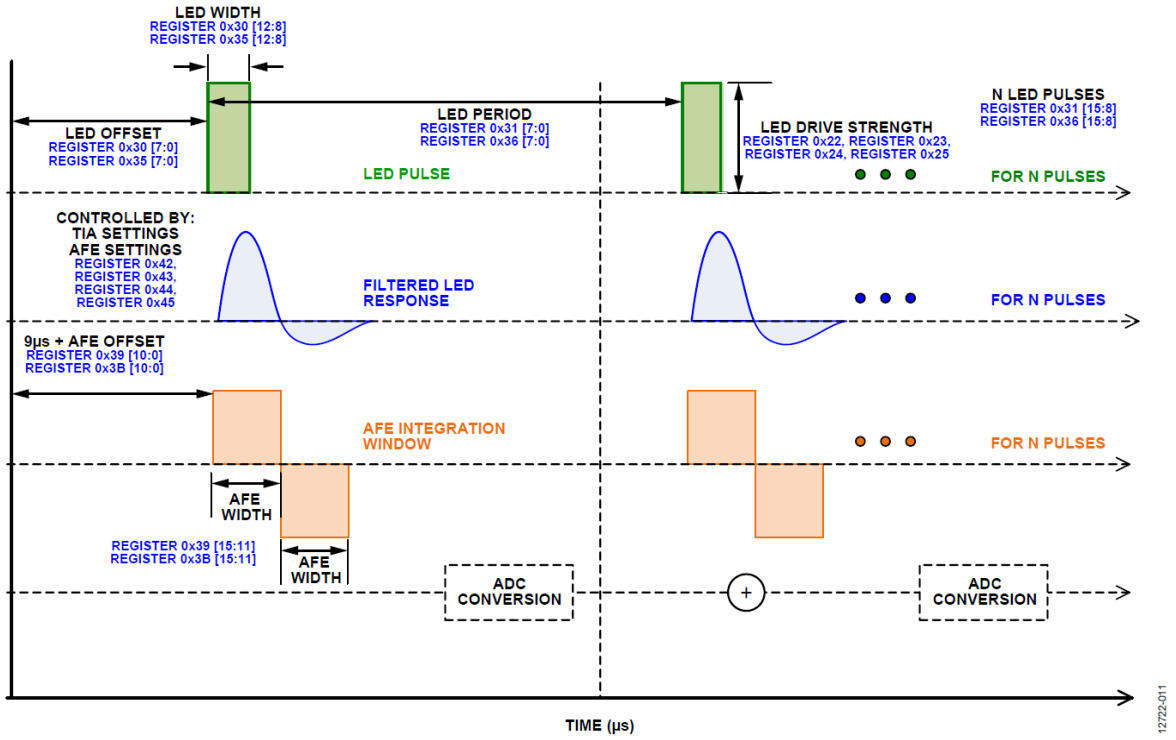

Figure 17. AFE Operation Diagram

AFE Integration Offset Starting Point

The starting point of this offset, as expressed in microseconds, is set such that the falling edge of the integration window aligns with the falling edge of the LED.

LED_FALLING_EDGE = *LED_OFFSET* + *LED_WIDTH*

and,

AFE_INTEGRATION_FALLING_EDGE = 9 + *AFE_OFFSET* + *AFE_WIDTH*

If both falling edges are set equal to each other, solve for AFE_OFFSET to obtain the following equation:

AFE_OFFSET_STARTING_POINT = *LED_OFFSET* + *LED_WIDTH* − 9 − *AFE_WIDTH*

Setting the AFE offset to any point in time earlier than the starting point is equivalent to setting the integration in the future; the AFE cannot integrate the result from an LED pulse that has not yet occurred. As a result, an AFE_OFFSET value less than the AFE_OFFSET_STARTING_POINT is an erroneous setting. Such a result may indicate that current in the TIA is operating in the reverse direction from the intended schematic, where the LED pulse is causing the current to leave the TIA rather than enter it.

Because, for most setups, the AFE_WIDTH is 1 µs wider than the LED_WIDTH, the AFE_OFFSET_STARTING_POINT value is typically 10 µs less than the LED_OFFSET value. Any value less than LED_OFFSET − 10 is erroneous. The optimal AFE offset is some time after the AFE_OFFSET_STARTING_POINT. The band-pass filter response, LED response, and photodiode response each add some delay. In general, the component choice, board layout, LED_OFFSET, and LED_WIDTH are the variables that can change the AFE_OFFSET. After a specific design is set, the AFE_OFFSET can be locked down and does not need to be optimized further.

Sweeping the AFE Position

The AFE offsets for Time Slot A and Time Slot B are controlled by Bits[10:0] of Register 0x39 and Register 0x3B, respectively. Each LSB represents one cycle of the 32 MHz clock, or 31.25 ns. The register can be thought of as 2^{11-1} of these 31.25 ns steps, or it can be broken into an AFE_COARSE setting using Bits[10:5] to represent 1 µs steps and Bits[4:0] to represent 31.25 ns steps. Sweeping the AFE position from the starting point to find a local maximum is the recommended way to optimize the AFE offset. The setup for this test is to allow the LED light to fall on the photodiode in a static way. This is typically done with a reflecting surface at a fixed distance. The AFE position can then be swept to look for changes in the output level. When adjusting the AFE position, it is important to sweep the position using the 31.25 ns steps. Typically, a local maximum is found within 2 µs of the starting point for most systems. Figure 18 shows an example of an AFE sweep, where 0 on the x-axis represents the AFE starting point defined previously. Each data point in the plot corresponds to one 31.25 ns step of the AFE_OFFSET. The optimal location for AFE_OFFSET in this example is 0.687 µs from the AFE starting point.

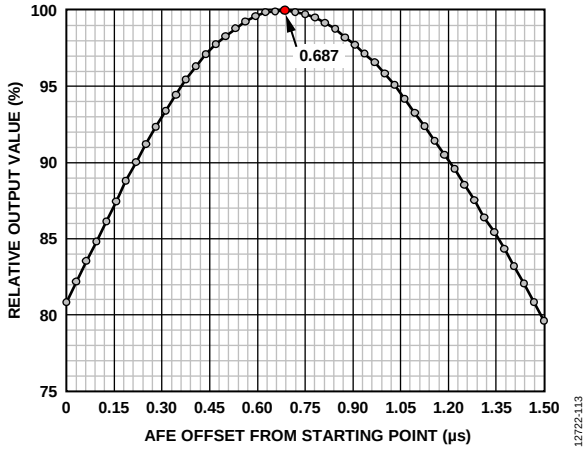

Figure 18. AFE Sweep Example

Table 14 lists some typical LED and AFE values after optimization. In general, it is not recommended to use the AFE_OFFSET numbers in Table 14 without first verifying them against the AFE sweep method. Repeat this method for every new LED width and with every new set of hardware made with the ADPD103. For maximum accuracy, it is recommended that the 32 MHz clock be calibrated prior to sweeping the AFE.

Table 14. AFE Window Settings

LED Register 0x30 or Register 0x35	AFE Register 0x39 or Register 0x3B	Comment
0x0219	0x19FB	2 µs LED pulse, 3 µs AFE width, 25 µs LED delay
0x0319	0x21F4	3 µs LED pulse, 4 µs AFE width, 25 µs LED delay

I²C SERIAL INTERFACE

The ADPD103 supports an I²C serial interface via the SDA (data) and SCL (clock) pins. All internal registers are accessed through the I²C interface.

The ADPD103 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 05—9 October 2012, available from NXP Semiconductors. It supports a fast mode (400 kbps) data transfer. Register read and write are supported, as shown in Figure 19. Figure 2 shows the timing diagram for the I²C interface.

Slave Address

The default 7-bit I²C slave address for the device is 0x64, followed by the R/$\overline{W}$ bit. For a write, the default I²C slave address is 0xC8; for a read, the default I²C address is 0xC9. The slave address is configurable by writing to Register 0x09, Bits[7:1]. When multiple ADPD103 devices are on the same bus lines, the INT and PDSO pins can be used to select specific devices for the address change. Register 0x0D can be used to select a key to enable address changes in specific devices. Use the following procedure to change the slave address when multiple ADPD103 devices are connected to the same I²C bus lines:

1. Using Register 0x4F, enable the input buffer of the PDSO pin, the INT pin, or both, depending on the key being used.
2. For the device identified as requiring an address change, set the INT and/or PDSO pins high or low to match the key being used.
3. Write the SLAVE_ADDRESS_KEY using Register 0x0D, Bits[15:0] to match the desired function. The allowed keys are shown in Table 24.
4. Write the desired SLAVE_ADDRESS using Register 0x09, Bits[7:1]. While writing to Register 0x09, Bits[7:1], write 0xAD to Register 0x09, Bit[15:8]. Register 0x09 must be written to immediately after writing to Register 0x0D.
5. Repeat Step 1 to Step 4 for all the devices that need the SLAVE_ADDRESS changed.
6. Set the INT and PDSO pins as desired for normal operation using the new SLAVE_ADDRESS for each device.

I²C Write and Read Operations

Figure 19 illustrates the ADPD103 I²C write and read operations. Single word and multiword read operations are supported. For a single register read, the host sends a no acknowledge after the second data byte is read and a new register address is needed for each access.

For multiword operations, each pair of data bytes is followed by an acknowledge from the host until the last byte of the last word is read. The host indicates the last read word by sending a no acknowledge. When reading from the FIFO (Register 0x60), the data is automatically advanced to the next word in the FIFO and the space is freed. When reading from other registers, the register address is automatically advanced to the next register, except at Register 0x5F or Register 0x7F, where the address does not increment. This allows lower overhead reading of sequential registers.

All register writes are single word only and require 16 bits (one word) of data.

The software reset (Register 0x0F, Bit 0) is the only command that does not return an acknowledge because the command is instantaneous.

Table 15. Definition of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The master is the device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The slave is the device addressed by a master. The ADPD103 operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high; all transactions begin with a start condition.
Start (Sr)	Repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the acknowledge or no acknowledge clock pulse, the SDA line is pulled low and remains low.
NACK	During the acknowledge or no acknowledge clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

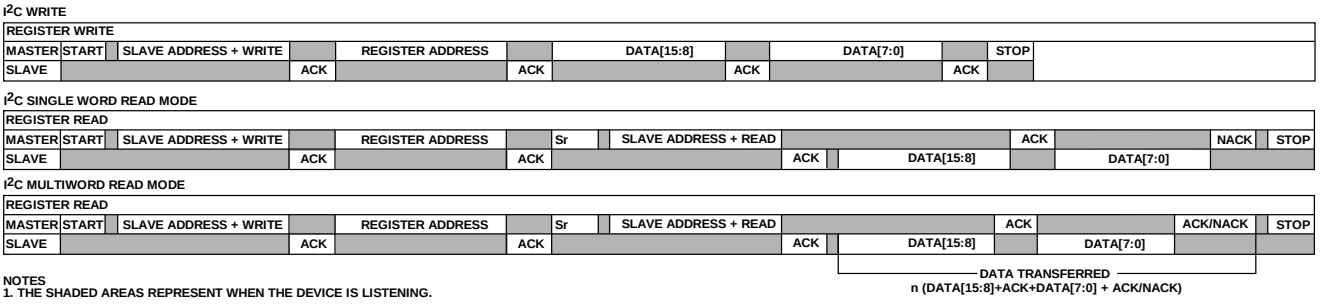

Figure 19. I²C Write and Read Operations

TYPICAL CONNECTION DIAGRAM

Figure 21 and Figure 22 show two possible photodiode input connections for the ADPD103. The 1.8 V I²C communication lines, SCL and SDA, along with the INT line, connect to a system microprocessor or sensor hub. The I²C signals can have pull-up resistors connected to a 1.8 V or a 3.3 V power supply. The INT and PDSO signals are only compatible with a 1.8 V supply and may need a level translator.

Provide the 1.8 V supply, V_{DD}, to AVDD and DVDD. Use single (V_{LED}) or multiple (V_{LED1}, V_{LED2}, and V_{LED3}) sources for the LED supply using standard regulator circuits according to the peak current requirements specified in Table 3 and calculated in the Calculating Current Consumption section.

For best noise performance, connect AGND, DGND (exposed pad), and LGND together at a large conductive surface such as a ground plane, a ground pour, or a large ground trace.

The number of photodiodes or LEDs used varies. There are multiple ways to connect photodiodes to the input channels, as shown in Table 16 and Figure 23. The photodiode anodes are connected to the PD1 to PD8 input pins, and the photodiode cathodes are connected to the cathode pin.

With large photodiodes, the dynamic range can be increased by splitting the current between multiple inputs. As a result, if only one large photodiode is used and the receive signal is expected to be large, the diode can be branched across all four inputs in a given time slot. This type of configuration is shown in Figure 21. For situations where the photodiode is small or the signal is greatly attenuated, the photodiode can be connected directly to a single channel such as PD1 or PD5. This connection, shown in Figure 22, maximizes SNR for low signals. Do not connect the same photodiode to all eight input channels. It is important to leave the unused input channels floating for proper device operation. The WLCSP package is internally wired for high dynamic range mode.

Figure 20 shows the recommended connection diagram and printed circuit board (PCB) layout for the ADPD103 WLCSP package. See Figure 21 or Figure 22 for connection details.

The current input pins (PD1 to PD8) have a typical voltage of 1.3 V during the sampling period. During the sleep period, these pins are connected to the cathode pin. The cathode and anode voltages are listed in Table 3.

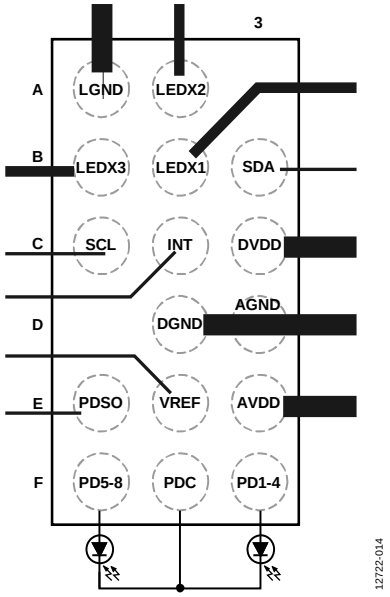

Figure 20. WLCSP Package Connection and PCB Layout Diagram (Top View)

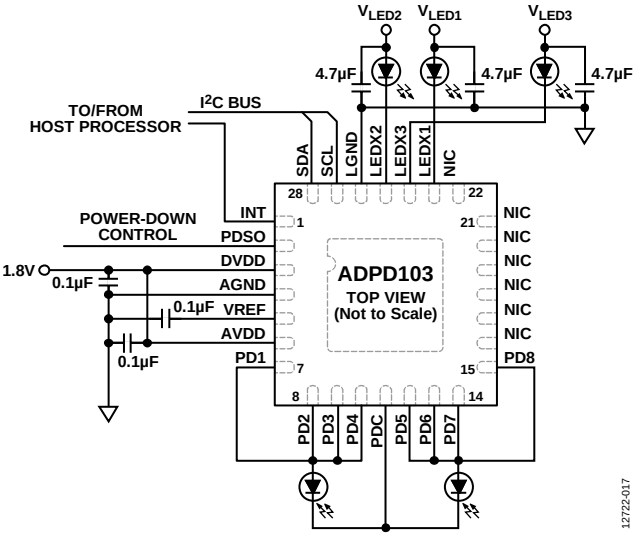

Figure 21. Connection Diagram for Increased Dynamic Range

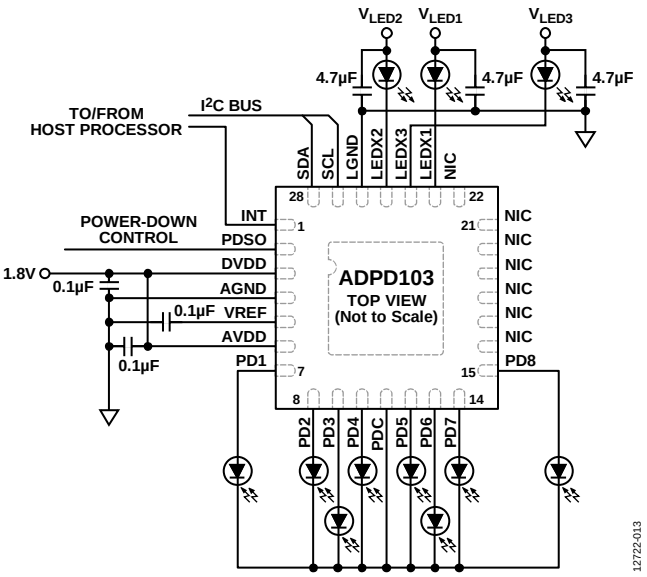

Figure 22. Connection Options for Individual Single Channel Diodes

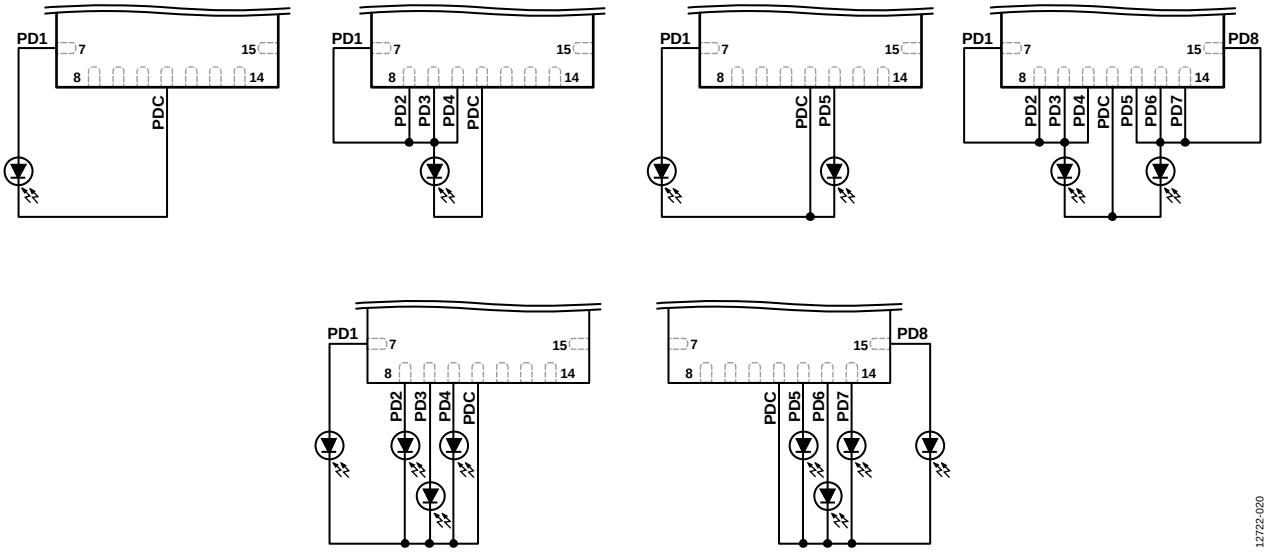

Figure 23. Typical Photodiode Connection Diagram

Table 16. Typical Photodiode Anode to Input Channel Connections

	Input Channel							
Photodiode Anode Configuration	**PD1**	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**	**PD8**
Single Photodiode (D1)	D1	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	NC[1]	NC[1]	NC[1]
	D1	D1	D1	D1	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	D1	D1	D1
Two Photodiodes (D1, D2)	D1	NC[1]	NC[1]	NC[1]	D2	NC[1]	NC[1]	NC[1]
	D1	D1	D1	D1	D2	D2	D2	D2
Four Photodiodes (D1 to D4)	D1	D2	D3	D4	NC[1]	NC[1]	NC[1]	NC[1]
	NC[1]	NC[1]	NC[1]	NC[1]	D1	D2	D3	D4
Eight Photodiodes (D1 to D8)	D1	D2	D3	D4	D5	D6	D7	D8

[1] NC means do not connect under the conditions provided in Table 16. Leave all unused inputs floating.

LED DRIVER PINS AND LED SUPPLY VOLTAGE

The LEDx1, LEDx2, and LEDx3 pins have an absolute maximum voltage rating of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LEDx pins must not be confused with the supply voltages for the LED themselves (V_{LEDx}). V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LEDx pin is the input of the internal current driver, and the pins are connected to the cathode of the external LED.

LED DRIVER OPERATION

The LED driver for the ADPD103 is a current sink requiring 0.2 V of compliance above ground to maintain the programmed current level. Figure 24 shows the basic schematic of how the ADPD103 connects to an LED through the LED driver. The Determining the Average Current and the Determining CVLED sections define the requirements for the bypass capacitor (C_{VLED}) and the supply voltages of the LEDs (V_{LEDx}).

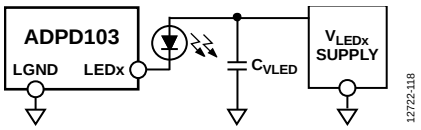

Figure 24. V_{LEDx} Supply Schematic

DETERMINING THE AVERAGE CURRENT

The ADPD103 drives an LED in a series of short pulses. Figure 25 shows the typical ADPD103 configuration of a pulse burst sequence.

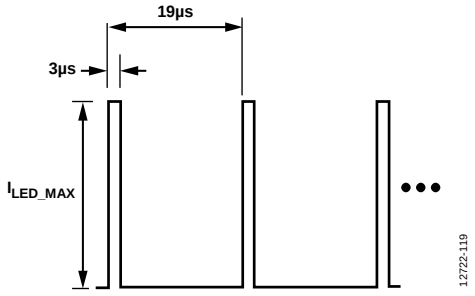

Figure 25. Typical LED Pulse Burst Sequence Configuration

In this example, the LED pulse width, t_{LED_PULSE}, is 3 µs, and the LED pulse period, t_{LED_PERIOD}, is 19 µs. The LED being driven is a pair of green LEDs driven to a 250 mA peak. The goal of C_{VLED} is to buffer the LED between individual pulses. In the worst case scenario, where the pulse train shown in Figure 25 is a continuous sequence of short pulses, the V_{LEDx} supply must supply the average current. Therefore, calculate $I_{LED_AVERAGE}$ as follows:

$$I_{LED_AVERAGE} = (t_{LED_PULSE}/t_{LED_PERIOD}) \times I_{LED_PEAK} \quad (1)$$

where:

$I_{LED_AVERAGE}$ is the average current needed from the V_{LEDx} supply during the pulse period, and it is also the V_{LEDx} supply current rating.

I_{LED_PEAK} is peak current setting of the LED.

For the numbers shown in Equation 1, $I_{LED_AVERAGE} = 3/19 \times I_{LED_PEAK}$. For typical LED timing, the average V_{LEDx} supply current is 3/19 × 250 mA = 39.4 mA, indicating that the V_{LEDx} supply must support a dc current of 40 mA.

DETERMINING C_{VLED}

To determine the C_{VLED} capacitor value, determine the maximum forward-biased voltage, $V_{FB_LED_MAX}$, of the LED in operation. The LED current, $I_{FB_LED_MAX}$, converts to $V_{FB_LED_MAX}$ as shown in Figure 26. In this example, 250 mA of current through two green LEDs in parallel yields $V_{FB_LED_MAX}$ = 3.95 V. Any series resistance in the LED path must also be included in this voltage. When designing the LED path, keep in mind that small resistances can add up to large voltage drops due to the LED peak current being very large. In addition, these resistances can be unnecessary constraints on the V_{LEDx} supply.

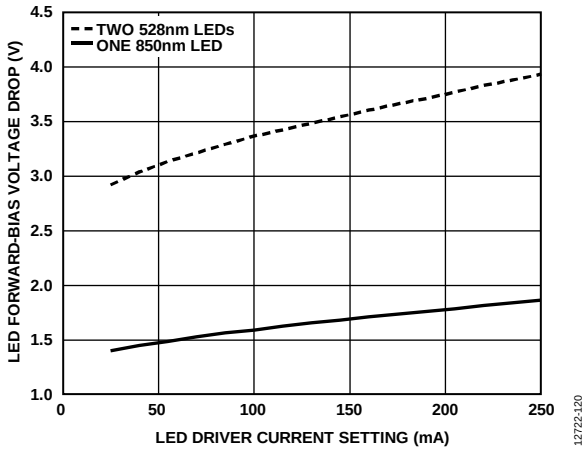

Figure 26. Example of the Average LED Forward-Biased Voltage Drop as a Function of the Driver Current

To correctly size the C_{VLED} capacitor, do not deplete it during the pulse of the LED to the point where the voltage on the capacitor is less than the forward bias on the LED.

To calculate the minimum value for the V_{LEDx} bypass capacitor, use the following equation:

$$C_{VLED} = \frac{t_{LED_PULSE} \times I_{FB_LED_MAX}}{V_{LED_MIN} - (V_{FB_LED_MAX} + 0.2)} \quad (2)$$

where:

t_{LED_PULSE} is the LED pulse width.

$I_{FB_LED_MAX}$ is the maximum forward-biased current on the LED used in operating the device.

V_{LED_MIN} is the lowest voltage from the VLEDx supply with no load.

$V_{FB_LED_MAX}$ is the maximum forward-biased voltage required on the LED to achieve I_{LED_PEAK}.

The numerator of the C_{VLED} equation sets up the total discharge amount in coulombs from the bypass capacitor to satisfy a single programmed LED pulse of the maximum current. The denominator represents the difference between the lowest voltage from the V_{LEDx} supply and the LED required voltage. The LED required voltage is the voltage of the anode of the LED such that the 0.2 V compliance of the LED driver and the forward-biased voltage of the LED operating at the maximum current is satisfied. For a typical ADPD103 example, assume that the lowest value for the V_{LEDx} supply is 4.4 V, and that the peak current is 250 mA for two 528 nm LEDs in parallel. The minimum value for C_{VLED} is then equal to 3 µF.

$$C_{VLED} = (3 \times 10^{-6} \times 0.250)/(4.4 - (3.95 + 0.2)) = 3\ \mu F \quad (3)$$

As shown in the Equation 3, as the minimum supply voltage drops close to the maximum anode voltage, the demands on C_{VLED} become more stringent, forcing the capacitor value higher. It is important to insert the correct values into these equations. For example, using an average value for V_{LED_MIN} instead of the worst case value for V_{LED_MIN} can cause a serious design deficiency, resulting in a C_{VLED} value that is too small and that causes insufficient optical power in the application. Therefore, adding a sufficient margin on C_{VLED} is strongly recommended. Add additional margin to C_{VLED} to account for derating of the capacitor value over voltage, bias, temperature and other factors over the life of the component.

LED INDUCTANCE CONSIDERATIONS

The LED drivers (LEDXx) on the ADPD103 have configurable slew rate settings (Register 0x22, Bits[6:4], Register 0x23, Bits[6:4], and Register 0x24, Bits[6:4]). These slew rates are defined in Table 3. Even at the lowest setting, careful consideration must be taken in board design and layout. If a large series inductor, such as a long PCB trace, is placed between the LED cathode and one of the LEDXx pins, voltage spikes from the switched inductor can cause violations of absolute maximum and minimum voltages on the LEDXx pins during the slew portion of the LED pulse.

To verify that there are no voltage spikes on the LEDXx pins due to parasitic inductance, use an oscilloscope on the LEDXx pins to monitor the voltage during normal operation. Any positive spike >3.6 V may damage the device.

In addition, a negative spike <−0.3 V may also damage the device.

RECOMMENDED START-UP SEQUENCE

At power-up, the device is in standby mode (Register 0x10 = 0x0), as shown in Figure 14. The ADPD103 does not require a particular power-up sequence.

From standby mode, to begin measurement, initiate the ADPD103 as follows:

1. Set the CLK32K_EN bit (Register 0x4B, Bit 7) to start the sample clock (32 kHz clock). This clock controls the state machine. If this clock is off, the state machine is not able to transition as defined by Register 0x10.
2. Write 0x1 to Register 0x10 to force the device into program mode. Step 1 and Step 2 can be swapped, but the actual state transition does not occur until both steps occur.
3. Write additional control registers in any order while the device is in program mode to configure the device as required.
4. Write 0x2 to Register 0x10 to start normal sampling operation.

To terminate normal operation, follow this sequence to place the ADPD103 in standby mode:

1. Write 0x1 to Register 0x10 to force the device into program mode.
2. Write to the registers in any order while the device is in program mode.
3. Write 0x00FF to Register 0x00 to clear all interrupts. If desired, clear the FIFO as well by setting the DIGITAL_CLOCK_ENA bit (Register 0x5F, Bit 0) and writing 0x80FF to Register 0x00.
4. Write 0x0 to Register 0x10 to force the device into standby mode.
5. Optionally, stop the 32 kHz clock by resetting the CLK32K_EN bit (Register 0x4B, Bit 7). Register 0x4B, Bit 7 = 0 is the only write that must be written when the device is in standby mode (Register 0x10 = 0x0). If 0 is written to this bit while in program mode or normal mode, the device becomes unable to transition into any other mode, including standby mode, even if it is subsequently written to do so. As a result, the power consumption in what appears to be standby mode is greatly elevated. For this reason, and due to the very low current draw of the 32 kHz clock while in operation, it is recommended from an ease of use perspective to keep the 32 kHz clock running after it is turned on.

READING DATA

The ADPD103 provides multiple methods for accessing the sample data. Each time slot can be independently configured to provide data access using the FIFO or the data registers. Interrupt signaling is also available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADPD103 includes a 128-byte FIFO memory buffer that can be configured to store data from either or both time slots. Register 0x11 selects the kind of data from each time slot to be

written to the FIFO. Note that both time slots can be enabled to use the FIFO, but only if their output data rate is the same.

$$Output\ data\ rate = f_{SAMPLE}/N$$

where:
f_{SAMPLE} is the sampling frequency.
N is the averaging factor for each time slot (N_A for Time Slot A and N_B for Time Slot B). In other words, $N_A = N_B$ must be true to store data from both time slots in the FIFO.

Data packets are written to the FIFO at the output data rate. A data packet for the FIFO consists of a complete sample for each enabled time slot. Data for each photodiode channel can be stored as either 16 or 32 bits. Each time slot can store 2, 4, 8, or 16 bytes of data per sample, depending on the mode and data format. To ensure that data packets are intact, new data is only written to the FIFO if there is sufficient space for a complete packet. Any new data that arrives when there is not enough space is lost. The FIFO continues to store data when sufficient space exists. Always read FIFO data in complete packets to ensure that data packets remain intact.

The number of bytes currently stored in the FIFO is available in Register 0x00, Bits[15:8]. A dedicated FIFO interrupt is also available and automatically generates when a specified amount of data is written to the FIFO.

Interrupt-Based Method

To read data from the FIFO using an interrupt-based method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write Register 0x11 with the desired data format for each time slot.
3. Set FIFO_THRESH in Register 0x06, Bits[13:8] to the interrupt threshold. A good value for this is the number of 16-bit words in a data packet, minus 1. This causes an interrupt to generate when there is at least one complete packet in the FIFO.
4. Enable the FIFO interrupt by writing a 0 to the FIFO_INT_MASK in Register 0x01, Bit 8. Also, configure the interrupt pin (INT) by writing the appropriate value to the bits in Register 0x02.
5. Enter normal operation mode by setting Register 0x10 to 0x2.
6. When an interrupt occurs
   a. There is no requirement to read the FIFO_SAMPLES register, because the interrupt is generated only if there is one or more full packets. Optionally, the interrupt routine can check for the presence of more than one available packet by reading this register.
   b. Write 1 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0) twice in two consecutive write operations.
   c. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.
   d. Write 0 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0).

The interrupt automatically clears when enough data is read from the FIFO to bring the data level below the threshold.

Polling Method

To read data from the FIFO in a polling method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write Register 0x11 with the desired data format for each time slot.
3. Enter normal operation mode by setting Register 0x10 to 2.

Next, begin the polling operations.

1. Wait for the polling interval to expire.
2. Read the FIFO_SAMPLES bits (Register 0x00, Bits[15:8]).
3. If FIFO_SAMPLES ≥ the packet size, read a packet using the following steps:
   a. Write 1 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0) twice in two consecutive write operations.
   b. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.
   c. Write 0 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0).
   d. Repeat Step 1.

When a mode change is required, or any other disruption to normal sampling is necessary, the FIFO must be cleared. Use the following procedure to clear the state and empty the FIFO:

1. Enter program mode by setting Register 0x10 to 0x1.
2. Write 1 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0) twice in two consecutive write operations.
3. Write 1 to Register 0x00, Bit 15.
4. Write 0 to the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0).

Reading Data from Registers Using Interrupts

The latest sample data is always available in the data registers and is updated simultaneously at the end of each time slot. The data value for each photodiode channel is available as a 16-bit value in Register 0x64 through Register 0x67 for Time Slot A, and Register 0x68 through Register 0x6B for Time Slot B. If allowed to reach their maximum value, Register 0x64 through Register 0x6B clip. If Register 0x64 through Register 0x6B saturate, the unsaturated (up to 27 bits) values for each channel are available in Register 0x70 through Register 0x77 for Time Slot A and Register 0x78 through Register 0x7F for Time Slot B. Sample interrupts are available to

indicate when the registers are updated and can be read. To use the interrupt for a given time slot, use the following procedure:

1. Enable the sample interrupt by writing a 0 to the appropriate bit in Register 0x01. To enable the interrupt for Time Slot A, write 0 to Bit 5. To enable the interrupt for Time Slot B, write 0 to Bit 6. Either or both interrupts can be set.
2. Configure the interrupt pin by writing the appropriate value to the bits in Register 0x02.
3. An interrupt generates when the data registers are updated.
4. The interrupt handler must perform the following:
   a. Read Register 0x00 and observe Bit 5 or Bit 6 to confirm which interrupt has occurred. This step is not required if only one interrupt is in use.
   b. Read the data registers before the next sample can be written. The system must have interrupt latency and service time short enough to respond before the next data update, based on the output data rate.
   c. Write a 1 to Bit 5 or Bit 6 in Register 0x00 to clear the interrupt.

If both time slots are in use, it is possible to use only the Time Slot B interrupt to signal when all registers can be read. It is recommended to use the multiword read to transfer the data from the data registers.

Reading Data from Registers Without Interrupts

If the system interrupt response is not fast or predictable enough to use the interrupt method, or if the interrupt pin is not used, it is possible to get reliable data access by using the data hold mechanism. To guarantee that the data read from the registers is from the same sample time, it is necessary to prevent the update of samples while reading the current values. The method for doing register reads without interrupt timing is as follows:

1. Write a 1 to SLOTA_DATA_HOLD or SLOTB_DATA_HOLD (Register 0x5F, Bit 1 and Bit 2, respectively) for the time slot requiring access (both time slots can be accessed). This prevents sample updates.
2. Read the registers as desired.
3. Write a 0 to the SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits (Register 0x5F, Bit 1 and Bit 2, respectively) previously set. Sample updates are allowed again.

Because a new sample may arrive while the reads are occurring, this method prevents the new sample from partially overwriting the data being read.

CLOCKS AND TIMING CALIBRATION

The ADPD103 operates using two internal time bases: a 32 kHz clock sets the sample timing, and a 32 MHz clock controls the timing of the internal functions such as LED pulsing and data capture. Both clocks are internally generated and exhibit device-to-device variation of approximately 10% (typical).

Heart rate monitoring applications require an accurate time base to achieve an accurate count of beats per minute. The ADPD103 provides a simple calibration procedure for both clocks.

1. Calibrating the 32 kHz clock. This calibrates items associated with the output data rate. Calibration of this clock is important for applications where an accurate data rate is important, such as heart rate measurements.
   a. Set the sampling frequency to the highest the system can handle, such as 2000 Hz. Because the 32 kHz clock controls sample timing, its frequency is readily accessible via the INT pin. Configure the interrupt by writing the appropriate value to the bits in Register 0x02 and set the interrupt to occur at the sampling frequency by writing 0 to Register 0x01, Bit 5 or Bit 6. Monitor the INT pin. The interrupt frequency must match the set sample frequency.
   b. If the monitored interrupt frequency is less than the set sampling frequency, increase the CLK32K_ADJUST bit (Register 0x4B, Bits[5:0]). If the monitored interrupt frequency is larger than the set sampling frequency, decrease the CLK32K_ADJUST bits.
   c. Repeat Step b until the monitored interrupt signal frequency is close enough to the set sampling frequency.
2. Calibrate the 32 MHz clock. This calibrates items associated with the fine timing within a sample period, such as LED pulse width and spacing, assuming that the 32 kHz clock has been calibrated.
   a. Write 0x1 to Register 0x5F, Bit 0.
   b. Enable the CLK_RATIO calculation by writing 0x1 to Register 0x50, Bit 5. This function counts the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. With this function enabled, this cycle value is stored in Register 0xA, Bits[11:0] and nominally this ratio is 2000 (0x7D0).
   c. Calculate the 32 MHz clock error as follows:

      $$Clock\ Error = 32\ MHz \times (1 - CLK_RATIO/2000)$$

   d. Adjust the frequency by setting Bits[7:0] in Register 0x4D per the following equation:

      $$CLK32M_ADJUST = Clock\ Error/109\ kHz$$

   e. Write 0x0 to Register 0x50, Bit 5 to reset the CLK_RATIO function.

Repeat Step 2b through Step 2e until the desired accuracy is achieved.

Write 0x0 to Register 0x5F, Bit 0. Also, set the INT pin back to the mode desired for normal operation.

CALCULATING CURRENT CONSUMPTION

The current consumption of the ADPD103 depends on the user selected operating configuration, as described in the following equations.

Total Power Consumption

To calculate the total power consumption, use Equation 4.

$$Total\ Power = I_{VDD_AVG} \times V_{DD} + I_{LEDA_AVG} \times V_{LEDA} + I_{LEDB_AVG} \times V_{LEDB} \quad (4)$$

Average V_{DD} Supply Current

To calculate the average V_{DD} supply current, use Equation 5.

$$I_{VDD_AVG} = DR \times ((I_{AFE_A} \times t_{SLOTA}) + (I_{AFE_B} \times t_{SLOTB}) + Q_{PROC}) + I_{VDD_STANDBY} \quad (5)$$

where:
DR = the data rate in Hz.
$I_{VDD_STANDBY} = 3.5 \times 10^{-3}$ mA.
Q_{PROC} is an average charge associated with a processing time, as follows:

- Only Time Slot A enabled: $Q_{PROC} = 0.64 \times 10^{-3}$ mC
- Only Time Slot B enabled: $Q_{PROC} = 0.51 \times 10^{-3}$ mC
- Time Slot A and Time Slot B enabled: $Q_{PROC} = 0.69 \times 10^{-3}$ mC

$$I_{AFE_x}\ (\text{mA}) = 2.9 + (1.5 \times NUM_CHANNELS) + (LEDx_{PEAK} - 25)/225 \quad (6)$$

$$t_{SLOTx}\ (\text{sec}) = LEDx_OFFSET + LEDx_PERIOD \times PULSE_COUNT \quad (7)$$

where:
NUM_CHANNELS is the number of active channels.
$LEDx_{PEAK}$ is the peak LED current expressed in mA.
LEDx_OFFSET is the pulse start time offset expressed in seconds.
LEDx_PERIOD is the pulse period expressed in seconds.
PULSE_COUNT is the number of pulses.

Note that if either Time Slot A or Time Slot B are disabled, I_{AFE_x} = 0 for that respective time slot. Additionally, if operating in digital integrate mode, power savings can be realized by setting Register 0x3C, Bits[8:3] = b010010. This setting disables the band-pass filters that are bypassed in digital integrate mode, changing the AFE power contribution calculation to:

$$I_{AFE_x}\ (\text{mA}) = 2.9 + (1.0 \times NUM_CHANNELS) + (LEDx_{PEAK} - 25)/225$$

Average V_{LEDA} Supply Current

To calculate the average V_{LEDA} supply current, use Equation 8.

$$I_{LED_AVG_A} = (SLOTA_LED_WIDTH/1 \times 10^{6}) \times LEDA_{PEAK} \times DR \times PULSE_COUNT \quad (8)$$

where $LEDA_{PEAK}$ is $LED1_{PEAK}$, $LED2_{PEAK}$, or $LED3_{PEAK}$, expressed in mA, for whichever LED is selected for Time Slot A.

Average V_{LEDB} Supply Current

To calculate the average V_{LEDB} supply current, use Equation 9.

$$I_{LED_AVG_B} = (SLOTB_LED_WIDTH/1 \times 10^{6}) \times LEDB_{PEAK} \times DR \times PULSE_COUNT \quad (9)$$

where $LEDB_{PEAK}$ is $LED1_{PEAK}$, $LED2_{PEAK}$, or $LED3_{PEAK}$, expressed in mA, for whichever LED is selected for Time Slot B.

OPTIMIZING SNR PER WATT

The ADPD103 offers a variety of parameters that the user can adjust to achieve the best signal. One of the key goals of system performance is to obtain the best system SNR for the lowest total power. This is often referred to as optimizing SNR/watt. Even in systems where only the SNR matters and power is a secondary concern, there may be a lower power or a high power means of achieving the same SNR.

Optimizing for Peak SNR

The first step in optimizing for peak SNR is to find a TIA gain and LED level that gives the best performance where the number of LED pulses remains constant. If peak SNR is the goal, the noise section of Table 3 can be used as a guide. It is important to note that the SNR improves as a square root of the number of pulses averaged together, whereas the increase in the LED power consumed is directly proportional to the number of LED pulses. In other words, for every doubling of the LED pulse count, there is a doubling of the LED power consumed and a 3 dB SNR improvement. As a result, avoid any change in the gain configuration that provides less than 3 dB of improvement for a 2× power penalty; any TIA gain configuration that provides more than 3 dB of improvement for a 2× power penalty is a good choice. If peak SNR is the goal and there is no issue saturating the photodiode with LED current at any gain, the 50k TIA gain setting is an optimal choice. After the SNR per pulse per channel is optimized, the user can then increase the number of pulses to achieve the desired system SNR.

Optimizing SNR per Watt in a Signal Limited System

In practice, optimizing for peak SNR is not always practical. One scenario in which the photoplethysmography (PPG) signal has a poor SNR is the signal limited regime. In this scenario, the LED current reaches an upper limit before the desired dc return level is achieved.

Tuning in this case starts where the peak SNR tuning stops. The starting point is nominally a 50k gain, as long as the lowest LED current setting of 8 mA does not saturate the photodiode and the 50k gain provides enough protection against intense background light. In these cases, use a 25k gain as the starting point.

The goal of the tuning process is to bring the dc return signal to a specific ADC range, such as 50% or 60%. The ADC range

choice is a function of the margin of headroom needed to prevent saturation as the dc level fluctuates over time. The SNR of the PPG waveform is always some percentage of the dc level. If the target level cannot be achieved at the base gain, increase the gain and repeat the procedure. The tuning system may need to place an upper limit on the gain to prevent saturation from ambient signals.

Tuning the Pulse Count

After the LED peak current and TIA gain are optimized, increasing the number of pulses per sample increases the SNR by the square root of the number of pulses. There are two ways to increase the pulse count. The pulse count registers (Register 0x31, Bits[15:8], and Register 0x36, Bits[15:8]) change the number of pulses per internal sample. Register 0x15, Bits[6:4] and Bits[10:8], controls the number of internal samples that are averaged together before the data is sent to the output. Therefore, the number of pulses per sample is the pulse count register multiplied by the number of subsequent samples being averaged. In general, the internal sampling rate increases as the number of internal sample averages increase to maintain the desired output data rate. The SNR/watt is most optimal with pulse count values of 16 or less. Above pulse count values of 16, the square root relationship does not hold in the pulse count register. However, this relationship continues to hold when averaged between samples using Register 0x15.

Note that increasing LED peak current increases SNR almost directly proportional to LED power, whereas increasing the number of pulses by a factor of n results in only a nominal$\sqrt{(n)}$ increase in SNR.

When using the sample sum/average function (Register 0x15), the output data rate decreases by the number of summed samples. To maintain a static output data rate, increase the sample frequency (Register 0x12) by the same factor as that selected in Register 0x15. For example, for a 100 Hz output data rate and a sample sum/average of four samples, set the sample frequency to 400 Hz.

SINGLE AFE CHANNEL MODE

When using a single photodiode in an application, and that photodiode is connected to a single AFE channel (see Table 16), the ADPD103 has an option to power down Channel 2, Channel 3, and Channel 4, which places the device in single AFE channel mode. Because three of the four AFE channels are turned off in this mode, the power consumption is considerably reduced.

It is important to leave the unused input channels floating for proper device operation. To run the device in single AFE channel mode, write 0x38 to Register 0x3C, Bits[8:3]. If it is not required to run the device in single AFE channel mode, leave Register 0x3C, Bits[8:3] at 0x00.

TIA_ADC MODE

There is a way to put the device into a mode that effectively runs the TIA directly in the ADC without using the analog band-pass filter and integrator. This mode is referred to as TIA_ADC mode. There are two basic applications of TIA_ADC mode. In normal operation, all of the background light is blocked from the signal chain, and therefore cannot be measured. TIA_ADC mode can be used to measure the amount of background/ambient light. This mode can also be used to measure other dc input currents, such as leakage resistance.

When the device is in TIA_ADC mode, the band-pass filter and the integrator stage are bypassed. This effectively wires the TIA directly into the ADC. At the set sampling frequency, the ADC samples Channel 1 through Channel 4 (or Channel 5 through Channel 8) in sequential order, and each sample is taken at 1 µs intervals. The TIA is in an inverting configuration; therefore, the signal drops as more light hits the photodiode. Zero light or dark conditions result in approximately 13,000 LSBs from the ADC.

To put the ADPD103 in TIA_ADC mode during Time Slot A, write 0xB065 to Register 0x43 to bypass the band-pass filter and integrator. Similarly, to place the ADPD103 in TIA_ADC mode during Time Slot B, write 0xB065 to Register 0x45. One way to monitor dc and pulsed signal at the same time is to operate TIA_ADC mode in one time slot and pulse mode in the other time slot. In TIA_ADC mode, increasing light level causes a decrease in ADC codes because the TIA stage is inverting.

Protecting Against TIA Saturation in Normal Operation

One of the reasons to monitor TIA_ADC mode is to protect against environments that may cause saturation. One concern when operating in high light conditions, especially with larger photodiodes, is that the TIA stage may become saturated and the ADPD103 continues to communicate data. The resulting saturation is not typical. The TIA, based on its settings, can only handle a certain level of photodiode current. Based on the way the ADPD103 is configured, if there is a current level from the photodiode that is larger than the TIA can handle, the TIA output during the LED pulse effectively extends the current pulse, making it wider. The AFE timing is then violated because the positive portion of the band-pass filter output extends into the negative section of the integration window. Thus, the photosignal is subtracted from itself, causing the output signal to decrease when the effective light signal increases.

To measure the response from the TIA and verify that this stage is not saturating, place the device in TIA_ADC mode and slightly modify the timing. Specifically, sweep SLOTx_AFE_OFFSET until two or three of the four channels reach a minimum value (note that TIA is in an inverting configuration). All four channels do not reach this minimum value because, typically, 3 µs LED pulse widths are used and the ADC samples the four channels sequentially at 1 µs intervals. This procedure aligns the ADC

sampling time with the LED pulse to measure the total amount of light falling on the photodetector (for example, background light + LED pulse).

If this minimum value is above 0 LSB, the TIA is not saturated. However, take care, because even if the result is not 0 LSB, operating the device near saturation can quickly result in saturation if light conditions change. A safe operating region is typically at ¾ full scale and lower. Use Table 17 to determine how the input codes map to ADC levels on a per channel per pulse basis. These codes are not the same as in normal mode because the band-pass filter and integrator are not unity-gain elements.

Coarse Ambient Light Measurement

Using the typical values in Table 17, TIA_ADC mode can be used to measure or quantify the amount of background or ambient light present on the photodetector. The settings are the same in the method described in the Protecting Against TIA Saturation in Normal Operation section, except the timing used in the normal operating mode is sufficient for this mode. There is no need to sweep AFE_OFFSET. If AFE_OFFSET is in the same place as the normal mode operation, the TIA_ADC mode does not return the same value, regardless of whether the LED is on or off.

In TIA_MODE, the dark level is a high level near 13,000 LSBs per channel per pulse (see Table 17). To measure this value, select no PD by writing a 0x0 to Register 0x14, Bits[11:8] for Time Slot B or Register 0x14, Bits[7:4] for Time Slot A. This setting internally opens the photodiode connection. This gives a baseline LSB value that coincides with a zero signal input.

After Register 0x14 is restored to its normal value, while connecting the photodiode to the TIA, this TIA_ADC result can be subtracted from the open photodiode case to yield a background light measurement. Use Table 17 to translate this measurement into an input photocurrent. Use this result for coarse absolute measurements only, because it is typically only accurate to within 10%.

Measuring PCB Parasitic Input Resistance

During the process of mounting the ADPD103, undesired resistance can develop on the inputs through assembly errors or debris on the PCB. These resistances can form between the anode and cathode, or between the anode and some other supply or ground. In normal operation, the ambient rejection feature of the ADPD103 masks the primary effects of these resistances, making it very difficult to detect them. However, even at 1 MΩ to 10 MΩ, such resistance can impact performance significantly through added noise or decreased dynamic range. TIA_ADC mode can be used to screen for these assembly issues.

Measuring Shunt Resistance on the Photodiode

A shunt resistor across the photodiode does not generally affect the output level of the device in operation because the effective impedance of the TIA is very low. This is especially true if the photodiode is held to 0 V in operation. However, such resistance can add noise to the system, degrading performance. The best way to detect photodiode leakage, also called photodiode shunt resistance, is to place the device in TIA_ADC mode in the dark and vary the operation mode cathode voltage. When the cathode is at 1.3 V, this places 0 V across the photodiode because the anode is always at 1.3 V while in operation. When the cathode is at 1.8 V, this places 0.5 V across the photodiode. Using the register settings in Table 3 to control the cathode voltage, measure the TIA_ADC value at both voltages. Next, divide the voltage difference of 0.5 V by the difference of the ADC result after converting it to a current. This result is the approximate shunt resistance. Values greater than 10 MΩ may be difficult to measure, but this method is useful in identifying gross failures.

Table 17. Analog Specifications for TIA_ADC and Digital Integrate Modes

Parameter	Test Conditions/Comments	Typ	Unit
TIA_ADC/Digital Integration Saturation Levels	Values expressed per channel, per sample		
	TIA Feedback Resistor:		
	25 kΩ	38.32	µA
	50 kΩ	19.16	µA
	100 kΩ	9.58	µA
	200 kΩ	4.79	µA
TIA_ADC Resolution	Values expressed per channel, per sample		
	TIA Feedback Resistor:		
	25 kΩ	2.92	nA/LSB
	50 kΩ	1.5	nA/LSB
	100 kΩ	0.73	nA/LSB
	200 kΩ	0.37	nA/LSB
Output with No Input Current	ADC offset (Register 0x18 to Register 0x21) = 0x0	13000	LSB

Measuring TIA Input Shunt Resistance

Another problem that can occur is for a resistance to develop between the TIA input and another supply or ground on the PCB. These resistances can force the TIA into saturation prematurely. This, in turn, takes away dynamic range from the device in operation and adds a Johnson noise component to the input. To measure these resistances, place the device in TIA_ADC mode in the dark and start by measuring the TIA_ADC offset level with the photodiode inputs disconnected (Register 0x14, Bits[11:8] = 0 or Register 0x14, Bits[7:4] = 0). From this, subtract the value of TIA_ADC mode with the darkened photodiode connected and convert the difference into a current. If the value is positive, and the ADC signal decreased, the resistance is to a voltage higher than 1.3 V, such as V_{DD}. Current entering the TIA causes the output to drop. If the output difference is negative due to an increase of codes at the ADC, current is being pulled out of the TIA and there is a shunt resistance to a lower potential than 1.3 V, such as ground.

DIGITAL INTEGRATE MODE

Digital integrate mode is built into the ADPD103 and allows the device to accommodate longer LED/AFE pulse widths and different types of sensors at the input. The analog integration mode described in the AFE Operation section is ideally suited for applications requiring a large LED duty cycle, or applications that require customization of the sampling scheme. Digital integrate mode allows the integration function to be performed after the ADC in the digital domain. This mode enables the device to handle a much wider range of sensors at the input.

In digital integrate mode, the ADC performs a conversion every 1 µs during the integration window. During the integration window, the digital engine either adds to or subtracts from the previous sample. The band-pass filter is bypassed and the integrator is converted to a voltage buffer, allowing the digital engine to perform the integration function. In this mode, after the timing is optimized, the output of the ADC increases as the light level on the photodiode increases.

The integration window is a combination of negative and positive windows where the duration of these windows is set by SLOTx_AFE_WIDTH. At the end of the digital integration window, the resulting sum is sent to the decimate unit as the sample for that LED pulse. There is one sample per time slot for every sample cycle. Table 18 lists the registers required for placing the device in digital integrate mode.

There may also be changes needed in the SLOTx_AFE_OFFSET registers and FIFO configuration register (0x11). To read the final value through the FIFO, set the appropriate values in Register 0x11, Bits[4:2] for Time Slot A, and Register 0x11, Bits[8:6] for Time Slot B. Alternatively, the final output is also available through the data registers; Register 0x64, Register 0x70, and Register 0x74 for Time Slot A, and Register 0x68, Register 0x78, and Register 0x7C for Time Slot B.

To put the ADPD103 into digital integration mode during Time Slot A, write 0x1 to Register 0x58, Bit 12. To put the ADPD103 into digital integration mode in Time Slot B, write 0x1 to Register 0x58, Bit 13. The other writes required to switch to digital integration mode are listed in Table 18.

When using digital integrate mode, up to two photodiodes can be connected to the ADPD103 inputs; one photodiode per PDx input group (PD1/PD2/PD3/PD4 or PD5/PD6/PD7/PD8). Never connect the same photodiode across the two PDx groups. In digital integrate mode, there are options to connect the photodiode to all four AFE channels (PD1/PD2/PD3/PD4 or PD5/PD6/PD7/PD8), or just a single AFE channel (PD1 or PD5). When connecting to a single AFE channel, write 0x1 to Register 0x54, Bit 14 for Time Slot A, or, for Time Slot B, write 0x1 to Register 0x54, Bit 15.

When connecting to a single AFE channel, there is also an option to turn off Channel 2, Channel 3, and Channel 4 (and to save power) by writing 0x7 to Register 0x55, Bits[15:13]. When connecting to all four channels (PD1/PD2/PD3/PD4 or PD5/PD6/PD7/PD8), write 0x0 (default)to Register 0x54, Bit 14 for Time Slot A, or write 0x0 (default) to Register 0x54, Bit 15 for Time Slot B. Ensure that all AFE channels are powered up by writing 0x0 to Register 0x55, Bits[15:13].

Connecting the single photodiode to a single AFE channel offers the best SNR performance in cases where signal is limited, whereas connecting the single photodiode to all four AFE channels offers the best dynamic range in cases where signal is large.

Digital Integration Sampling Modes

There are two sampling modes that can be used while the device is in digital integration mode. These modes are single-sample pair mode and double-sample pair mode.

In single-sample pair mode, there is a single negative sample region and a single positive sample region, shown in Figure 29 and Figure 30. To use single-sample pair mode, write 0x1 to Register 5A, Bit 5 for Time Slot A, or Register 5A, Bit 6 for Time Slot B. The negative sample region starts at SLOTx_AFE_OFFSET + 9 and its duration (the number of samples taken) is set by SLOTx_AFE_WIDTH. The positive sample region starts at SLOTx_AFE_OFFSET + 9 + SLOTx_AFE_WIDTH, and its duration is also set by SLOTx_AFE_WIDTH. Set the timing such that the negative sample region falls entirely in the flat (dark) portion of the LED response, whereas the positive sample region falls in the pulsed region of the LED response. Placing the LED pulse offset, SLOTx_LED_OFFSET, at the beginning of SLOTx_AFE_OFFSET + 9 + SLOTx_AFE_WIDTH achieves this timing. The output is the difference of the signals in the two regions.

Double-sample pair mode is another way to sample. In this mode, there are two negative sample regions and one long positive sample region (see Figure 27 and Figure 28). To use double-sample pair mode, write 0x0 to Register 0x5A, Bit 5 for Time Slot A, or Bit 6 for Time Slot B. The first negative sample region starts at SLOTx_AFE_OFFSET + 9 and its duration is set by SLOTx_AFE_WIDTH. The positive sample region starts at SLOTx_AFE_OFFSET + 9+ SLOTx_AFE_WIDTH and its duration is twice the SLOTx_AFE_WIDTH. After this, there is another negative sample region that starts at SLOTx_AFE_OFFSET + 9+ 3 × SLOTx_AFE_WIDTH, and its duration is SLOTx_AFE_WIDTH. Set the timing such that both of the negative sample regions fall in the flat (dark) portion of the LED response and the positive sample region falls in the pulsed portion of the LED response. Placing the LED pulse offset, SLOTx_LED_OFFSET at the beginning of SLOTx_AFE_OFFSET + 9 + SLOTx_AFE_WIDTH achieves this timing. The output is calculated by summing the response of all the regions in a negative/positive/negative manner. The double-sample pair mode is useful for cases when the background light is not constant because it has better background rejection, but it also uses more power than single-sample pair mode.

Sample Timing Modes

There are two options for timing the sample regions: gapped mode and continuous mode.

In gapped timing mode, there is a space between the negative and positive sample regions. The width of this region is specified by SLOTA_AFE_FOFFSET for Time Slot A and SLOTB_AFE_FOFFSET for Time Slot B in microseconds. To enable this feature, write 0x1 to Register 0x5A, Bit 7. This bit enables gapped timing for the time slot (or time slots) that are in digital integrate mode. This mode is helpful when there are unwanted transients in the LED response that must be ignored for an accurate output.

If there are no concerns about LED response transients, select continuous timing mode. In this mode, there is no space between the negative and positive sample regions. Write 0x0 to Register 0x5A, Bit 7 for continuous timing of the sample regions.

Both gapped and continuous sample timing modes can be used with single-sample pair or double-sample pair mode. Some example timing diagrams are shown in Figure 27, Figure 28, Figure 29, and Figure 30.

Background Values

In digital integrate mode, the digital integration background value, DI_BACKGROUND, or dark values are also stored and available as output data. This is in addition to the output value during the LED pulse, DI_OUTPUT, which has the dark value subtracted. DI_BACKGROUND is the sum of the negative region samples.

To include these values in the FIFO, set Register 0x11, Bits[4:2] for Time Slot A, and Register 0x11, Bits[8:6] for Time Slot B. For 16-bit data, set this value to 0x3; for 32-bit data, set this value to 0x04. These settings are also available through the data registers; Register 0x65, Register 0x71, and Register 0x75 for Time Slot A, and Register 0x69, Register 0x79, and Register 0x7D for Time Slot B. It is recommended that the channel offsets (Register 0x18 to Register 0x21) be set to 0x1F00 when including the background values in the FIFO in digital integration mode. These channel offsets do not affect the sample values, but do provide more headroom for the background values.

Saturation Detection in Digital Integrate Mode

In normal operation, when using the band-pass filter and the integrator, the ADC almost always saturates before the TIA. Unlike in normal operation, saturation of the TIA or the ADC cannot be detected solely by looking at the signal value where the signal value is the positive sample region minus the reference region in digital integrate mode. This is because the integrated value does not by itself contain any information indicating if one of the ADC conversions during the integration period exceeded the ADC output range. As a result, the real-time output may have saturated only for a fraction of the ADC conversions within a sample and the final accumulated sum may not reflect this. To detect TIA saturation in digital integration mode, both the background values, DI_BACKGROUND, and the signal values, DI_OUTPUT, must be collected. Refer to the Background Values section for the correct settings for Register 0x11 that provide these values.

For single-sample pair mode, saturation has occurred when

$$(DI_OUTPUT/(min(LED_WIDTH, AFE_WIDTH)) + DI_BACKGROUND/AFE_WIDTH)/NUM_PULSES > 0x3FFF$$

For double-sample pair mode, saturation has occurred when

$$(DI_OUTPUT/(min(LED_WIDTH, 2 \times AFE_WIDTH)) + DI_BACKGROUND/(2 \times AFE_WIDTH))/NUM_PULSES > 0x3FFF$$

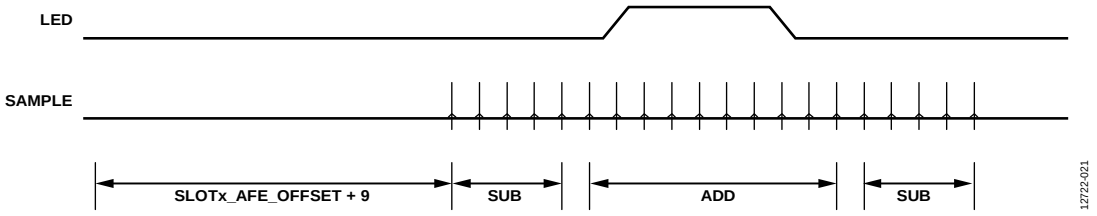

Figure 27. Digital Integration Mode in Double-Sample Pair Mode with Continuous Sample Timing

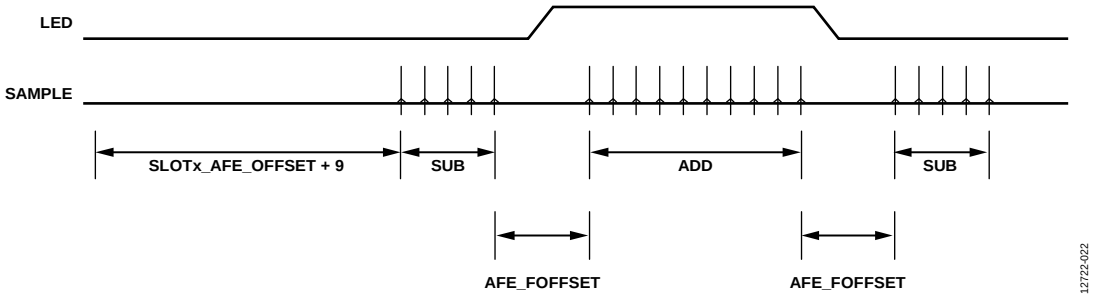

Figure 28. Digital Integration Mode in Double-Sample Pair Mode with Gapped Sample Timing

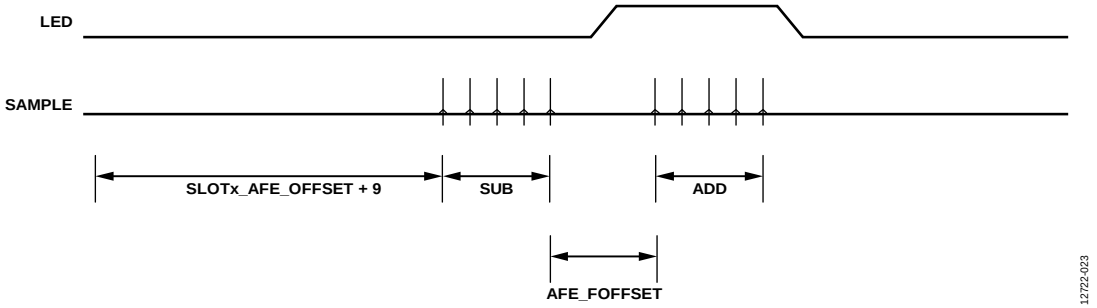

Figure 29. Digital Integration Mode in Single-Sample Pair Mode with Gapped Sample Timing

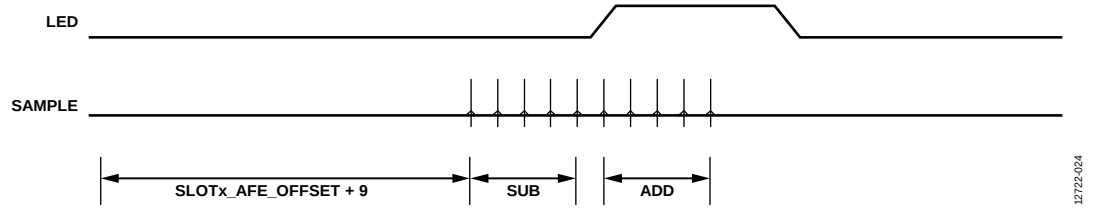

Figure 30. Digital Integration Mode in Single-Sample Pair Mode with Continuous Sample Timing

Table 18. Configuration Registers to Switch Between the Normal Sample Mode, TIA_ADC Mode, and Digital Integration Mode

Address	Data Bits	Bit Name	Normal Mode Value	TIA_ADC Mode Value	Digital Integration Mode Value	Description
0x42	[15:8]	SLOTA_AFE_MODE	0x1C	Not applicable	0x1D	In normal mode, this setting configures the integrator block for optimal operation. In digital integration mode, this setting configures the integrator block as a buffer. This setting is not important for TIA_ADC mode.
0x43	[15:0]	SLOTA_AFE_CFG	0xADA5	0xB065	0xAE65	Time Slot A AFE connection. 0xAE65 bypasses the band-pass filter. 0xB065 bypasses the band-pass filter and the integrator.
0x44	[15:8]	SLOTB_AFE_MODE	0x1C	Not applicable	0x1D	In normal mode, this setting configures the integrator block for optimal operation. In digital integration mode, this setting configures the integrator block as a buffer. This setting is not important for TIA_ADC mode.
0x45	[15:0]	SLOTB_AFE_CFG	0xADA5	0xB065	0xAE65	Time Slot B AFE connection. 0xAE65 bypasses the band-pass filter. 0xB065 bypasses the BPF and the integrator.
0x4E	[15:0]	ADC_TIMING	Not applicable	Not applicable	0x0040	Set ADC Clock to 1 MHz in TIA_ADC mode.
0x58	13	SLOTB_DIGITAL_INT_EN	0x0	0x0	0x1	Digital integrate mode enable Time Slot B. 0: disable. 1: enable.
	12	SLOTA_DIGITAL_INT_EN	0x0	0x0	0x1	Digital integrate mode enable Time Slot A. 0: disable. 1: enable.
0x5A	[15:0]	DIG_INT_CFG	Not applicable	Not applicable	Variable	Configuration of digital integration depends on the use case. This register is ignored for other modes.

REGISTER LISTING

Table 19. Numeric Register Listing[1]

Hex Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x00	Status	[15:8]	FIFO_SAMPLES[15:8]								0x0000	R/W
		[7:0]	Reserved	SLOTB_INT	SLOTA_INT	Reserved[4:0]						
0x01	INT_MASK	[15:8]	Reserved[15:9]							FIFO_INT_MASK	0x00FF	R/W
		[7:0]	Reserved	SLOTB_INT_MASK	SLOTA_INT_MASK	Reserved[4:0]						
0x02	INT_IO_CTL	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	Reserved[7:3]					INT_ENA	INT_DRV	INT_POL		
0x06	FIFO_THRESH	[15:8]	Reserved[15:14]		FIFO_THRESH[13:8]						0x0000	R/W
		[7:0]	Reserved[7:0]									
0x08	DEVID	[15:8]	REV_NUM[15:8]								0x0416	R
		[7:0]	DEV_ID[7:0]									
0x09	I2CS_ID	[15:8]	ADDRESS_WRITE_KEY[15:8]								0x00C8	R/W
		[7:0]	SLAVE_ADDRESS[7:1]							Reserved		
0x0A	CLK_RATIO	[15:8]	Reserved[15:12]				CLK_RATIO[11:8]				0x0000	R
		[7:0]	CLK_RATIO[7:0]									
0x0D	SLAVE_ADDRESS_KEY	[15:8]	SLAVE_ADDRESS_KEY[15:8]								0x0000	R/W
		[7:0]	SLAVE_ADDRESS_KEY[7:0]									
0x0F	SW_RESET	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	Reserved[7:1]							SW_RESET		
0x10	Mode	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	Reserved[7:2]						Mode[1:0]			
0x11	SLOT_EN	[15:8]	Reserved[15:14]		RDOUT_MODE	FIFO_OVRN_PREVENT	Reserved[11:9]			SLOTB_FIFO_MODE	0x1000	R/W
		[7:0]	SLOTB_FIFO_MODE[7:6]		SLOTB_EN	SLOTA_FIFO_MODE[4:2]			Reserved	SLOTA_EN		
0x12	FSAMPLE	[15:8]	FSAMPLE[15:8]								0x0028	R/W
		[7:0]	FSAMPLE[7:0]									
0x14	PD_LED_SELECT	[15:8]	Reserved[15:12]				SLOTB_PD_SEL[11:8]				0x0541	R/W
		[7:0]	SLOTA_PD_SEL[7:4]				SLOTB_LED_SEL[3:2]		SLOTA_LED_SEL[1:0]			
0x15	NUM_AVG	[15:8]	Reserved					SLOTB_NUM_AVG			0x0600	R/W
		[7:0]	Reserved	SLOTA_NUM_AVG			Reserved					
0x18	SLOTA_CH1_OFFSET	[15:8]	SLOTA_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH1_OFFSET[7:0]									
0x19	SLOTA_CH2_OFFSET	[15:8]	SLOTA_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH2_OFFSET[7:0]									
0x1A	SLOTA_CH3_OFFSET	[15:8]	SLOTA_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH3_OFFSET[7:0]									
0x1B	SLOTA_CH4_OFFSET	[15:8]	SLOTA_CH4_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH4_OFFSET[7:0]									
0x1E	SLOTB_CH1_OFFSET	[15:8]	SLOTB_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH1_OFFSET[7:0]									
0x1F	SLOTB_CH2_OFFSET	[15:8]	SLOTB_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH2_OFFSET[7:0]									
0x20	SLOTB_CH3_OFFSET	[15:8]	SLOTB_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH3_OFFSET[7:0]									
0x21	SLOTB_CH4_OFFSET	[15:8]	SLOTB_CH4_OFFSET[15:8]								0x2000	RW
		[7:0]	SLOTB_CH4_OFFSET[7:0]									

Hex Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x22	ILED3_COARSE	[15:8]	Reserved[15:14]		ILED3_SCALE	Reserved[12:8]					0x3000	R/W
		[7:0]	Reserved	ILED3_SLEW[6:4]			ILED3_COARSE[3:0]					
0x23	ILED1_COARSE	[15:8]	Reserved[15:14]		ILED1_SCALE	Reserved[12:8]					0x3000	R/W
		[7:0]	Reserved	ILED1_SLEW[6:4]			ILED1_COARSE[3:0]					
0x24	ILED2_COARSE	[15:8]	Reserved[15:14]		ILED2_SCALE	Reserved[12:8]					0x3000	R/W
		[7:0]	Reserved	ILED2_SLEW[6:4]			ILED2_COARSE[3:0]					
0x25	ILED_FINE	[15:8]	ILED3_FINE[15:11]					ILED2_FINE[10:8]			0x630C	R/W
		[7:0]	ILED2_FINE[7:6]		Reserved	ILED1_FINE[4:0]						
0x30	SLOTA_LED_PULSE	[15:8]	Reserved[15:13]			SLOTA_LED_WIDTH[12:8]					0x0320	R/W
		[7:0]	SLOTA_LED_OFFSET[7:0]									
0x31	SLOTA_NUM-PULSES	[15:8]	SLOTA_LED_NUMBER[15:8]								0x0818	R/W
		[7:0]	SLOTA_LED_PERIOD[7:0]									
0x34	LED_DISABLE	[15:8]	Reserved[15:10]						SLOTB_LED_DIS	SLOTA_LED_DIS	0x0000	R/W
		[7:0]	Reserved[7:0]									
0x35	SLOTB_LED_PULSE	[15:8]	Reserved[15:13]			SLOTB_LED_WIDTH[12:8]					0x0320	R/W
		[7:0]	SLOTB_LED_OFFSET[7:0]									
0x36	SLOTB_NUM-PULSES	[15:8]	SLOTB_LED_NUMBER[15:8]								0x0818	R/W
		[7:0]	SLOTB_LED_PERIOD[7:0]									
0x38	TIMING_CFG	[15:8]	Reserved	EXT_SYNC_ENA	Reserved[13:8]						0x000	R/W
		[7:0]	Reserved[7:0]									
0x39	SLOTA_AFE_WINDOW	[15:8]	SLOTA_AFE_WIDTH[15:11]					SLOTA_AFE_OFFSET[10:8]			0x22FC	R/W
		[7:0]	SLOTA_AFE_OFFSET[10:5]			SLOTA_AFE_FOFFSET[4:0]						
0x3B	SLOTB_AFE_WINDOW	[15:8]	SLOTB_AFE_WIDTH[15:11]					SLOTB_AFE_OFFSET[10:8]			0x22FC	R/W
		[7:0]	SLOTB_AFE_OFFSET[10:5]			SLOTB_AFE_FOFFSET[4:0]						
0x3C	AFE_PWR_CFG1	[15:8]	Reserved[15:14]		Reserved[13:11]			Reserved	V_CATHODE	AFE_POWER-DOWN	0x3006	R/W
		[7:0]	AFE_POWERDOWN[7:3]					Reserved[2:0]				
0x42	SLOTA_TIA_CFG	[15:8]	SLOTA_AFE_MODE[15:8]								0x1C38	R/W
		[7:0]	Reserved	SLOTA_TIA_IND_EN	Reserved[5:2] (write 0xD)				SLOTA_TIA_GAIN[1:0]			
0x43	SLOTA_AFE_CFG	[15:8]	SLOTA_AFE_CFG[15:8]								0xADA5	R/W
		[7:0]	SLOTA_AFE_CFG[7:0]									
0x44	SLOTB_TIA_CFG	[15:8]	SLOTB_AFE_MODE[15:8]								0x1C38	R/W
		[7:0]	Reserved	SLOTB_TIA_IND_EN	Reserved[5:2] (write 0xD)				SLOTB_TIA_GAIN[1:0]			
0x45	SLOTB_AFE_CFG	[15:8]	SLOTB_AFE_CFG[15:8]								0xADA5	R/W
		[7:0]	SLOTB_AFE_CFG[7:0]									
0x4B	SAMPLE_CLK	[15:8]	Reserved[15:8]								0x2612	R/W
		[7:0]	CLK32K_EN	Reserved	CLK32K_ADJUST[5:0]							
0x4D	CLK32M_ADJUST	[15:8]	RESERVED[15:8]								0x425E	R/W
		[7:0]	CLK32M_ADJUST[7:0]									
0x4E	ADC_CLOCK	[15:8]	ADC_CLOCK[15:8]								0x0060	R/W
		[7:0]	ADC_CLOCK[7:0]									
0x4F	EXT_SYNC_SEL	[15:8]	Reserved[15:8]								0x2090	R/W
		[7:0]	Reserved	PDSO_OE	PDSO_IE	Reserved	EXT_SYNC_SEL[3:2]		INT_IE	Reserved		

Hex Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x50	CLK32M_CAL_EN	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	Reserved	PDSO_CTRL	CLK32M_CAL_EN	Reserved[4:0]						
0x54	AFE_PWR_CFG2	[15:8]	SLOTB_SINGLE_CH_DIG_INT	SLOTA_SINGLE_CH_DIG_INT	SLEEP_V_CATHODE[13:12]		SLOTB_V_CATHODE[11:10]		SLOTA_V_CATHODE[9:8]		0x0020	R/W
		[7:0]	REG54_VCAT_ENABLE	Reserved[6:0]								
0x55	TIA_INDEP_GAIN	[15:8]	DIGINT_POWER[15:13]			Reserved	SLOTB_TIA_GAIN_4 [11:10]		SLOTB_TIA_GAIN_3[9:8]		0x0000	R/W
		[7:0]	SLOTB_TIA_GAIN_2[7:6]		SLOTA_TIA_GAIN_4[5:4]		SLOTA_TIA_GAIN_3[3:2]		SLOTA_TIA_GAIN_2[1:0]			
0x58	DIGITAL_INT_EN	[15:8]	Reserved[15:14]		SLOTB_DIGITAL_INT_EN	SLOTA_DIGITAL_INT_EN	Reserved[11:8]				0x0000	R/W
		[7:0]	Reserved[7:0]									
0x5A	DIG_INT_CFG	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	DIG_INT_GAPMODE	SLOTB_DIG_INT_SAMPLE-MODE	SLOTA_DIG_INT_SAMPLE-MODE	Reserved[4:0]						
0x5F	DATA_ACCESS_CTL	[15:8]	Reserved[15:8]								0x0000	R/W
		[7:0]	Reserved[7:3]					SLOTB_DATA_HOLD	SLOTA_DATA_HOLD	DIGITAL_CLOCK_ENA		
0x60	FIFO_ACCESS	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x64	SLOTA_PD1_16BIT	[15:8]	SLOTA_CH1_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_16BIT[7:0]									
0x65	SLOTA_PD2_16BIT	[15:8]	SLOTA_CH2_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_16BIT[7:0]									
0x66	SLOTA_PD3_16BIT	[15:8]	SLOTA_CH3_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_16BIT[7:0]									
0x67	SLOTA_PD4_16BIT	[15:8]	SLOTA_CH4_16BIT[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_16BIT[7:0]									
0x68	SLOTB_PD1_16BIT	[15:8]	SLOTB_CH1_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_16BIT[7:0]									
0x69	SLOTB_PD2_16BIT	[15:8]	SLOTB_CH2_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_16BIT[7:0]									
0x6A	SLOTB_PD3_16BIT	[15:8]	SLOTB_CH3_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_16BIT[7:0]									
0x6B	SLOTB_PD4_16BIT	[15:8]	SLOTB_CH4_16BIT[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_16BIT[7:0]									
0x70	A_PD1_LOW	[15:8]	SLOTA_CH1_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_LOW[7:0]									
0x71	A_PD2_LOW	[15:8]	SLOTA_CH2_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_LOW[7:0]									
0x72	A_PD3_LOW	[15:8]	SLOTA_CH3_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_LOW[7:0]									
0x73	A_PD4_LOW	[15:8]	SLOTA_CH4_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_LOW[7:0]									
0x74	A_PD1_HIGH	[15:8]	SLOTA_CH1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH1_HIGH[7:0]									

Hex Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x75	A_PD2_HIGH	[15:8]	SLOTA_CH2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH2_HIGH[7:0]									
0x76	A_PD3_HIGH	[15:8]	SLOTA_CH3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH3_HIGH[7:0]									
0x77	A_PD4_HIGH	[15:8]	SLOTA_CH4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_CH4_HIGH[7:0]									
0x78	B_PD1_LOW	[15:8]	SLOTB_CH1_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_LOW[7:0]									
0x79	B_PD2_LOW	[15:8]	SLOTB_CH2_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_LOW[7:0]									
0x7A	B_PD3_LOW	[15:8]	SLOTB_CH3_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_LOW[7:0]									
0x7B	B_PD4_LOW	[15:8]	SLOTB_CH4_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_LOW[7:0]									
0x7C	B_PD1_HIGH	[15:8]	SLOTB_CH1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH1_HIGH[7:0]									
0x7D	B_PD2_HIGH	[15:8]	SLOTB_CH2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH2_HIGH[7:0]									
0x7E	B_PD3_HIGH	[15:8]	SLOTB_CH3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH3_HIGH[7:0]									
0x7F	B_PD4_HIGH	[15:8]	SLOTB_CH4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_CH4_HIGH[7:0]									

[1] Recommended values not shown. Only power-on reset values are in Table 19. The recommended values are largely dependent on use case. See Table 20 to Table 26 for the recommended values.

LED CONTROL REGISTERS

Table 20. LED Control Registers

Address	Data Bit	Default Value	Access	Name	Description
0x14	[15:12]	0x0	R/W	Reserved	Write 0x0 to these bits for proper operation.
	[11:8]	0x5	R/W	SLOTB_PD_SEL	PDx connection selection for Time Slot B. See Figure 13. 0x1: All photodiode inputs are connected during Time Slot B. 0x4: PD5/PD6/PD7/PD8 are connected during Time Slot B. 0x5: PD1/PD2/PD3/PD4 are connected during Time Slot B. Other: reserved.
	[7:4]	0x4	R/W	SLOTA_PD_SEL	PDx connection selection for Time Slot A. See Figure 13. 0x1: All photodiode inputs are connected during Time Slot A. 0x4: PD5/PD6/PD7/PD8 are connected during Time Slot A. 0x5: PD1/PD2/PD3/PD4 are connected during Time Slot A. Other: reserved.
	[3:2]	0x0	R/W	SLOTB_LED_SEL	Time Slot B LED configuration. These bits determine which LED is associated with Time Slot B. 0x0: reserved. 0x1: LEDX1 pulses during Time Slot B. 0x2: LEDX2 pulses during Time Slot B. 0x3: LEDX3 pulses during Time Slot B.
	[1:0]	0x1	R/W	SLOTA_LED_SEL	Time Slot A LED configuration. These bits determine which LED is associated with Time Slot A. 0x0: reserved. 0x1: LEDX1 pulses during Time Slot A. 0x2: LEDX2 pulses during Time Slot A. 0x3: LEDX3 pulses during Time Slot A.
0x22	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED3_SCALE	LEDX3 current scale factor. 1: 100% strength. 0: 40% strength; sets the LEDX3 driver in low power mode. LEDX3 Current Scale = 0.4 + 0.6 × (Register 0x22, Bit 13).
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	ILED3_SLEW	LEDX3 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0: the slowest slew rate. … 7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED3_COARSE	LEDX3 coarse current setting. Coarse current sink target value of LEDX3 in standard operation. 0: 25 mA. 1: 40 mA. 2: 55 mA. … 15: 250 mA. $LED3_{PEAK} = LED3_{COARSE} \times LED3_{FINE} \times LED3_{SCALE}$ where: $LED3_{PEAK}$ is the LEDX3 peak target value (mA). $LED3_{COARSE}$ = 28 + 15.46 × (Register 0x22, Bits[3:0]). $LED3_{FINE}$ = 0.71 + 0.024 × (Register 0x25, Bits[15:11]). $LED3_{SCALE}$ = 0.4 + 0.6 × (Register 0x22, Bit 13).

Address	Data Bit	Default Value	Access	Name	Description
0x23	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED1_SCALE	LEDX1 current scale factor. 1: 100% strength. 0: 40% strength; sets the LEDX1 driver in low power mode. *LEDX1 Current Scale* = 0.4 + 0.6 × (*Register 0x23, Bit 13*).
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	ILED1_SLEW	LEDX1 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0: the slowest slew rate. … 7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED1_COARSE	LEDX1 coarse current setting. Coarse current sink target value of LEDX1 in standard operation. 0: 25 mA. 1: 40 mA. 2: 55 mA. … 15: 250 mA. $LED1_{PEAK} = LED1_{COARSE} \times LED1_{FINE} \times LED1_{SCALE}$ where: $LED1_{PEAK}$ is the LEDX1 peak target value (mA). $LED1_{COARSE}$ = 28 + 15.46 × (Register 0x23, Bits[3:0]). $LED1_{FINE}$ = 0.71 + 0.024 × (Register 0x25, Bits[4:0]). $LED1_{SCALE}$ = 0.4 + 0.6 × (Register 0x23, Bit 13).
0x24	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x1	R/W	ILED2_SCALE	LEDX2 current scale factor. 1: 100% strength. 0: 40% strength; sets the LEDX2 driver in low power mode. *LED2 Current Scale* = 0.4 + 0.6 × (*Register 0x24, Bit 13*)
	12	0x1	R/W	Reserved	Write 0x1.
	[11:7]	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	ILED2_SLEW	LEDX2 driver slew rate control. The slower the slew rate, the safer the performance in terms of reducing the risk of overvoltage of the LED driver. 0: the slowest slew rate. … 7: the fastest slew rate.
	[3:0]	0x0	R/W	ILED2_COARSE	LEDX2 coarse current setting. Coarse current sink target value of LED2 in standard operation. See Register 0x23, Bits[3:0] for values. $LED2_{PEAK} = LED2_{COARSE} \times LED2_{FINE} \times LED2_{SCALE}$ where: $LED2_{PEAK}$ is the LEDX2 peak target value (mA). $LED2_{COARSE}$ = 28 + 15.46 × (Register 0x24, Bits[3:0]). $LED2_{FINE}$ = 0.71 + 0.024 × (Register 0x25, Bits[10:6]). $LED2_{SCALE}$ = 0.4 + 0.6 × (Register 0x24, Bit 13).

Address	Data Bit	Default Value	Access	Name	Description
0x25	[15:11]	0xC	R/W	ILED3_FINE	LEDX3 fine adjust. Current adjust multiplier for LED3. *LEDX3 fine adjust* = 0.71 + 0.024 × (*Register 0x25, Bits[15:11]*). See Register 0x22, Bits[3:0], for the full LED3 formula.
	[10:6]	0xC	R/W	ILED2_FINE	LEDX2 fine adjust. Current adjust multiplier for LED2. *LEDX2 fine adjust* = 0.71 + 0.024 × (*Register 0x25, Bits[10:6]*). See Register 0x24, Bits[3:0], for the full LED2 formula.
	5	0x0	R/W	Reserved	Write 0x0.
	[4:0]	0xC	R/W	ILED1_FINE	LEDX1 fine adjust. Current adjust multiplier for LED1. *LEDX1 fine adjust* = 0.71 + 0.024 × (*Register 0x25, Bits[4:0]*). See Register 0x23, Bits[3:0], for the full LED1 formula.
0x30	[15:13]	0x0	R/W	Reserved	Write 0x0.
	[12:8]	0x3	R/W	SLOTA_LED_WIDTH	LED pulse width (in 1 µs step) for Time Slot A.
	[7:0]	0x20	R/W	SLOTA_LED_OFFSET	LED offset width (in 1 µs step) for Time Slot A.
0x31	[15:8]	0x08	R/W	SLOTA_LED_NUMBER	LED Time Slot A pulse count. n_A: number of LED pulses in Time Slot A. This is typically LED1. Adjust in the application. A setting of six pulses (0x06) is typical.
	[7:0]	0x18	R/W	SLOTA_LED_PERIOD	LED Time Slot A pulse period (in 1 µs step).
0x34	[15:10]	0x00	R/W	Reserved	Write 0x0.
	9	0x0	R/W	SLOTB_LED_DIS	Time Slot B LED disable. 1: disables the LED assigned to Time Slot B. Register 0x34 keeps the drivers active and prevents them from pulsing current to the LEDs. Disabling both LEDs via this register is often used to measure the dark level. Use Register 0x11 instead to enable or disable the actual time slot usage and not only the LED.
	8	0x0	R/W	SLOTA_LED_DIS	Time Slot A LED disable. 1: disables the LED assigned to Time Slot A. Use Register 0x11 instead to enable or disable the actual time slot usage and not only the LED.
	[7:0]	0x00	R/W	Reserved	Write 0x00.
0x35	[15:13]	0x0	R/W	Reserved	Write 0x0.
	[12:8]	0x3		SLOTB_LED_WIDTH	LED pulse width (in 1 µs step) for Time Slot B.
	[7:0]	0x20		SLOTB_LED_OFFSET	LED offset width (in 1 µs step) for Time Slot B.
0x36	[15:8]	0x08	R/W	SLOTB_LED_NUMBER	LED Time Slot B pulse count. n_B: number of LED pulses in Time Slot B. This is typically LED2. A setting of six pulses (0x06) is typical.
	[7:0]	0x18	R/W	SLOTB_LED_PERIOD	LED Time Slot B pulse period (in 1 µs step).
0x3C	[15:14]	0x0	R/W	RESERVED	Write 0x0.
	[13:11]	0x6	R/W	RESERVED	Write 0x6.
	10	0x0	R/W	Reserved	Write 0x0.
	9	0x0	R/W	V_CATHODE	0x0: 1.3 V (identical to anode voltage); recommended setting. 0x1: 1.8 V (reverse bias photodiode by 550 mV; this setting may add noise).
	[8:3]	0x0	R/W	AFE_POWERDOWN	AFE channels power-down select. 0x38: powers down AFE Channel 2, Channel 3, and Channel 4. 0x0: keeps all channels on.
	[2:0]	0x6	R/W	Reserved	Write 0x6.

AFE CONFIGURATION REGISTERS

Table 21. AFE Global Configuration Registers

Address	Data Bit	Default Value	Access	Name	Description
0x3C	[15:14]	0x0	R/W	RESERVED	Write 0x0.
	[13:11]	0x6	R/W	RESERVED	Write 0x6.
	10	0x0	R/W	Reserved	Write 0x0.
	9	0x0	R/W	V_CATHODE	0x0: 1.3 V (identical to anode voltage); recommended setting. 0x1: 1.8 V (reverse bias photodiode by 550 mV. This setting may add noise).
	[8:3]	0x0	R/W	AFE_POWERDOWN	AFE channels power-down select. 0x38: powers down AFE Channel 2, Channel 3, and Channel 4. 0x0: keeps all channels on.
	[2:0]	0x6	R/W	Reserved	Write 0x6.
0x54	15	0x0	R/W	SLOTB_SINGLE_CH_DIG_INT	0: In Time Slot B, use all four photodiode channels in parallel for digital integration (default setting for highest dynamic range) 1: In Time Slot B, use only Channel 1 for digital integration. This limits connection to PD1 or PD5.
	14	0x0	R/W	SLOTA_SINGLE_CH_DIG_INT	0: In Time Slot A, use all four photodiode channels in parallel for digital integration (default setting for highest dynamic range) 1: In Time Slot A, use only Channel 1 for digital integration. This limits connection to PD1 or PD5.
	[13:12]	0x0	R/W	SLEEP_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in sleep mode. The anode voltage is always set to the cathode voltage in sleep mode. 0x0: V_{DD} (1.8 V). 0x1: 1.3 V. 0x2: 1.55 V. 0x3: 0.0 V.
	[11:10]	0x0	R/W	SLOTB_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in Time Slot B operation. The anode voltage is always 1.3 V in Time Slot B mode. 0x0: V_{DD} (1.8 V). 0x1: 1.3 V. 0x2: 1.55 V. 0x3: 0.0 V (this forward biases a diode at the input).
	[9:8]	0x0	R/W	SLOTA_V_CATHODE	If Bit 7 = 1; this setting is applied to the cathode voltage while the device is in Time Slot A operation. The anode voltage is always 1.3 V in Time Slot A mode. 0x0: VDD (1.8 V). 0x1: 1.3 V. 0x2: 1.55 V. 0x3: 0.0 V (this forward biases a diode at the input).
	7	0x0	R/W	REG54_VCAT_ENABLE	0: use the cathode voltage settings defined by Register 0x3C, Bit 9. 1: override Register 0x3C, Bit 9 with cathode settings defined by Register 0x54, Bits[13:8].
	[6:0]	0x20	R/W	Reserved	Write 0x20.

Address	Data Bit	Default Value	Access	Name	Description
0x58	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x0	R/W	SLOTB_DIGITAL_INT_EN	0x0: Time Slot B operating in normal mode. 0x1: Time Slot B operating in digital integration mode.
	12	0x0	R/W	SLOTA_DIGITAL_INT_EN	0x0: Time Slot A operating in normal mode. 0x1: Time Slot A operating in digital integration mode.
	[11:0]	0x000	R/W	Reserved	Write 0x000.
0x5A	[15:8]	0x00	R/W	Reserved	Write 0x00.
	7	0x0	R/W	DIG_INT_GAPMODE	Digital integrate gapped mode enable. 0: no gap between negative and positive sample regions. 1: use SLOTA_AFE_FOFFSET for Time Slot A or SLOTB_AFE_FOFFSET for Time Slot B to specify the gap in µs.
	6	0x0	R/W	SLOTB_DIG_INT_SAMPLE_MODE	Digital integrate single sample pair mode for Time Slot B. 0: double sample pair mode. 1: single sampled pair mode.
	5	0x0	R/W	SLOTA_DIG_INT_SAMPLE_MODE	Digital integrate single sample pair mode for Time Slot A. 0: double sample pair mode. 1: single sampled pair mode.
	[4:0]	0x00	R/W	Reserved	Write 0x00.

Table 22. AFE Configuration Registers, Time Slot A

Address	Data Bit	Default Value	Access	Name	Description
0x39	[15:11]	0x4	R/W	SLOTA_AFE_WIDTH	AFE integration window width (in 1 µs step) for Time Slot A.
	[10:5]	0x17	R/W	SLOTA_AFE_OFFSET	AFE integration window coarse offset (in 1 µs step) for Time Slot A.
	[4:0]	0x1C	R/W	SLOTA_AFE_FOFFSET	AFE integration window fine offset (in 31.25 ns step) for Time Slot A.
0x42	[15:8]	0x1C	R/W	SLOTA_AFE_MODE	0x1C: Time Slot A AFE setting for normal mode. All four blocks of the signal chain are in use during normal mode (the TIA, the BPF, followed by the integrator (INT), and finally the ADC). 0x1D: Time Slot A AFE setting for digital integrate mode.
	7	0x0	R/W	Reserved	Write 0x0.
	6	0x0	R/W	SLOTA_TIA_IND_EN	Enable Time Slot A TIA gain individual settings. When it is enabled, the Channel 1 TIA gain is set via Register 0x42, Bits[1:0], and the Channel 2 through Channel 4 TIA gain is set via Register 0x55, Bits[5:0]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:2]	0xE	R/W	Reserved	Reserved. Write 0xD.
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN	Transimpedance amplifier gain for Time Slot A. When SLOTA_TIA_IND_EN is enabled, this value is for Time Slot B, Channel 1 TIA gain. When SLOTA_TIA_IND_EN is disabled, it is for all four Time Slot A channel TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Address	Data Bit	Default Value	Access	Name	Description
0x43	[15:0]	0xADA5	R/W	SLOTA_AFE_CFG	AFE connection in Time Slot A. 0xADA5: analog full path mode (TIA_BPF_INT_ADC). 0xB065: TIA_ADC mode. 0xAE65: digital integration mode. Others: reserved.
0x55	[15:13]	0x0	R/W	DIGINT_POWER	Power-down for Channel 2, Channel 3, and Channel 4 in digital integration mode. 0: keep all channels powered up. 7: powers down Channel 2, Channel 3, and Channel 4.
	12	0x0	R/W	Reserved	Write 0x0.
	[11:10]	0x0	R/W	SLOTB_TIA_GAIN_4	TIA gain for Time Slot B, Channel 4 (PD4). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[9:8]	0x0	R/W	SLOTB_TIA_GAIN_3	TIA gain for Time Slot B, Channel 3 (PD3). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[7:6]	0x0	R/W	SLOTB_TIA_GAIN_2	TIA gain for Time Slot B, Channel 2 (PD2). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[5:4]	0x0	R/W	SLOTA_TIA_GAIN_4	TIA gain for Time Slot A, Channel 4 (PD4). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[3:2]	0x0	R/W	SLOTA_TIA_GAIN_3	TIA gain for Time Slot A, Channel 3 (PD3). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN_2	TIA gain for Time Slot A, Channel 2 (PD2). 0: 200 kΩ 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Address	Data Bit	Default Value	Access	Name	Description
0x5A	[15:8]	0x0	R/W	Reserved	Write 0x0.
	7	0x0	R/W	DIG_INT_GAPMODE	Digital integration gapped mode enable. 0: no gap between negative and positive sample regions. 1: use SLOTA_AFE_FOFFSET for Time Slot A or SLOTB_AFE_FOFFSET for Time Slot B to specify the gap in µs.
	6	0x0	R/W	SLOTB_DIG_INT_SAMPLEMODE	Digital integration single-sample pair mode for Time Slot B. 0: double sample pair mode. 1: single-sampled pair mode.
	5	0x0	R/W	SLOTA_DIG_INT_SAMPLEMODE	Digital integration single-sample pair mode for Time Slot A. 0: double sample pair mode. 1: single-sampled pair mode.
	[4:0]	0x0	R/W	Reserved	Write 0x0.

Table 23. AFE Configuration Registers, Time Slot B

Address	Data Bit	Default Value	Access	Name	Description
0x3B	[15:11]	0x4	R/W	SLOTB_AFE_WIDTH	AFE integration window width (in 1 µs step) for Time Slot B.
	[10:5]	0x17	R/W	SLOTB_AFE_OFFSET	AFE integration window coarse offset (in 1 µs step) for Time Slot B.
	[4:0]	0x1C	R/W	SLOTB_AFE_FOFFSET	AFE integration window fine offset (in 31.25 ns step) for Time Slot B.
0x44	[15:8]	0x1C	R/W	SLOTB_AFE_MODE	0x1C: Time Slot B AFE setting for normal mode (TIA_BPF_INT_ADC). 0x1D: Time Slot B AFE setting for digital integrate mode.
	7	0x0	R/W	Reserved	Write 0x0.
	6	0x0	R/W	SLOTB_TIA_IND_EN	Enable Time Slot B TIA gain individual settings. When it is enabled, the Channel 1 TIA gain is set via Register 0x44, Bits[1:0], and the Channel 2 through Channel 4 TIA gain is set via Register 0x55, Bits[11:6]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:2]	0xE	R/W	Reserved	Write 0xD.
	[1:0]	0x0	R/W	SLOTB_TIA_GAIN	Transimpedance amplifier gain for Time Slot B. When SLOTB_TIA_IND_EN is enabled, this value is for Time Slot B, Channel 1 TIA gain. When SLOTB_TIA_IND_EN is disabled, it is for all four Time Slot B channel TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
0x45	[15:0]	0xADA5	R/W	SLOTB_AFE_CFG	AFE connection in Time Slot B. 0xADA5: analog full path mode (TIA_BPF_INT_ADC). 0xB065: TIA_ADC mode. 0xAE65: digital integration mode. Others: reserved.

Address	Data Bit	Default Value	Access	Name	Description
0x58	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x0	R/W	DIG_INT_EN_B	Digital integration mode, enable Time Slot B. 0: disable. 1: enable.
	12	0x0	R/W	DIG_INT_EN_A	Digital integration mode, enable Time Slot A. 0: disable. 1: enable.
	[11:0]	0x0000	R/W	Reserved	Write 0x0000.

SYSTEM REGISTERS

Table 24. System Registers

Address	Data Bit	Default	Access	Name	Description
0x00	[15:8]	0x00	R/W	FIFO_SAMPLES	FIFO status. Number of available bytes to be read from the FIFO. When comparing this to the FIFO length threshold (Register 0x06, Bits[13:8]), note that the FIFO status value is in bytes and the FIFO length threshold is in words, where one word = two bytes. With the FIFO_ACCESS_ENA bit set, write 1 to Bit 15 of FIFO_SAMPLES to clear the contents of the FIFO.
	7	0x0	R/W	Reserved	Write 0x1 to clear this bit to 0x0.
	6	0x0	R/W	SLOTB_INT	Time Slot B interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing, the register goes to 0. Writing a 0 to this register has no effect.
	5	0x0	R/W	SLOTA_INT	Time Slot A interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing, the register goes to 0. Writing a 0 to this register has no effect
	[4:0]	0x00	R/W	Reserved	Write 0x1F to clear these bits to 0x00.
0x01	[15:9]	0x00	R/W	Reserved	Write 0x00.
	8	0x0	R/W	FIFO_INT_MASK	Sends an interrupt when the FIFO data length has exceeded the FIFO length threshold in Register 0x06, Bits[13:8]. A 0 enables the interrupt.
	7	0x1	R/W	Reserved	Write 0x1.
	6	0x1	R/W	SLOTB_INT_MASK	Sends an interrupt on the Time Slot B sample. Write a 1 to disable the interrupt. Write a 0 to enable the interrupt.
	5	0x1	R/W	SLOTA_INT_MASK	Sends an interrupt on the Time Slot A sample. Write a 1 to disable the interrupt. Write a 0 to enable the interrupt.
	[4:0]	0x1F	R/W	Reserved	Write 0x1F.
0x02	[15:3]	0x0000	R/W	Reserved	Write 0x0000.
	2	0x0	R/W	INT_ENA	INT pin enable. 0: disable the INT pin. The INT pin floats regardless of interrupt status. The status register (Address 0x00) remains active. 1: enable the INT pin.
	1	0x0	R/W	INT_DRV	INT drive. 0: the INT pin is always driven. 1: the INT pin is driven when the interrupt is asserted; otherwise, it is left floating and requires a pull-up or pull-down resistor, depending on polarity (operates as open drain). Use this setting if multiple devices need to share the INT pin.
	0	0x0	R/W	INT_POL	INT polarity. 0: the INT pin is active high. 1: the INT pin is active low.
0x06	[15:14]	0x0	R/W	Reserved	Write 0x0.
	[13:8]	0x00	R/W	FIFO_THRESH	FIFO length threshold. An interrupt is generated when the number of data-words in the FIFO exceeds the value in FIFO_THRESH. The interrupt pin automatically deasserts when the number of data-words available in the FIFO no longer exceeds the value in FIFO_THRESH.
	[7:0]	0x00	R/W	Reserved	Write 0x00.
0x08	[15:8]	0x04	R	REV_NUM	Revision number.
	[7:0]	0x16	R	DEV_ID	Device ID.

Address	Data Bit	Default	Access	Name	Description
0x09	[15:8]	0x0	W	ADDRESS_WRITE_KEY	Write 0xAD when writing to SLAVE_ADDRESS. Otherwise, do not access.
	[7:1]	0x64	R/W	SLAVE_ADDRESS	I^2C slave address.
	0	0x0	R	Reserved	Do not access.
0x0A	[15:12]	0x0	R	Reserved	Reserved. Read only.
	[11:0]	0x000	R	CLK_RATIO	When the CLK32M_CAL_EN bit (Register 0x50, Bit 5) is set, the device calculates the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. The result, nominally 2000 (0x07D0), is stored in the CLK_RATIO bits.
0x0D	[15:0]	0x0	R/W	SLAVE_ADDRESS_KEY	Enable changing the I^2C address using Register 0x09. 0x04AD: enable address change always. 0x44AD: enable address change if INT is high. 0x84AD: enable address change if PDSO is high. 0xC4AD: enable address change if both INT and PDSO are high.
0x0F	[15:1]	0x0000	R	Reserved	Reserved. Read only.
	0	0x0	R/W	SW_RESET	Software reset. Write 0x1 to reset the device. This bit clears itself after a reset. This command does not return an acknowledge because the command is instantaneous.
0x10	[15:2]	0x000	R/W	Reserved	Write 0x000.
	[1:0]	0x0	R/W	Mode	Determines the operating mode of the ADPD103. 0x0: standby. 0x1: program. 0x2: normal operation.
0x11	[15:14]	0x0	R/W	Reserved	Write 0x0.
	13	0x0	R/W	RDOUT_MODE	Readback data mode for extended data registers 0x0: Block sum of N samples 0x1: Block average of N samples
	12	0x1	R/W	FIFO_OVRN_PREVENT	0x0: wrap around FIFO, overwriting old data with new. 0x1: new data if FIFO is not full (recommended setting).
	[11:9]	0x0	R/W	Reserved	Write 0x0.
	[8:6]	0x0	R/W	SLOTB_FIFO_MODE	Time Slot B FIFO data format. 0: no data to FIFO. 1: 16-bit sample in digital integration mode or 16-bit sum of all 4 channels when not in digital integration mode. 2: 32-bit sample in digital integration mode or 32-bit sum of all 4 channels when not in digital integration mode. 3: 16-bit sample and 16-bit background value in digital integration mode 4: 32-bit sample and 32-bit background value in digital integration mode or 4 channels of 16-bit sample data for Time Slot B when not in digital integration mode. 6: 4 channels of 32-bit extended sample data for Time Slot B when not in digital integration mode. Others: reserved. The selected Time Slot B data is saved in the FIFO. Available only if Time Slot A has the same averaging factor, N (Register 0x15, Bits[10:8] = Bits[6:4]), or if Time Slot A is not saving data to the FIFO (Register 0x11, Bits[4:2] = 0).
	5	0x0	R/W	SLOTB_EN	Time Slot B enable. 1: enables Time Slot B.

Address	Data Bit	Default	Access	Name	Description
	[4:2]	0x0	R/W	SLOTA_FIFO_MODE	Time Slot A FIFO data format. 0: no data to FIFO. 1: 16-bit sample in digital integration mode or 16-bit sum of all 4 channels when not in digital integration mode. 2: 32-bit sample in digital integration mode or 32-bit sum of all 4 channels when not in digital integration mode. 3: 16-bit sample and 16-bit background value in digital integration mode 4: 32-bit sample and 32-bit background value in digital integration mode or 4 channels of 16-bit sample data for Time Slot B when not in digital integration mode. 6: 4 channels of 32-bit extended sample data for Time Slot B when not in digital integration mode. Others: reserved.
	1	0x0	R/W	Reserved	Write 0x0.
	0	0x0	R/W	SLOTA_EN	Time Slot A enable. 1: enables Time Slot A.
0x38	15	0x0	R/W	Reserved	Write 0x0.
	14	0x0	R/W	EXT_SYNC_ENA	Enables external sampling trigger. 0x0: samples triggered internally. 0x1: samples triggered externally. Must be set to 1 if EXT_SYNC_SEL is b01 or b10.
	[13:0]	0x0	R/W	Reserved	Write 0x0.
0x4B	[15:9]	0x13	R/W	Reserved	Write 0x13.
	8	0x0	R/W	CLK32K_BYP	Bypass internal 32 kHz clock oscillator. 0x0: normal operation. 0x1: use an external clock on the PDSO pin.
	7	0x0	R/W	CLK32K_EN	Sample clock power-up. Enables the data sample clock. 0x0: clock disabled. 0x1: normal operation.
	6	0x0	R/W	Reserved	Write 0x0.
	[5:0]	0x12	R/W	CLK32K_ADJUST	Data sampling (32 kHz) clock frequency adjust. This register is used to calibrate the sample frequency of the device to achieve high precision on the data rate as defined in Register 0x12. Adjusts the sample master 32 kHz clock by 0.6 kHz per LSB. For a 100 Hz sample rate as defined in Register 0x12, 1 LSB of Register 0x4B, Bits[5:0], is 1.9 Hz. Note that a larger value produces a lower frequency. See the Clocks and Timing Calibration section for more information regarding clock adjustment. 00 0000: maximum frequency. 10 0010: typical center frequency. 11 1111: minimum frequency.
0x4D	[15:8]	0x42	R/W	Reserved	Write 0x42.
	[7:0]	0x5E	R/W	CLK32M_ADJUST	Internal timing (32 MHz) clock frequency adjust. This register is used to calibrate the internal clock of the device to achieve precisely timed LED pulses. Adjusts the 32 MHz clock by 109 kHz per LSB. See the Clocks and Timing Calibration section for more information regarding clock adjustment. 0000 0000: minimum frequency. 0101 1110: default frequency. 1111 1111: maximum frequency.
0x4E[1]	[15:0]	0x0060	R/W	ADC_TIMING[1]	0x0040: ADC clock speed = 1 MHz. 0x0060: ADC clock speed = 500 kHz.

Address	Data Bit	Default	Access	Name	Description
0x4F	[15:7]	0x41	R/W	Reserved	Write 0x41.
	6	0x0	R/W	PDSO_OE	PDSO pin output enable.
	5	0x0	R/W	PDSO_IE	PDSO pin input enable.
	4	0x1	R/W	Reserved	Write 0x1.
	[3:2]	0x0	R/W	EXT_SYNC_SEL	Sample sync select. 00: use the internal 32 kHz clock with FSAMPLE to select sample timings. 01: use the INT pin to trigger sample cycle. 10: use the PDSO pin to trigger sample cycle. 11: reserved.
	1	0x0	R/W	INT_IE	INT pin input enable.
	0	0x0	R/W	Reserved	Write 0x0.
0x50	[15:7]	0x000	R/W	Reserved	Write 0x000.
	6	0x0	R/W	PDSO_CTRL	Controls the PDSO output when the PDSO output is enabled (PDSO_OE = 0x1). 0x0: PDSO output driven low. 0x1: PDSO output driven by the AFE power-down signal.
	5	0x0	R/W	CLK32M_CAL_EN	As part of the 32 MHz clock calibration routine, write 1 to begin the clock ratio calculation. Read the result of this calculation from the CLK_RATIO bits in Register 0x0A. Reset this bit to 0 prior to reinitiating the calculation.
	[4:0]	0x0	R/W	Reserved	Write 0x0.
0x5F	[15:3]	0x0000	R/W	Reserved	Write 0x0000.
	2	0x0	R/W	SLOTB_DATA_HOLD	Setting this bit prevents the update of the data registers corresponding to Time Slot B. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels. 1: hold data registers for Time Slot B. 0: allow data register update.
	1	0x0	R/W	SLOTA_DATA_HOLD	Setting this bit prevents the update of the data registers corresponding to Time Slot A. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels. 1: hold data registers for Time Slot A. 0: allow data register update.
	0	0x0	R/W	FIFO_ACCESS_ENA	Set to 1 twice to enable FIFO access. It is necessary to write 1 to the FIFO_ACCESS_ENA bit in two consecutive write operations in order to read data from the FIFO. During clock calibration, set to 1 to force the 32 MHz clock to run. For power savings, reset to 0 when the previously described operations are complete.

[1] Clock speed setting is only relevant during digital integrate mode.

ADC REGISTERS

Table 25. ADC Registers

Address	Data Bits	Default	Access	Name	Description
0x12	[15:0]	0x0028	R/W	FSAMPLE	Sampling frequency: f_{SAMPLE} = 32 kHz/(Register 0x12, Bits[15:0] × 4). For example, 100 Hz = 0x0050; 200 Hz = 0x0028.
0x15	[15:11]	0x0	R/W	Reserved	Write 0x0.
	[10:8]	0x6	R/W	SLOTB_NUM_AVG	Sample sum/average for Time Slot B. Specifies the averaging factor, N_B, which is the number of consecutive samples that is summed and averaged after the ADC. Register 0x70 to Register 0x7F hold the data sum. Register 0x64 to Register 0x6B and the data buffer in Register 0x60 hold the data average, which can be used to increase SNR without clipping, in 16-bit registers. The data rate is decimated by the value of the SLOTB_NUMB_AVG bits. 0: 1. 1: 2. 2: 4. 3: 8. 4: 16. 5: 32. 6: 64. 7: 128.
	7	0x0	R/W	Reserved	Write 0x0.
	[6:4]	0x0	R/W	SLOTA_NUM_AVG	Sample sum/average for Time Slot A. N_A: same as Bits[10:8] but for Time Slot A. See description in Register 0x15, Bits[10:8].
	[3:0]	0x0	R/W	Reserved	Write 0x0.
0x18	[15:0]	0x2000	R/W	SLOTA_CH1_OFFSET	Time Slot A Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x19	[15:0]	0x2000	R/W	SLOTA_CH2_OFFSET	Time Slot A Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1A	[15:0]	0x2000	R/W	SLOTA_CH3_OFFSET	Time Slot A Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1B	[15:0]	0x2000	R/W	SLOTA_CH4_OFFSET	Time Slot A Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1E	[15:0]	0x2000	R/W	SLOTB_CH1_OFFSET	Time Slot B Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1F	[15:0]	0x2000	R/W	SLOTB_CH2_OFFSET	Time Slot B Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x20	[15:0]	0x2000	R/W	SLOTB_CH3_OFFSET	Time Slot B Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x21	[15:0]	0x2000	R/W	SLOTB_CH4_OFFSET	Time Slot B Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.

DATA REGISTERS

Table 26. Data Registers

Address	Data Bits	Access	Name	Description
0x60	[15:0]	R	FIFO_DATA	Next available word in FIFO. Prior to reading this register, set the FIFO_ACCESS_ENA bit to 0x1 twice with two consecutive write operations to enable FIFO access (Register 0x5F, Bit 0). Reset this bit to 0 when the FIFO access sequence is complete.
0x64	[15:0]	R	SLOTA_CH1_16BIT	16-bit value of Channel1 in Time Slot A.
0x65	[15:0]	R	SLOTA_CH2_16BIT	16-bit value of Channel 2 in Time Slot A.
0x66	[15:0]	R	SLOTA_CH3_16BIT	16-bit value of Channel 3 in Time Slot A.
0x67	[15:0]	R	SLOTA_ CH4_16BIT	16-bit value of Channel 4 in Time Slot A.
0x68	[15:0]	R	SLOTB_ CH1_16BIT	16-bit value of Channel 1 in Time Slot B.
0x69	[15:0]	R	SLOTB_CH2_16BIT	16-bit value of Channel 2 in Time Slot B.
0x6A	[15:0]	R	SLOTB_CH3_16BIT	16-bit value of Channel 3 in Time Slot B.
0x6B	[15:0]	R	SLOTB_CH4_16BIT	16-bit value of Channel 4 in Time Slot B.
0x70	[15:0]	R	SLOTA_CH1_LOW	Low data-word for Channel 1 in Time Slot A.
0x71	[15:0]	R	SLOTA_CH2_LOW	Low data-word for Channel 2 in Time Slot A.
0x72	[15:0]	R	SLOTA_CH3_LOW	Low data-word for Channel 3 in Time Slot A.
0x73	[15:0]	R	SLOTA_CH4_LOW	Low data-word for Channel 4 in Time Slot A.
0x74	[15:0]	R	SLOTA_CH1_HIGH	High data-word for Channel 1 in Time Slot A.
0x75	[15:0]	R	SLOTA_CH2_HIGH	High data-word for Channel 2 in Time Slot A.
0x76	[15:0]	R	SLOTA_CH3_HIGH	High data-word for Channel 3 in Time Slot A.
0x77	[15:0]	R	SLOTA_CH4_HIGH	High data-word for Channel 4 in Time Slot A.
0x78	[15:0]	R	SLOTB_CH1_LOW	Low data-word for Channel 1 in Time Slot B.
0x79	[15:0]	R	SLOTB_CH2_LOW	Low data-word for Channel 2 in Time Slot B.
0x7A	[15:0]	R	SLOTB_CH3_LOW	Low data-word for Channel 3 in Time Slot B.
0x7B	[15:0]	R	SLOTB_CH4_LOW	Low data-word for Channel 4 in Time Slot B.
0x7C	[15:0]	R	SLOTB_CH1_HIGH	High data-word for Channel 1 in Time Slot B.
0x7D	[15:0]	R	SLOTB_CH2_HIGH	High data-word for Channel 2 in Time Slot B.
0x7E	[15:0]	R	SLOTB_CH3_HIGH	High data-word for Channel 3 in Time Slot B.
0x7F	[15:0]	R	SLOTB_CH4_HIGH	High data-word for Channel 4 in Time Slot B.

Table 27. Required Start-Up Load Sequence

Step Number	Address	Comment
1	0x4B, Bit 7	Write to 0x1 to enable the clock that drives the state machine.
2	0x10	Write 0x0001 to enter program mode.
3	Other registers	Register order is not important while the device is in program mode.
4	0x10	Write 0x0002 to start normal sampling operation.

OUTLINE DIMENSIONS

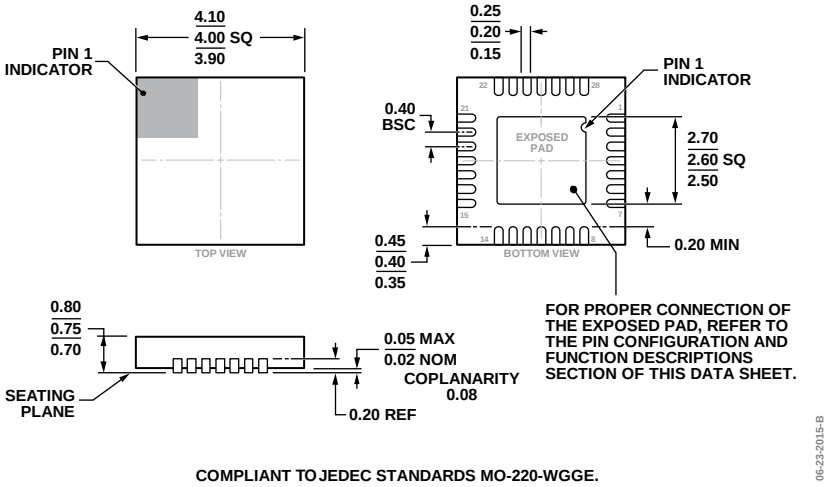

Figure 31. 28-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-28-5)
Dimensions shown in millimeters

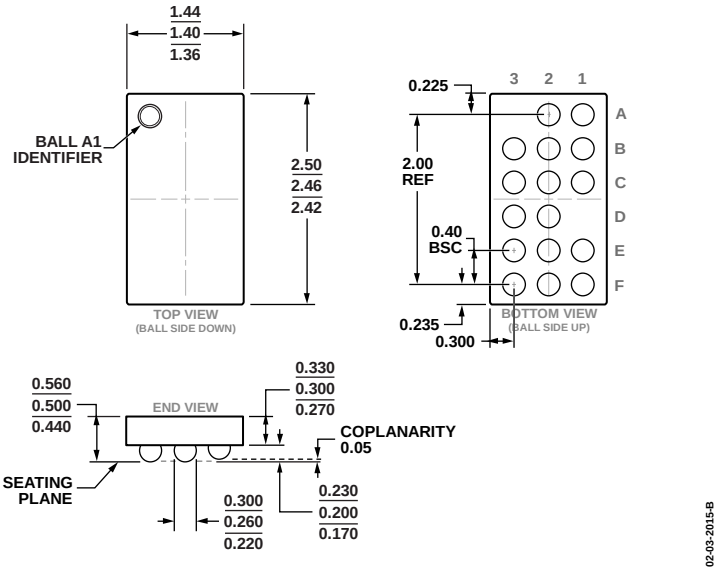

Figure 32. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-18)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPD103BCPZ	−40°C to +85°C	28-Lead LFCSP_WQ	CP-28-5
ADPD103BCPZRL	−40°C to +85°C	28-Lead LFCSP_WQ	CP-28-5
ADPD103BCBZRL7	−40°C to +85°C	16-Ball WLCSP	CB-16-18
EVAL-ADPD103Z-GEN		Generic ADPD103 Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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