Integrated Power Solution with Quad Buck Regulators and Supervisory Circuits

Data Sheet **ADP5053**

FEATURES

- Wide input voltage range: 4.5 V to 15.0 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory fuse
- Power regulation
  - Channel 1 and Channel 2: programmable 1.2 A/2.5 A/4 A sync buck regulators with low-side FET driver
  - Channel 3 and Channel 4: 1.2 A sync buck regulators
- Single 8 A output (Channel 1 and Channel 2 operated in parallel)
- Precision enable with 0.8 V accurate threshold
- Active output discharge switch
- FPWM or automatic PWM/PSM selection
- Frequency synchronization input or output
- Optional latch-off protection on OVP/OCP failure
- Power-good flag on selected channels
- UVLO, OCP, and TSD protection
- Open-drain processor reset with external adjustable threshold monitoring
- Watchdog refresh input
- Manual reset input

APPLICATIONS

- Small cell base stations
- FPGA and processor applications
- Security and surveillance
- Medical applications

TYPICAL APPLICATION CIRCUIT

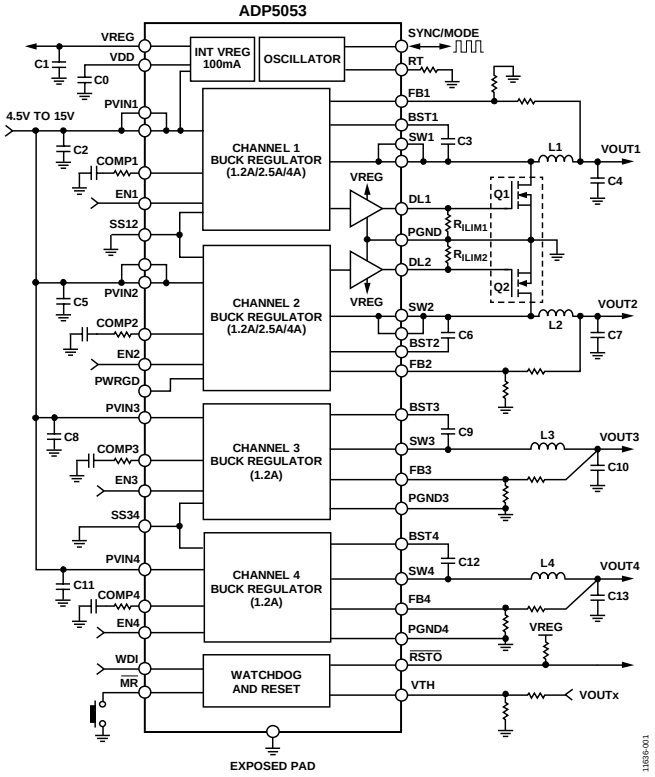


Figure 1.

GENERAL DESCRIPTION

The ADP5053 combines four high performance buck regulators, a supervisory circuit, a watchdog timer, and a manual reset in a 48-lead LFCSP package that meets demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15.0 V with no preregulators.

Channel 1 and Channel 2 integrate high-side power MOSFET and low-side MOSFET drivers. External NFETs can be used in low-side power devices to achieve an efficiency optimized solution and deliver a programmable output current of 1.2 A, 2.5 A, or 4 A. Combining Channel 1 and Channel 2 in a parallel configuration can provide a single output with up to 8 A of current.

Channel 3 and Channel 4 integrate both high-side and low-side MOSFETs to deliver an output current of 1.2 A.

The switching frequency of the ADP5053 can be programmed or synchronized to an external clock. The ADP5053 contains a precision enable pin on each channel for easy power-up sequencing or adjustable UVLO threshold.

The ADP5053 contains supervisory circuits that monitor the voltage level. The watchdog timer can generate a reset if the WDI pin is not toggled within a preset timeout period. Processor reset mode or system power on/off switch mode can be selected for manual reset functionality.

Table 1. Family Models

Model	Channels	I²C	Package
ADP5050	Four bucks, one LDO	Yes	48-Lead LFCSP
ADP5051	Four bucks, supervisory	Yes	48-Lead LFCSP
ADP5052	Four bucks, one LDO	No	48-Lead LFCSP
ADP5053	Four bucks, supervisory	No	48-Lead LFCSP
ADP5054	Four high current bucks	No	48-Lead LFCSP

Rev. C
Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2013–2017 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
Typical Application Circuit ... 1
General Description ... 1
Revision History ... 3
Detailed Functional Block Diagram ... 4
Specifications ... 5
  Buck Regulator Specifications ... 6
  Supervisory Specifications ... 8
Absolute Maximum Ratings ... 9
  Thermal Resistance ... 9
  ESD Caution ... 9
Pin Configuration and Function Descriptions ... 10
Typical Performance Characteristics ... 12
Theory of Operation ... 17
  Buck Regulator Operational Modes ... 17
  Adjustable and Fixed Output Voltages ... 17
  Internal Regulators (VREG and VDD) ... 17
  Separate Supply Applications ... 18
  Low-Side Device Selection ... 18
  Bootstrap Circuitry ... 18
  Active Output Discharge Switch ... 18
  Precision Enabling ... 18
  Oscillator ... 18
  Synchronization Input/Output ... 19
  Soft Start ... 19
  Parallel Operation ... 20
  Startup with Precharged Output ... 20
  Current-Limit Protection ... 20
  Frequency Foldback ... 21
  Hiccup Protection ... 21
  Latch-Off Protection ... 21
  Undervoltage Lockout (UVLO) ... 22
  Power-Good Function ... 22
  Thermal Shutdown ... 22
  Supervisory Circuit ... 22
Applications Information ... 24
  ADIsimPower Design Tool ... 24
  Programming the Adjustable Output Voltage ... 24
  Voltage Conversion Limitations ... 24
  Current-Limit Setting ... 24
  Soft Start Setting ... 25
  Inductor Selection ... 25
  Output Capacitor Selection ... 25
  Input Capacitor Selection ... 26
  Low-Side Power Device Selection ... 26
  Programming the UVLO Input ... 26
  Compensation Components Design ... 27
  Power Dissipation ... 27
  Junction Temperature ... 28
Design Example ... 29
  Setting the Switching Frequency ... 29
  Setting the Output Voltage ... 29
  Setting the Current Limit ... 29
  Selecting the Inductor ... 29
  Selecting the Output Capacitor ... 30
  Selecting the Low-Side MOSFET ... 30
  Designing the Compensation Network ... 30
  Selecting the Soft Start Time ... 30
  Selecting the Input Capacitor ... 30
  Recommended External Components ... 31
Circuit Board Layout Recommendations ... 32
Typical Application Circuits ... 33
Factory Default Options ... 36
Outline Dimensions ... 37
  Ordering Guide ... 37

REVISION HISTORY

7/2017—Rev. B to Rev. C

Changes to Factory Default Options Section 36
Updated Outline Dimensions 37
Changes to Ordering Guide 37

10/2016—Rev. A to Rev. B

Deleted Factory Programmable Options Section and Table 16 to Table 30; Renumbered Sequentially 33
Updated Outline Dimensions 34

9/2015—Rev. 0 to Rev. A

Changes to Table 1 1

11/2013—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

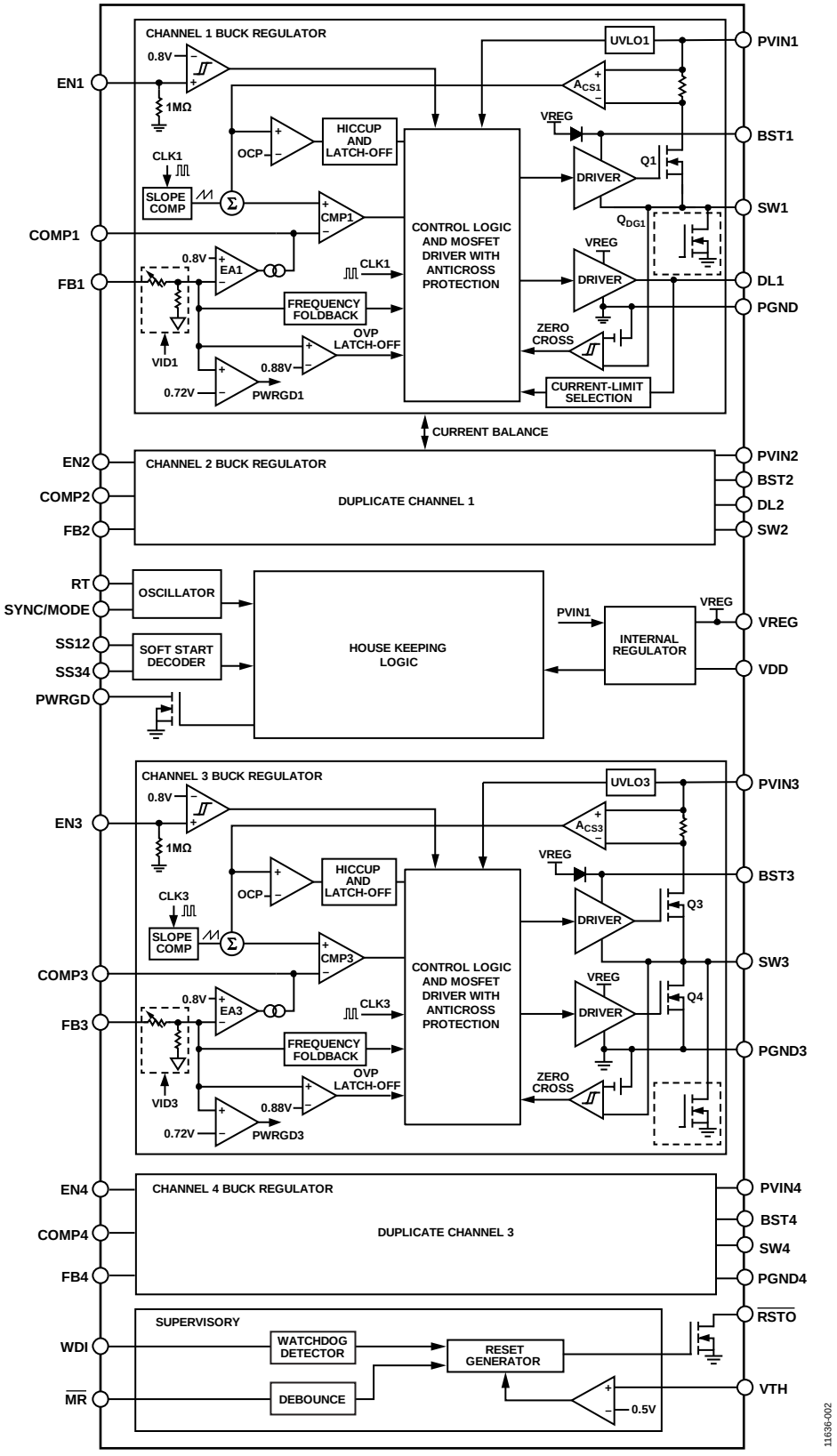


Figure 2.

SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	4.5		15.0	V	PVIN1, PVIN2, PVIN3, PVIN4 pins
QUIESCENT CURRENT						PVIN1, PVIN2, PVIN3, PVIN4 pins
Operating Quiescent Current	I_Q		4.8	6.35	mA	No switching, all ENx pins high
	I_{SHDN}		25	65	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT	UVLO					PVIN1, PVIN2, PVIN3, PVIN4 pins
Threshold						
Rising	$V_{UVLO-RISING}$		4.2	4.36	V	
Falling	$V_{UVLO-FALLING}$	3.6	3.78		V	
Hysteresis	V_{HYS}		0.42		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	700	740	780	kHz	RT = 25.5 kΩ
Range		250		1400	kHz	
SYNC Input						
Input Clock Range	f_{SYNC}	250		1400	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC_MIN_ON}$	100			ns	
Minimum Off Time	$t_{SYNC_MIN_OFF}$	100			ns	
Input Clock High Voltage	$V_{H\ (SYNC)}$	1.3			V	
Input Clock Low Voltage	$V_{L\ (SYNC)}$			0.4	V	
SYNC Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK_PULSE_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK_RISE_FALL}$		10		ns	
High Level Voltage	$V_{H\ (SYNC_OUT)}$		V_{VREG}		V	
PRECISION ENABLING						EN1, EN2, EN3, EN4 pins
High Level Threshold	$V_{TH_H\ (EN)}$		0.806	0.832	V	
Low Level Threshold	$V_{TH_L\ (EN)}$	0.688	0.725		V	
Pull-Down Resistor	$R_{PULL-DOWN\ (EN)}$		1.0		MΩ	
POWER GOOD						
Internal Power-Good						
Rising Threshold	$V_{PWRGD\ (RISE)}$	86.3	90.5	95	%	
Hysteresis	$V_{PWRGD\ (HYS)}$		3.3		%	
Falling Delay	t_{PWRGD_FALL}		50		µs	
Rising Delay for PWRGD Pin	$t_{PWRGD_PIN_RISE}$		1		ms	
Leakage Current for PWRGD Pin	$I_{PWRGD_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		50	100	mV	I_{PWRGD} = 1 mA
INTERNAL REGULATORS						
VDD						
Output Voltage	V_{VDD}	3.2	3.305	3.4	V	I_{VDD} = 10 mA
Current Limit	I_{LIM_VDD}	20	51	80	mA	
VREG						
Output Voltage	V_{VREG}	4.9	5.1	5.3	V	
Dropout Voltage	$V_{DROPOUT}$		225		mV	I_{VREG} = 50 mA
Current Limit	I_{LIM_VREG}	50	95	140	mA	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		150		°C	
Hysteresis	T_{HYS}		15		°C	

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
FB1 Pin						
Fixed Output Options	V_{OUT1}	0.85		1.60	V	Fuse trim
Adjustable Feedback Voltage	V_{FB1}		0.800		V	
Feedback Voltage Accuracy	$V_{FB1\ (DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage
SW1 Pin						
High-Side Power FET On Resistance	$R_{DSON\ (1H)}$		100		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH\ (ILIM1)}$	3.50	4.4	5.28	A	R_{ILIM1} = floating
		1.91	2.63	3.08	A	R_{ILIM1} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM1} = 22 kΩ
Minimum On Time	t_{MIN_ON1}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF1}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL1 Pin						
Rising Time	$t_{RISING1}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING1}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING1}$		10		Ω	
Sinking Resistor	$t_{SINKING1}$		0.95		Ω	
Error Amplifier (EA), COMP1 Pin						
EA Transconductance	g_{m1}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS1}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP1}$		7 × t_{SS1}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		250		Ω	
CHANNEL 2 SYNC BUCK REGULATOR						
FB2 Pin						
Fixed Output Options	V_{OUT2}	3.3		5.0	V	Fuse trim
Adjustable Feedback Voltage	V_{FB2}		0.800		V	
Feedback Voltage Accuracy	$V_{FB2\ (DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	Adjustable voltage
SW2 Pin						
High-Side Power FET On Resistance	$R_{DSON\ (2H)}$		110		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH\ (ILIM2)}$	3.50	4.4	5.28	A	R_{ILIM2} = floating
		1.91	2.63	3.08	A	R_{ILIM2} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM2} = 22 kΩ
Minimum On Time	t_{MIN_ON2}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF2}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL2 Pin						
Rising Time	$t_{RISING2}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING2}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING2}$		10		Ω	
Sinking Resistor	$t_{SINKING2}$		0.95		Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Error Amplifier (EA), COMP2 Pin						
EA Transconductance	g_{m2}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS2}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP2}$		$7 \times t_{SS2}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		250		Ω	
CHANNEL 3 SYNC BUCK REGULATOR						
FB3 Pin						
Fixed Output Options	V_{OUT3}	1.20		1.80	V	Fuse trim
Adjustable Feedback Voltage	V_{FB3}		0.800		V	
Feedback Voltage Accuracy	$V_{FB3\ (DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DSON\ (3H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON\ (3L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH\ (ILIM3)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON3}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF3}		$1/9 \times t_{SW}$		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP3 Pin						
EA Transconductance	g_{m3}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS3}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP3}$		$7 \times t_{SS3}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		250		Ω	
CHANNEL 4 SYNC BUCK REGULATOR						
FB4 Pin						
Fixed Output Options	V_{OUT4}	2.5		5.5	V	Fuse trim
Adjustable Feedback Voltage	V_{FB4}		0.800		V	
Feedback Voltage Accuracy	$V_{FB4\ (DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB4}			0.1	µA	Adjustable voltage
SW4 Pin						
High-Side Power FET On Resistance	$R_{DSON\ (4H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON\ (4L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH\ (ILIM4)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON4}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF4}		$1/9 \times t_{SW}$		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP4 Pin						
EA Transconductance	g_{m4}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS4}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP4}$		$7 \times t_{SS4}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		250		Ω	

SUPERVISORY SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLD VOLTAGE	V_{TH}	0.494	0.500	0.505	V	
RESET TIMEOUT PERIOD	t_{RP}					
Option 0		1.05	1.4	1.97	ms	
Option 1		21	28	38	ms	
Option 2		160	200	260	ms	
Option 3		1.15	1.6	2.17	sec	
V_{CC} TO RESET DELAY	t_{RD}		80		µs	VTH falling at 1 mV/µs
WATCHDOG INPUT						
Watchdog Timeout Period	t_{WD}					
Option 0		4.8	6.3	8	ms	
Option 1		79	102	135	ms	
Option 2		1.14	1.6	2.15	sec	
Option 3			25.6		sec	
WDI Pulse Width		80			ns	
WDI Input Threshold		0.4		1.2	V	
WDI Input Current (Source)		8.5	14	18.5	µA	$V_{WDI} = V_{CC}$, time average
WDI Input Current (Sink)		−15	−22	−30	µA	V_{WDI} = 0 V, time average
MANUAL RESET INPUT						
$\overline{MR}$ Input Pulse Width		1			µs	
$\overline{MR}$ Glitch Rejection			280		ns	
$\overline{MR}$ Pull-Up Resistance		32	55	80	kΩ	
$\overline{MR}$ to Reset Delay			310		ns	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
PVIN1 to PGND	−0.3 V to +18 V
PVIN2 to PGND	−0.3 V to +18 V
PVIN3 to PGND3	−0.3 V to +18 V
PVIN4 to PGND4	−0.3 V to +18 V
SW1 to PGND	−0.3 V to +18 V
SW2 to PGND	−0.3 V to +18 V
SW3 to PGND3	−0.3 V to +18 V
SW4 to PGND4	−0.3 V to +18 V
PGND to GND	−0.3 V to +0.3 V
PGND3 to GND	−0.3 V to +0.3 V
PGND4 to GND	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
BST4 to SW4	−0.3 V to +6.5 V
DL1 to PGND	−0.3 V to +6.5 V
DL2 to PGND	−0.3 V to +6.5 V
SS12, SS34 to GND	−0.3 V to +6.5 V
EN1, EN2, EN3, EN4 to GND	−0.3 V to +6.5 V
VREG to GND	−0.3 V to +6.5 V
SYNC/MODE to GND	−0.3 V to +6.5 V
WDI, $\overline{\text{RSTO}}$, VTH to GND	−0.3 V to +6.5 V
$\overline{\text{MR}}$ to GND	−0.3 V to +3.6 V
RT to GND	−0.3 V to +3.6 V
PWRGD to GND	−0.3 V to +6.5 V
FB1, FB2, FB3, FB4 to GND[1]	−0.3 V to +3.6 V
FB2 to GND[2]	−0.3 V to +6.5 V
FB4 to GND[2]	−0.3 V to +7 V
COMP1, COMP2, COMP3, COMP4 to GND	−0.3 V to +3.6 V
VDD to GND	−0.3 V to +3.6 V
Storage Temperate Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C

[1] This rating applies to the adjustable output voltage models of the ADP5053.
[2] This rating applies to the fixed output voltage models of the ADP5053.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LFCSP	27.87	2.99	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

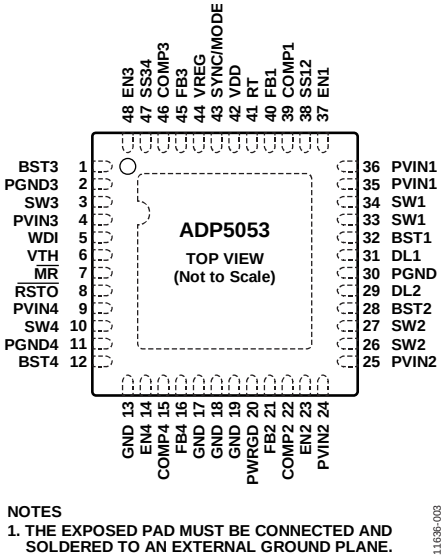


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST3	High-Side FET Driver Power Supply for Channel 3.
2	PGND3	Power Ground for Channel 3.
3	SW3	Switching Node Output for Channel 3.
4	PVIN3	Power Input for Channel 3. Connect a bypass capacitor between this pin and ground.
5	WDI	Watchdog Refresh Input from Processor.
6	VTH	Monitoring Voltage Threshold Programming.
7	$\overline{MR}$	Manual Reset Input, Active Low.
8	$\overline{RSTO}$	Open-Drain Reset Output, Active Low.
9	PVIN4	Power Input for Channel 4. Connect a bypass capacitor between this pin and ground.
10	SW4	Switching Node Output for Channel 4.
11	PGND4	Power Ground for Channel 4.
12	BST4	High-Side FET Driver Power Supply for Channel 4.
13	GND	This pin is for internal test purposes. Connect this pin to ground.
14	EN4	Enable Input for Channel 4. Use an external resistor divider to set the turn-on threshold.
15	COMP4	Error Amplifier Output for Channel 4. Connect an RC network from this pin to ground.
16	FB4	Feedback Sensing Input for Channel 4.
17, 18, 19	GND	These pins are for internal test purposes. Connect these pins to ground.
20	PWRGD	Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels.
21	FB2	Feedback Sensing Input for Channel 2.
22	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground.
23	EN2	Enable Input for Channel 2. Use an external resistor divider to set the turn-on threshold.
24, 25	PVIN2	Power Input for Channel 2. Connect a bypass capacitor between this pin and ground.
26, 27	SW2	Switching Node Output for Channel 2.
28	BST2	High-Side FET Driver Power Supply for Channel 2.
29	DL2	Low-Side FET Gate Driver for Channel 2. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 2.
30	PGND	Power Ground for Channel 1 and Channel 2.
31	DL1	Low-Side FET Gate Driver for Channel 1. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 1.

Pin No.	Mnemonic	Description
32	BST1	High-Side FET Driver Power Supply for Channel 1.
33, 34	SW1	Switching Node Output for Channel 1.
35, 36	PVIN1	Power Input for the Internal 5.1 V VREG Linear Regulator and the Channel 1 Buck Regulator. Connect a bypass capacitor between this pin and ground.
37	EN1	Enable Input for Channel 1. An external resistor divider can be used to set the turn-on threshold.
38	SS12	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 1 and Channel 2 (see the Soft Start section). This pin is also used to configure parallel operation of Channel 1 and Channel 2 (see the Parallel Operation section).
39	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from this pin to ground.
40	FB1	Feedback Sensing Input for Channel 1.
41	RT	Frequency Setting. Connect a resistor from RT to ground to program the switching frequency from 250 kHz to 1.4 MHz. For more information, see the Oscillator section.
42	VDD	Output of the Internal 3.3 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
43	SYNC/MODE	Synchronization Input/Output (SYNC). To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 250 kHz to 1.4 MHz. The SYNC function of this pin can also be configured as a synchronization output by factory fuse. Forced PWM or Automatic PWM/PSM Selection Pin (MODE). When this pin is logic high, the device operates in forced PWM (FPWM) mode. When this pin is logic low, the device operates in automatic PWM/PSM mode.
44	VREG	Output of the Internal 5.1 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
45	FB3	Feedback Sensing Input for Channel 3.
46	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from this pin to ground.
47	SS34	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 3 and Channel 4 (see the Soft Start section).
48	EN3	Enable Input for Channel 3. Use an external resistor divider to set the turn-on threshold.
0	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected and soldered to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

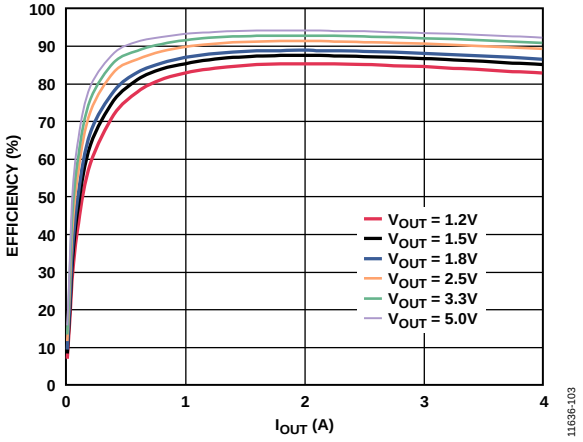


Figure 4. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

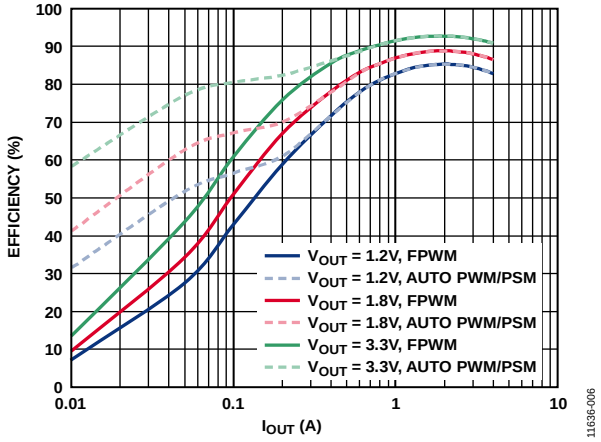


Figure 7. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

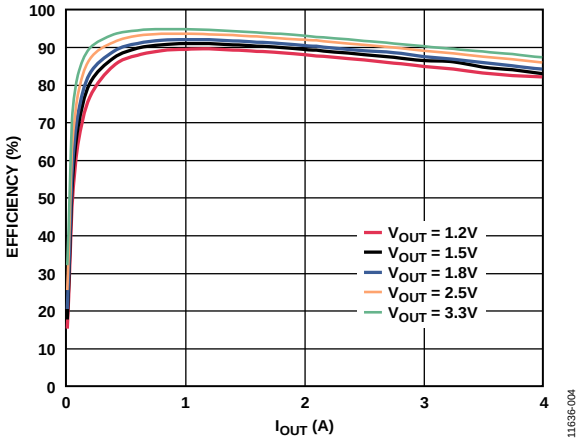


Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

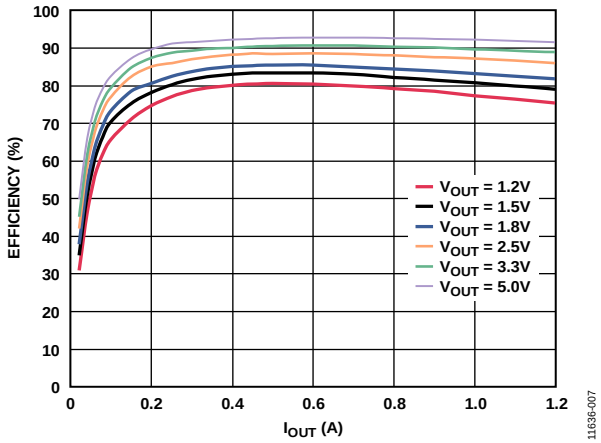


Figure 8. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

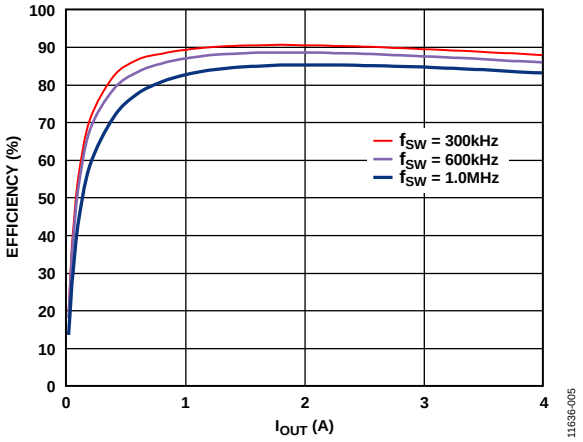


Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

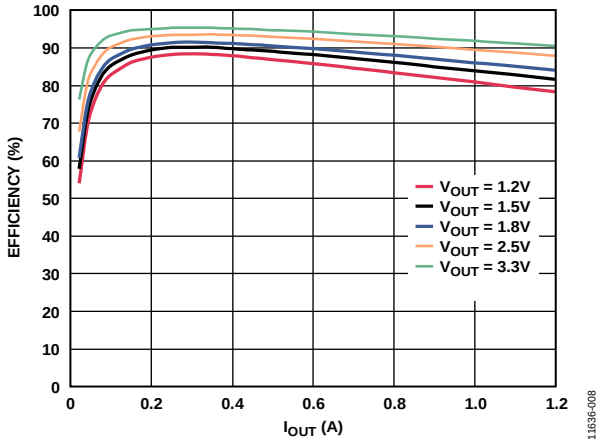


Figure 9. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

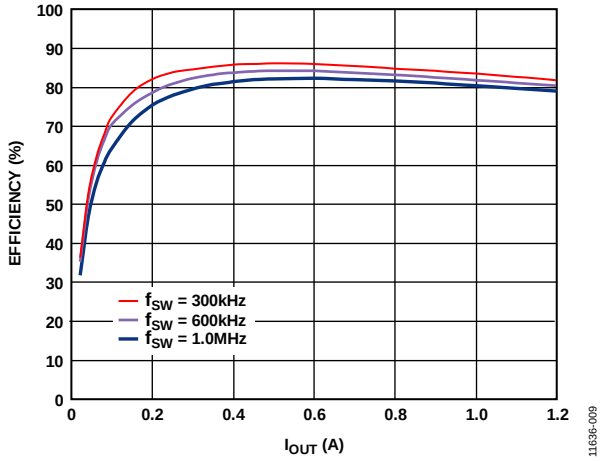


Figure 10. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

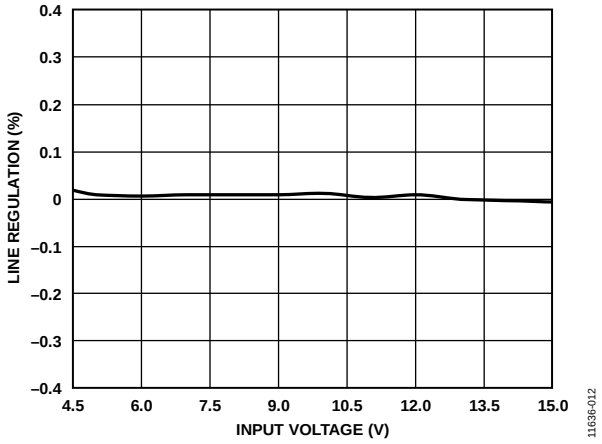


Figure 13. Channel 1 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, FPWM Mode

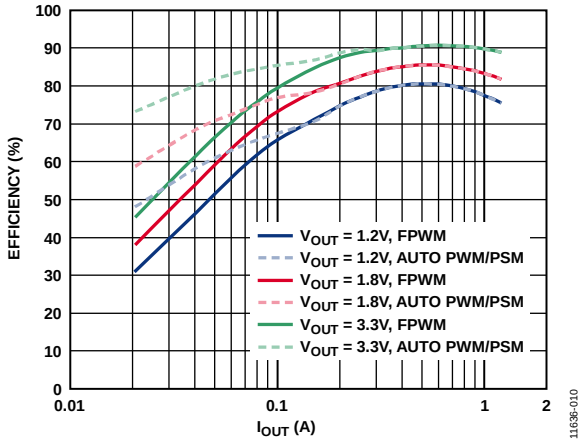


Figure 11. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

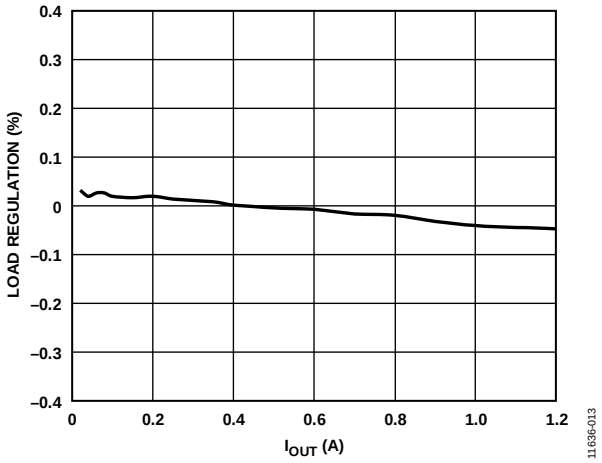


Figure 14. Channel 3 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

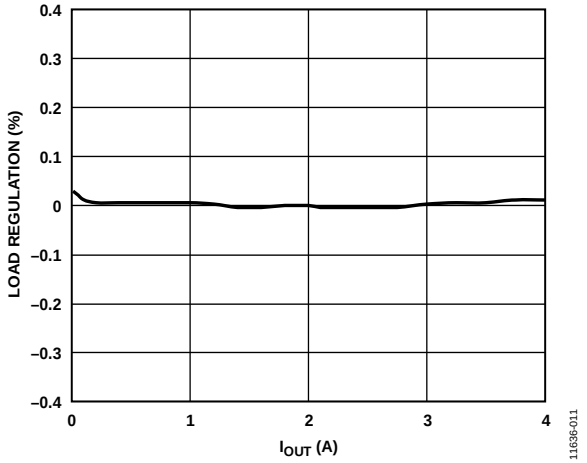


Figure 12. Channel 1 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

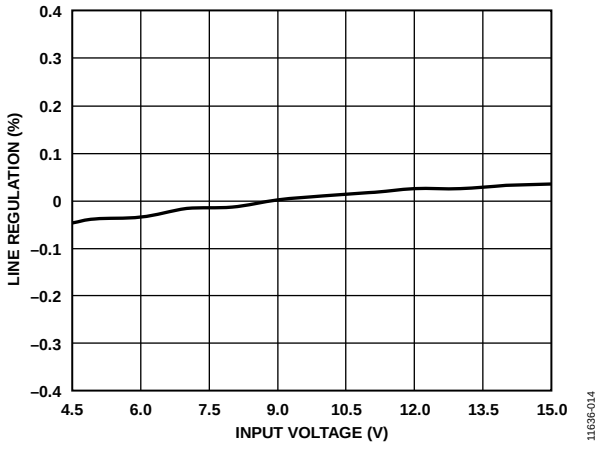


Figure 15. Channel 3 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 600 kHz, FPWM Mode

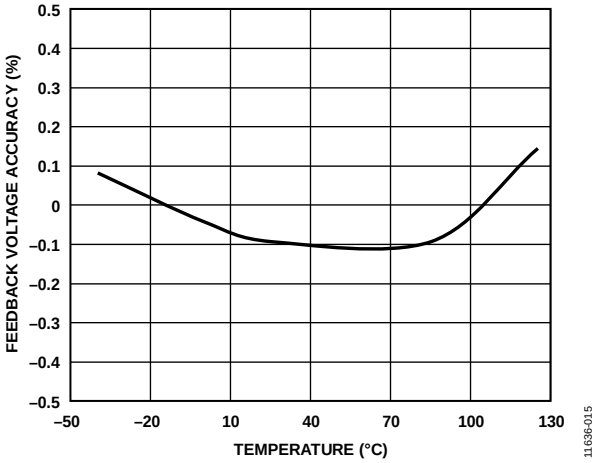


Figure 16. 0.8 V Feedback Voltage Accuracy vs. Temperature for Channel 1, Adjustable Output Model

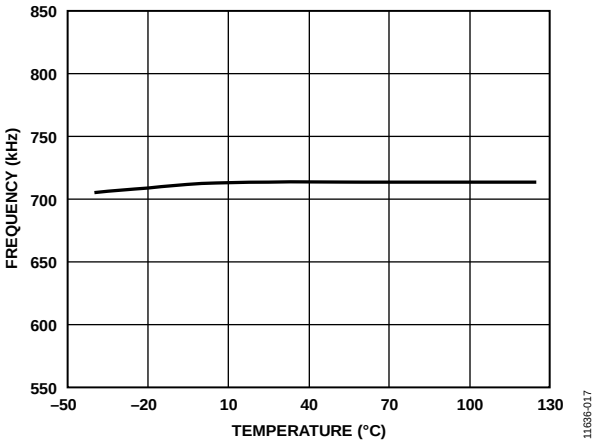


Figure 17. Frequency vs. Temperature, V_{IN} = 12 V

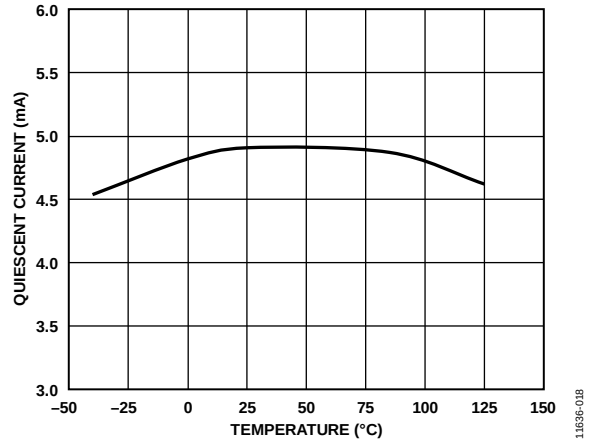


Figure 18. Quiescent Current vs. Temperature (Includes PVIN1, PVIN2, PVIN3, and PVIN4)

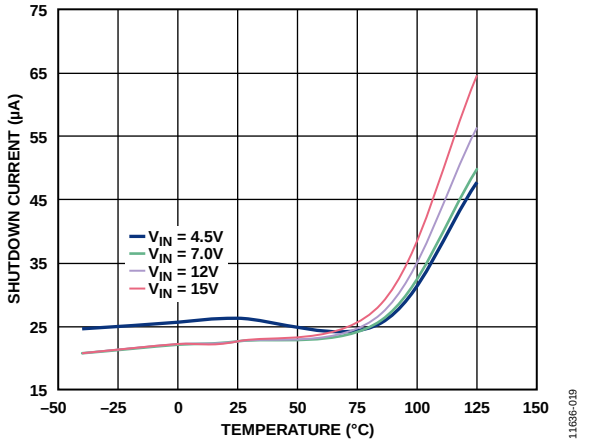


Figure 19. Shutdown Current vs. Temperature (EN1, EN2, EN3, and EN4 Low)

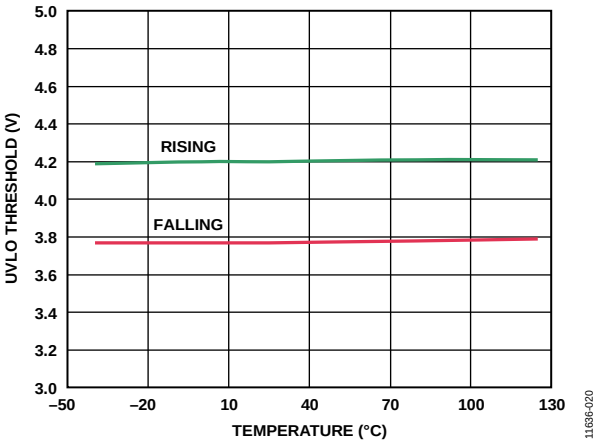


Figure 20. UVLO Threshold vs. Temperature

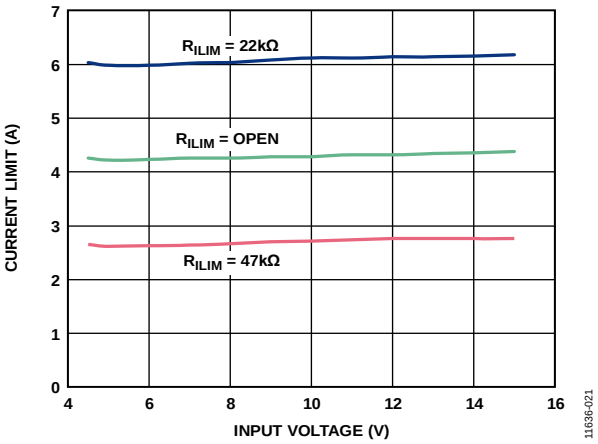


Figure 21. Channel 1/Channel 2 Current Limit vs. Input Voltage

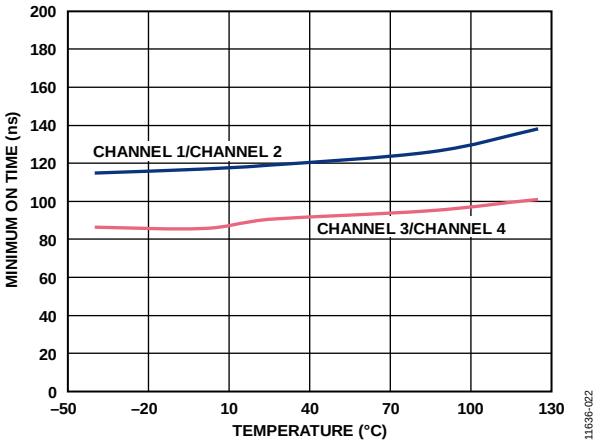


Figure 22. Minimum On Time vs. Temperature

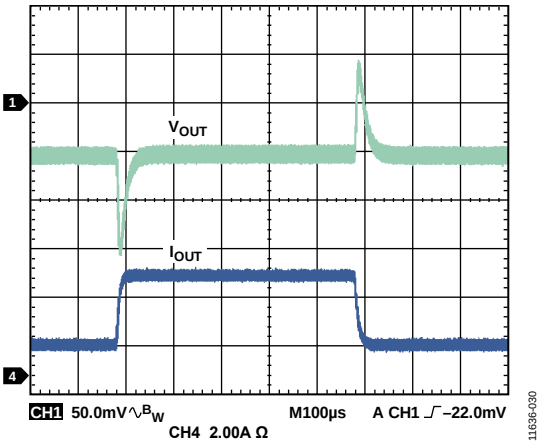


Figure 25. Channel 1/Channel 2 Load Transient, 1 A to 4 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 2.2 µH, C_{OUT} = 47 µF × 2

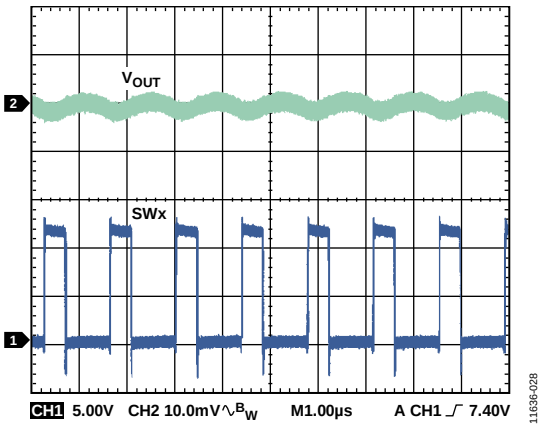


Figure 23. Steady State Waveform at Heavy Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, FPWM Mode

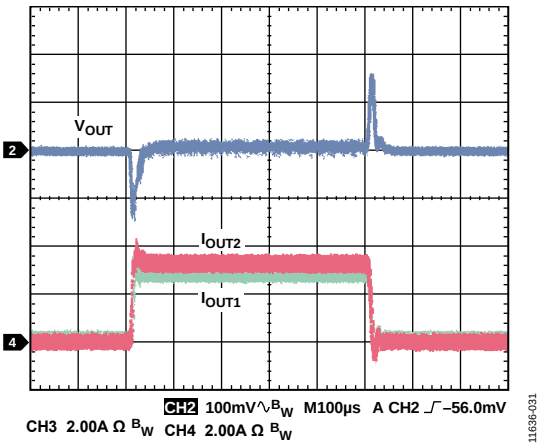


Figure 26. Load Transient, Channel 1/Channel 2 Parallel Output, 0 A to 6 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 4

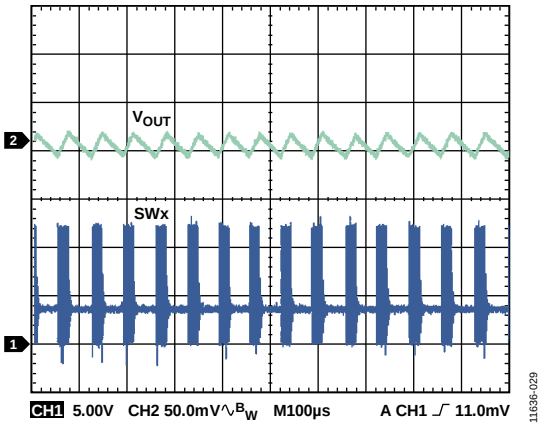


Figure 24. Steady State Waveform at Light Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 30 mA, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, Automatic PWM/PSM Mode

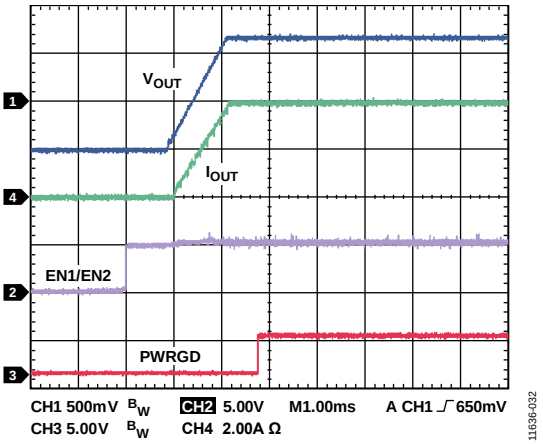


Figure 27. Channel 1/Channel 2 Soft Start with 4 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

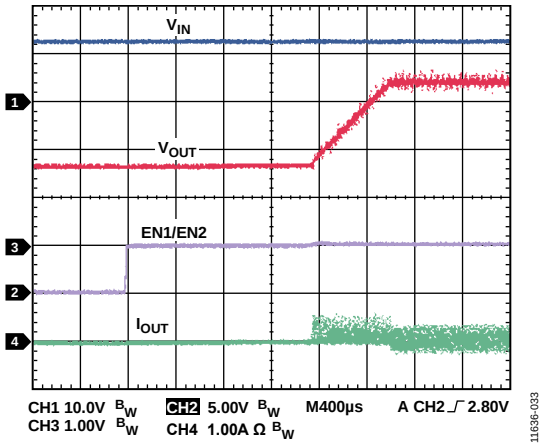


Figure 28. Startup with Precharged Output, V_{IN} = 12 V, V_{OUT} = 3.3 V

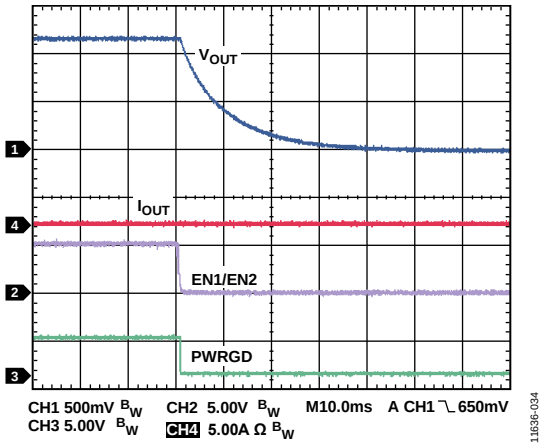


Figure 29. Channel 1/Channel 2 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

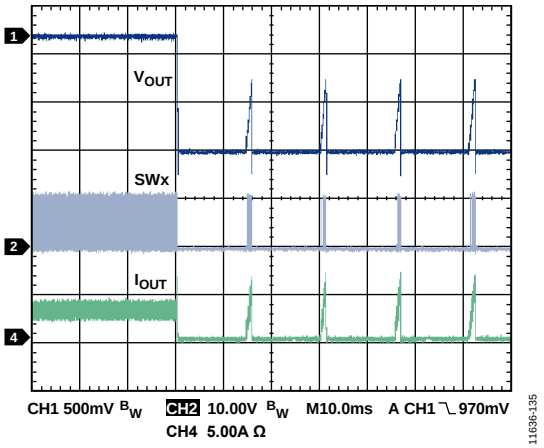


Figure 30. Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

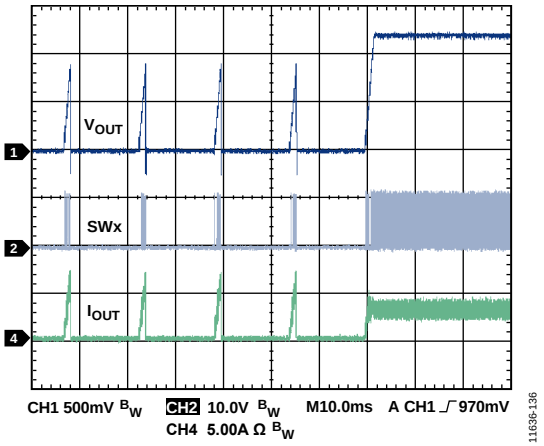


Figure 31. Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

THEORY OF OPERATION

The ADP5053 is a micropower management unit that combines four high performance buck regulators in a 48-lead LFCSP package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15.0 V with no preregulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

Pulse-Width Modulation (PWM) Mode

In PWM mode, the buck regulators in the ADP5053 operate at a fixed frequency; this frequency is set by an internal oscillator that is programmed by the RT pin. At the start of each oscillator cycle, the high-side MOSFET turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak inductor current threshold that turns off the high-side MOSFET; this threshold is set by the error amplifier output.

During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle. The buck regulators in the ADP5053 regulate the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

To achieve higher efficiency, the buck regulators in the ADP5053 smoothly transition to variable frequency PSM operation when the output load falls below the PSM current threshold. When the output voltage falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET turns off, and the output capacitor supplies all the output current.

The PSM comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM operation is larger than the ripple in the forced PWM mode of operation under light load conditions.

Forced PWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in PWM mode using the SYNC/MODE pin. In forced PWM (FPWM) mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In PWM mode, efficiency is lower when compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5053 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation; in PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the output current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

When the SYNC/MODE pin is connected to VREG, the device operates in forced PWM (FPWM) mode. When the SYNC/MODE pin is connected to ground, the device operates in automatic PWM/PSM mode.

ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The ADP5053 provides adjustable and fixed output voltage settings via factory fuse. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage (0.8 V for Channel 1 to Channel 4).

For the fixed output settings, the feedback resistor divider is built into the ADP5053, and the feedback pin (FBx) must be tied directly to the output. Table 8 lists the available fixed output voltage ranges for each buck regulator channel.

Table 8. Fixed Output Voltage Ranges

Channel	Fixed Output Voltage Range
Channel 1	0.85 V to 1.6 V in 25 mV steps
Channel 2	3.3 V to 5.0 V in 300 mV or 200 mV steps
Channel 3	1.2 V to 1.8 V in 100 mV steps
Channel 4	2.5 V to 5.5 V in 100 mV steps

The output range can also be programmed by factory fuse. If a different output voltage range is required, contact your local Analog Devices, Inc., sales or distribution representative.

INTERNAL REGULATORS (VREG AND VDD)

The internal VREG regulator in the ADP5053 provides a stable 5.1 V power supply for the bias voltage of the MOSFET drivers. The internal VDD regulator in the ADP5053 provides a stable 3.3 V power supply for internal control circuits. Connect a 1.0 µF ceramic capacitor between VREG and ground; connect another 1.0 µF ceramic capacitor between VDD and ground. The internal VREG and VDD regulators are active as long as PVIN1 is available.

The internal VREG regulator can provide a total load of 95 mA including the MOSFET driving current, and it can be used as an always alive 5.1 V power supply for a small system current demand. The current-limit circuit is included in the VREG regulator to protect the circuit when the device is heavily loaded.

The VDD regulator is strictly for internal circuit use and is not recommended for other purposes.

SEPARATE SUPPLY APPLICATIONS

The ADP5053 supports separate input voltages for the four buck regulators. This means that the input voltages for the four buck regulators can be connected to different supply voltages.

The PVIN1 voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans to use separate supply voltages for the buck regulators, the PVIN1 voltage must be above the UVLO threshold before the other channels begin to operate.

To ensure that PVIN1 is high enough to support the outputs in regulation, use precision enabling to monitor the PVIN1 voltage and to delay the startup of the outputs. For more information, see the Precision Enabling section.

The ADP5053 supports cascading supply operation for the four buck regulators. As shown in Figure 32, PVIN2, PVIN3, and PVIN4 are powered from the Channel 1 output (V_{OUT1}). In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2, PVIN3, and PVIN4.

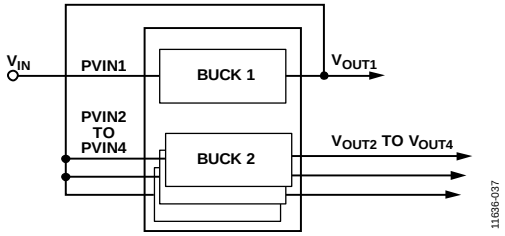


Figure 32. Cascading Supply Application

LOW-SIDE DEVICE SELECTION

The buck regulators in Channel 1 and Channel 2 integrate 4 A high-side power MOSFET and low-side MOSFET drivers. The N-channel MOSFETs selected for use with the ADP5053 must be compatible with the synchronized buck regulators. In general, a low R_{DSON} N-channel MOSFET achieves higher efficiency; dual MOSFETs in one package (for both Channel 1 and Channel 2) are recommended to save space on the printed circuit board (PCB). For more information, see the Low-Side Power Device Selection section.

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5053 has an integrated bootstrap regulator. The bootstrap regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5053 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 250 Ω for Channel 1 to Channel 4.

Enable or disable the discharge switch function for all four buck regulators by factory fuse.

PRECISION ENABLING

The ADP5053 has an enable control pin for each regulator. The enable control pin (ENx) features a precision enable circuit with a 0.8 V reference voltage. A voltage greater than 0.8 V at the ENx pin enables the regulator. A voltage less than 0.725 V at the ENx pin disables the regulator. An internal 1 MΩ pull-down resistor prevents errors when the ENx pin is left floating.

The precision enable threshold voltage allows easy sequencing of channels within the device, as well as sequencing between the ADP5053 and other input/output supplies. The ENx pin can also be used as a programmable UVLO input using a resistor divider (see Figure 33). For more information, see the Programming the UVLO Input section.

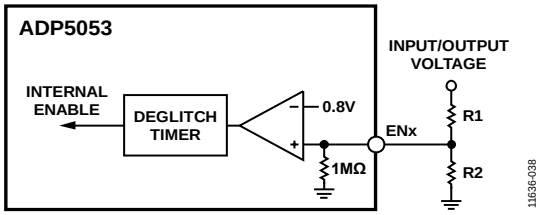


Figure 33. Precision Enable Diagram for One Channel

OSCILLATOR

The switching frequency (f_{SW}) of the ADP5053 can be set to a value from 250 kHz to 1.4 MHz by connecting a resistor from the RT pin to ground. Calculate the value of the RT resistor as follows:

$$R_{RT}\,(\text{k}\Omega) = [14{,}822/f_{SW}\,(\text{kHz})]^{1.081}$$

Figure 34 shows the typical relationship between the switching frequency (f_{SW}) and the RT resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and solution size.

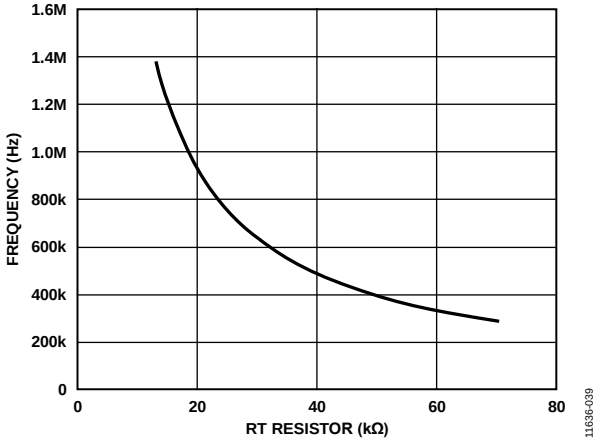


Figure 34. Switching Frequency vs. RT Resistor

For Channel 1 and Channel 3, the frequency can be set to half the master switching frequency set by the RT pin. This setting can be selected by factory fuse. If the master switching frequency is less than 250 kHz, this halving of the frequency for Channel 1 or Channel 3 is not recommended.

Phase Shift

The phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180°. Therefore, Channel 3 is in phase with Channel 1, and Channel 4 is in phase with Channel 2 (see Figure 35). This phase shift maximizes the benefits of out-of-phase operation by reducing the input ripple current and lowering the ground noise.

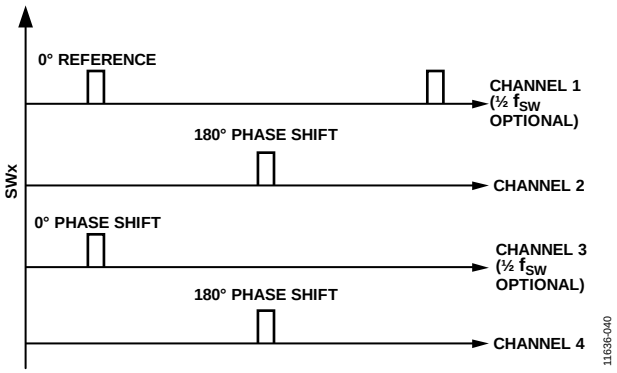


Figure 35. Phase Shift Diagram, Four Buck Regulators

SYNCHRONIZATION INPUT/OUTPUT

The switching frequency of the ADP5053 can be synchronized to an external clock with a frequency range from 250 kHz to 1.4 MHz. The ADP5053 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for effective synchronization; the suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output by factory fuse. Regardless of the synchronization configuration method, the SYNC/MODE pin generates a positive clock pulse with a 50% duty cycle and a frequency equal to the internal switching frequency set by the RT pin. There is a short delay time (approximately 15% of t_{SW}) from the generated synchronization clock to the Channel 1 switching node.

Figure 36 shows two ADP5053 devices configured for frequency synchronization mode: one ADP5053 device is configured as the clock output to synchronize another ADP5053 device. It is recommended that a 100 kΩ pull-up resistor be used to prevent logic errors when the SYNC/MODE pin remains floating.

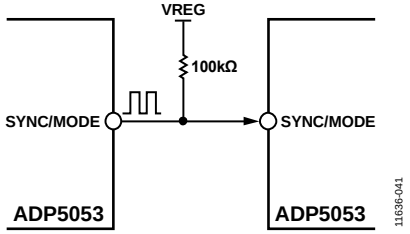


Figure 36. Two ADP5053 Devices Configured for Synchronization Mode

In the configuration shown in Figure 36, the phase shift between Channel 1 of the first ADP5053 device and Channel 1 of the second ADP5053 device is 0° (see Figure 37).

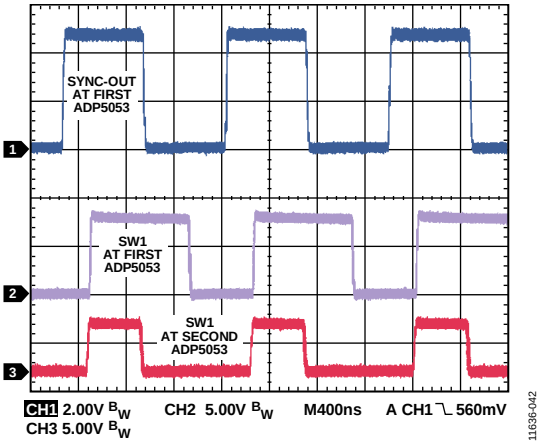


Figure 37. Waveforms of Two ADP5053 Devices Operating in Synchronization Mode

SOFT START

The buck regulators in the ADP5053 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 2 ms for each buck regulator when the SS12 and SS34 pins are tied to VREG.

To set the soft start time to a value of 2 ms, 4 ms, or 8 ms, connect a resistor divider from the SS12 or SS34 pin to the VREG pin and ground (see Figure 38). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor.

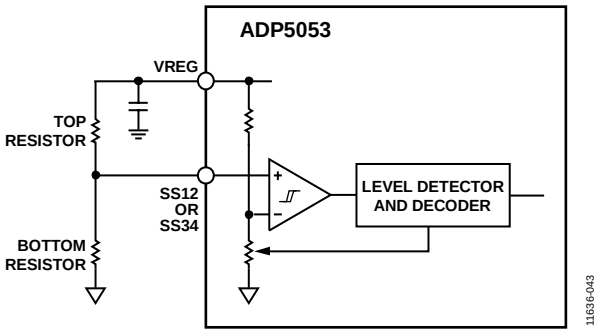


Figure 38. Level Detector Circuit for Soft Start

Use the SS12 pin to program the soft start time and parallel operation for Channel 1 and Channel 2. Use the SS34 pin to program the soft start time for Channel 3 and Channel 4.

Table 9 provides the required resister values to set the soft start time.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

		Soft Start Time			
R_{TOP} (kΩ)	R_{BOT} (kΩ)	Channel 1	Channel 2	Channel 3	Channel 4
0	N/A[1]	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A[1]	0	8 ms	8 ms	8 ms	8 ms

[1] N/A = not applicable.

PARALLEL OPERATION

The ADP5053 supports two-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 8 A of current. Take the following actions to configure Channel 1 and Channel 2 as a two-phase single output in parallel operation (see Figure 39):

- Use the SS12 pin to select parallel operation as specified in Table 9.
- Leave the COMP2 pin open.
- Use the FB1 pin to set the output voltage.
- Connect the FB2 pin to ground (FB2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

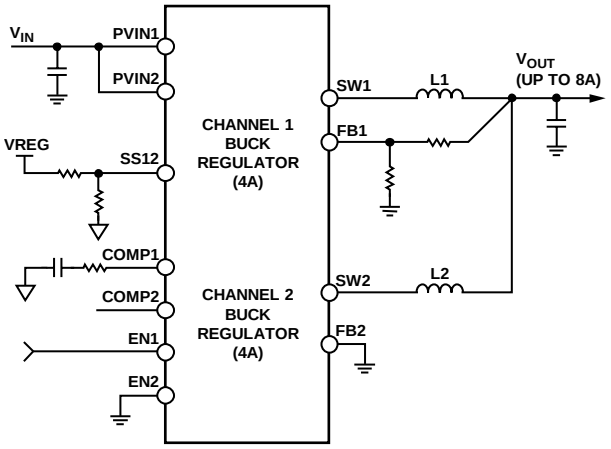


Figure 39. Parallel Operation for Channel 1 and Channel 2

When operating Channel 1 and Channel 2 in the parallel configuration, configure the channels as follows:

- Set the input voltages and current-limit settings for Channel 1 and Channel 2 to the same values.
- Operate both channels in forced PWM mode.

Current balance in parallel configuration is well regulated by the internal control loop. Figure 40 shows the typical current balance matching in the parallel output configuration.

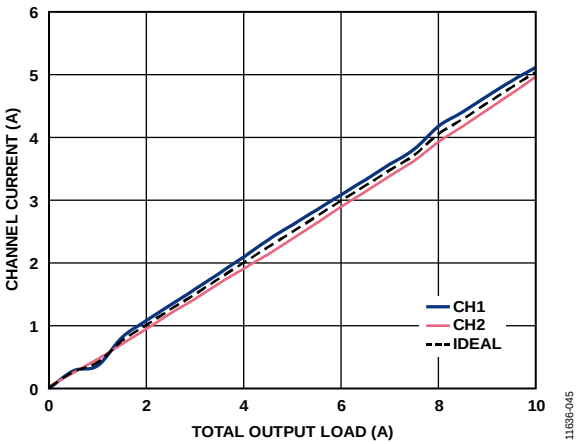


Figure 40. Current Balance in Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5053 include a precharged start-up feature to protect the low-side MOSFETS from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents the reverse inductor current, which discharges the output capacitor, until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

CURRENT-LIMIT PROTECTION

The buck regulators in the ADP5053 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows for the use of small size inductors for low current applications.

To configure the current-limit threshold for Channel 1, connect a resistor from the DL1 pin to ground. To configure the current-limit threshold for Channel 2, connect another resistor from the DL2 pin to ground. Table 10 lists the peak current-limit threshold settings for Channel 1 and Channel 2.

Table 10. Peak Current-Limit Threshold Settings for Channel 1 and Channel 2

R_{ILIM1} or R_{ILIM2}	Typical Peak Current-Limit Threshold (A)
Floating	4.4
47 kΩ	2.63
22 kΩ	6.44

The buck regulators in the ADP5053 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET.

FREQUENCY FOLDBACK

The buck regulators in the ADP5053 include frequency foldback to prevent output current runaway when a hard short occurs on the output. Implement frequency foldback as follows:

- If the voltage at the FBx pin falls below half the target output voltage, the switching frequency is reduced by half.
- If the voltage at the FBx pin falls again to below one-fourth the target output voltage, the switching frequency is reduced to half its current value, that is, to one-fourth of f_{SW}.

The reduced switching frequency allows more time for the inductor current to decrease but also increases the ripple current during peak current regulation. This results in a reduction in average current and prevents output current runaway.

Pulse Skip Mode Under Maximum Duty Cycle

Under maximum duty cycle conditions, frequency foldback maintains the output in regulation. If the maximum duty cycle is reached, for example, when the input voltage decreases, the PWM modulator skips every other PWM pulse, resulting in a switching frequency foldback of one-half. If the duty cycle increases further, the PWM modulator skips two of every three PWM pulses, resulting in a switching frequency foldback to one-third of the switching frequency. Frequency foldback increases the effective maximum duty cycle, thereby decreasing the dropout voltage between the input and output voltages.

HICCUP PROTECTION

The buck regulators in the ADP5053 include a hiccup mode for overcurrent protection (OCP). When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle.

When hiccup mode is active, the overcurrent fault counter is incremented. If the overcurrent fault counter reaches 15 and overflows (indicating a short-circuit condition), both the high-side and low-side MOSFETs turn off. The buck regulator remains in hiccup mode for a period equal to seven soft start cycles and then attempts to restart from soft start. If the short-circuit fault has cleared, the regulator resumes normal operation; otherwise, it reenters hiccup mode after the soft start.

Hiccup protection is masked during the initial soft start cycle to enable startup of the buck regulator under heavy load conditions. For the buck regulator to recover from hiccup mode under heavy loads, careful design and proper component selection is required. To enable or disable hiccup protection for all four buck regulators, use the factory fuse. When hiccup protection is disabled, the frequency foldback feature continues to be available for overcurrent protection.

LATCH-OFF PROTECTION

The buck regulators in the ADP5053 have an optional latch-off mode to protect the device from serious problems such as short-circuit and overvoltage conditions. Enable latch-off mode by factory fuse.

Short-Circuit Latch-Off Mode

Short-circuit latch-off mode is enabled by factory fuse (on or off for all four buck regulators). When short-circuit latch-off mode is enabled and the protection circuit detects an overcurrent status after a soft start, the buck regulator enters hiccup mode and attempts to restart. If after completing seven continuous restart attempts, the regulator remains in the fault condition, then the regulator is shut down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply. Note that short-circuit latch-off mode does not work if hiccup protection is disabled.

Figure 41 shows the short-circuit latch-off detection function.

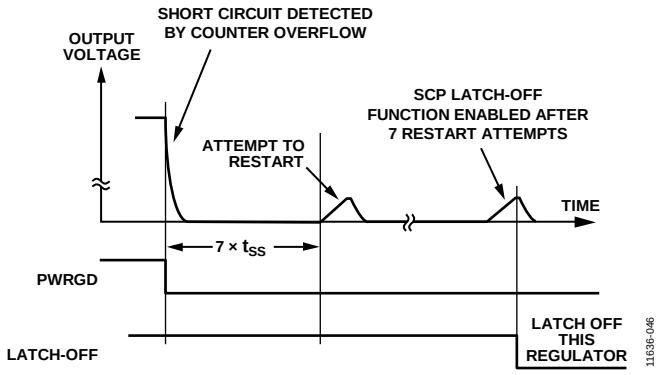


Figure 41. Short-Circuit Latch-Off Detection

Overvoltage Latch-Off Mode

Enable overvoltage latch-off mode by factory fuse (on or off for all four buck regulators). The overvoltage latch-off threshold is 124% of the nominal output voltage level. When the output voltage exceeds this threshold, the protection circuit detects the overvoltage status and the regulator shuts down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply.

Figure 42 shows the overvoltage latch-off detection function.

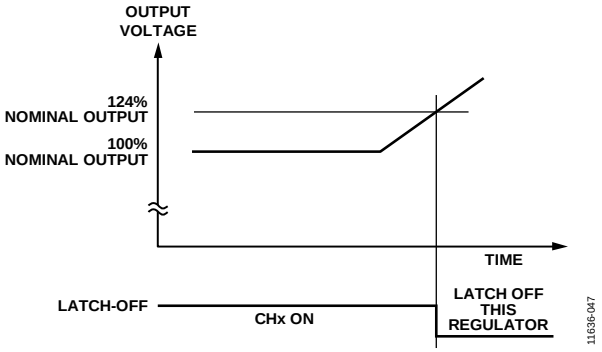


Figure 42. Overvoltage Latch-Off Detection

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry monitors the input voltage level of each buck regulator in the ADP5053. If any input voltage (PVINx pin) falls below 3.78 V (typical), the corresponding channel is turned off. The soft start period initiates after the input voltage rises above 4.2 V (typical), and setting the ENx pin high enables the corresponding channel.

Note that a UVLO condition on Channel 1 (PVIN1 pin) has a higher priority than a UVLO condition on other channels, which means that the PVIN1 supply must be available before other channels become operational.

POWER-GOOD FUNCTION

The ADP5053 includes an open-drain power-good output (PWRGD pin) that becomes active high when the selected buck regulators are operating normally. By default, the PWRGD pin monitors the output voltage on Channel 1. Other channels can be configured to control the PWRGD pin when the ADP5053 is ordered.

A logic high on the PWRGD pin indicates that the regulated output voltage of the buck regulator is above 90.5% (typical) of its nominal output. When the regulated output voltage of the buck regulator falls below 87.2% (typical) of its nominal output for a delay time greater than approximately 50 µs, the PWRGD pin goes low.

The output of the PWRGD pin is the logical AND of the internal PWRGx signals. An internal PWRGx signal must be high for a validation time of 1 ms before the PWRGD pin goes high; if one PWRGx signal fails, the PWRGD pin goes low with no delay. The channels that control the PWRGD pin (Channel 1 to Channel 4) can be specified by factory fuse. The default PWRGD setting is to monitor the output of Channel 1.

THERMAL SHUTDOWN

If the ADP5053 junction temperature exceeds 150°C, the thermal shutdown (TSD) circuit turns off the IC except for the internal linear regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5053 does not return to operation after thermal shutdown until the on-chip temperature falls below 135°C. When the device exits thermal shutdown, a soft start initiates for each enabled channel.

SUPERVISORY CIRCUIT

The ADP5053 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored with a watchdog timer. Note that the supervisory circuitry activates only when one of the ENx pins of the four buck regulators is set high.

Reset Output

The ADP5053 has an active low, open-drain reset output ($\overline{\text{RSTO}}$). This output requires an external pull-up resistor to connect the reset output to a voltage rail no higher than 6 V. The resistor must comply with the logic low and logic high voltage level requirements of the microprocessor while also supplying input current and leakage paths to the $\overline{\text{RSTO}}$ pin. A 10 kΩ resistor is adequate in most situations.

The reset output asserts when the monitored rail is below the threshold (V_{TH}), and when WDI is not serviced within the watchdog timeout period (t_{WD}). The $\overline{\text{RSTO}}$ pin remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold or after the watchdog timer times out. There are four options are available for the reset active timeout period (t_{RP}) via the factory fuse: 1.4 ms, 28 ms, 200 ms (default), or 1600 ms. Figure 43 illustrates the behavior of the $\overline{\text{RSTO}}$ output, assuming that V_{OUT2} is selected as the rail to be monitored and it supplies the external pull-up connected to the $\overline{\text{RSTO}}$ output.

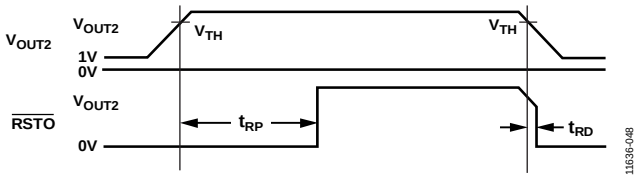


Figure 43. Reset Timing Diagram

The ADP5053 has a dedicated sensing input pin (VTH) to monitor the supply rail. The reset threshold at the VTH input is typically 0.5 V. To monitor a voltage greater than 0.5 V, connect a resistor divider network to the device.

Do not allow the VTH input to float or to be grounded. Instead, connect the VTH input to a supply voltage greater than its specified threshold voltage (V_{TH}). Add a small capacitor on the VTH pin to improve noise rejection and false reset generation.

When monitoring the input voltage, if the selected voltage falls below the UVLO level, the reset output ($\overline{\text{RSTO}}$) asserts low with the delay time (t_{RD}). The reset output is then kept low to restart the processor.

Watchdog Input

The ADP5053 features a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low to high or high to low logic transition on the watchdog input pin (WDI), which detects pulses as short as 80 ns. If the timer proceeds through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Therefore, failure of the microprocessor to toggle the WDI pin within the timeout period indicates a code execution error, and the reset pulse generated restarts the micro-processor in a known state. Four options are available for the watchdog timeout period via the factory fuse: 6.3 ms, 102 ms, 1600 ms (default), or 25.6 sec.

In addition to the logic transition on the WDI pin, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{OUT2}. When a reset is asserted, the watchdog timer clears, and the timer does not begin counting again until the reset is deasserted. Disable the watchdog timer by leaving WDI floating or by three-stating the WDI driver. Figure 44 shows the watchdog timing diagram.

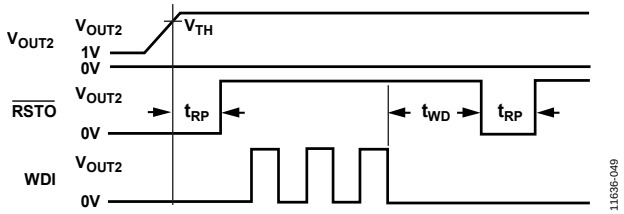


Figure 44. Watchdog Timing Diagram

Manual Reset Input

The ADP5053 features a manual reset input ($\overline{MR}$ pin, active low) with two operation modes: processor manual reset mode or power on/off switch mode. The default setting is the processor manual reset mode; however, $\overline{MR}$ operation mode selection can be configured by factory fuse.

The $\overline{MR}$ input has an internal 55 kΩ pull-up resistor so that the input remains high when unconnected. To generate a reset, connect an external push-button switch between $\overline{MR}$ and ground. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

Processor Manual Reset Mode

In processor manual reset mode, when $\overline{MR}$ is driven low, the reset output is asserted. When $\overline{MR}$ transitions from low to high, the reset remains asserted for the duration of the reset active timeout period (t_{RP}) before deasserting. Figure 45 shows the behavior of the $\overline{MR}$ pin in processor manual reset mode.

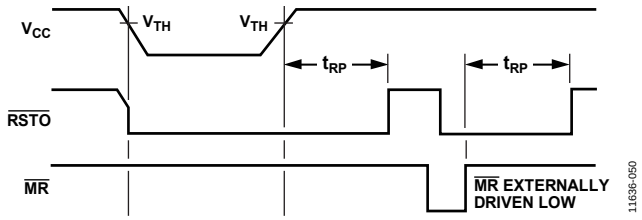


Figure 45. $\overline{MR}$ Timing Diagram in Processor Reset Mode

Power On/Off Switch Mode

In power on/off switch mode, when $\overline{MR}$ is driven low for more than 4 sec, all channels in the ADP5053 shut down, and the internal control registers reset. In this shutdown standby condition, if $\overline{MR}$ is driven low for 500 ms again, all channels in the ADP5053 restart according to the individual ENx pin status.

Figure 46 shows the $\overline{MR}$ timing diagram in power on/off switch mode.

To prepare for automatic startup, clear the $\overline{MR}$ shutdown condition by pulling down all external ENx pins.

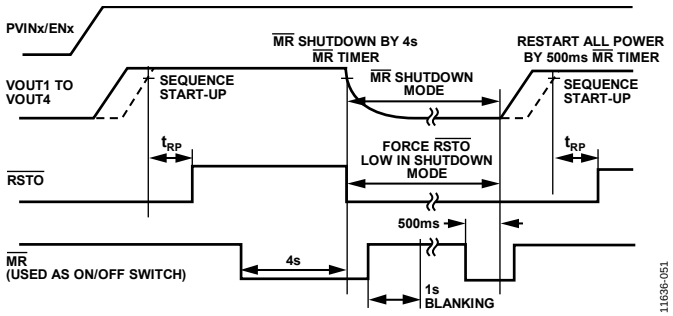


Figure 46. $\overline{MR}$ Timing Diagram in Power On/Off Switch Mode

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP5053 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower optimizes designs for cost, area, efficiency, and device count while taking into consideration the operating conditions and limitations of the IC and all real external components. Access the ADIsimPower tool at www.analog.com/ADIsimPower; the user can request an unpopulated board through the tool.

PROGRAMMING THE ADJUSTABLE OUTPUT VOLTAGE

The output voltage of the ADP5053 is externally set by a resistive voltage divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to feedback bias current, ensure that the bottom resistor in the divider is not too large; a value of less than 50 kΩ is recommended.

The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
V_{OUT} is the output voltage.
V_{REF} is the feedback reference voltage (0.8 V for Channel 1 to Channel 4).
R_{TOP} is the feedback resistor from V_{OUT} to FBx.
R_{BOT} is the feedback resistor from FBx to ground.

No resistor divider is required in the fixed output options. If a different fixed output voltage is required, contact your local Analog Devices sales or distribution representative.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, upper and lower limitations on the output voltage exist due to the minimum on time and the minimum off time.

The minimum output voltage for a given input voltage and switching frequency is limited by the minimum on time. The minimum on time for Channel 1 and Channel 2 is 117 ns (typical); the minimum on time for Channel 3 and Channel 4 is 90 ns (typical). The minimum on time increases at higher junction temperatures.

Note that in forced PWM mode, Channel 1 and Channel 2 can potentially exceed the nominal output voltage when the minimum on time limit is exceeded. Careful switching frequency selection is required to avoid this problem.

Calculate the minimum output voltage in continuous conduction mode (CCM) for a given input voltage and switching frequency using the following equation:

$$V_{OUT_MIN} = V_{IN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MIN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON2} + R_L) \times I_{OUT_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON1} is the on resistance of the high-side MOSFET.
R_{DSON2} is the on resistance of the low-side MOSFET.
I_{OUT_MIN} is the minimum output current.
R_L is the resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is limited by the minimum off time and the maximum duty cycle. Note that the frequency foldback feature helps to increase the effective maximum duty cycle by lowering the switching frequency, thereby decreasing the dropout voltage between the input and output voltages (see the Frequency Foldback section).

Calculate the maximum output voltage for a given input voltage and switching frequency using the following equation:

$$V_{OUT_MAX} = V_{IN} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MAX} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON2} + R_L) \times I_{OUT_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
f_{SW} is the switching frequency.
R_{DSON1} is the on resistance of the high-side MOSFET.
R_{DSON2} is the on resistance of the low-side MOSFET.
I_{OUT_MAX} is the maximum output current.
R_L is the resistance of the output inductor.

As shown in Equation 1 and Equation 2, reducing the switching frequency eases the minimum on time and off time limitations.

CURRENT-LIMIT SETTING

The ADP5053 has three selectable current-limit thresholds for Channel 1 and Channel 2. Make sure that the selected current-limit value is larger than the peak current of the inductor, I_{PEAK}. See Table 10 for the current-limit configuration for Channel 1 and Channel 2.

SOFT START SETTING

The buck regulators in the ADP5053 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. To set the soft start time to a value of 2 ms, 4 ms, or 8 ms, connect a resistor divider from the SS12 or SS34 pin to the VREG pin and ground (see the Soft Start section).

INDUCTOR SELECTION

The input voltage, output voltage, inductor ripple current, and switching frequency determine the inductor value. Using a small inductor value yields faster transient response but degrades efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and better efficiency but results in slower transient response. Thus, a trade-off is required between transient response and efficiency. As a guideline, the inductor ripple current, ΔI_L, is typically set to a value from 30% to 40% of the maximum load current. Calculate the inductor value using the following equation:

$$L = [(V_{IN} - V_{OUT}) \times D]/(\Delta I_L \times f_{SW})$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.

The ADP5053 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%. Because the internal current sense signal is required, the inductor value must not be larger than 10 µH for Channel 1 and Channel 2 or 22 µH for Channel 3 and Channel 4.

Calculate the peak inductor current using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, to prevent the inductor from becoming saturated by ensuring that the saturation current rating of the inductor is higher than the current-limit threshold of the buck regulator.

Calculate the rms current of the inductor using the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 11 lists recommended inductors.

Table 11. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)	Size (mm)
Coilcraft	XFL4020-102	1.0	5.4	11	10.8	4 × 4
	XFL4020-222	2.2	3.7	8.0	21.35	4 × 4
	XFL4020-332	3.3	2.9	5.2	34.8	4 × 4
	XFL4020-472	4.7	2.7	5.0	52.2	4 × 4
	XAL4030-682	6.8	3.6	3.9	67.4	4 × 4
	XAL4040-103	10	3.0	3.1	84	4 × 4
	XAL6030-102	1.0	23	18	5.62	6 × 6
	XAL6030-222	2.2	15.9	10	12.7	6 × 6
	XAL6030-332	3.3	12.2	8.0	19.92	6 × 6
	XAL6060-472	4.7	10.5	11	14.4	6 × 6
	XAL6060-682	6.8	9.2	9.0	18.9	6 × 6
TOKO	FDV0530-1R0	1.0	11.2	9.1	9.4	6.2 × 5.8
	FDV0530-2R2	2.2	7.1	7.0	17.3	6.2 × 5.8
	FDV0530-3R3	3.3	5.5	5.3	29.6	6.2 × 5.8
	FDV0530-4R7	4.7	4.6	4.2	46.6	6.2 × 5.8

OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of the output voltage.

Calculate the output capacitance required to meet the undershoot (voltage droop) requirement using the following equation:

$$C_{OUT_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT_UV}}$$

where:
K_{UV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, causing an overshoot of the output voltage.

Calculate the output capacitance required to meet the overshoot requirement using the following equation:

$$C_{OUT_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{OUT_OV})^2 - {V_{OUT}}^2}$$

where:
K_{OV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The equivalent series resistance (ESR) of the output capacitor and its capacitance value determine the output voltage ripple. Use the following equations to select a capacitor that can meet the output ripple requirements:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{\Delta I_L}$$

where:
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple requirements.

The voltage rating of the selected output capacitor must be greater than the output voltage. Determine the minimum rms current rating of the output capacitor by the following equation:

$$I_{C_{OUT}_rms} = \frac{\Delta I_L}{\sqrt{12}}$$

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. Use a ceramic capacitor and place it near the PVINx pin. Keep the loop composed of the input capacitor, the high-side NFET, and the low-side NFET as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the following equation:

$$I_{C_{IN}_rms} = I_{OUT} \times \sqrt{D \times (1-D)}$$

where D is the duty cycle ($D = V_{OUT}/V_{IN}$).

LOW-SIDE POWER DEVICE SELECTION

Channel 1 and Channel 2 include integrated low-side MOSFET drivers that drive low-side N-channel MOSFETs (NFETs). The selection of the low-side N-channel MOSFET affects the performance of the buck regulator.

The selected MOSFET must meet the following requirements:

- Drain-to-source voltage (V_{DS}) must be higher than $1.2 \times V_{IN}$.
- Drain current (I_D) must be greater than $1.2 \times I_{LIMIT_MAX}$, where I_{LIMIT_MAX} is the selected maximum current-limit threshold.
- The selected MOSFET can be fully turned on at $V_{GS} = 4.5$ V.
- Total gate charge (Qg at $V_{GS} = 4.5$ V) must be less than 20 nC. Lower Qg characteristics provide higher efficiency.

When the high-side MOSFET is turned off, the low-side MOSFET supplies the inductor current. For low duty cycle applications, the low-side MOSFET supplies the current for most of the period. To achieve higher efficiency, it is important to select a MOSFET with low on resistance. The power conduction loss for the low-side MOSFET can be calculated using the following equation:

$$P_{FET_LOW} = I_{OUT}^2 \times R_{DSON} \times (1 - D)$$

where:
R_{DSON} is the on resistance of the low-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Table 12 lists recommended dual MOSFETs for various current-limit settings. Ensure that the MOSFET can handle thermal dissipation due to power loss.

Table 12. Recommended Dual MOSFETs

Vendor	Part No.	V_{DS} (V)	I_D (A)	R_{DSON} (mΩ)	Qg (nC)	Size (mm)
IR	IRFHM8363	30	10	20.4	6.7	3 × 3
	IRLHS6276	20	3.4	45	3.1	2 × 2
Fairchild	FDMA1024	20	5.0	54	5.2	2 × 2
	FDMB3900	25	7.0	33	11	3 × 2
	FDMB3800	30	4.8	51	4	3 × 2
	FDC6401	20	3.0	70	3.3	3 × 3
Vishay	Si7228DN	30	23	25	4.1	3 × 3
	Si7232DN	20	25	16.4	12	3 × 3
	Si7904BDN	20	6	30	9	3 × 3
	Si5906DU	30	6	40	8	3 × 2
	Si5908DC	20	5.9	40	5	3 × 2
	SiA906EDJ	20	4.5	46	3.5	2 × 2
AOS	AON7804	30	22	26	7.5	3 × 3
	AON7826	20	22	26	6	3 × 3
	AO6800	30	3.4	70	4.7	3 × 3
	AON2800	20	4.5	47	4.1	2 × 2

PROGRAMMING THE UVLO INPUT

Use the precision enable input to program the UVLO threshold of the input voltage, as shown in Figure 33. To limit the degradation of the input voltage accuracy due to the internal 1 MΩ pull-down resistor tolerance, ensure that the bottom resistor in the divider is not too large; a value of less than 50 kΩ is recommended.

The precision turn-on threshold is 0.8 V. Calculate the resistive voltage divider for the programmable V_{IN} start-up voltage as follows:

$$V_{IN_STARTUP} = (0.8\ \text{nA} + (0.8\ \text{V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1\ \text{M}\Omega}{R_{BOT_EN} + 1\ \text{M}\Omega} \right)$$

where:
R_{TOP_EN} is the resistor from V_{IN} to EN.
R_{BOT_EN} is the resistor from EN to ground.

COMPENSATION COMPONENTS DESIGN

For the peak current mode control architecture, simplify the power stage as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the output capacitor ESR. The control-to-output transfer function is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 10 A/V for Channel 1 or Channel 2, and 3.33 A/V for Channel 3 or Channel 4.
R is the load resistance.
s = the frequency domain factor.
R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

The ADP5053 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 47 shows the simplified peak current mode control small signal circuit.

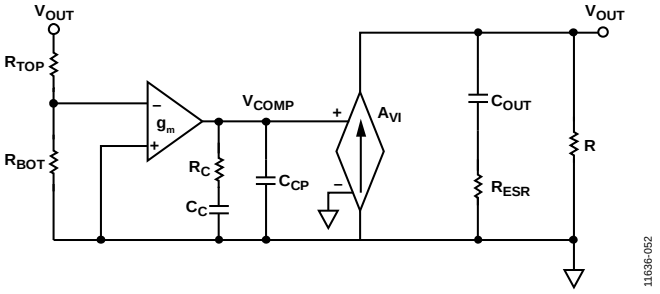


Figure 47. Simplified Peak Current Mode Control Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero; R_C and the optional C_{CP} contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following guidelines define how the compensation components (R_C, C_C, and C_{CP}) selection for ceramic output capacitor applications.

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.8\,\text{V} \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole (f_P). Calculate C_C using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor. Calculate C_{CP} using the following equation:

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

POWER DISSIPATION

The total power dissipation in the ADP5053 simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3} + P_{BUCK4}$$

Buck Regulator Power Dissipation

The power dissipation (P_{LOSS}) for each buck regulator includes power switch conduction losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Power Switch Conduction Loss (P_{COND})

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches, each of which has its own internal on resistance (R_{DSON}).

Use the following equation to estimate the power switch conduction loss:

$$P_{COND} = (R_{DSON_HS} \times D + R_{DSON_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
R_{DSON_LS} is the on resistance of the low-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE_HS} + C_{GATE_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.
f_{SW} is the switching frequency.

Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source-to-drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

Thermal Shutdown

Channel 1 and Channel 2 store the value of the inductor current only during the on time of the internal high-side MOSFET. Therefore, a small amount of power (as well as a small amount of input rms current) dissipates inside the ADP5053, which reduces thermal constraints.

However, when Channel 1 and Channel 2 are operating under maximum load with high ambient temperature and high duty cycle, the input rms current can become very large and cause the junction temperature to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the regulator enters thermal shutdown and recovers when the junction temperature falls below 135°C.

JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 6).
P_D is the power dissipation in the package.

An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz. of copper, as specified in the JEDEC standard, whereas real-world applications may use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect the exposed pad to the ground plane with several vias.

DESIGN EXAMPLE

This section provides an example of the step-by-step design procedures and the external components required for Channel 1. Table 13 lists the design requirements for this specific example.

Table 13. Example Design Requirements for Channel 1

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V ± 5%
Output Voltage	V_{OUT1} = 1.2 V
Output Current	I_{OUT1} = 4 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 12 mV in CCM mode
Load Transient	±5% at 20% to 80% load transient, 1 A/µs

Although this example shows step-by-step design procedures for Channel 1, the procedures apply to all other buck regulator channels (Channel 2 to Channel 4).

SETTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency for the ADP5053 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5053 can be set to a value from 250 kHz to 1.4 MHz by connecting a resistor from the RT pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size. (For more information, see the Oscillator section.) However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 600 kHz achieves a good combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz, use the following equation to calculate the resistor value, R_{RT}:

$$R_{RT}\ (\text{k}\Omega) = [14{,}822/f_{SW}\ (\text{kHz})]^{1.081}$$

Therefore, select standard resistor R_{RT} = 31.6 kΩ.

SETTING THE OUTPUT VOLTAGE

Select a 10 kΩ bottom resistor (R_{BOT}) and then calculate the top feedback resistor using the following equation:

$$R_{BOT} = R_{TOP} \times (V_{REF}/(V_{OUT} - V_{REF}))$$

where:
V_{REF} is 0.8 V for Channel 1.
V_{OUT} is the output voltage.

To set the output voltage to 1.2 V, choose the following resistor values: R_{TOP} = 4.99 kΩ and R_{BOT} = 10 kΩ.

SETTING THE CURRENT LIMIT

For 4 A output current operation, the typical peak current limit is 6.44 A. For this example, choose R_{ILIM1} = 22 kΩ (see Table 10). For more information, see the Current-Limit Protection section.

SELECTING THE INDUCTOR

The peak-to-peak inductor ripple current, ΔI_L, is set to 35% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = [(V_{IN} - V_{OUT}) \times D]/(\Delta I_L \times f_{SW})$$

where:
V_{IN} = 12 V.
V_{OUT} = 1.2 V.
D is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.1).
ΔI_L = 35% × 4 A = 1.4 A.
f_{SW} = 600 kHz.

The resulting value for L is 1.28 µH. The closest standard inductor value is 1.5 µH; therefore, the inductor ripple current, ΔI_L, is 1.2 A.

The peak inductor current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 4.6 A.

Calculate the rms current of the inductor using the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

The rms current of the inductor is approximately 4.02 A.

Therefore, an inductor with a minimum rms current rating of 4.02 A and a minimum saturation current rating of 4.6 A is required. However, to prevent the inductor from reaching its saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 7.48 A, for reliable operation.

Based on these requirements and recommendations, the TOKO FDV0530-1R5 inductor, with a DCR of 13.5 mΩ, is selected for this design.

SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, C_{OUT_RIPPLE}, is 20.8 µF, and the calculated R_{ESR} is 10 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT_UV}}$$

$$C_{OUT_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT_OV})^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, C_{OUT_OV} = 117 µF and C_{OUT_UV} = 13.3 µF.

The ESR of the output capacitor must be less than 13.3 mΩ, and the output capacitance must be greater than 117 µF. It is recommended that three ceramic capacitors be used (47 µF, X5R, 6.3 V), such as the GRM21BR60J476ME15 from Murata with an ESR of 2 mΩ.

SELECTING THE LOW-SIDE MOSFET

A low R_{DSON} N-channel MOSFET must be selected for high efficiency solutions. The MOSFET breakdown voltage (V_{DS}) must be greater than 1.2 × V_{IN}, and the drain current must be greater than 1.2 × I_{LIMIT_MAX}.

It is recommended that a 20 V, dual N-channel MOSFET, such as the Si7232DN from Vishay, be used for both Channel 1 and Channel 2. The R_{DSON} of the Si7232DN at 4.5 V driver voltage is 16.4 mΩ, and the total gate charge is 12 nC.

DESIGNING THE COMPENSATION NETWORK

For better load transient and stability performance, set the cross frequency, f_C, to f_{SW}/10. In this example, f_{SW} is set to 600 kHz; therefore, f_C is set to 60 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 40 µF.

$$R_C = \frac{2 \times \pi \times 1.2\,\text{V} \times 3 \times 40\,\mu\text{F} \times 60\,\text{kHz}}{0.8\,\text{V} \times 470\,\mu\text{S} \times 10\,\text{A/V}} = 14.4\,\text{k}\Omega$$

$$C_C = \frac{(0.3\,\Omega + 0.001\,\Omega) \times 3 \times 40\,\mu\text{F}}{14.4\,\text{k}\Omega} = 2.51\,\text{nF}$$

$$C_{CP} = \frac{0.001\,\Omega \times 3 \times 40\,\mu\text{F}}{14.4\,\text{k}\Omega} = 8.3\,\text{pF}$$

Choose standard components: R_C = 15 kΩ and C_C = 2.7 nF. C_{CP} is optional.

Figure 48 shows the Bode plot for the 1.2 V output rail. The cross frequency is 62 kHz, and the phase margin is 58°. Figure 49 shows the load transient waveform.

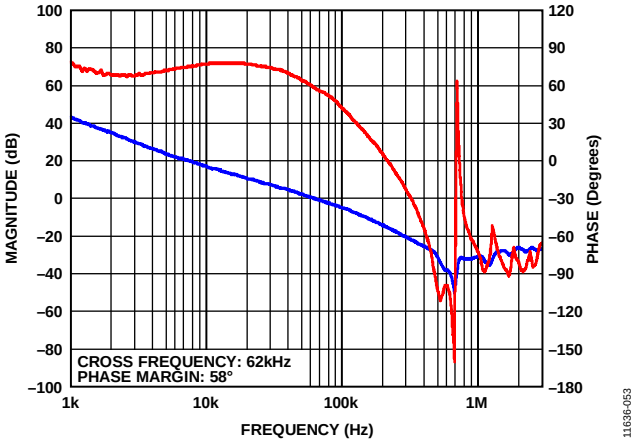


Figure 48. Bode Plot for 1.2 V Output

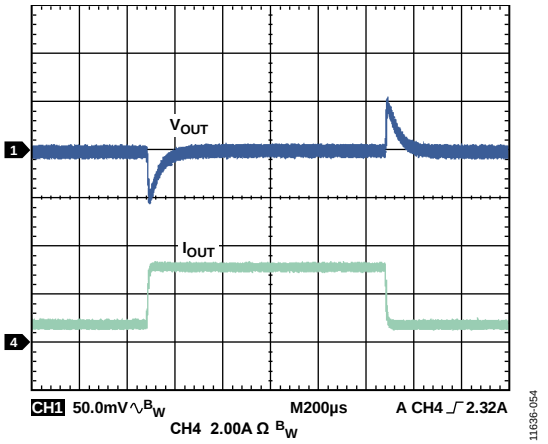


Figure 49. 0.8 A to 3.2 A Load Transient for 1.2 V Output

SELECTING THE SOFT START TIME

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current.

Use the SS12 pin to program a soft start time of 2 ms, 4 ms, or 8 ms and to configure parallel operation of Channel 1 and Channel 2. For more information, see the Soft Start section and Table 9.

SELECTING THE INPUT CAPACITOR

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF; place the input capacitor near to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

RECOMMENDED EXTERNAL COMPONENTS

Table 14 lists the recommended external components for 4 A applications used with Channel 1 and Channel 2 of the ADP5053. Table 15 lists the recommended external components for 1.2 A applications used with Channel 3 and Channel 4.

Table 14. Recommended External Components for Typical 4 A Applications, Channel 1 and Channel 2 (±1% Output Ripple, ±7.5% Tolerance at ~60% Step Transient)

f_{SW} (kHz)	I_{OUT} (A)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	Dual FET
300	4	12 (or 5)	1.2	3.3	2 × 100[1]	4.99	10	10	4700	Si7232DN
		12 (or 5)	1.5	3.3	2 × 100[1]	8.87	10.2	10	4700	Si7232DN
		12 (or 5)	1.8	3.3	3 × 47[2]	12.7	10.2	6.81	4700	Si7232DN
		12 (or 5)	2.5	4.7	3 × 47[2]	21.5	10.2	10	4700	Si7232DN
		12 (or 5)	3.3	6.8	3 × 47[2]	31.6	10.2	10	4700	Si7232DN
		12	5.0	6.8	47[3]	52.3	10	4.7	4700	Si7232DN
600	4	12 (or 5)	1.2	1.5	2 × 47[2]	4.99	10	10	2700	Si7232DN
		12 (or 5)	1.5	1.5	2 × 47[2]	8.87	10.2	10	2700	Si7232DN
		12 (or 5)	1.8	2.2	2 × 47[2]	12.7	10.2	10	2700	Si7232DN
		12 (or 5)	2.5	2.2	2 × 47[2]	21.5	10.2	10	2700	Si7232DN
		12 (or 5)	3.3	3.3	2 × 47[2]	31.6	10.2	15	2700	Si7232DN
		12	5.0	3.3	47[3]	52.3	10	10	2700	Si7232DN
1000	4	5	1.2	1.0	2 × 47[2]	4.99	10	15	1500	Si7232DN
		5	1.5	1.0	2 × 47[2]	8.87	10.2	15	1500	Si7232DN
		12 (or 5)	1.8	1.0	47[2]	12.7	10.2	10	1500	Si7232DN
		12 (or 5)	2.5	1.5	47[2]	21.5	10.2	10	1500	Si7232DN
		12 (or 5)	3.3	1.5	47[2]	31.6	10.2	10	1500	Si7232DN
		12	5.0	2.2	47[3]	52.3	10	15	1500	Si7232DN

[1] 100 µF capacitor: Murata GRM31CR60J107ME39 (6.3 V, X5R, 1206).
[2] 47 µF capacitor: Murata GRM21BR60J476ME15 (6.3 V, X5R, 0805).
[3] 47 µF capacitor: Murata GRM31CR61A476ME15 (10 V, X5R, 1206).

Table 15. Recommended External Components for Typical 1.2 A Applications, Channel 3 and Channel 4 (±1% Output Ripple, ±7.5% Tolerance at ~60% Step Transient)

f_{SW} (kHz)	I_{OUT} (A)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)
300	1.2	12 (or 5)	1.2	10	2 × 22[1]	4.99	10	6.81	4700
		12 (or 5)	1.5	10	2 × 22[1]	8.87	10.2	6.81	4700
		12 (or 5)	1.8	15	2 × 22[1]	12.7	10.2	6.81	4700
		12 (or 5)	2.5	15	2 × 22[1]	21.5	10.2	6.81	4700
		12 (or 5)	3.3	22	2 × 22[1]	31.6	10.2	6.81	4700
		12	5.0	22	22[2]	52.3	10	6.81	4700
600	1.2	12 (or 5)	1.2	4.7	22[1]	4.99	10	6.81	2700
		12 (or 5)	1.5	6.8	22[1]	8.87	10.2	6.81	2700
		12 (or 5)	1.8	6.8	22[1]	12.7	10.2	6.81	2700
		12 (or 5)	2.5	10	22[1]	21.5	10.2	6.81	2700
		12 (or 5)	3.3	10	22[1]	31.6	10.2	6.81	2700
		12	5.0	10	22[2]	52.3	10	6.81	2700
1000	1.2	5	1.2	2.2	22[1]	4.99	10	10	1800
		12 (or 5)	1.5	3.3	22[1]	8.87	10.2	10	1800
		12 (or 5)	1.8	4.7	22[1]	12.7	10.2	10	1800
		12 (or 5)	2.5	4.7	22[1]	21.5	10.2	10	1800
		12 (or 5)	3.3	6.8	22[1]	31.6	10.2	10	1800
		12	5.0	6.8	22[2]	52.3	10	15	1800

[1] 22 µF capacitor: Murata GRM188R60J226MEA0 (6.3 V, X5R, 0603).
[2] 22 µF capacitor: Murata GRM219R61A226MEA0 (10 V, X5R, 0805).

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Effective circuit board layout is essential to obtain the best performance from the ADP5053 (see Figure 51). Poor layout can affect the regulation and stability of the device, as well as the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance. Refer to the following guidelines for the most effective PCB layout.

- Place the input capacitor, inductor, MOSFET, output capacitor, and bootstrap capacitor near to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGNDx, and SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible. Figure 50 shows the high current path.
- Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connected to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors near to the VREG and VDD pins.
- Place the frequency setting resistor near to the RT pin.
- Place the feedback resistor divider near to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use 0402 or 0603 size resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

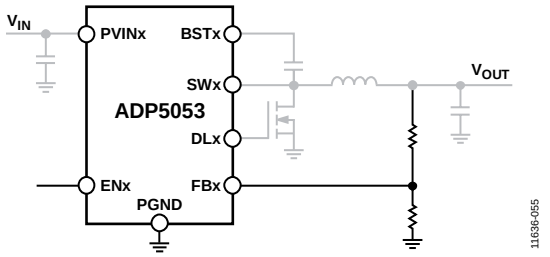


Figure 50. Typical Circuit with High Current Traces Shown in Gray

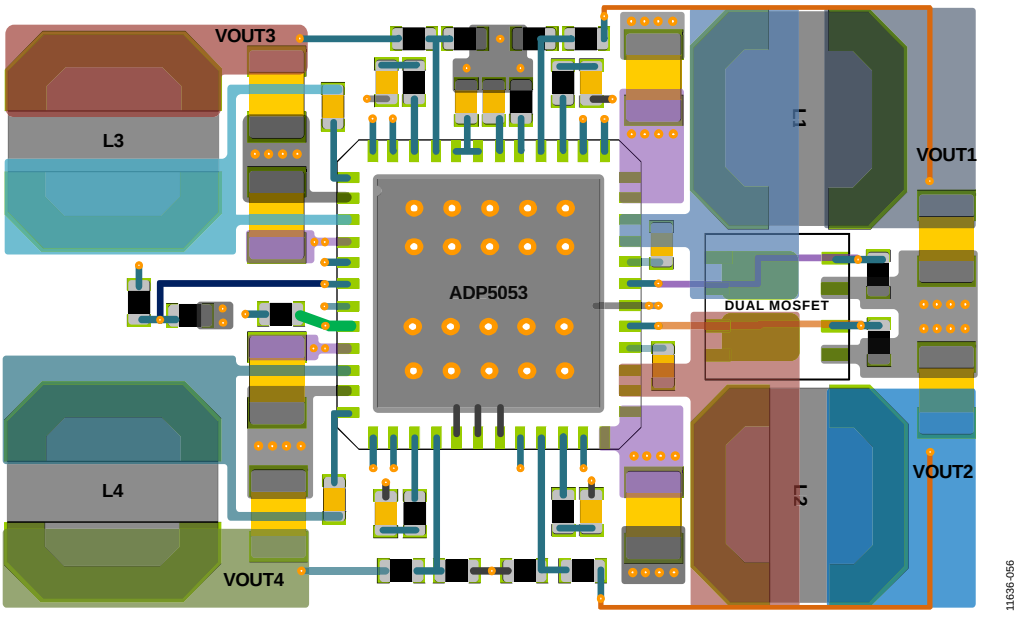


Figure 51. Typical PCB Layout

TYPICAL APPLICATION CIRCUITS

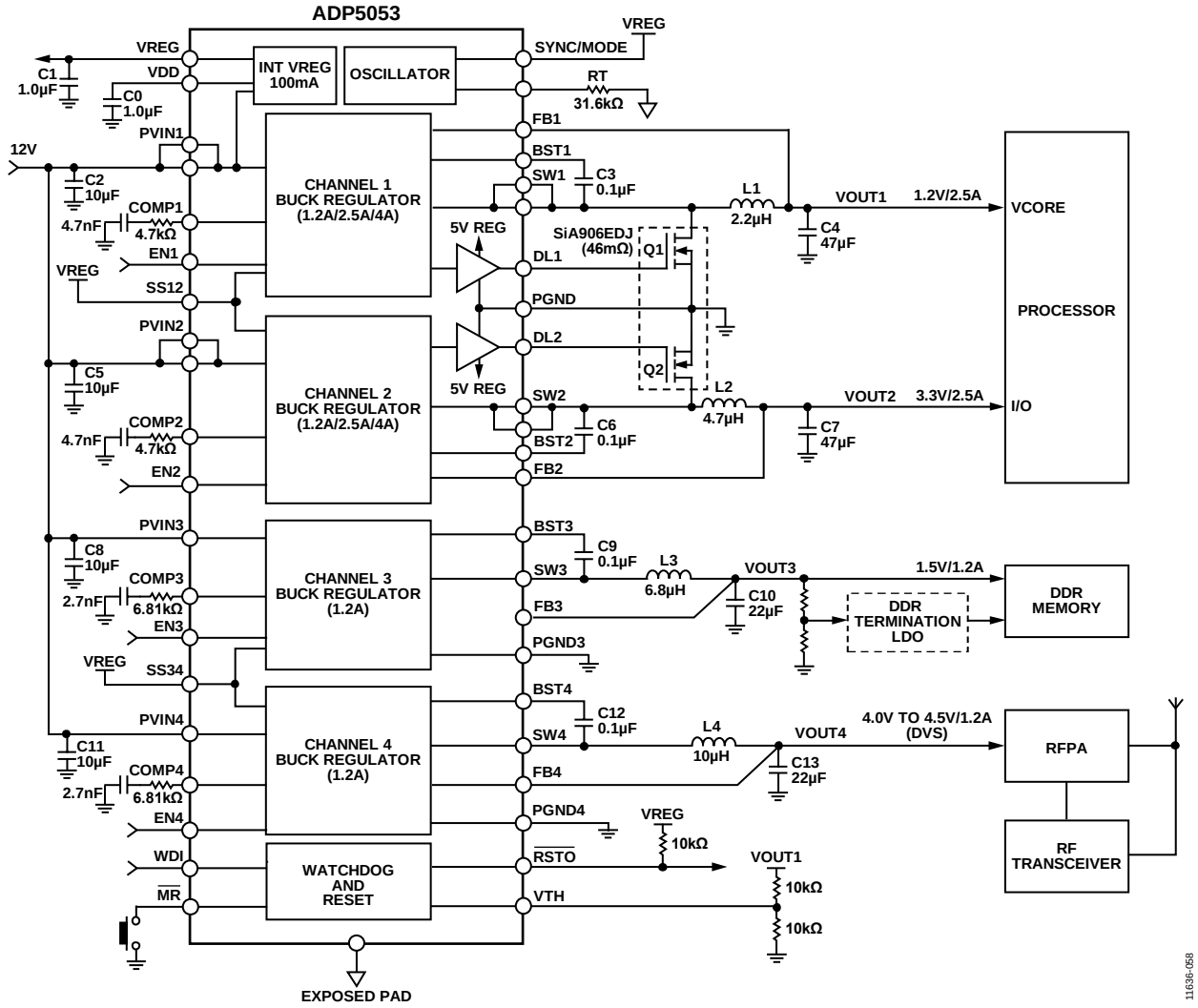


Figure 52. Typical Femtocell Application, 600 kHz Switching Frequency, Fixed Output Model

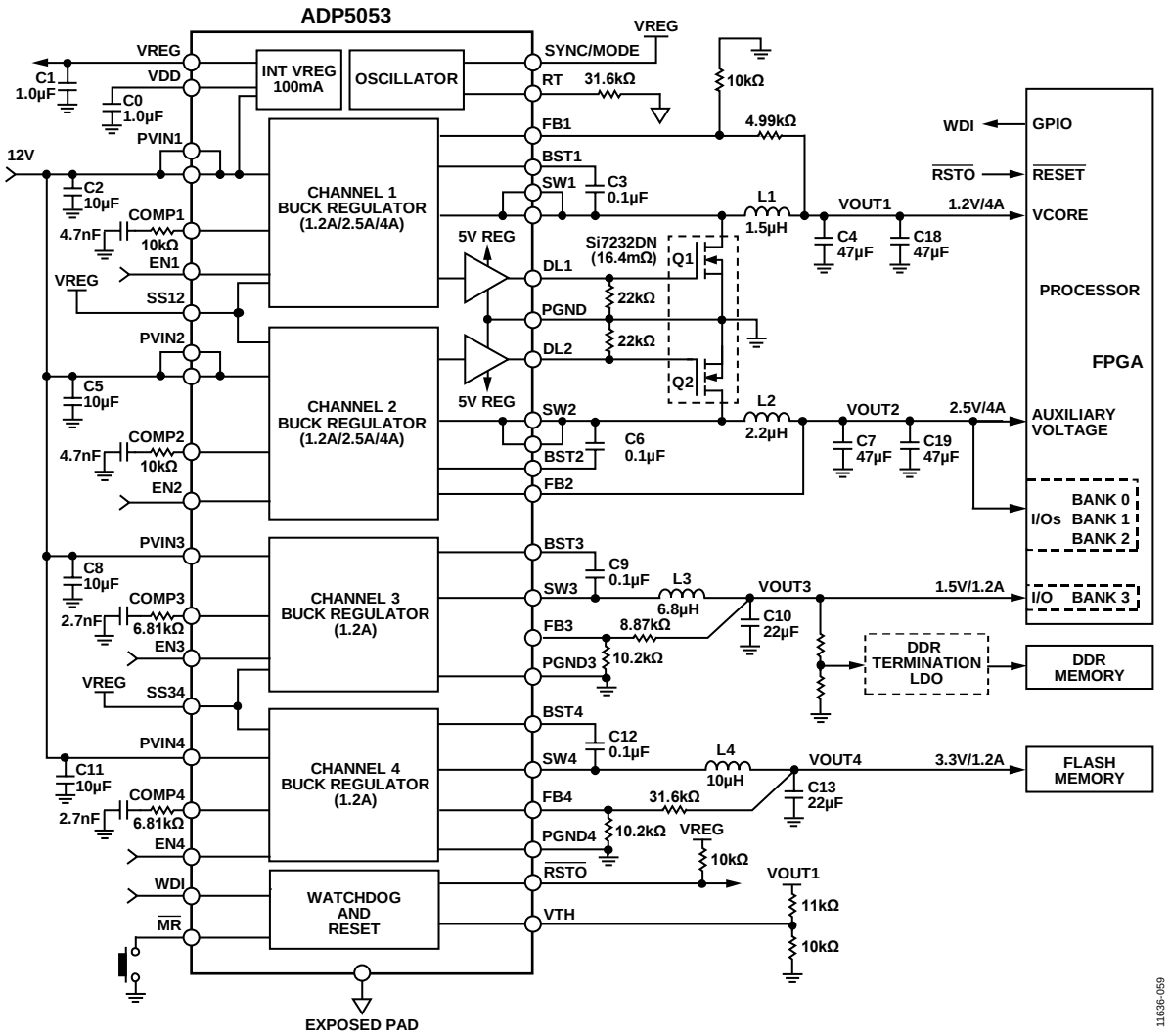


Figure 53. Typical FPGA Application, 600 kHz Switching Frequency, Adjustable Output Model

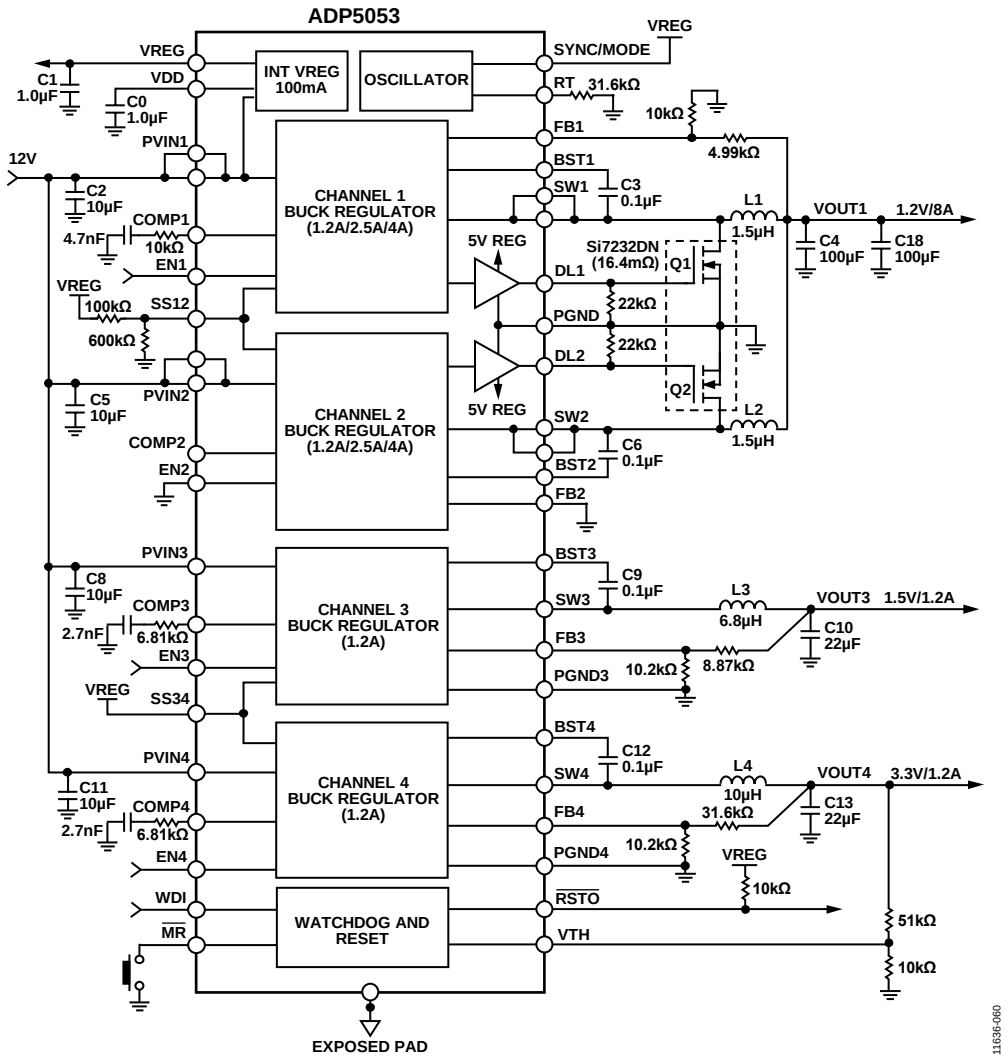


Figure 54. Typical Channel 1/Channel 2 Parallel Output Application, 600 kHz Switching Frequency, Adjustable Output Model

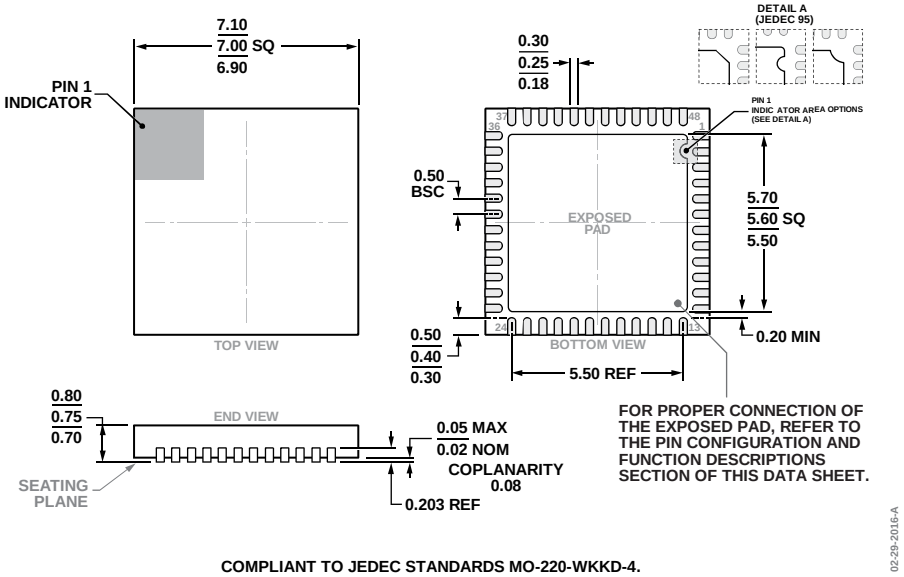
FACTORY DEFAULT OPTIONS

Table 16 lists the factory default options programmed into the ADP5053 when the device is ordered (see the Ordering Guide).

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 × switching frequency set by the RT pin
Switching Frequency on Channel 3	1 × switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Overvoltage Latch-Off Function	Disabled for output overvoltage events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4.

Figure 55. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADP5053ACPZ-R7	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
ADP5053-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Table 16 lists the factory default options for the device.

©2013–2017 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D11636-0-7/17(C)