5-Channel Integrated Power Solution with Quad Buck Regulators and 200 mA LDO Regulator

Data Sheet

ADP5050

FEATURES

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory fuse or I²C interface
- I²C interface with interrupt on fault conditions
- Power regulation
  - Channel 1 and Channel 2: programmable 1.2 A/2.5 A/4 A sync buck regulators with low-side FET driver
  - Channel 3 and Channel 4: 1.2 A sync buck regulators
  - Channel 5: 200 mA low dropout (LDO) regulator
- Single 8 A output (Channel 1 and Channel 2 operated in parallel)
- Dynamic voltage scaling (DVS) for Channel 1 and Channel 4
- Precision enable with 0.8 V accurate threshold
- Active output discharge switch
- Programmable phase shift in 90° steps
- Individual channel FPWM/PSM mode selection
- Frequency synchronization input or output
- Optional latch-off protection on OVP/OCP failure
- Power-good flag on selected channels
- Low input voltage detection
- Overheat detection on junction temperature
- UVLO, OCP, and TSD protection
- 48-lead, 7 mm × 7 mm LFCSP package
- –40°C to +125°C junction temperature

APPLICATIONS

- Small cell base stations
- FPGA and processor applications
- Security and surveillance
- Medical applications

GENERAL DESCRIPTION

The ADP5050 combines four high performance buck regulators and one 200 mA low dropout (LDO) regulator in a 48-lead LFCSP package that meets demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15 V with no preregulators.

Channel 1 and Channel 2 integrate high-side power MOSFETs and low-side MOSFET drivers. External NFETs can be used in low-side power devices to achieve an efficiency optimized solution and deliver a programmable output current of 1.2 A, 2.5 A, or 4 A. Combining Channel 1 and Channel 2 in a parallel configuration can provide a single output with up to 8 A of current.

Channel 3 and Channel 4 integrate both high-side and low-side MOSFETs to deliver output current of 1.2 A.

TYPICAL APPLICATION CIRCUIT

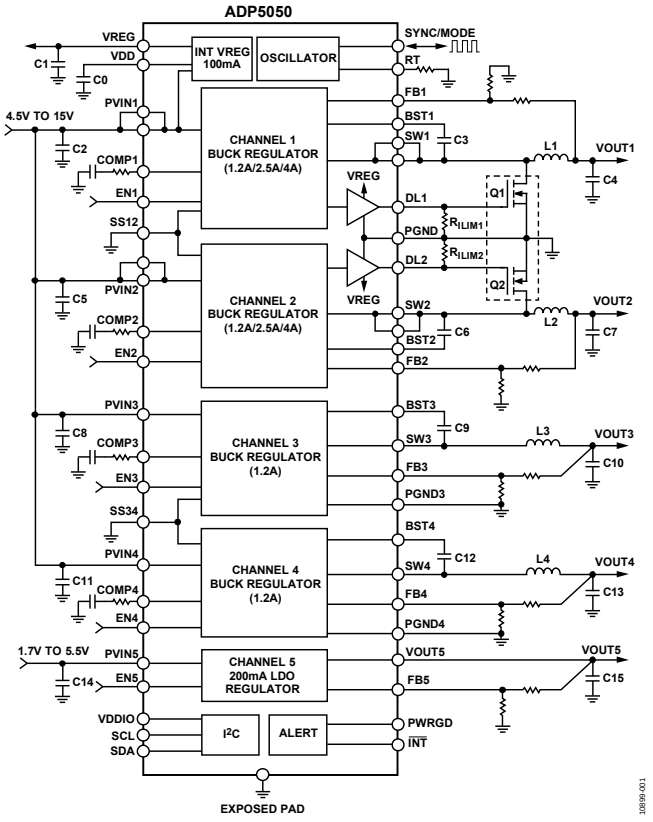


Figure 1.

Table 1. Family Models

Model	Channels	I²C	Package
ADP5050	Four bucks, one LDO	Yes	48-Lead LFCSP
ADP5051	Four bucks, supervisory	Yes	48-Lead LFCSP
ADP5052	Four bucks, one LDO	No	48-Lead LFCSP
ADP5053	Four bucks, supervisory	No	48-Lead LFCSP
ADP5054	Four high current bucks	No	48-Lead LFCSP

The switching frequency of the ADP5050 can be programmed or synchronized to an external clock. The ADP5050 contains a precision enable pin on each channel for easy power-up sequencing or adjustable UVLO threshold.

The ADP5050 integrates a general-purpose LDO regulator with low quiescent current and low dropout voltage that provides up to 200 mA of output current.

The optional I²C interface provides the user with flexible configuration options, including adjustable and fixed output voltage options, junction temperature overheat warning, low input voltage detection, and dynamic voltage scaling (DVS).

Rev. C
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REVISION HISTORY

10/2016—Rev. B to Rev. C

Deleted Factory Programmable Options Section and Table 52 to Table 65; Renumbered Sequentially 54
Changes to Factory Default Options Section 54
Updated Outline Dimensions 55

9/2015—Rev. A to Rev. B

Changes to Figure 1 and Table 1 1

3/2014—Rev. 0 to Rev. A

Changed Pin 13 from nINT to $\overline{INT}$ .... Throughout
Added Table 1; Renumbered Sequentially 1
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Updated Outline Dimensions (Exposed Paddle Changed for JEDEC Compliance) 57

5/2013—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

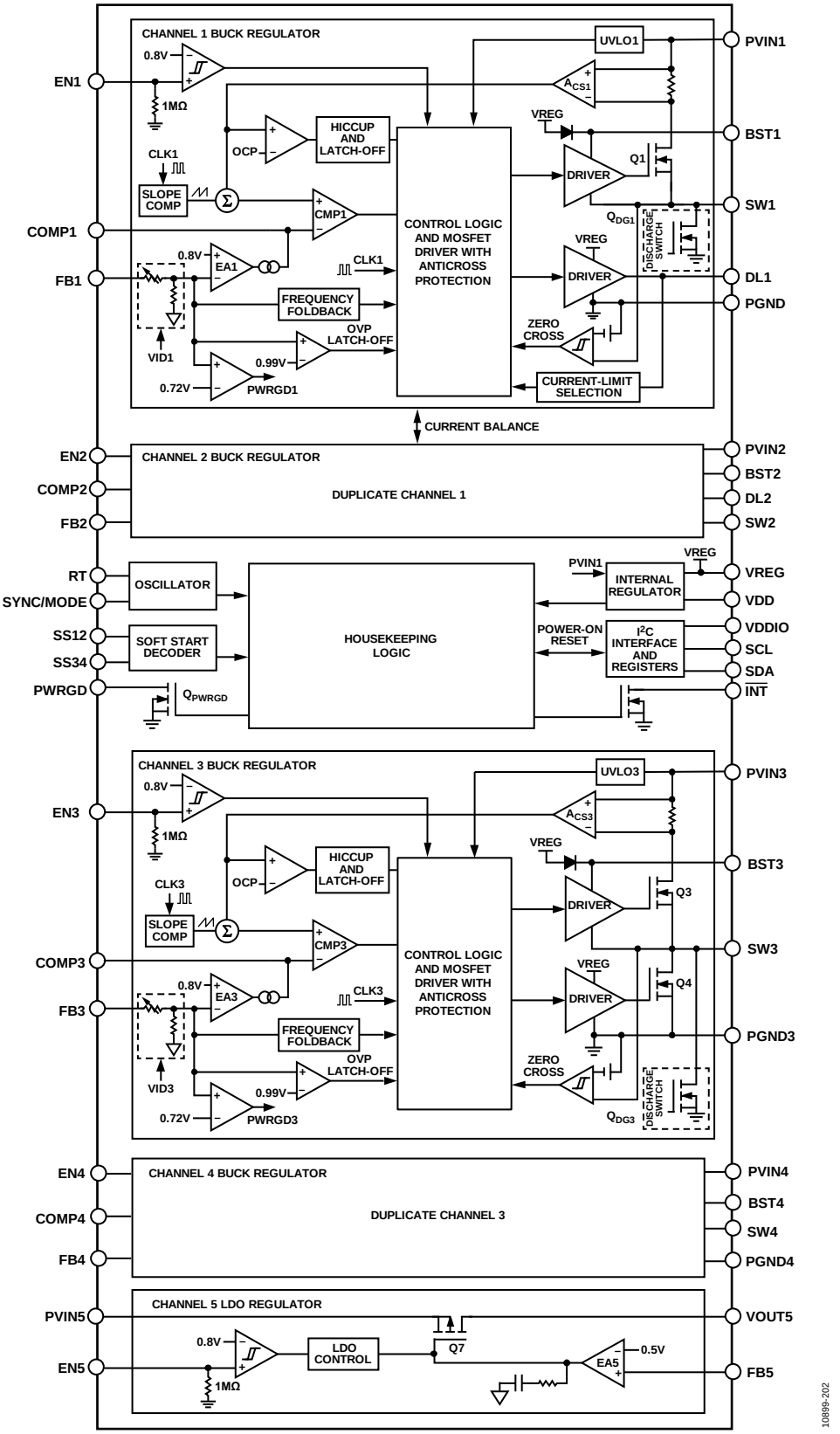


Figure 2.

SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	4.5		15.0	V	PVIN1, PVIN2, PVIN3, PVIN4 pins
QUIESCENT CURRENT						PVIN1, PVIN2, PVIN3, PVIN4 pins
Operating Quiescent Current	$I_{Q(4\text{-}BUCKS)}$		4.8	6.25	mA	No switching, all ENx pins high
	$I_{SHDN(4BUCKS+LDO)}$		25	65	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT	UVLO					PVIN1, PVIN2, PVIN3, PVIN4 pins
Rising Threshold	$V_{UVLO\text{-}RISING}$		4.2	4.36	V	
Falling Threshold	$V_{UVLO\text{-}FALLING}$	3.6	3.78		V	
Hysteresis	V_{HYS}		0.42		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	700	740	780	kHz	RT = 25.5 kΩ
Switching Frequency Range		250		1400	kHz	
SYNC Input						
Input Clock Range	f_{SYNC}	250		1400	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC_MIN_ON}$	100			ns	
Minimum Off Time	$t_{SYNC_MIN_OFF}$	100			ns	
Input Clock High Voltage	$V_{H(SYNC)}$	1.3			V	
Input Clock Low Voltage	$V_{L(SYNC)}$			0.4	V	
SYNC Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK_PULSE_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK_RISE_FALL}$		10		ns	
High Level Voltage	$V_{H(SYNC_OUT)}$		V_{VREG}		V	
PRECISION ENABLING						EN1, EN2, EN3, EN4, EN5 pins
High Level Threshold	$V_{TH_H(EN)}$		0.806	0.832	V	
Low Level Threshold	$V_{TH_L(EN)}$	0.688	0.725		V	
Pull-Down Resistor	$R_{PULL\text{-}DOWN(EN)}$		1.0		MΩ	
POWER GOOD						
Internal Power-Good Rising Threshold	$V_{PWRGD(RISE)}$	86.3	90.5	95	%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		3.3		%	
Internal Power-Good Falling Delay	t_{PWRGD_FALL}		50		µs	
Rising Delay for PWRGD Pin	$t_{PWRGD_PIN_RISE}$		1		ms	
Leakage Current for PWRGD Pin	$I_{PWRGD_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		50	100	mV	I_{PWRGD} = 1 mA
LOGIC INPUTS (SCL AND SDA PINS)						VDDIO = 3.3 V
High Level Threshold	V_{LOGIC_HIGH}	0.7 × VDDIO			V	
Low Level Threshold	V_{LOGIC_LOW}			0.3 × VDDIO	V	
LOGIC OUTPUTS						
Low Level Output Voltage						
SDA Pin	V_{SDA_LOW}			0.4	V	VDDIO = 3.3 V, I_{SDA} = 3 mA
$\overline{INT}$ Pin	$V_{\overline{INT}_LOW}$			0.4	V	$I_{\overline{INT}}$ = 3 mA
INTERNAL REGULATORS						
VDD Output Voltage	V_{VDD}	3.2	3.305	3.4	V	I_{VDD} = 10 mA
VDD Current Limit	I_{LIM_VDD}	20	51	80	mA	
VREG Output Voltage	V_{VREG}	4.9	5.1	5.3	V	
VREG Dropout Voltage	$V_{DROPOUT}$		225		mV	I_{VREG} = 50 mA
VREG Current Limit	I_{LIM_VREG}	50	95	140	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW INPUT VOLTAGE DETECTION						
Low Input Voltage Threshold	$V_{LVIN-TH}$	4.07	4.236	4.39	V	LVIN_TH[3:0] = 0000
		10.05	10.25	10.4	V	LVIN_TH[3:0] = 1100
Low Input Voltage Threshold Range		4.2		11.2	V	I^2C programmable (4-bit value)
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}		150		°C	
Thermal Shutdown Hysteresis	T_{HYS}		15		°C	
THERMAL OVERHEAT WARNING						
Thermal Overheat Threshold	T_{HOT}		115		°C	TEMP_TH[1:0] = 10
Overheat Threshold Range		105		125	°C	I^2C programmable (2-bit value)
Thermal Overheat Hysteresis	$T_{HOT(HYS)}$		5		°C	

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.1 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
FB1 Pin						
Fixed Output Options	V_{OUT1}	0.85		1.60	V	Fuse trim or I^2C interface (5-bit value)
Adjustable Feedback Voltage	V_{FB1}		0.800		V	
Feedback Voltage Accuracy	$V_{FB1(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage
SW1 Pin						
High-Side Power FET On Resistance	$R_{DSON(1H)}$		100		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM1)}$	3.50	4.4	5.28	A	R_{ILIM1} = floating
		1.91	2.63	3.08	A	R_{ILIM1} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM1} = 22 kΩ
Minimum On Time	t_{MIN_ON1}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF1}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL1 Pin						
Rising Time	$t_{RISING1}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING1}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING1}$		10		Ω	
Sinking Resistor	$t_{SINKING1}$		0.95		Ω	
Error Amplifier (EA), COMP1 Pin						
EA Transconductance	g_{m1}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS1}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP1}$		7 × t_{SS1}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		250		Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 2 SYNC BUCK REGULATOR						
FB2 Pin						
Fixed Output Options	V_{OUT2}	3.3		5.0	V	Fuse trim or I²C interface (3-bit value)
Adjustable Feedback Voltage	V_{FB2}		0.800		V	
Feedback Voltage Accuracy	$V_{FB2(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	Adjustable voltage
SW2 Pin						
High-Side Power FET On Resistance	$R_{DSON(2H)}$		110		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM2)}$	3.50	4.4	5.28	A	R_{ILIM2} = floating
		1.91	2.63	3.08	A	R_{ILIM2} = 47 kΩ
		4.95	6.44	7.48	A	R_{ILIM2} = 22 kΩ
Minimum On Time	t_{MIN_ON2}		117	155	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF2}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Low-Side Driver, DL2 Pin						
Rising Time	$t_{RISING2}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING2}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING2}$		10		Ω	
Sinking Resistor	$t_{SINKING2}$		0.95		Ω	
Error Amplifier (EA), COMP2 Pin						
EA Transconductance	g_{m2}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS2}		2.0		ms	SS12 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP2}$		7 × t_{SS2}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		250		Ω	
CHANNEL 3 SYNC BUCK REGULATOR						
FB3 Pin						
Fixed Output Options	V_{OUT3}	1.20		1.80	V	Fuse trim or I²C interface (3-bit value)
Adjustable Feedback Voltage	V_{FB3}		0.800		V	
Feedback Voltage Accuracy	$V_{FB3(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DSON(3H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON(3L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM3)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON3}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF3}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP3 Pin						
EA Transconductance	g_{m3}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS3}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP3}$		7 × t_{SS3}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		250		Ω	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 4 SYNC BUCK REGULATOR						
FB4 Pin						
Fixed Output Options	V_{OUT4}	2.5		5.5	V	Fuse trim or I^2C interface (5-bit value)
Adjustable Feedback Voltage	V_{FB4}		0.800		V	
Feedback Voltage Accuracy	$V_{FB4(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB4}			0.1	µA	
SW4 Pin						
High-Side Power FET On Resistance	$R_{DSON(4H)}$		225		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON(4L)}$		150		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM4)}$	1.7	2.2	2.55	A	
Minimum On Time	t_{MIN_ON4}		90	120	ns	f_{SW} = 250 kHz to 1.4 MHz
Minimum Off Time	t_{MIN_OFF4}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 1.4 MHz
Error Amplifier (EA), COMP4 Pin						
EA Transconductance	g_{m4}	310	470	620	µS	
Soft Start						
Soft Start Time	t_{SS4}		2.0		ms	SS34 connected to VREG
Programmable Soft Start Range		2.0		8.0	ms	
Hiccup Time	$t_{HICCUP4}$		7 × t_{SS4}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		250		Ω	

LDO REGULATOR SPECIFICATIONS

V_{IN5} = (VOUT5 + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V; C_{IN} = C_{OUT} = 1 µF; T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	1.7		5.5	V	PVIN5 pin
OPERATIONAL SUPPLY CURRENT					
Bias Current for LDO Regulator		30	130	µA	I_{OUT5} = 200 µA
		60	170	µA	I_{OUT5} = 10 mA
		145	320	µA	I_{OUT5} = 200 mA
VOLTAGE FEEDBACK (FB5 PIN)					
Adjustable Feedback Voltage		0.500		V	
Feedback Voltage Accuracy	−1.0		+1.0	%	T_J = 25°C
	−1.6		+1.6	%	0°C ≤ T_J ≤ 85°C
	−2.0		+2.0	%	−40°C ≤ T_J ≤ +125°C
DROPOUT VOLTAGE					I_{OUT5} = 200 mA
		80		mV	VOUT5 = 3.3 V
		100		mV	VOUT5 = 2.5 V
		180		mV	VOUT5 = 1.5 V
CURRENT-LIMIT THRESHOLD	250	510		mA	Specified from the output voltage drop to 90% of the specified typical value
OUTPUT NOISE		92		µV rms	10 Hz to 100 kHz, V_{PVIN5} = 5 V, VOUT5 = 1.8 V
POWER SUPPLY REJECTION RATIO					V_{PVIN5} = 5 V, VOUT5 = 1.8 V, I_{OUT5} = 1 mA
		77		dB	10 kHz
		66		dB	100 kHz

I²C INTERFACE TIMING SPECIFICATIONS

T_A = 25°C, V_{VDD} = 3.3 V, V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_{HIGH}	0.6			µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU,DAT}$	100			ns	Data setup time
$t_{HD,DAT}$	0		0.9	µs	Data hold time[1]
$t_{SU,STA}$	0.6			µs	Setup time for a repeated start condition
$t_{HD,STA}$	0.6			µs	Hold time for a start or repeated start condition
t_{BUF}	1.3			µs	Bus free time between a stop condition and a start condition
$t_{SU,STO}$	0.6			µs	Setup time for a stop condition
t_R	20 + 0.1C_B[2]		300	ns	Rise time of SCL and SDA
t_F	20 + 0.1C_B[2]		300	ns	Fall time of SCL and SDA
t_{SP}	0		50	ns	Pulse width of suppressed spike
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

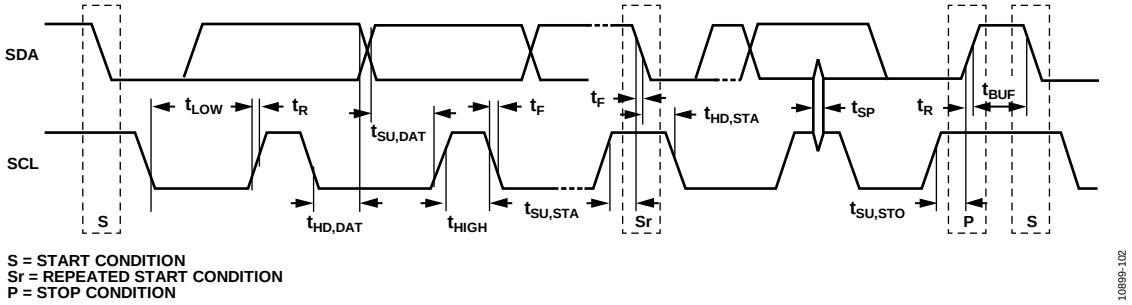


Figure 3. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
PVIN1 to PGND	−0.3 V to +18 V
PVIN2 to PGND	−0.3 V to +18 V
PVIN3 to PGND3	−0.3 V to +18 V
PVIN4 to PGND4	−0.3 V to +18 V
PVIN5 to GND	−0.3 V to +6.5 V
SW1 to PGND	−0.3 V to +18 V
SW2 to PGND	−0.3 V to +18 V
SW3 to PGND3	−0.3 V to +18 V
SW4 to PGND4	−0.3 V to +18 V
PGND to GND	−0.3 V to +0.3 V
PGND3 to GND	−0.3 V to +0.3 V
PGND4 to GND	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
BST4 to SW4	−0.3 V to +6.5 V
DL1 to PGND	−0.3 V to +6.5 V
DL2 to PGND	−0.3 V to +6.5 V
SS12, SS34 to GND	−0.3 V to +6.5 V
EN1, EN2, EN3, EN4, EN5 to GND	−0.3 V to +6.5 V
VREG to GND	−0.3 V to +6.5 V
SYNC/MODE to GND	−0.3 V to +6.5 V
VOUT5, FB5 to GND	−0.3 V to +6.5 V
RT to GND	−0.3 V to +3.6 V
$\overline{\text{INT}}$, PWRGD to GND	−0.3 V to +6.5 V
FB1, FB2, FB3, FB4 to GND[1]	−0.3 V to +3.6 V
FB2 to GND[2]	−0.3 V to +6.5 V
FB4 to GND[2]	−0.3 V to +7 V
COMP1, COMP2, COMP3, COMP4 to GND	−0.3 V to +3.6 V
VDD, VDDIO to GND	−0.3 V to +3.6 V
SCL, SDA	−0.3 V to VDDIO + 0.3 V
Storage Temperate Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C

[1] This rating applies to the adjustable output voltage models of the ADP5050.
[2] This rating applies to the fixed output voltage models of the ADP5050.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LFCSP	27.87	2.99	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

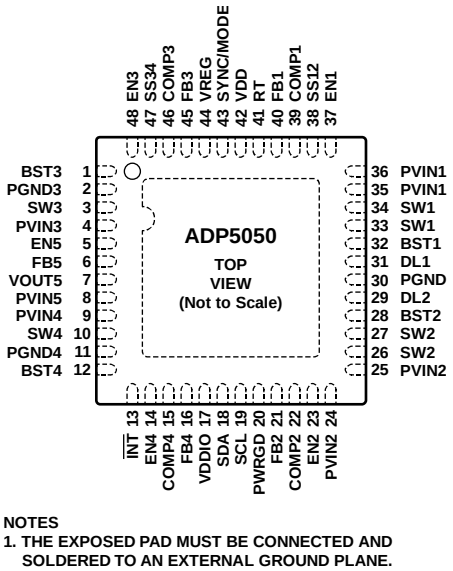


Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST3	High-Side FET Driver Power Supply for Channel 3.
2	PGND3	Power Ground for Channel 3.
3	SW3	Switching Node Output for Channel 3.
4	PVIN3	Power Input for Channel 3. Connect a bypass capacitor between this pin and ground.
5	EN5	Enable Input for Channel 5. An external resistor divider can be used to set the turn-on threshold.
6	FB5	Feedback Sensing Input for Channel 5.
7	VOUT5	Power Output for Channel 5.
8	PVIN5	Power Input for Channel 5. Connect a bypass capacitor between this pin and ground.
9	PVIN4	Power Input for Channel 4. Connect a bypass capacitor between this pin and ground.
10	SW4	Switching Node Output for Channel 4.
11	PGND4	Power Ground for Channel 4.
12	BST4	High-Side FET Driver Power Supply for Channel 4.
13	$\overline{\text{INT}}$	Interrupt Output on Fault Condition. Open-drain output port.
14	EN4	Enable Input for Channel 4. An external resistor divider can be used to set the turn-on threshold.
15	COMP4	Error Amplifier Output for Channel 4. Connect an RC network from this pin to ground.
16	FB4	Feedback Sensing Input for Channel 4.
17	VDDIO	Power Supply for the I^2C Interface.
18	SDA	Data Input/Output for the I^2C Interface. Open-drain I/O port.
19	SCL	Clock Input for the I^2C Interface.
20	PWRGD	Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels. This pin can be programmed by the factory to set the I^2C address of the part; the I^2C address setting function replaces the power-good function on this pin. For more information, see the I^2C Addresses section.
21	FB2	Feedback Sensing Input for Channel 2.
22	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground.
23	EN2	Enable Input for Channel 2. An external resistor divider can be used to set the turn-on threshold.
24, 25	PVIN2	Power Input for Channel 2. Connect a bypass capacitor between this pin and ground.
26, 27	SW2	Switching Node Output for Channel 2.
28	BST2	High-Side FET Driver Power Supply for Channel 2.
29	DL2	Low-Side FET Gate Driver for Channel 2. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 2.

Pin No.	Mnemonic	Description
30	PGND	Power Ground for Channel 1 and Channel 2.
31	DL1	Low-Side FET Gate Driver for Channel 1. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 1.
32	BST1	High-Side FET Driver Power Supply for Channel 1.
33, 34	SW1	Switching Node Output for Channel 1.
35, 36	PVIN1	Power Input for the Internal 5.1 V VREG Linear Regulator and the Channel 1 Buck Regulator. Connect a bypass capacitor between this pin and ground.
37	EN1	Enable Input for Channel 1. An external resistor divider can be used to set the turn-on threshold.
38	SS12	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 1 and Channel 2 (see the Soft Start section). This pin is also used to configure parallel operation of Channel 1 and Channel 2 (see the Parallel Operation section).
39	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from this pin to ground.
40	FB1	Feedback Sensing Input for Channel 1.
41	RT	Connect a resistor from RT to ground to program the switching frequency from 250 kHz to 1.4 MHz. For more information, see the Oscillator section.
42	VDD	Output of the Internal 3.3 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
43	SYNC/MODE	Synchronization Input/Output (SYNC). To synchronize the switching frequency of the part to an external clock, connect this pin to an external clock with a frequency from 250 kHz to 1.4 MHz. This pin can also be configured as a synchronization output using the I^2C interface or by factory fuse. Forced PWM or Automatic PWM/PSM Selection Pin (MODE). When this pin is logic high, each channel operates in forced PWM or automatic PWM/PSM mode, as specified by the PSMx_ON bits in Register 6. When this pin is logic low, all channels operate in automatic PWM/PSM mode, and the PSMx_ON settings in Register 6 are ignored.
44	VREG	Output of the Internal 5.1 V Linear Regulator. Connect a 1 µF ceramic capacitor between this pin and ground.
45	FB3	Feedback Sensing Input for Channel 3.
46	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from this pin to ground.
47	SS34	Connect a resistor divider from this pin to VREG and ground to configure the soft start time for Channel 3 and Channel 4 (see the Soft Start section).
48	EN3	Enable Input for Channel 3. An external resistor divider can be used to set the turn-on threshold.
	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected and soldered to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

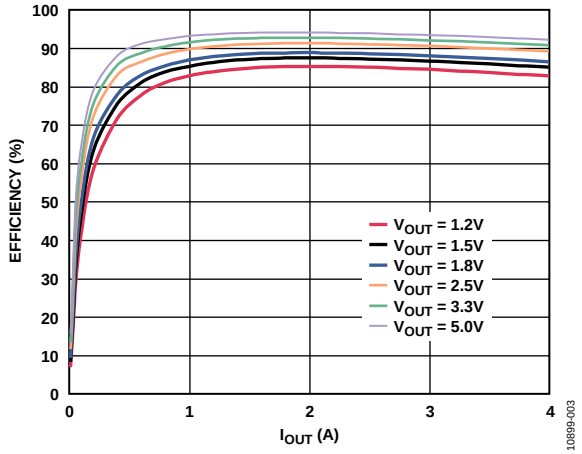


Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

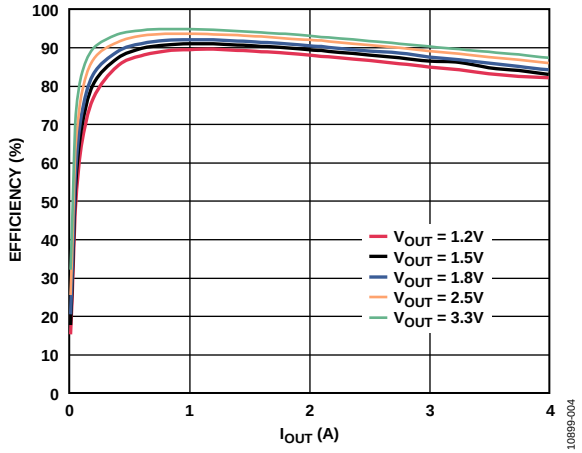


Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

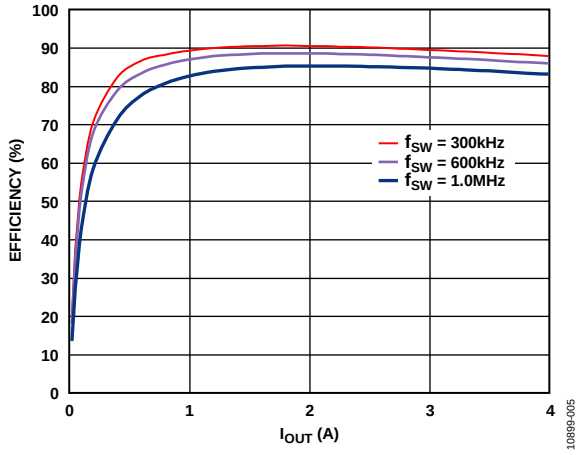


Figure 7. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

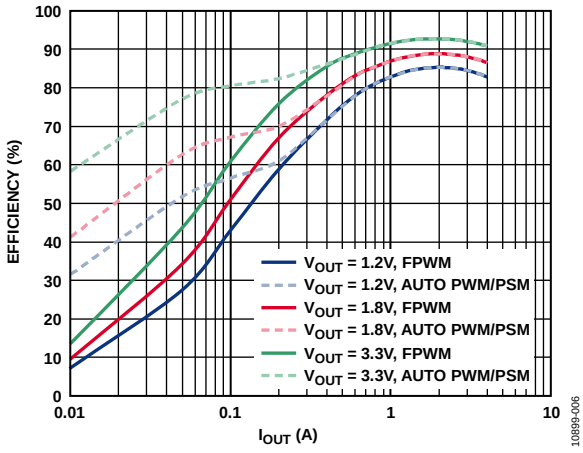


Figure 8. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

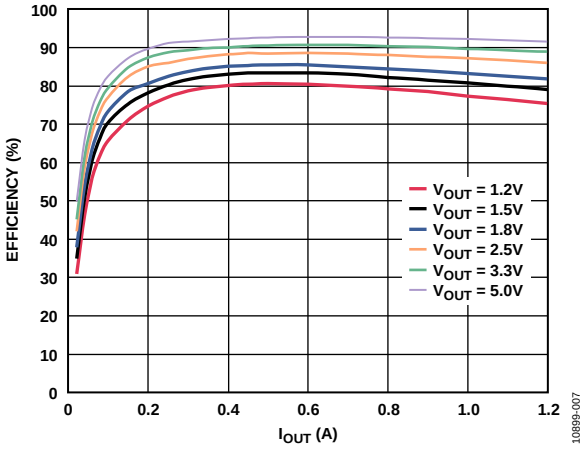


Figure 9. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

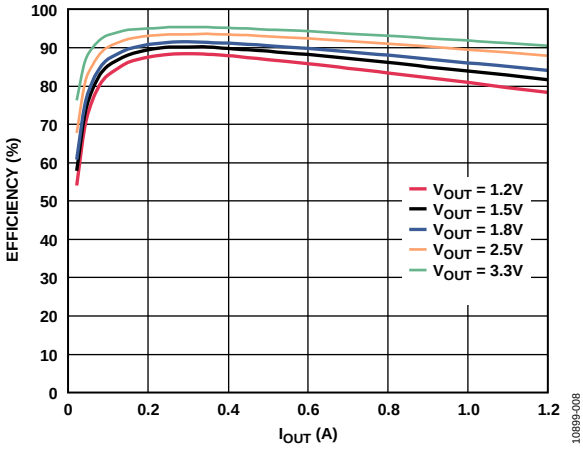


Figure 10. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

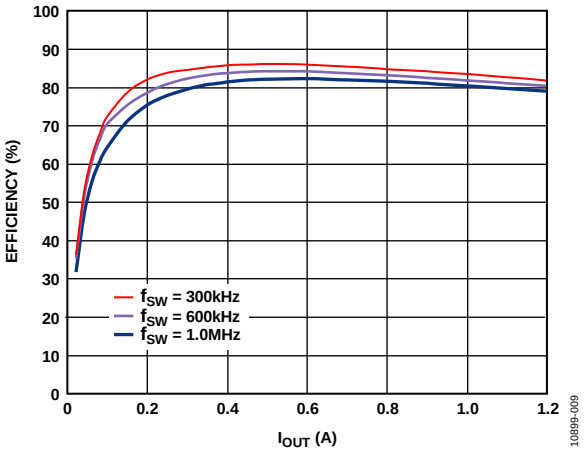


Figure 11. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

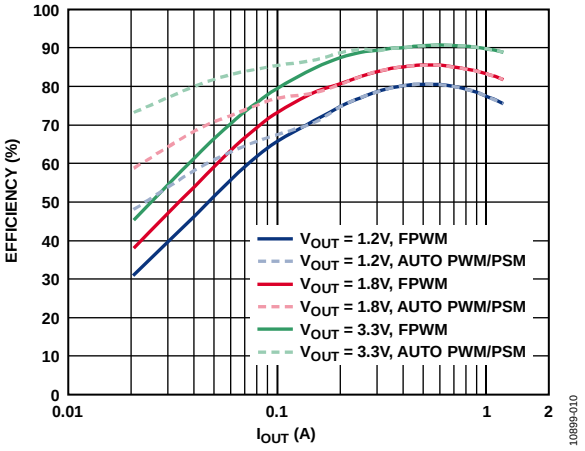


Figure 12. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and and Automatic PWM/PSM Modes

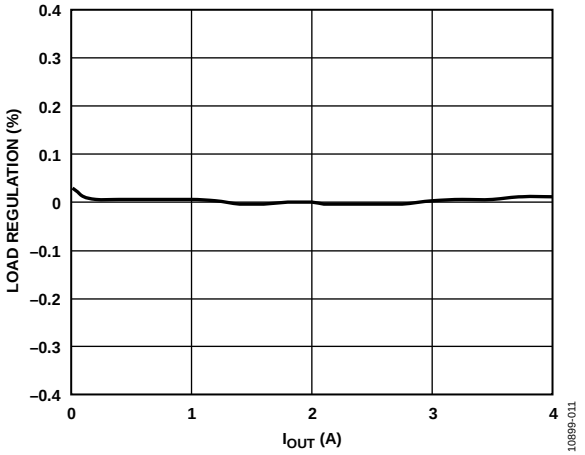


Figure 13. Channel 1 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

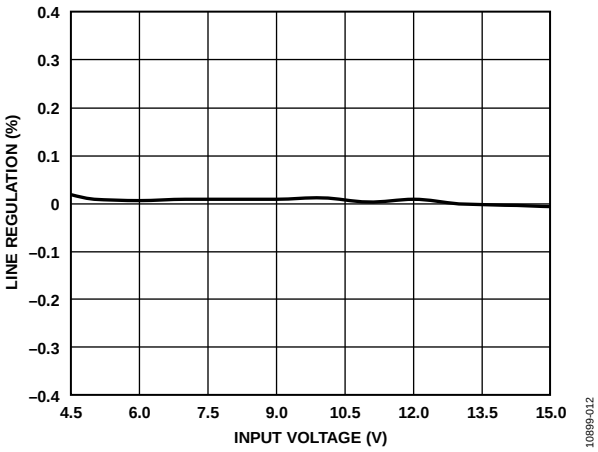


Figure 14. Channel 1 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, FPWM Mode

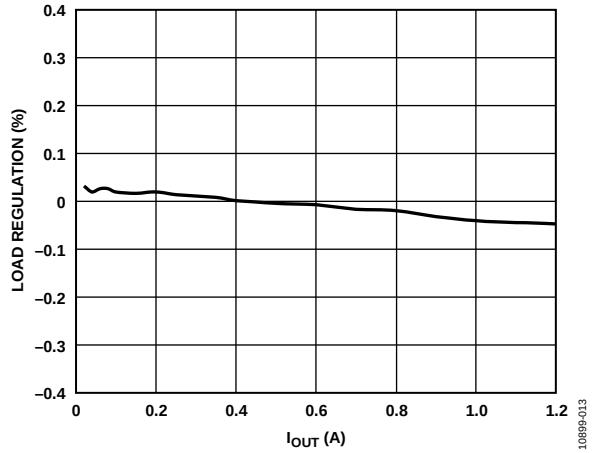


Figure 15. Channel 3 Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, FPWM Mode

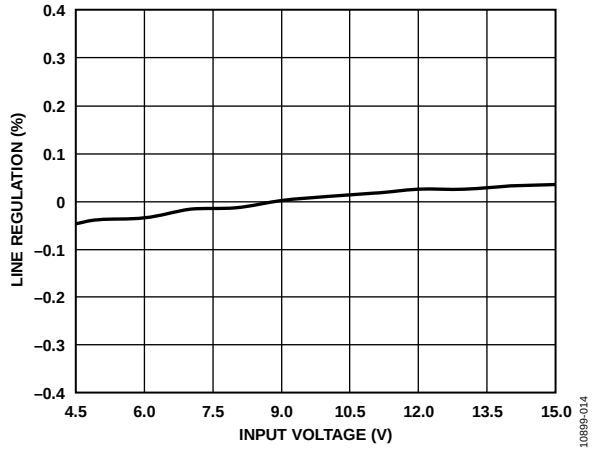


Figure 16. Channel 3 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 1 A, f_{SW} = 600 kHz, FPWM Mode

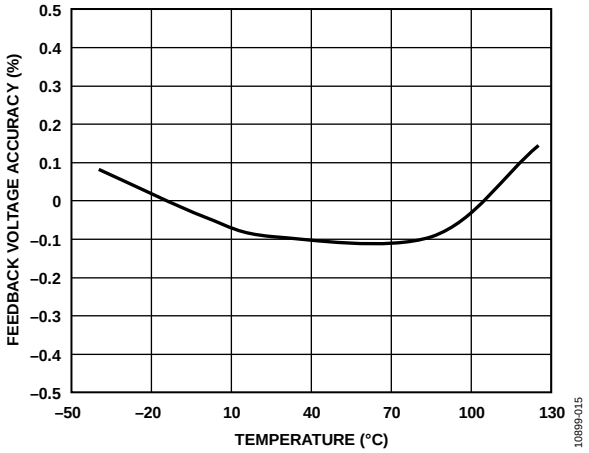


Figure 17. 0.8 V Feedback Voltage Accuracy vs. Temperature for Channel 1, Adjustable Output Model

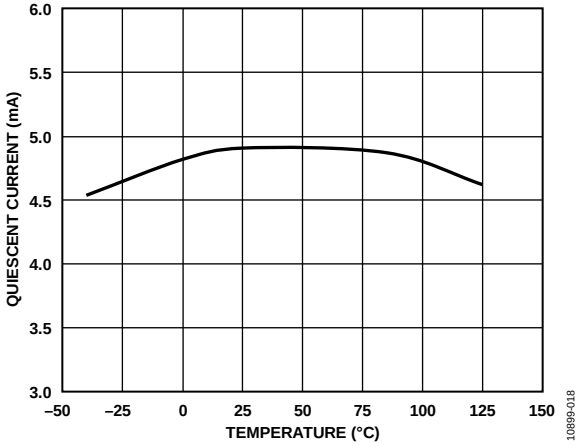


Figure 20. Quescient Current vs. Temperature (Includes PVIN1, PVIN2, PVIN3, and PVIN4)

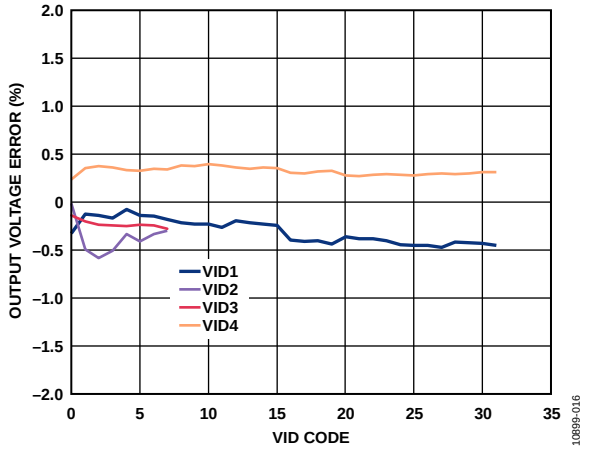


Figure 18. Output Voltage Error vs. VID Code, Adjustable Output Model

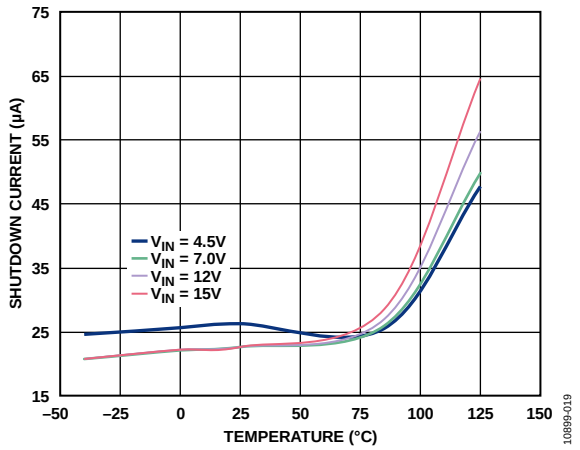


Figure 21. Shutdown Current vs. Temperature (EN1, EN2, EN3, EN4, and EN5 Low)

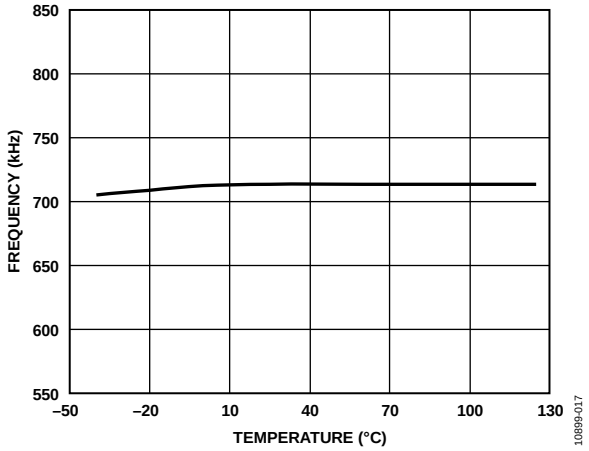


Figure 19. Frequency vs. Temperature, V_{IN} = 12 V

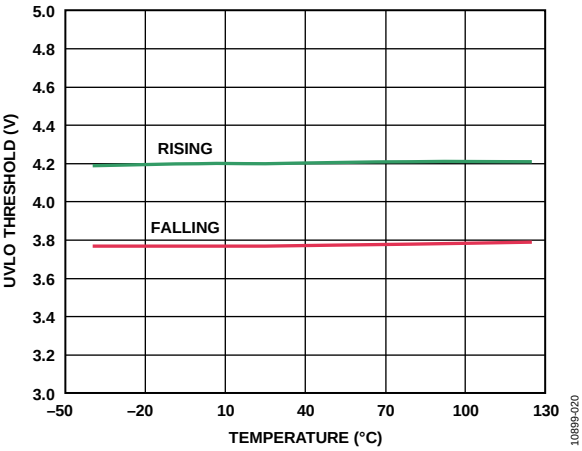


Figure 22. UVLO Threshold vs. Temperature

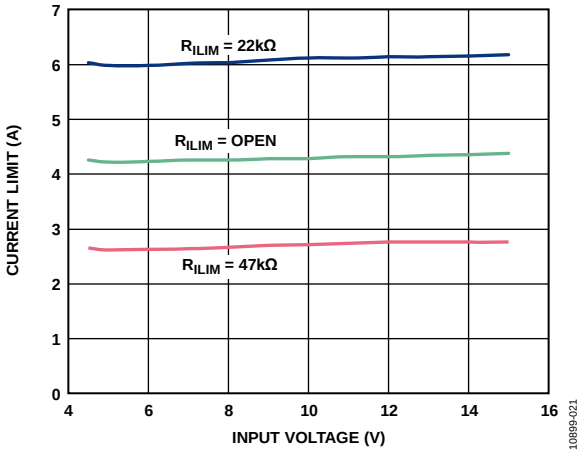


Figure 23. Channel 1/Channel 2 Current Limit vs. Input Voltage

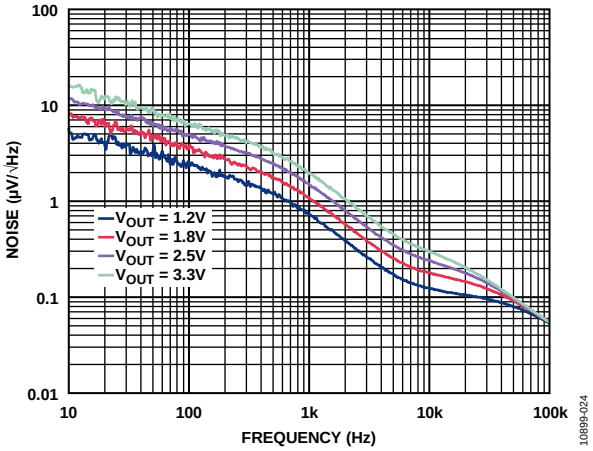


Figure 26. Channel 5 (LDO Regulator) Output Noise Spectrum, V_{IN} = 5 V, C_{OUT} = 1 μF, I_{OUT} = 10 mA

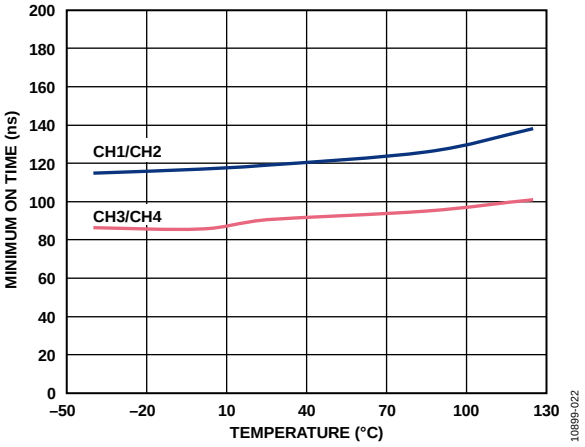


Figure 24. Minimum On Time vs. Temperature

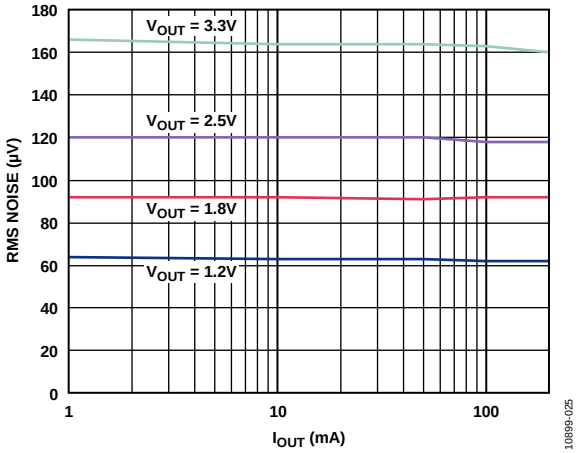


Figure 27. Channel 5 (LDO Regulator) Output Noise vs. Output Load, V_{IN} = 5 V, C_{OUT} = 1 μF

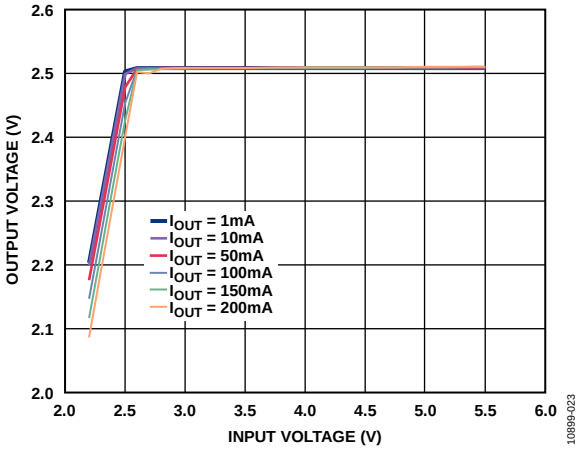


Figure 25. Channel 5 (LDO Regulator) Line Regulation over Output Load

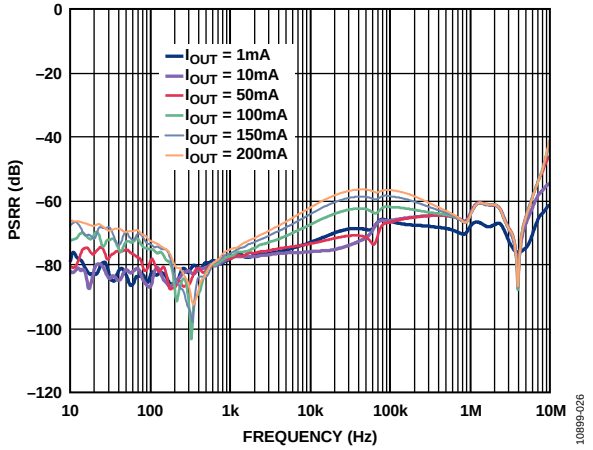


Figure 28. Channel 5 (LDO Regulator) PSRR over Output Load, V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

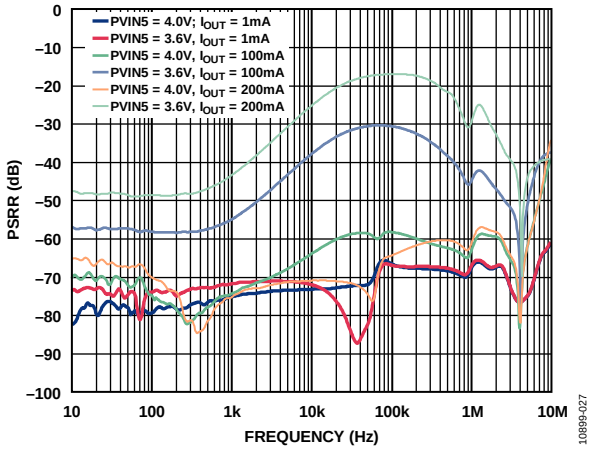


Figure 29. Channel 5 (LDO Regulator) PSRR over Various Loads and Dropout Voltages, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

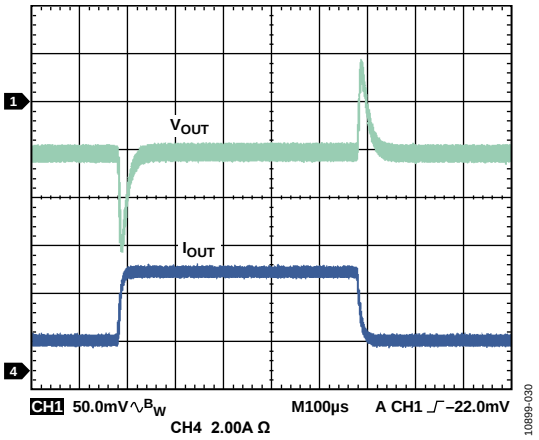


Figure 32. Channel 1/Channel 2 Load Transient, 1 A to 4 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 2.2 µH, C_{OUT} = 47 µF × 2

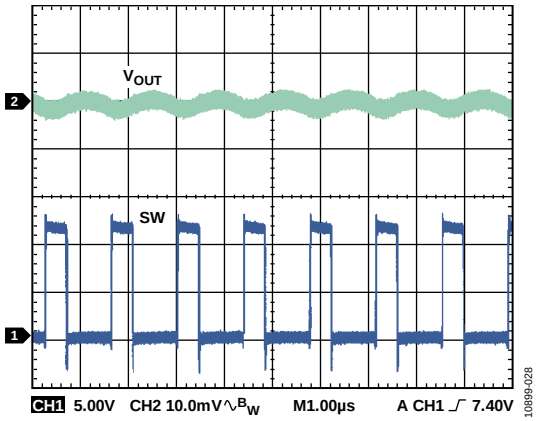


Figure 30. Steady State Waveform at Heavy Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, FPWM Mode

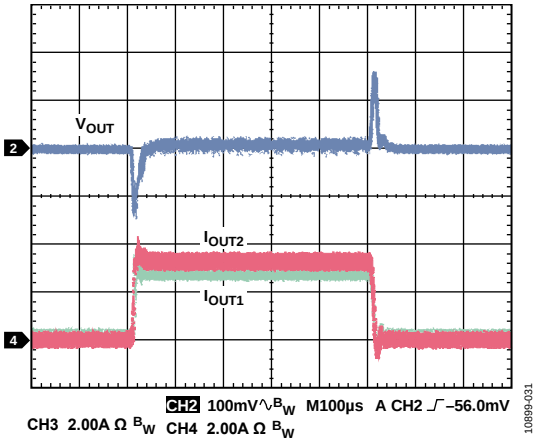


Figure 33. Load Transient, Channel 1/Channel 2 Parallel Output, 0 A to 6 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 4

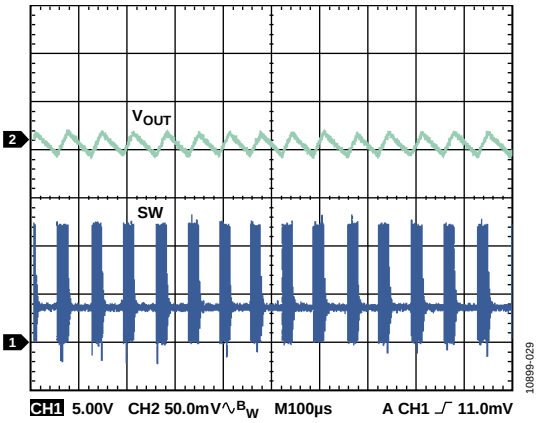


Figure 31. Steady State Waveform at Light Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 30 mA, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, Automatic PWM/PSM Mode

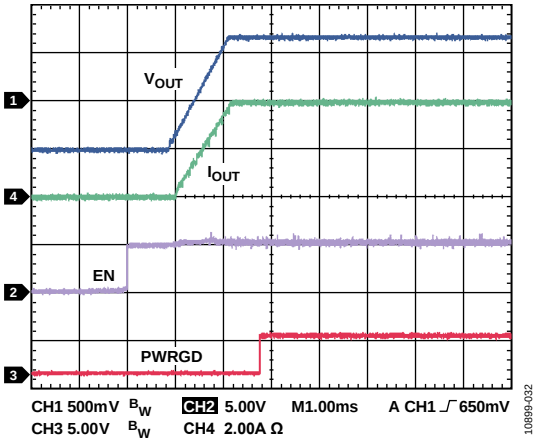


Figure 34. Channel 1/Channel 2 Soft Start with 4 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

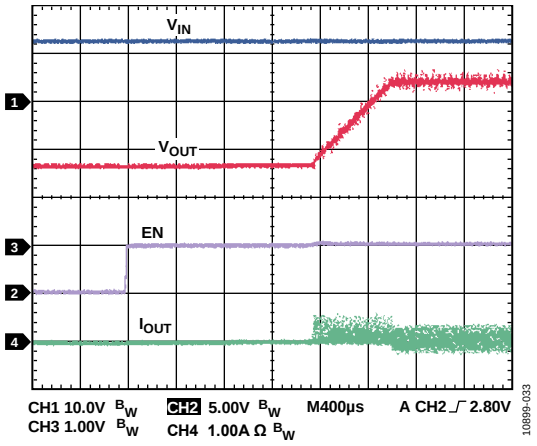


Figure 35. Startup with Precharged Output, V_{IN} = 12 V, V_{OUT} = 3.3 V

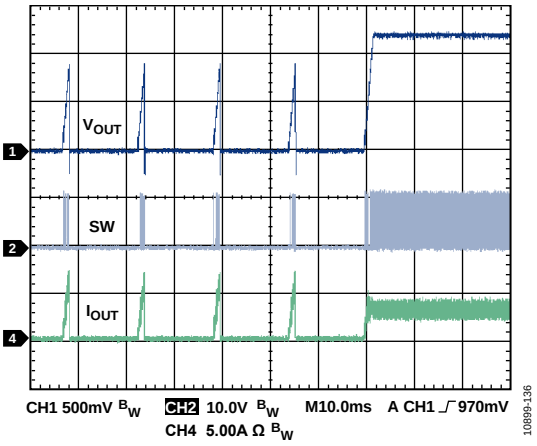


Figure 38. Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

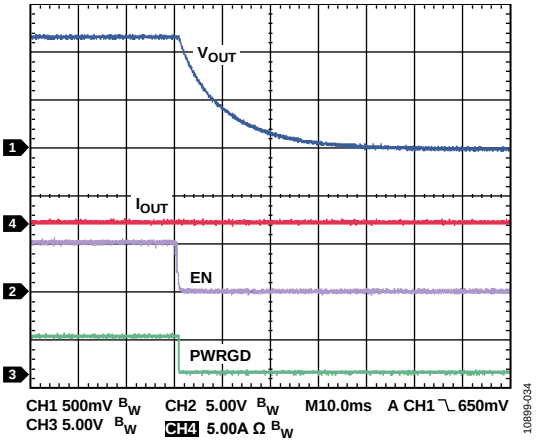


Figure 36. Channel 1/Channel 2 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

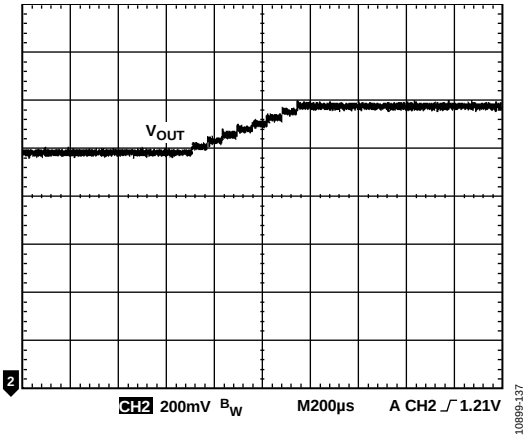


Figure 39. Channel 1 Dynamic Voltage Scaling (DVS) from 1.1 V to 1.3 V, 62.5 µs Interval, V_{IN} = 12 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

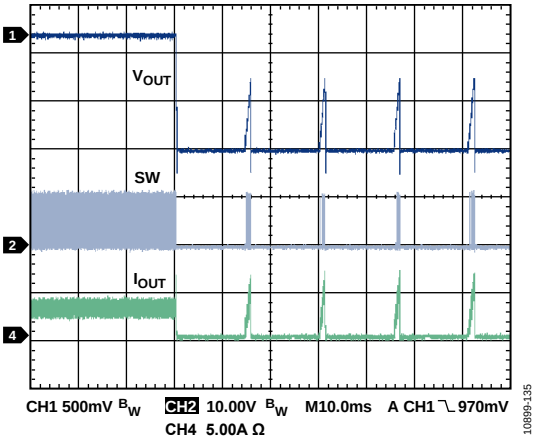


Figure 37. Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

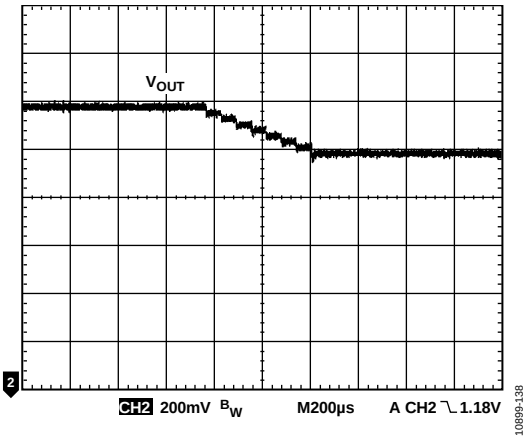


Figure 40. Channel 1 Dynamic Voltage Scaling (DVS) from 1.3 V to 1.1 V, 62.5 µs Interval, V_{IN} = 12 V, I_{OUT} = 4 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2

THEORY OF OPERATION

The ADP5050 is a micropower management unit that combines four high performance buck regulators with a 200 mA low dropout (LDO) regulator in a 48-lead LFCSP package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages up to 15 V with no pre-regulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

PWM Mode

In pulse-width modulation (PWM) mode, the buck regulators in the ADP5050 operate at a fixed frequency; this frequency is set by an internal oscillator that is programmed by the RT pin. At the start of each oscillator cycle, the high-side MOSFET turns on and sends a positive voltage across the inductor. The inductor current increases until the current-sense signal exceeds the peak inductor current threshold that turns off the high-side MOSFET; this threshold is set by the error amplifier output.

During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle. The buck regulators in the ADP5050 regulate the output voltage by adjusting the peak inductor current threshold.

PSM Mode

To achieve higher efficiency, the buck regulators in the ADP5050 smoothly transition to variable frequency power save mode (PSM) operation when the output load falls below the PSM current threshold. When the output voltage falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET turns off, and the output capacitor supplies all the output current.

The PSM comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM operation is larger than the ripple in the forced PWM mode of operation under light load conditions.

Forced PWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in PWM mode using the SYNC/MODE pin and the I²C interface. In forced PWM (FPWM) mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In PWM mode, efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5050 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin and the I²C interface. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation; in PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the output current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

The user can alternate between forced PWM (FPWM) mode and automatic PWM/PSM mode during operation. The flexible configuration capability during operation of the device enables efficient power management.

When a logic high level is applied to the SYNC/MODE pin (or when SYNC/MODE is configured as a clock input or output), the operational mode of each channel is set by the PSMx_ON bit in Register 6. A value of 0 for the PSMx_ON bit configures the channel for forced PWM mode; a value of 1 configures the channel for automatic PWM/PSM mode.

When a logic low level is applied to the SYNC/MODE pin, the operational mode of all four buck regulators is automatic PWM/PSM mode, and the settings of the PSMx_ON bits in Register 6 are ignored.

Table 9 describes the function of the SYNC/MODE pin in setting the operational mode of the device.

Table 9. Configuring the Mode of Operation Using the SYNC/MODE Pin

SYNC/MODE Pin	Mode of Operation for Each Channel
High	Specified by the PSMx_ON bit setting in Register 6 (0 = forced PWM mode; 1 = automatic PWM/PSM mode)
Clock Input/Output	Specified by the PSMx_ON bit setting in Register 6 (0 = forced PWM mode; 1 = automatic PWM/PSM mode)
Low	Automatic PWM/PSM mode (PSMx_ON bit settings in Register 6 are ignored)

For example, with the SYNC/MODE pin high, write 1 to the PSM4_ON bit in Register 6 to configure automatic PWM/PSM mode operation for Channel 4, and write 0 to the PSM1_ON, PSM2_ON, and PSM3_ON bits to configure forced PWM mode for Channel 1, Channel 2, and Channel 3.

ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The ADP5050 provides adjustable and fixed output voltage settings via the I²C interface or factory fuse. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage (0.8 V for Channel 1 to Channel 4, and 0.5 V for Channel 5).

For the fixed output settings, the feedback resistor divider is built into the ADP5050, and the feedback pin (FBx) must be tied directly to the output. Each buck regulator channel can be programmed for a specific output voltage range using the VIDx bits in Register 2 to Register 4. Table 10 lists the fixed output voltage ranges configured by the VIDx bits.

Table 10. Fixed Output Voltage Ranges Set by the VIDx Bits

Channel	Fixed Output Voltage Range Set by the VIDx Bits
Channel 1	0.85 V to 1.6 V in 25 mV steps
Channel 2	3.3 V to 5.0 V in 300 mV or 200 mV steps
Channel 3	1.2 V to 1.8 V in 100 mV steps
Channel 4	2.5 V to 5.5 V in 100 mV steps

The output range can also be programmed by factory fuse. If a different output voltage range is required, contact your local Analog Devices, Inc., sales or distribution representative.

DYNAMIC VOLTAGE SCALING (DVS)

The ADP5050 provides a dynamic voltage scaling (DVS) function for Channel 1 and Channel 4; these outputs can be programmed in real time via the I²C interface (Register 5, DVS_CFG). The DVS_CFG register is used to enable DVS and to set the step interval during the transition (see Table 29).

It is recommended that the user enable the DVS function before setting the output voltage for Channel 1 or Channel 4. (The output voltage for Channel 1 is set using the VID1 bits in Register 2; the output voltage for Channel 4 is set using the VID4 bits in Register 4.) If DVS is enabled after the VID value is set, the output voltage changes rapidly to the next target voltage, which can result in problems such as a PWRGD failure or OVP and OCP events. Figure 41 shows the dynamic voltage scaling function.

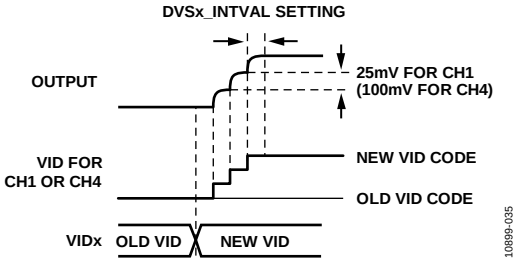


Figure 41. Dynamic Voltage Scaling

During the DVS transition period, the regulator is forced into PWM mode operation, and OVP latch-off, SCP latch-off, and hiccup protection are masked.

INTERNAL REGULATORS (VREG AND VDD)

The internal VREG regulator in the ADP5050 provides a stable 5.1 V power supply for the bias voltage of the MOSFET drivers. The internal VDD regulator in the ADP5050 provides a stable 3.3 V power supply for internal control circuits. Connect a 1.0 µF ceramic capacitor between VREG and ground, and connect another 1.0 µF ceramic capacitor between VDD and ground. The internal VREG and VDD regulators are active as long as PVIN1 is available.

The internal VREG regulator can provide a total load of 95 mA including the MOSFET driving current, and it can be used as an always alive 5.1 V power supply for a small system current demand. The current-limit circuit is included in the VREG regulator to protect the circuit when the part is heavily loaded.

The VDD regulator is for internal circuit use and is not recommended for other purposes.

SEPARATE SUPPLY APPLICATIONS

The ADP5050 supports separate input voltages for the four buck regulators. This means that the input voltages for the four buck regulators can be connected to different supply voltages.

The PVIN1 voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans to use separate supply voltages for the buck regulators, the PVIN1 voltage must be above the UVLO threshold before the other channels begin to operate.

Precision enabling can be used to monitor the PVIN1 voltage and to delay the startup of the outputs to ensure that PVIN1 is high enough to support the outputs in regulation. For more information, see the Precision Enabling section.

The ADP5050 supports cascading supply operation for the four buck regulators. As shown in Figure 42, PVIN2, PVIN3, and PVIN4 are powered from the Channel 1 output. In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2, PVIN3, and PVIN4.

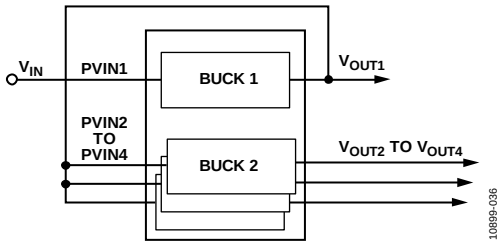


Figure 42. Cascading Supply Application

LOW-SIDE DEVICE SELECTION

The buck regulators in Channel 1 and Channel 2 integrate 4 A high-side power MOSFETs and low-side MOSFET drivers. The N-channel MOSFETs selected for use with the ADP5050 must be able to work with the synchronized buck regulators. In general, a low R_{DSON} N-channel MOSFET can be used to achieve higher efficiency; dual MOSFETs in one package (for both Channel 1 and Channel 2) are recommended to save space on the PCB. For more information, see the Low-Side Power Device Selection section.

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5050 has an integrated bootstrap regulator. The bootstrap regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5050 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 250 Ω for Channel 1 to Channel 4.

The discharge switch function can be enabled or disabled for each channel by factory fuse or by using the I²C interface (Register 6, OPT_CFG).

PRECISION ENABLING

The ADP5050 has an enable control pin for each regulator, including the LDO regulator. The enable control pin (ENx) features a precision enable circuit with a 0.8 V reference voltage. When the voltage at the ENx pin is greater than 0.8 V, the regulator is enabled. When the voltage at the ENx pin falls below 0.725 V, the regulator is disabled. An internal 1 MΩ pull-down resistor prevents errors if the ENx pin is left floating.

The precision enable threshold voltage allows easy sequencing of channels within the part, as well as sequencing between the ADP5050 and other input/output supplies. The ENx pin can also be used as a programmable UVLO input using a resistor divider (see Figure 43). For more information, see the Programming the UVLO Input section.

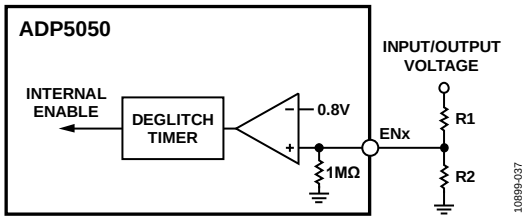


Figure 43. Precision Enable Diagram for One Channel

In addition to the ENx pins, the I²C interface (Register 1, PCTRL) can also be used to enable and disable each channel. The on/off status of a channel is controlled by the I²C enable bit for the channel (CHx_ON) and the external hardware enable pin for the channel (logical AND).

The default value of the I²C enable bit (CHx_ON = 1) specifies that the channel enable is controlled by the external hardware enable pin. Pulling the external ENx pin low resets the channel and forces the corresponding CHx_ON bit to the default value, 1, to support another startup when the external ENx pin is pulled high again.

OSCILLATOR

The switching frequency (f_{SW}) of the ADP5050 can be set to a value from 250 kHz to 1.4 MHz by connecting a resistor from the RT pin to ground. The value of the RT resistor can be calculated as follows:

$$R_{RT}\ (\text{k}\Omega) = [14{,}822/f_{SW}\ (\text{kHz})]^{1.081}$$

Figure 44 shows the typical relationship between the switching frequency (f_{SW}) and the RT resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and solution size.

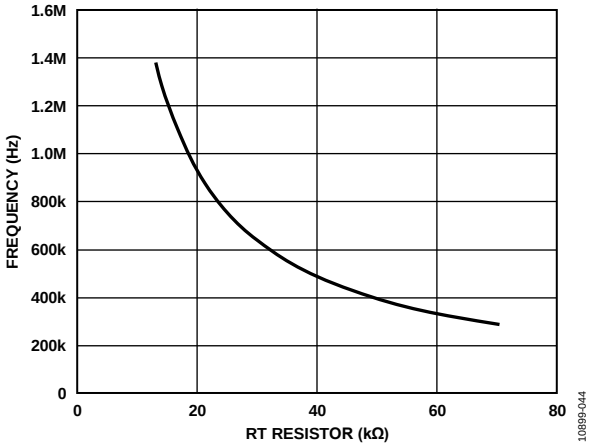


Figure 44. Switching Frequency vs. RT Resistor

For Channel 1 and Channel 3, the frequency can be set to half the master switching frequency set by the RT pin. This setting is configured using Register 8 (Bit 7 for Channel 3, and Bit 6 for Channel 1). If the master switching frequency is less than 250 kHz, this halving of the frequency for Channel 1 or Channel 3 is not recommended.

Phase Shift

By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180° (see Figure 45). This value provides the benefits of out-of-phase operation by reducing the input ripple current and lowering the ground noise.

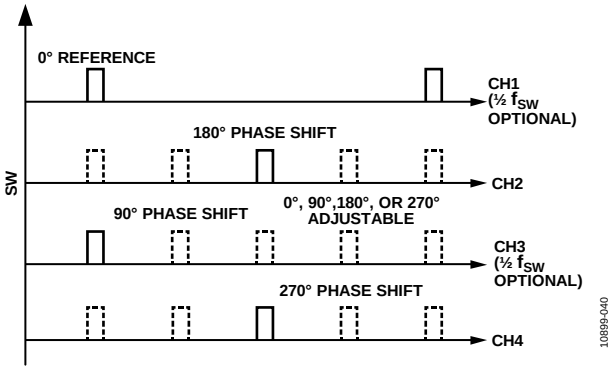


Figure 45. Phase Shift Diagram, Four Buck Regulators

For Channel 2 to Channel 4, the phase shift with respect to Channel 1 can be set to 0°, 90°, 180°, or 270° using Register 8, SW_CFG (see Figure 46). When parallel operation of Channel 1 and Channel 2 is configured, the switching frequency of Channel 2 is locked to a 180° phase shift with respect to Channel 1.

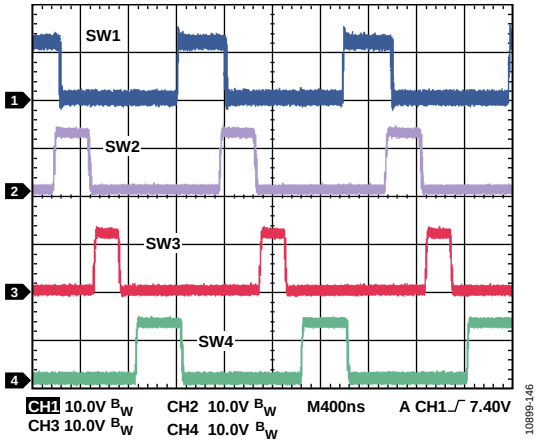


Figure 46. I²C Configurable 90° Phase Shift Waveforms, Four Buck Regulators

SYNCHRONIZATION INPUT/OUTPUT

The switching frequency of the ADP5050 can be synchronized to an external clock with a frequency range from 250 kHz to 1.4 MHz. The ADP5050 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization; the suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output by factory fuse or via the I²C interface (Register 10, HICCUP_CFG). A positive clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency set by the RT pin. There is a short delay time (approximately 15% of t_{SW}) from the generated synchronization clock to the Channel 1 switching node.

Figure 47 shows two ADP5050 devices configured for frequency synchronization mode: one ADP5050 device is configured as the clock output to synchronize another ADP5050 device. It is recommended that a 100 kΩ pull-up resistor be used to prevent logic errors when the SYNC/MODE pin is left floating.

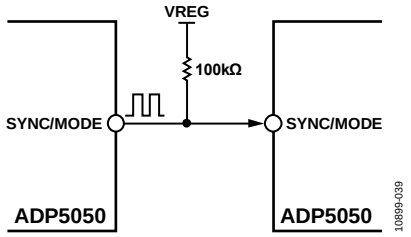


Figure 47. Two ADP5050 Devices Configured for Synchronization Mode

In the configuration shown in Figure 47, the phase shift between Channel 1 of the first ADP5050 device and Channel 1 of the second ADP5050 device is 0° (see Figure 48).

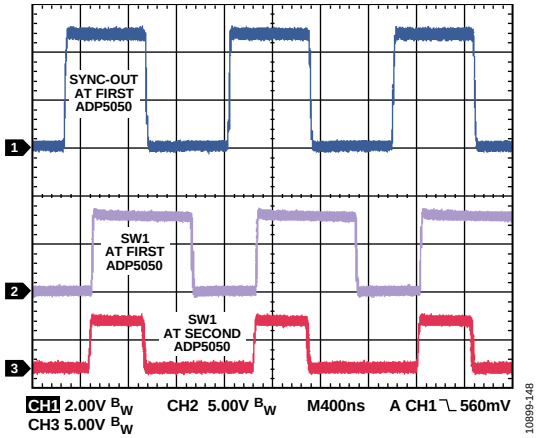


Figure 48. Waveforms of Two ADP5050 Devices Operating in Synchronization Mode

SOFT START

The buck regulators in the ADP5050 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 2 ms for each buck regulator when the SS12 and SS34 pins are tied to VREG.

To set the soft start time to a value of 2 ms, 4 ms, or 8 ms, connect a resistor divider from the SS12 or SS34 pin to the VREG pin and ground (see Figure 49). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor.

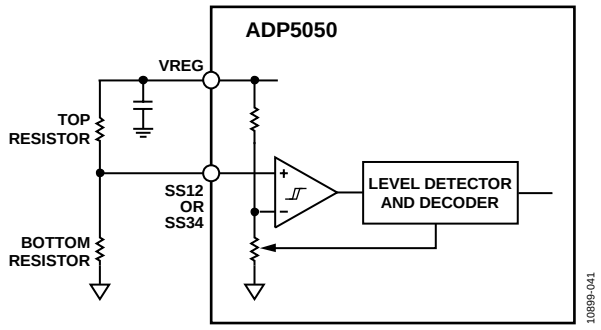


Figure 49. Level Detector Circuit for Soft Start

The SS12 pin can be used to program the soft start time and parallel operation for Channel 1 and Channel 2. The SS34 pin can be used to program the soft start time for Channel 3 and Channel 4. Table 11 provides the values of the resistors needed to set the soft start time.

Table 11. Soft Start Time Set by the SS12 and SS34 Pins

		Soft Start Time		Soft Start Time	
R_{TOP} (kΩ)	R_{BOT} (kΩ)	Channel 1	Channel 2	Channel 3	Channel 4
0	N/A	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A	0	8 ms	8 ms	8 ms	8 ms

PARALLEL OPERATION

The ADP5050 supports two-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 8 A of current. To configure Channel 1 and Channel 2 as a two-phase single output in parallel operation, do the following (see Figure 50):

- Use the SS12 pin to select parallel operation as specified in Table 11.
- Leave the COMP2 pin open.
- Use the FB1 pin to set the output voltage.
- Connect the FB2 pin to ground (FB2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

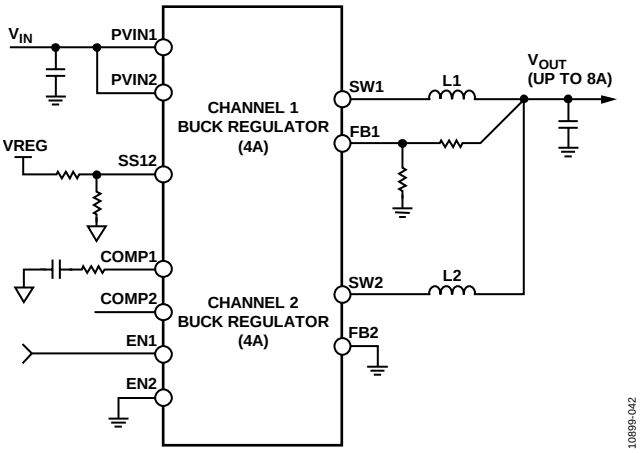


Figure 50. Parallel Operation for Channel 1 and Channel 2

When Channel 1 and Channel 2 are operated in the parallel configuration, configure the channels as follows:

- Set the input voltages and current-limit settings for Channel 1 and Channel 2 to the same values.
- Operate both channels in forced PWM mode.

Bits pertaining to Channel 2 in the configuration registers cannot be used. These bits include CH2_ON in Register 1, VID2 in Register 3, OVP2_ON and SCP2_ON in Register 7, PHASE2 in Register 8, and PWRG2 in Register 13.

Current balance in parallel configuration is well regulated by the internal control loop. Figure 51 shows the typical current balance matching in the parallel output configuration.

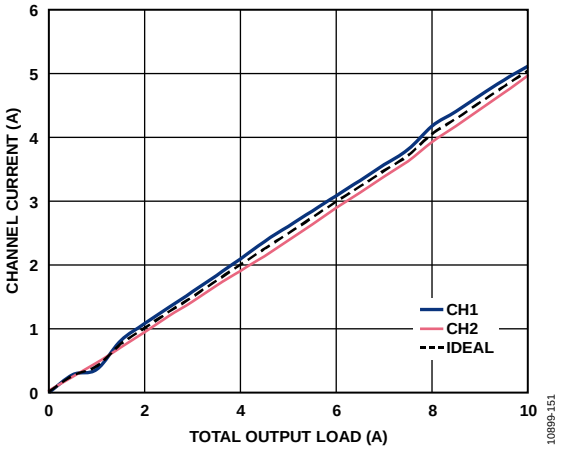


Figure 51. Current Balance in Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5050 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current—which discharges the output capacitor—until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

CURRENT-LIMIT PROTECTION

The buck regulators in the ADP5050 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows for the use of small size inductors for low current applications.

To configure the current-limit threshold for Channel 1, connect a resistor from the DL1 pin to ground; to configure the current-limit threshold for Channel 2, connect another resistor from the DL2 pin to ground. Table 12 lists the peak current-limit threshold settings for Channel 1 and Channel 2.

Table 12. Peak Current-Limit Threshold Settings for Channel 1 and Channel 2

R_{ILIM1} or R_{ILIM2}	Typical Peak Current-Limit Threshold
Floating	4.4 A
47 kΩ	2.63 A
22 kΩ	6.44 A

The buck regulators in the ADP5050 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET.

FREQUENCY FOLDBACK

The buck regulators in the ADP5050 include frequency foldback to prevent output current runaway when a hard short occurs on the output. Frequency foldback is implemented as follows:

- If the voltage at the FBx pin falls below half the target output voltage, the switching frequency is reduced by half.
- If the voltage at the FBx pin falls again to below one-fourth the target output voltage, the switching frequency is reduced to half its current value, that is, to one-fourth of f_{SW}.

The reduced switching frequency allows more time for the inductor current to decrease, but also increases the ripple current during peak current regulation. This results in a reduction in average current and prevents output current runaway.

Pulse Skip Mode Under Maximum Duty Cycle

Under maximum duty cycle conditions, frequency foldback maintains the output in regulation. If the maximum duty cycle is reached—for example, when the input voltage decreases—the PWM modulator skips every other PWM pulse, resulting in a switching frequency foldback of one-half. If the duty cycle increases further, the PWM modulator skips two of every three PWM pulses, resulting in a switching frequency foldback to one-third of the switching frequency. Frequency foldback increases the effective maximum duty cycle, thereby decreasing the dropout voltage between the input and output voltages.

HICCUP PROTECTION

The buck regulators in the ADP5050 include a hiccup mode for overcurrent protection (OCP). When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle.

When hiccup mode is active, the overcurrent fault counter is incremented. If the overcurrent fault counter reaches 15 and overflows (indicating a short-circuit condition), both the high-side and low-side MOSFETs are turned off. The buck regulator remains in hiccup mode for a period equal to seven soft start cycles and then attempts to restart from soft start. If the short-circuit fault has cleared, the regulator resumes normal operation; otherwise, it reenters hiccup mode after the soft start.

Hiccup protection is masked during the initial soft start cycle to enable startup of the buck regulator under heavy load conditions. Note that careful design and proper component selection are required to ensure that the buck regulator recovers from hiccup mode under heavy loads. The HICCUPx_OFF bits in Register 10 can be used to disable hiccup protection for each buck regulator. When hiccup protection is disabled, the frequency foldback feature is still available for overcurrent protection.

LATCH-OFF PROTECTION

The buck regulators in the ADP5050 have an optional latch-off mode to protect the device from serious problems such as short-circuit and overvoltage conditions. Latch-off mode can be enabled via the I^2C interface or by factory fuse.

Short-Circuit Latch-Off Mode

Short-circuit latch-off mode is enabled by factory fuse or by writing a 1 to the SCPx_ON bit in Register 7, LCH_CFG. When short-circuit latch-off mode is enabled and the protection circuit detects an overcurrent status after a soft start, the buck regulator enters hiccup mode and attempts to restart. If seven continuous restart attempts are made and the regulator remains in the fault condition, the regulator is shut down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply.

Figure 52 shows the short-circuit latch-off detection function.

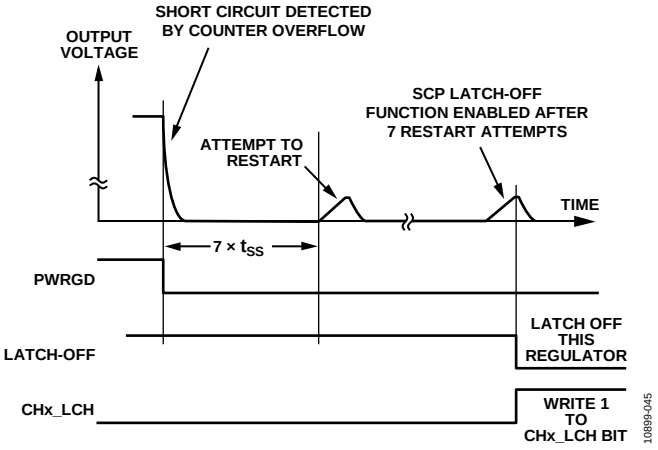


Figure 52. Short-Circuit Latch-Off Detection

The short-circuit latch-off status can be read from Register 12, LCH_STATUS. To clear the status bit, write a 1 to the bit (provided that the fault no longer persists). The status bit is latched until a 1 is written to the bit or the part is reset by the internal VDD power-on reset signal. Note that short-circuit latch-off mode does not work if hiccup protection is disabled.

Overvoltage Latch-Off Mode

Overvoltage latch-off mode is enabled by factory fuse or by writing a 1 to the OVPx_ON bit in Register 7, LCH_CFG. The overvoltage latch-off threshold is 124% of the nominal output voltage level. When the output voltage exceeds this threshold, the protection circuit detects the overvoltage status and the regulator shuts down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply.

Figure 53 shows the overvoltage latch-off detection function.

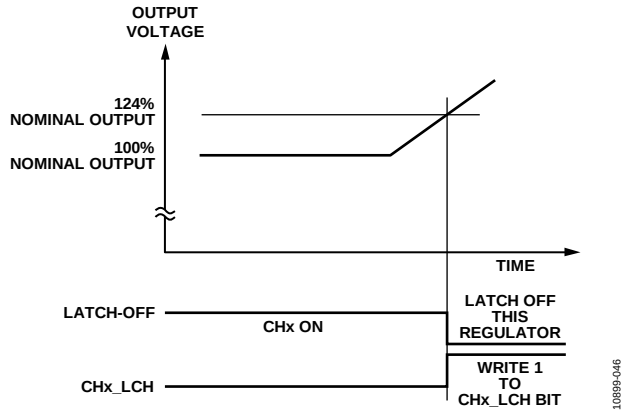


Figure 53. Overvoltage Latch-Off Detection

The overvoltage latch-off status can be read from Register 12, LCH_STATUS. To clear the status bit, write a 1 to the bit (provided that the fault no longer persists). The status bit is latched until a 1 is written to the bit or the part is reset by the internal VDD power-on reset signal.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry monitors the input voltage level of each buck regulator in the ADP5050. If any input voltage (PVINx pin) falls below 3.78 V (typical), the corresponding channel is turned off. After the input voltage rises above 4.2 V (typical), the soft start period is initiated, and the corresponding channel is enabled when the ENx pin is high.

Note that a UVLO condition on Channel 1 (PVIN1 pin) has a higher priority than a UVLO condition on other channels, which means that the PVIN1 supply must be available before other channels can be operated.

POWER-GOOD FUNCTION

The ADP5050 includes an open-drain power-good output (PWRGD pin) that becomes active high when the selected buck regulators are operating normally. By default, the PWRGD pin monitors the output voltage on Channel 1. Other channels can be configured to control the PWRGD pin when the ADP5050 is ordered.

The power-good status of each channel (PWRGx bit) can be read back via the I²C interface (Register 13, STATUS_RD). A value of 1 for the PWRGx bit indicates that the regulated output voltage of the buck regulator is above 90.5% (typical) of its nominal output. When the regulated output voltage of the buck regulator falls below 87.2% (typical) of its nominal output for a delay time greater than approximately 50 µs, the PWRGx bit is set to 0.

The output of the PWRGD pin is the logical AND of the internal unmasked PWRGx signals. An internal PWRGx signal must be high for a validation time of 1 ms before the PWRGD pin goes high; if one PWRGx signal fails, the PWRGD pin goes low with no delay. The channels that control the PWRGD pin (Channel 1 to Channel 4) are specified by factory fuse or by setting the appropriate bits in Register 11 (PWRGD_MASK) via the I²C interface.

INTERRUPT FUNCTION

The ADP5050 provides an interrupt output ($\overline{\text{INT}}$ pin) for fault conditions. During normal operation, the $\overline{\text{INT}}$ pin is pulled high (an external pull-up resistor should be used). When a fault condition occurs, the ADP5050 pulls the $\overline{\text{INT}}$ pin low to alert the I²C host processor that a fault condition has occurred.

Six interrupt sources can trigger the $\overline{\text{INT}}$ pin. By default, no interrupt sources are configured. To select one or more interrupt sources to trigger the $\overline{\text{INT}}$ pin, set the appropriate bits to 1 in Register 15, INT_MASK (see Table 49).

When the $\overline{\text{INT}}$ pin is triggered, one or more bits in Register 14 (Bits[5:0]) are set to 1. The fault condition that triggered the $\overline{\text{INT}}$ pin can be read from Register 14, INT_STATUS (see Table 13).

Table 13. Fault Conditions for Device Interrupt (Register 14)

Interrupt	Description
TEMP_INT	Junction temperature has exceeded the configured threshold (selected in Register 9)
LVIN_INT	PVIN1 voltage has fallen below the configured threshold (selected in Register 9)
PWRG4_INT	Power-good failure detected on Channel 4
PWRG3_INT	Power-good failure detected on Channel 3
PWRG2_INT	Power-good failure detected on Channel 2
PWRG1_INT	Power-good failure detected on Channel 1

To clear an interrupt, write a 1 to the appropriate bit in Register 14 (INT_STATUS), take all ENx pins low, or reset the part using the internal VDD power-on reset signal. Reading the interrupt or writing a 0 to the bit does not clear the interrupt.

THERMAL SHUTDOWN

If the ADP5050 junction temperature exceeds 150°C, the thermal shutdown circuit turns off the IC except for the internal linear regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5050 does not return to operation after thermal shutdown until the on-chip temperature falls below 135°C. When the part exits thermal shutdown, a soft start is initiated for each enabled channel.

The thermal shutdown status can be read via the I²C interface (Register 12, LCH_STATUS). When thermal shutdown is detected, the TSD_LCH bit (Bit 4) is set to 1. To clear the status bit, write a 1 to the bit (provided that the fault no longer persists). The status bit is latched until a 1 is written to the bit or the part is reset by the internal VDD power-on reset signal.

OVERHEAT DETECTION

In addition to thermal shutdown protection, the ADP5050 provides an overheat warning function, which compares the junction temperature with the specified overheat threshold: 105°, 115°, or 125°. The overheat threshold is configured in Register 9, TH_CFG. Unlike thermal shutdown, the overheat detection function sends a warning signal but does not shut down the part. When the junction temperature exceeds the overheat threshold, the status bit TEMP_INT in Register 14 is set to 1. The status bit is latched until a 1 is written to the bit, all ENx pins are taken low, or the part is reset by the internal VDD power-on reset signal.

The overheat detection function can be used to send a warning signal to the host processor. After the host processor detects the overheat warning signal, the processor can take action to prepare for a possible impending thermal shutdown.

Figure 54 shows the overheat warning function.

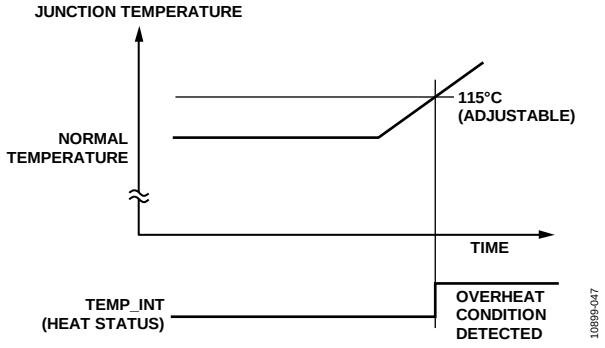


Figure 54. Overheat Warning Function

LOW INPUT VOLTAGE DETECTION

In addition to undervoltage lockout (UVLO), the ADP5050 provides a low input voltage detection circuit to monitor PVIN1; this circuit compares the input voltage with the specified voltage threshold. The voltage threshold can be set from 4.2 V to 11.2 V in steps of 0.5 V using Register 9, TH_CFG. Unlike UVLO shutdown, the low input voltage detection function sends a warning signal but does not shut down the part. When the PVIN1 input voltage falls below the threshold, the status bit LVIN_INT in Register 14 is set to 1. The status bit is latched until a 1 is written to the bit, all ENx pins are taken low, or the part is reset by the internal VDD power-on reset signal.

The low input voltage detection function can be used to send a warning signal to the host processor. After the host processor detects the low input voltage warning signal, the processor can take action to prepare for a possible impending UVLO shutdown.

Figure 55 shows the low input voltage warning function.

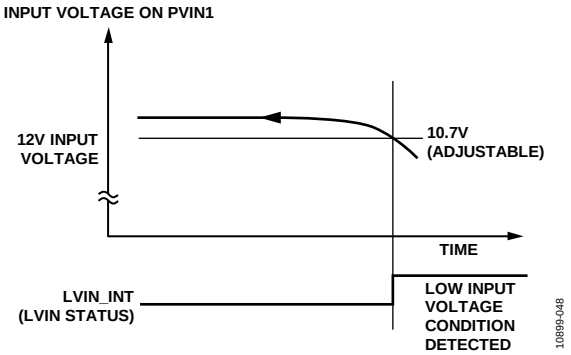


Figure 55. Low Input Voltage Warning Function (V_{IN} = 12 V)

LDO REGULATOR

The ADP5050 integrates a general-purpose LDO regulator with low quiescent current and low dropout voltage. The LDO regulator provides up to 200 mA of output current.

The LDO regulator operates with an input voltage of 1.7 V to 5.5 V. The wide supply range makes the regulator suitable for cascading configurations where the LDO supply voltage is provided from one of the buck regulators. The LDO output voltage is set using an external resistor divider (see Figure 56).

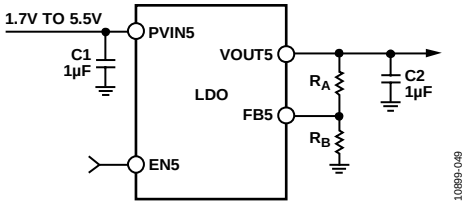


Figure 56. 200 mA LDO Regulator

The LDO regulator provides a high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response using small 1 µF ceramic input and output capacitors.

I²C INTERFACE

The ADP5050 includes an I²C-compatible serial interface for control of the power management blocks and for readback of system status (see Figure 57). The I²C interface operates at clock frequencies of up to 400 kHz.

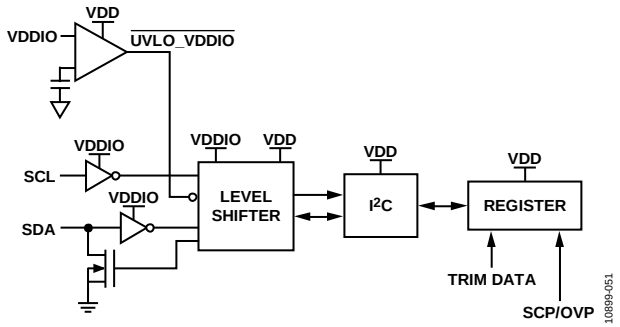


Figure 57. I²C Interface Block Diagram

Note that the ADP5050 does not respond to general calls. The ADP5050 accepts multiple masters, but if the device is in read mode, access is limited to one master until the data transmission is completed.

The I²C serial interface can be used to access the internal registers of the ADP5050. For complete information about the ADP5050 registers, see the Register Map section.

SDA AND SCL PINS

The ADP5050 has two dedicated I²C interface pins, SDA and SCL. SDA is an open-drain line for receiving and transmitting data. SCL is an input line for receiving the clock signal. Pull up these pins to the VDDIO supply using external resistors.

Serial data is transferred on the rising edge of SCL. The read data is generated at the SDA pin in read mode.

I²C ADDRESSES

The default 7-bit I²C chip address for the ADP5050 is 0x48 (1001000 in binary). A different I²C address can be configured using the optional A0 pin, which can replace the power-good functionality on Pin 20. (For information about obtaining an ADP5050 model with Pin 20 functioning as the A0 pin, contact your local Analog Devices sales or distribution representative.)

The A0 pin allows the use of two ADP5050 devices on the same I²C communication bus. Figure 58 shows two ADP5050 devices configured with different I²C addresses using the A0 pin.

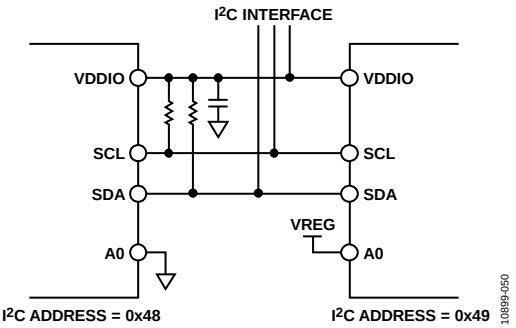


Figure 58. Two ADP5050 Devices Configured with Different I²C Addresses (A0 Function Replaces PWRGD Function on Pin 20)

SELF-CLEAR REGISTER BITS

Register 12 and Register 14 are status registers that contain self-clear register bits. These bit are cleared automatically when a 1 is written to the status bit. Therefore, it is not necessary to write a 0 to the status bit to clear it.

I²C INTERFACE TIMING DIAGRAMS

Figure 59 shows the timing diagram for the I²C write operation. Figure 60 shows the timing diagram for the I²C read operation.

The subaddress is used to select one of the user registers in the ADP5050. The ADP5050 sends data to and from the register specified by the subaddress.

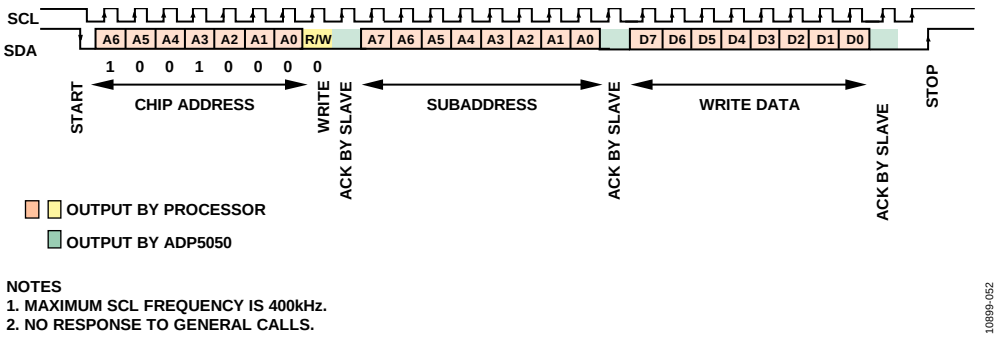


Figure 59. I²C Write to Register

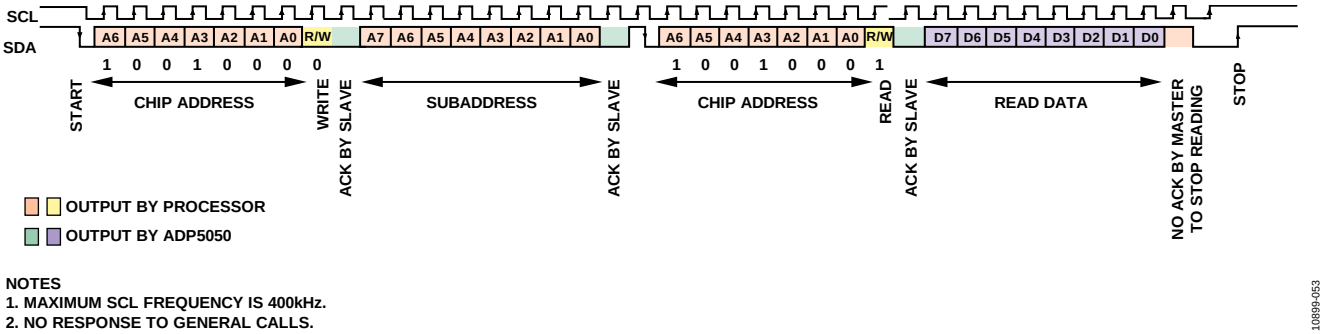


Figure 60. I²C Read from Register

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP5050 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and part count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/ADIsimPower; the user can request an unpopulated board through the tool.

PROGRAMMING THE ADJUSTABLE OUTPUT VOLTAGE

The output voltage of the ADP5050 is externally set by a resistive voltage divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to feedback bias current, ensure that the bottom resistor in the divider is not too large—a value of less than 50 kΩ is recommended.

The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
V_{OUT} is the output voltage.
V_{REF} is the feedback reference voltage: 0.8 V for Channel 1 to Channel 4 and 0.5 V for Channel 5.
R_{TOP} is the feedback resistor from V_{OUT} to FB.
R_{BOT} is the feedback resistor from FB to ground.

No resistor divider is required in the fixed output options. Each channel has VIDx bits to program the output voltage for a specific range (see Table 10). If a different fixed output voltage (default VID code) is required, contact your local Analog Devices sales or distribution representative.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, upper and lower limitations on the output voltage exist due to the minimum on time and the minimum off time.

The minimum output voltage for a given input voltage and switching frequency is limited by the minimum on time. The minimum on time for Channel 1 and Channel 2 is 117 ns (typical); the minimum on time for Channel 3 and Channel 4 is 90 ns (typical). The minimum on time increases at higher junction temperatures.

Note that in forced PWM mode, Channel 1 and Channel 2 can potentially exceed the nominal output voltage when the minimum on time limit is exceeded. Careful switching frequency selection is required to avoid this problem.

The minimum output voltage in continuous conduction mode (CCM) for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT_MIN} = V_{IN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MIN} \times t_{MIN_ON} \times f_{SW} - (R_{DSON2} + R_L) \times I_{OUT_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON1} is the on resistance of the high-side MOSFET.
R_{DSON2} is the on resistance of the low-side MOSFET.
I_{OUT_MIN} is the minimum output current.
R_L is the resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is limited by the minimum off time and the maximum duty cycle. Note that the frequency foldback feature helps to increase the effective maximum duty cycle by lowering the switching frequency, thereby decreasing the dropout voltage between the input and output voltages (see the Frequency Foldback section).

The maximum output voltage for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT_MAX} = V_{IN} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON1} - R_{DSON2}) \times I_{OUT_MAX} \times (1 - t_{MIN_OFF} \times f_{SW}) - (R_{DSON2} + R_L) \times I_{OUT_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
f_{SW} is the switching frequency.
R_{DSON1} is the on resistance of the high-side MOSFET.
R_{DSON2} is the on resistance of the low-side MOSFET.
I_{OUT_MAX} is the maximum output current.
R_L is the resistance of the output inductor.

As shown in Equation 1 and Equation 2, reducing the switching frequency eases the minimum on time and off time limitations.

CURRENT-LIMIT SETTING

The ADP5050 has three selectable current-limit thresholds for Channel 1 and Channel 2. Make sure that the selected current-limit value is larger than the peak current of the inductor, I_{PEAK}. See Table 12 for the current-limit configuration for Channel 1 and Channel 2.

SOFT START SETTING

The buck regulators in the ADP5050 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. To set the soft start time to a value of 2 ms, 4 ms, or 8 ms, connect a resistor divider from the SS12 or SS34 pin to the VREG pin and ground (see the Soft Start section).

INDUCTOR SELECTION

The inductor value is determined by the switching frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value yields faster transient response but degrades efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and better efficiency but results in slower transient response. Thus, a trade-off must be made between transient response and efficiency. As a guideline, the inductor ripple current, ΔI_L, is typically set to a value from 30% to 40% of the maximum load current. The inductor value can be calculated using the following equation:

$$L = [(V_{IN} - V_{OUT}) \times D]/(\Delta I_L \times f_{SW})$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.

The ADP5050 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%.

The peak inductor current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, make sure that the saturation current rating of the inductor is higher than the current-limit threshold of the buck regulator to prevent the inductor from becoming saturated.

The rms current of the inductor can be calculated using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 14 lists recommended inductors.

Table 14. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)	Size (mm)
Coilcraft	XFL4020-102	1.0	5.4	11	10.8	4 × 4
	XFL4020-222	2.2	3.7	8.0	21.35	4 × 4
	XFL4020-332	3.3	2.9	5.2	34.8	4 × 4
	XFL4020-472	4.7	2.7	5.0	52.2	4 × 4
	XAL4030-682	6.8	3.6	3.9	67.4	4 × 4
	XAL4040-103	10	3.0	3.1	84	4 × 4
	XAL6030-102	1.0	23	18	5.62	6 × 6
	XAL6030-222	2.2	15.9	10	12.7	6 × 6
	XAL6030-332	3.3	12.2	8.0	19.92	6 × 6
	XAL6060-472	4.7	10.5	11	14.4	6 × 6
	XAL6060-682	6.8	9.2	9.0	18.9	6 × 6
TOKO	FDV0530-1R0	1.0	11.2	9.1	9.4	6.2 × 5.8
	FDV0530-2R2	2.2	7.1	7.0	17.3	6.2 × 5.8
	FDV0530-3R3	3.3	5.5	5.3	29.6	6.2 × 5.8
	FDV0530-4R7	4.7	4.6	4.2	46.6	6.2 × 5.8

OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of the output voltage.

The output capacitance required to meet the undershoot (voltage droop) requirement can be calculated using the following equation:

$$C_{OUT_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT_UV}}$$

where:
K_{UV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, causing an overshoot of the output voltage.

The output capacitance required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT_OV})^2 - V_{OUT}^2}$$

where:
K_{OV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The output voltage ripple is determined by the ESR of the output capacitor and its capacitance value. Use the following equations to select a capacitor that can meet the output ripple requirements:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{\Delta I_L}$$

where:
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple requirements.

The voltage rating of the selected output capacitor must be greater than the output voltage. The minimum rms current rating of the output capacitor is determined by the following equation:

$$I_{C_{OUT}_rms} = \frac{\Delta I_L}{\sqrt{12}}$$

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. Use a ceramic capacitor and place it close to the PVINx pin. The loop composed of the input capacitor, the high-side NFET, and the low-side NFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. Make sure that the rms current rating of the input capacitor is larger than the following equation:

$$I_{C_{IN}_rms} = I_{OUT} \times \sqrt{D \times (1-D)}$$

where D is the duty cycle ($D = V_{OUT}/V_{IN}$).

LOW-SIDE POWER DEVICE SELECTION

Channel 1 and Channel 2 include integrated low-side MOSFET drivers, which can drive low-side N-channel MOSFETs (NFETs). The selection of the low-side N-channel MOSFET affects the performance of the buck regulator.

The selected MOSFET must meet the following requirements:

- Drain-to-source voltage (V_{DS}) must be higher than $1.2 \times V_{IN}$.
- Drain current (I_D) must be greater than $1.2 \times I_{LIMIT_MAX}$, where I_{LIMIT_MAX} is the selected maximum current-limit threshold.
- The selected MOSFET can be fully turned on at $V_{GS} = 4.5$ V.
- Total gate charge (Qg at $V_{GS} = 4.5$ V) must be less than 20 nC. Lower Qg characteristics provide higher efficiency.

When the high-side MOSFET is turned off, the low-side MOSFET supplies the inductor current. For low duty cycle applications, the low-side MOSFET supplies the current for most of the period. To achieve higher efficiency, it is important to select a MOSFET with low on resistance. The power conduction loss for the low-side MOSFET can be calculated using the following equation:

$$P_{FET_LOW} = I_{OUT}^2 \times R_{DSON} \times (1 - D)$$

where:
R_{DSON} is the on resistance of the low-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Table 15 lists recommended dual MOSFETs for various current-limit settings. Ensure that the MOSFET can handle thermal dissipation due to power loss.

Table 15. Recommended Dual MOSFETs

Vendor	Part No.	V_{DS} (V)	I_D (A)	R_{DSON} (mΩ)	Qg (nC)	Size (mm)
IR	IRFHM8363	30	10	20.4	6.7	3 × 3
	IRLHS6276	20	3.4	45	3.1	2 × 2
Fairchild	FDMA1024	20	5.0	54	5.2	2 × 2
	FDMB3900	25	7.0	33	11	3 × 2
	FDMB3800	30	4.8	51	4	3 × 2
	FDC6401	20	3.0	70	3.3	3 × 3
Vishay	Si7228DN	30	23	25	4.1	3 × 3
	Si7232DN	20	25	16.4	12	3 × 3
	Si7904BDN	20	6	30	9	3 × 3
	Si5906DU	30	6	40	8	3 × 2
	Si5908DC	20	5.9	40	5	3 × 2
	SiA906EDJ	20	4.5	46	3.5	2 × 2
AOS	AON7804	30	22	26	7.5	3 × 3
	AON7826	20	22	26	6	3 × 3
	AO6800	30	3.4	70	4.7	3 × 3
	AON2800	20	4.5	47	4.1	2 × 2

PROGRAMMING THE UVLO INPUT

The precision enable input can be used to program the UVLO threshold of the input voltage, as shown in Figure 43. To limit the degradation of the input voltage accuracy due to the internal 1 MΩ pull-down resistor tolerance, ensure that the bottom resistor in the divider is not too large—a value of less than 50 kΩ is recommended.

The precision turn-on threshold is 0.8 V. The resistive voltage divider for the programmable V_{IN} start-up voltage is calculated as follows:

$$V_{IN_STARTUP} = (0.8\ \text{nA} + (0.8\ \text{V}/R_{BOT_EN})) \times (R_{TOP_EN} + R_{BOT_EN})$$

where:
R_{TOP_EN} is the resistor from V_{IN} to EN.
R_{BOT_EN} is the resistor from EN to ground.

COMPENSATION COMPONENTS DESIGN

For the peak current-mode control architecture, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the output capacitor ESR. The control-to-output transfer function is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 10 A/V for Channel 1 or Channel 2, and 3.33 A/V for Channel 3 or Channel 4.
R is the load resistance.
R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

The ADP5050 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 61 shows the simplified peak current-mode control small signal circuit.

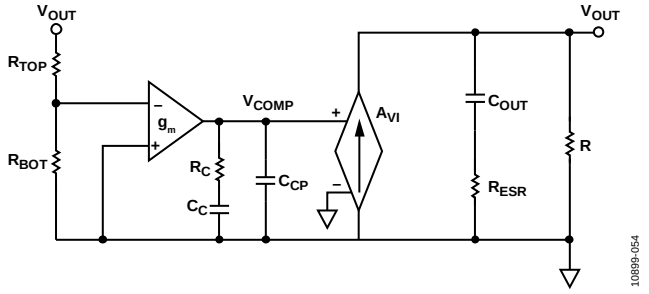


Figure 61. Simplified Peak Current-Mode Control Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero; R_C and the optional C_{CP} contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following guidelines show how to select the compensation components—R_C, C_C, and C_{CP}—for ceramic output capacitor applications.

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.8\text{V} \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole (f_P). Calculate C_C using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor. Calculate C_{CP} using the following equation:

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

POWER DISSIPATION

The total power dissipation in the ADP5050 simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3} + P_{BUCK4} + P_{LDO}$$

Buck Regulator Power Dissipation

The power dissipation (P_{LOSS}) for each buck regulator includes power switch conduction losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Power Switch Conduction Loss (P_{COND})

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches, each of which has its own internal on resistance (R_{DSON}).

Use the following equation to estimate the power switch conduction loss:

$$P_{COND} = (R_{DSON_HS} \times D + R_{DSON_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
R_{DSON_LS} is the on resistance of the low-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE_HS} + C_{GATE_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.
f_{SW} is the switching frequency.

Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source-to-drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

Thermal Shutdown

Channel 1 and Channel 2 store the value of the inductor current only during the on time of the internal high-side MOSFET. Therefore, a small amount of power (as well as a small amount of input rms current) is dissipated inside the ADP5050, which reduces thermal constraints.

However, when Channel 1 and Channel 2 are operating under maximum load with high ambient temperature and high duty cycle, the input rms current can become very large and cause the junction temperature to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the regulator enters thermal shutdown and recovers when the junction temperature falls below 135°C.

LDO Regulator Power Dissipation

The power dissipation of the LDO regulator is given by the following equation:

$$P_{LDO} = [(V_{IN} - V_{OUT}) \times I_{OUT}] + (V_{IN} \times I_{GND})$$

where:
V_{IN} and V_{OUT} are the input and output voltages of the LDO regulator.
I_{OUT} is the load current of the LDO regulator.
I_{GND} is the ground current of the LDO regulator.

Power dissipation due to the ground current is small in the ADP5050 and can be ignored.

JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 7).
P_D is the power dissipation in the package.

An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz. of copper, as specified in the JEDEC standard, whereas real-world applications may use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect the exposed pad to the ground plane with several vias.

DESIGN EXAMPLE

This section provides an example of the step-by-step design procedures and the external components required for Channel 1. Table 16 lists the design requirements for this example.

Table 16. Example Design Requirements for Channel 1

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V ± 5%
Output Voltage	V_{OUT1} = 1.2 V
Output Current	I_{OUT1} = 4 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 12 mV in CCM mode
Load Transient	±5% at 20% to 80% load transient, 1 A/µs

Although this example shows step-by-step design procedures for Channel 1, the procedures apply to all other buck regulator channels (Channel 2 to Channel 4).

SETTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency for the ADP5050 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5050 can be set to a value from 250 kHz to 1.4 MHz by connecting a resistor from the RT pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size. (For more information, see the Oscillator section.) However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 600 kHz is used to achieve a good combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz, use the following equation to calculate the resistor value, R_{RT}:

$$R_{RT}\,(\text{k}\Omega) = [14{,}822/f_{SW}\,(\text{kHz})]^{1.081}$$

Therefore, select standard resistor R_{RT} = 31.6 kΩ.

SETTING THE OUTPUT VOLTAGE

Select a 10 kΩ bottom resistor (R_{BOT}) and then calculate the top feedback resistor using the following equation:

$$R_{BOT} = R_{TOP} \times (V_{REF}/(V_{OUT} - V_{REF}))$$

where:
V_{REF} is 0.8 V for Channel 1.
V_{OUT} is the output voltage.

To set the output voltage to 1.2 V, choose the following resistor values: R_{TOP} = 4.99 kΩ, R_{BOT} = 10 kΩ.

SETTING THE CURRENT LIMIT

For 4 A output current operation, the typical peak current limit is 6.44 A. For this example, choose R_{ILIM1} = 22 kΩ (see Table 12). For more information, see the Current-Limit Protection section.

SELECTING THE INDUCTOR

The peak-to-peak inductor ripple current, ΔI_L, is set to 35% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = [(V_{IN} - V_{OUT}) \times D]/(\Delta I_L \times f_{SW})$$

where:
V_{IN} = 12 V.
V_{OUT} = 1.2 V.
D is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.1).
ΔI_L = 35% × 4 A = 1.4 A.
f_{SW} = 600 kHz.

The resulting value for L is 1.28 µH. The closest standard inductor value is 1.5 µH; therefore, the inductor ripple current, ΔI_L, is 1.2 A.

The peak inductor current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 4.6 A.

The rms current of the inductor can be calculated using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^{\,2} + \frac{\Delta I_L^{\,2}}{12}}$$

The rms current of the inductor is approximately 4.02 A.

Therefore, an inductor with a minimum rms current rating of 4.02 A and a minimum saturation current rating of 4.6 A is required. However, to prevent the inductor from reaching its saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 7.48 A, for reliable operation.

Based on these requirements and recommendations, the TOKO FDV0530-1R5, with a DCR of 13.5 mΩ, is selected for this design.

SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance:

$$C_{OUT_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, C_{OUT_RIPPLE}, is 20.8 µF, and the calculated R_{ESR} is 10 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT_UV}}$$

$$C_{OUT_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT_OV})^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, $C_{OUT_OV} = 117$ µF and $C_{OUT_UV} = 13.3$ µF.

The ESR of the output capacitor must be less than 13.3 mΩ, and the output capacitance must be greater than 117 µF. It is recommended that three ceramic capacitors be used (47 µF, X5R, 6.3 V), such as the GRM21BR60J476ME15 from Murata with an ESR of 2 mΩ.

SELECTING THE LOW-SIDE MOSFET

A low R_{DSON} N-channel MOSFET must be selected for high efficiency solutions. The MOSFET breakdown voltage (V_{DS}) must be greater than 1.2 × V_{IN}, and the drain current must be greater than 1.2 × I_{LIMIT_MAX}.

It is recommended that a 20 V, dual N-channel MOSFET—such as the Si7232DN from Vishay—be used for both Channel 1 and Channel 2. The R_{DSON} of the Si7232DN at 4.5 V driver voltage is 16.4 mΩ, and the total gate charge is 12 nC.

DESIGNING THE COMPENSATION NETWORK

For better load transient and stability performance, set the cross frequency, f_C, to $f_{SW}/10$. In this example, f_{SW} is set to 600 kHz; therefore, f_C is set to 60 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 40 µF.

$$R_C = \frac{2 \times \pi \times 1.2\,\text{V} \times 3 \times 40\,\mu\text{F} \times 60\,\text{kHz}}{0.8\,\text{V} \times 470\,\mu\text{S} \times 10\,\text{A/V}} = 14.4\,\text{k}\Omega$$

$$C_C = \frac{(0.3\,\Omega + 0.001\,\Omega) \times 3 \times 40\,\mu\text{F}}{14.4\,\text{k}\Omega} = 2.51\,\text{nF}$$

$$C_{CP} = \frac{0.001\,\Omega \times 3 \times 40\,\mu\text{F}}{14.4\,\text{k}\Omega} = 8.3\,\text{pF}$$

Choose standard components: R_C = 15 kΩ and C_C = 2.7 nF. C_{CP} is optional.

Figure 62 shows the Bode plot for the 1.2 V output rail. The cross frequency is 62 kHz, and the phase margin is 58°. Figure 63 shows the load transient waveform.

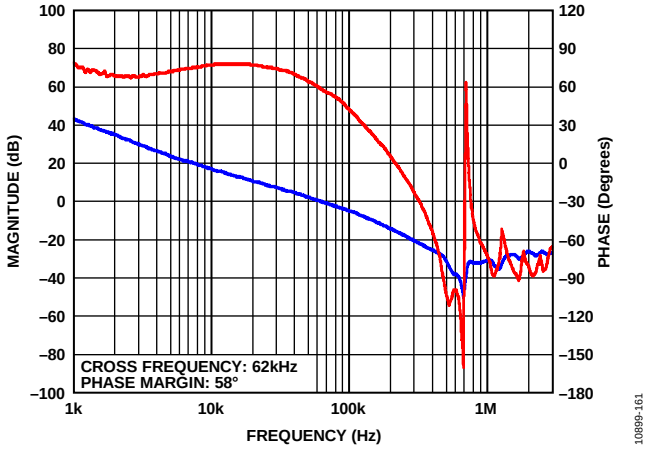


Figure 62. Bode Plot for 1.2 V Output

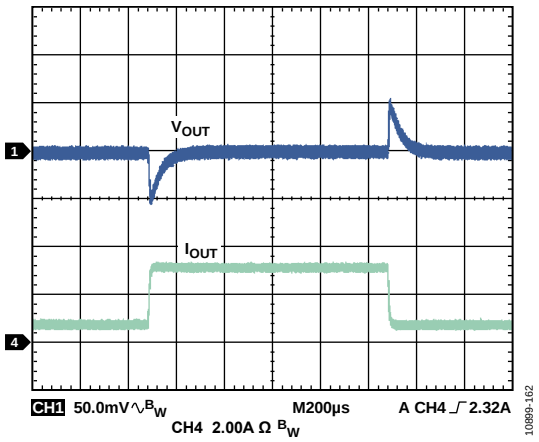


Figure 63. 0.8 A to 3.2 A Load Transient for 1.2 V Output

SELECTING THE SOFT START TIME

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current.

The SS12 pin can be used to program a soft start time of 2 ms, 4 ms, or 8 ms and can also be used to configure parallel operation of Channel 1 and Channel 2. For more information, see the Soft Start section and Table 11.

SELECTING THE INPUT CAPACITOR

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF; place the input capacitor close to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

RECOMMENDED EXTERNAL COMPONENTS

Table 17 lists the recommended external components for 4 A applications used with Channel 1 and Channel 2 of the ADP5050.
Table 18 lists the recommended external components for 1.2 A applications used with Channel 3 and Channel 4.

Table 17. Recommended External Components for Typical 4 A Applications, Channel 1 and Channel 2 (±1% Output Ripple, ±7.5% Tolerance at ~60% Step Transient)

f_{SW} (kHz)	I_{OUT} (A)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	Dual FET
300	4	12 (or 5)	1.2	3.3	2 × 100[1]	4.99	10	10	4700	Si7232DN
		12 (or 5)	1.5	3.3	2 × 100[1]	8.87	10.2	10	4700	Si7232DN
		12 (or 5)	1.8	3.3	3 × 47[2]	12.7	10.2	6.81	4700	Si7232DN
		12 (or 5)	2.5	4.7	3 × 47[2]	21.5	10.2	10	4700	Si7232DN
		12 (or 5)	3.3	6.8	3 × 47[2]	31.6	10.2	10	4700	Si7232DN
		12	5.0	6.8	47[3]	52.3	10	4.7	4700	Si7232DN
600	4	12 (or 5)	1.2	1.5	2 × 47[2]	4.99	10	10	2700	Si7232DN
		12 (or 5)	1.5	1.5	2 × 47[2]	8.87	10.2	10	2700	Si7232DN
		12 (or 5)	1.8	2.2	2 × 47[2]	12.7	10.2	10	2700	Si7232DN
		12 (or 5)	2.5	2.2	2 × 47[2]	21.5	10.2	10	2700	Si7232DN
		12 (or 5)	3.3	3.3	2 × 47[2]	31.6	10.2	15	2700	Si7232DN
		12	5.0	3.3	47[3]	52.3	10	10	2700	Si7232DN
1000	4	5	1.2	1.0	2 × 47[2]	4.99	10	15	1500	Si7232DN
		5	1.5	1.0	2 × 47[2]	8.87	10.2	15	1500	Si7232DN
		12 (or 5)	1.8	1.0	47[2]	12.7	10.2	10	1500	Si7232DN
		12 (or 5)	2.5	1.5	47[2]	21.5	10.2	10	1500	Si7232DN
		12 (or 5)	3.3	1.5	47[2]	31.6	10.2	10	1500	Si7232DN
		12	5.0	2.2	47[3]	52.3	10	15	1500	Si7232DN

[1] 100 µF capacitor: Murata GRM31CR60J107ME39 (6.3 V, X5R, 1206).
[2] 47 µF capacitor: Murata GRM21BR60J476ME15 (6.3 V, X5R, 0805).
[3] 47 µF capacitor: Murata GRM31CR61A476ME15 (10 V, X5R, 1206).

Table 18. Recommended External Components for Typical 1.2 A Applications, Channel 3 and Channel 4 (±1% Output Ripple, ±7.5% Tolerance at ~60% Step Transient)

f_{SW} (kHz)	I_{OUT} (A)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)
300	1.2	12 (or 5)	1.2	10	2 × 22[1]	4.99	10	6.81	4700
		12 (or 5)	1.5	10	2 × 22[1]	8.87	10.2	6.81	4700
		12 (or 5)	1.8	15	2 × 22[1]	12.7	10.2	6.81	4700
		12 (or 5)	2.5	15	2 × 22[1]	21.5	10.2	6.81	4700
		12 (or 5)	3.3	22	2 × 22[1]	31.6	10.2	6.81	4700
		12	5.0	22	22[2]	52.3	10	6.81	4700
600	1.2	12 (or 5)	1.2	4.7	22[1]	4.99	10	6.81	2700
		12 (or 5)	1.5	6.8	22[1]	8.87	10.2	6.81	2700
		12 (or 5)	1.8	6.8	22[1]	12.7	10.2	6.81	2700
		12 (or 5)	2.5	10	22[1]	21.5	10.2	6.81	2700
		12 (or 5)	3.3	10	22[1]	31.6	10.2	6.81	2700
		12	5.0	10	22[2]	52.3	10	6.81	2700
1000	1.2	5	1.2	2.2	22[1]	4.99	10	10	1800
		12 (or 5)	1.5	3.3	22[1]	8.87	10.2	10	1800
		12 (or 5)	1.8	4.7	22[1]	12.7	10.2	10	1800
		12 (or 5)	2.5	4.7	22[1]	21.5	10.2	10	1800
		12 (or 5)	3.3	6.8	22[1]	31.6	10.2	10	1800
		12	5.0	6.8	22[2]	52.3	10	15	1800

[1] 22 µF capacitor: Murata GRM188R60J226MEA0 (6.3 V, X5R, 0603).
[2] 22 µF capacitor: Murata GRM219R61A226MEA0 (10 V, X5R, 0805).

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtain the best performance from the ADP5050 (see Figure 65). Poor layout can affect the regulation and stability of the part, as well as the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance. Refer to the following guidelines for a good PCB layout.

- Place the input capacitor, inductor, MOSFET, output capacitor, and bootstrap capacitor close to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGNDx, and SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible. Figure 64 shows the high current path.
- Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors close to the VREG and VDD pins.
- Place the frequency setting resistor close to the RT pin.
- Place the feedback resistor divider close to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use Size 0402 or 0603 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

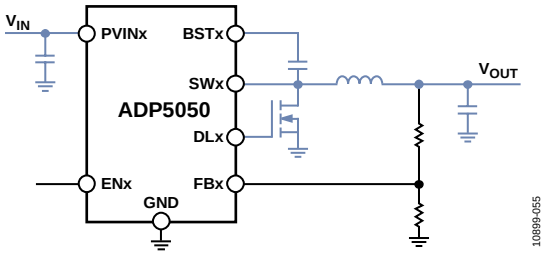


Figure 64. Typical Circuit with High Current Traces Shown in Blue

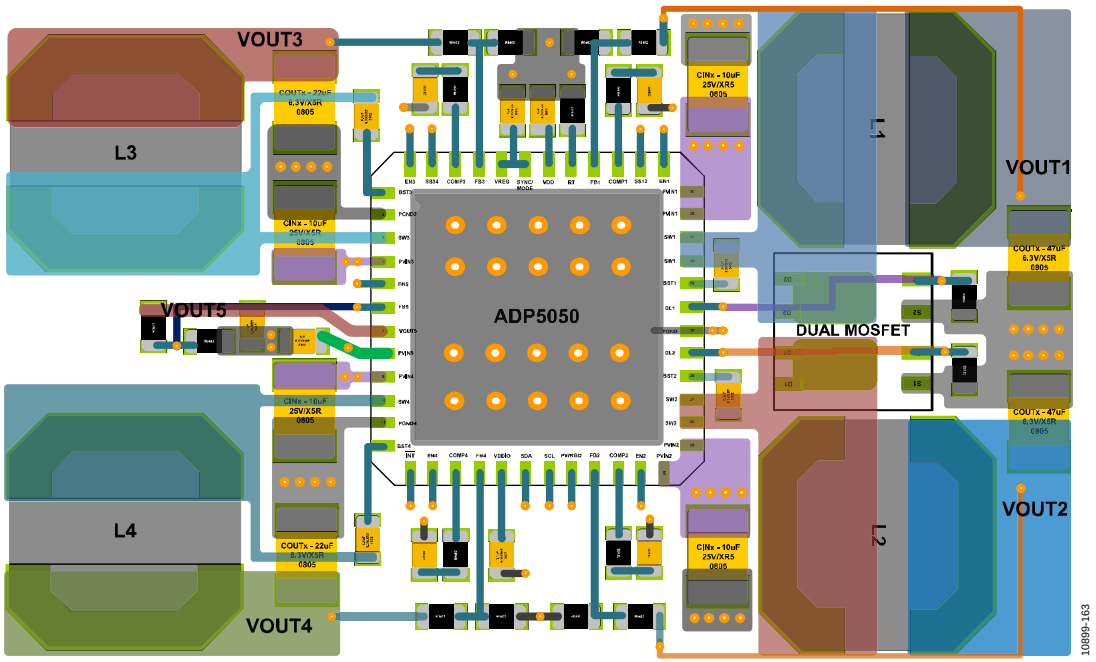


Figure 65. Typical PCB Layout for the ADP5050

TYPICAL APPLICATION CIRCUITS

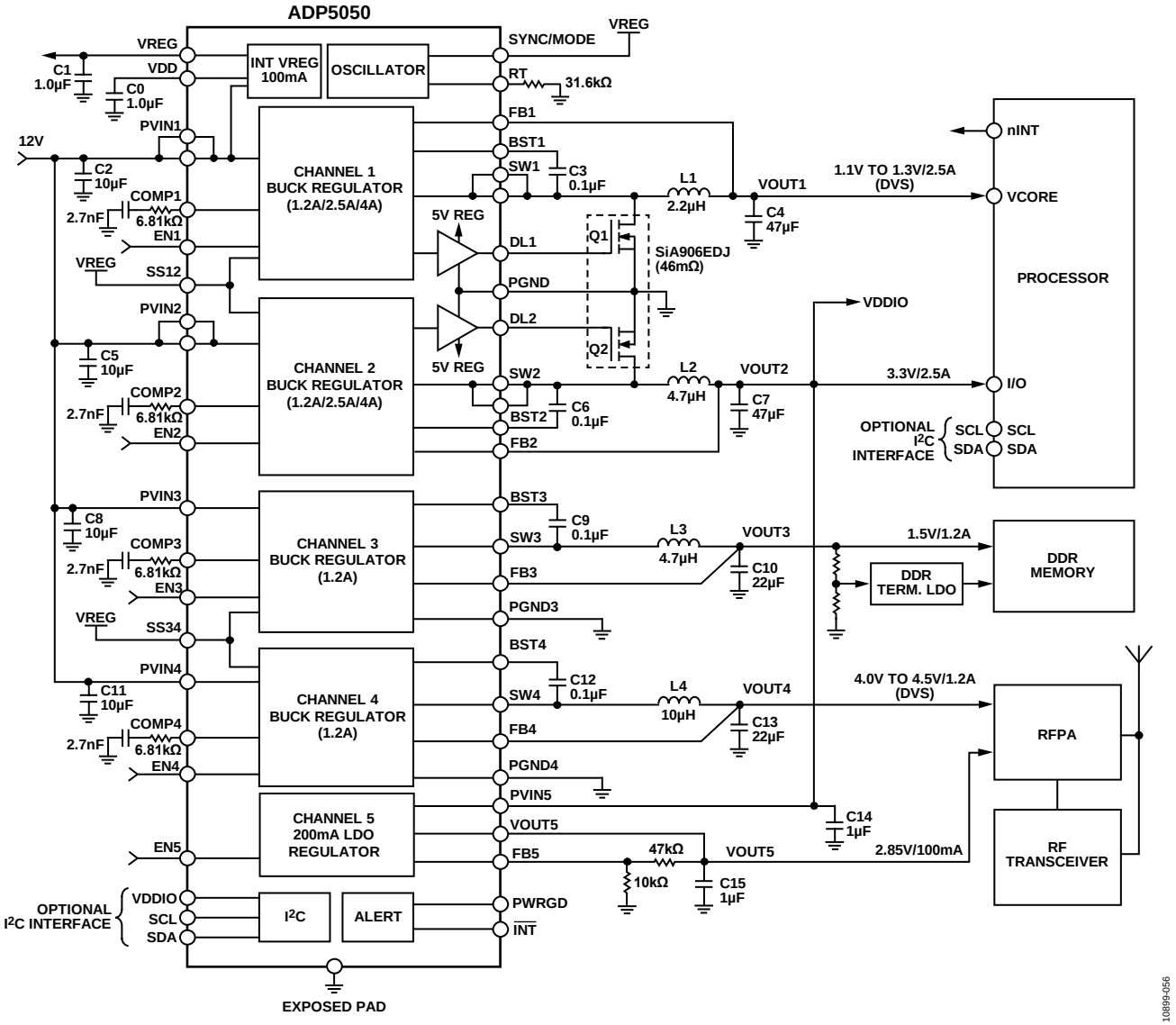


Figure 66. Typical Femtocell Application, 600 kHz Switching Frequency, Fixed Output Model

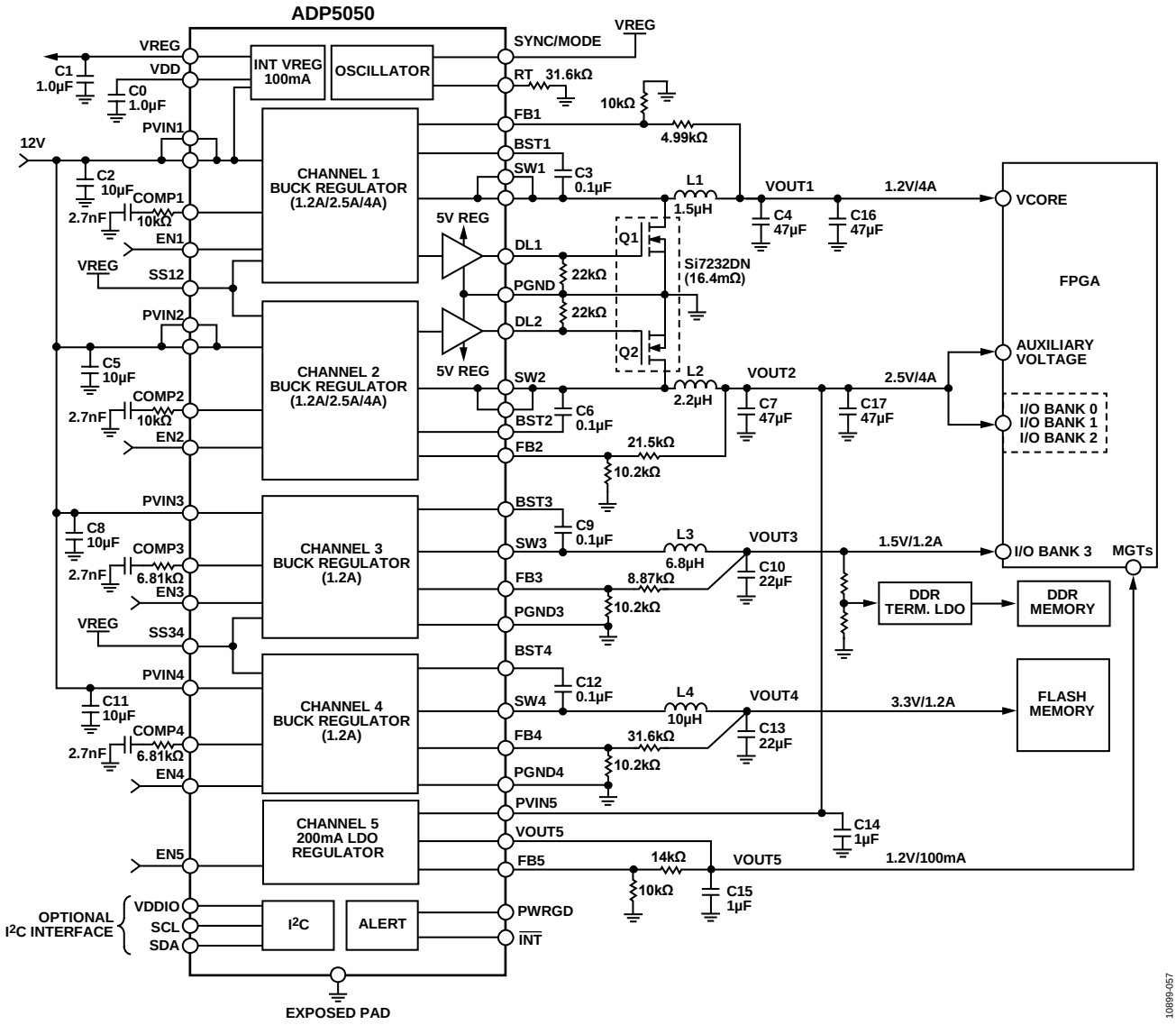


Figure 67. Typical FPGA Application, 600 kHz Switching Frequency, Adjustable Output Model

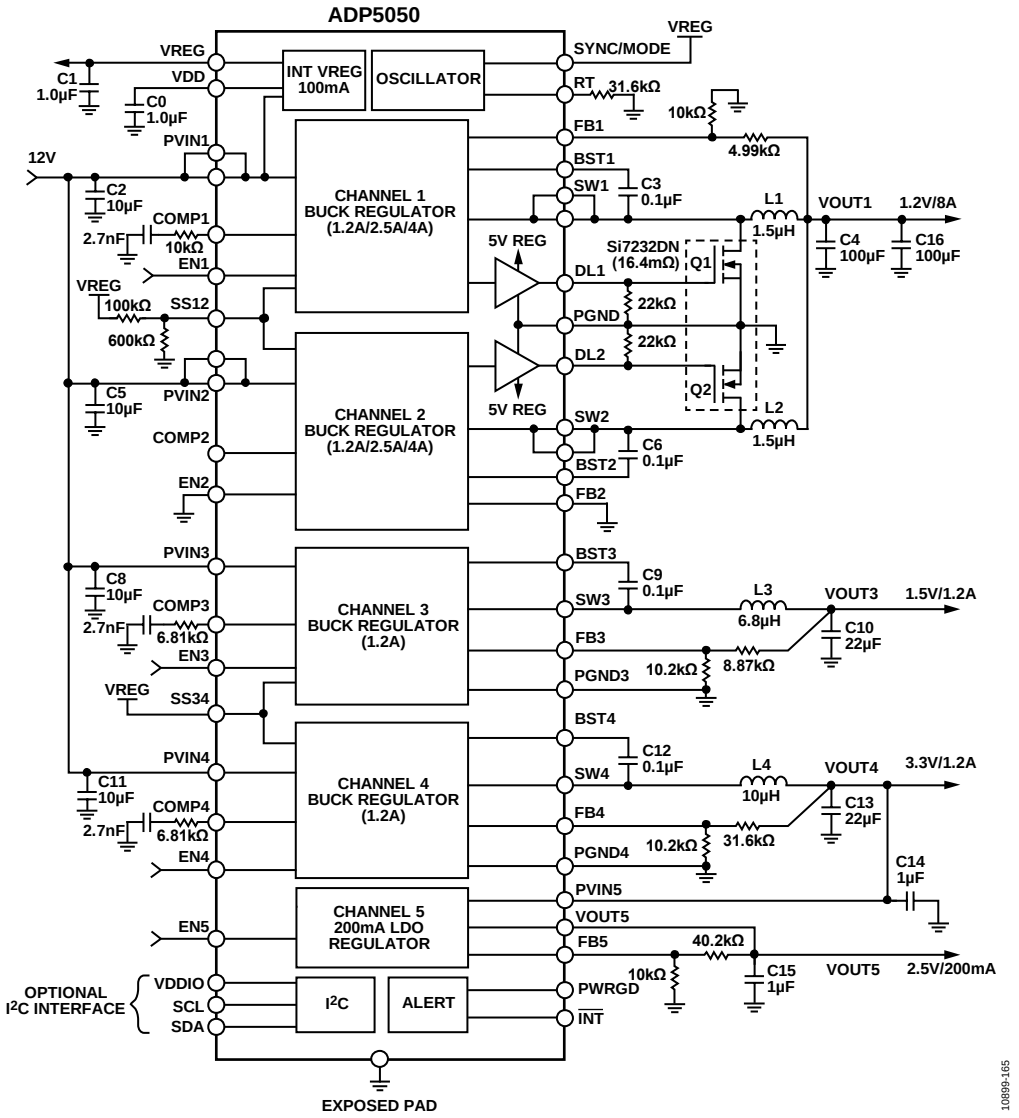


Figure 68. Typical Channel 1/Channel 2 Parallel Output Application, 600 kHz Switching Frequency, Adjustable Output Model

REGISTER MAP

Table 19. Register Map

Reg.	Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0x00	Reserved	Reserved							
1	0x01	PCTRL	Reserved			CH5_ON	CH4_ON	CH3_ON	CH2_ON	CH1_ON
2	0x02	VID1	Reserved			VID1[4:0]				
3	0x03	VID23	Reserved	VID3[2:0]			Reserved	VID2[2:0]		
4	0x04	VID4	Reserved			VID4[4:0]				
5	0x05	DVS_CFG	Reserved	DVS4_ON	DVS4_INTVAL[1:0]		Reserved	DVS1_ON	DVS1_INTVAL[1:0]	
6	0x06	OPT_CFG	DSCG4_ON	DSCG3_ON	DSCG2_ON	DSCG1_ON	PSM4_ON	PSM3_ON	PSM2_ON	PSM1_ON
7	0x07	LCH_CFG	OVP4_ON	OVP3_ON	OVP2_ON	OVP1_ON	SCP4_ON	SCP3_ON	SCP2_ON	SCP1_ON
8	0x08	SW_CFG	FREQ3	FREQ1	PHASE4[1:0]		PHASE3[1:0]		PHASE2[1:0]	
9	0x09	TH_CFG	Reserved		TEMP_TH[1:0]		LVIN_TH[3:0]			
10	0x0A	HICCUP_CFG	SYNC_OUT	Reserved			HICCUP4_OFF	HICCUP3_OFF	HICCUP2_OFF	HICCUP1_OFF
11	0x0B	PWRGD_MASK	Reserved				MASK_CH4	MASK_CH3	MASK_CH2	MASK_CH1
12	0x0C	LCH_STATUS	Reserved			TSD_LCH	CH4_LCH	CH3_LCH	CH2_LCH	CH1_LCH
13	0x0D	STATUS_RD	Reserved				PWRG4	PWRG3	PWRG2	PWRG1
14	0x0E	INT_STATUS	Reserved		TEMP_INT	LVIN_INT	PWRG4_INT	PWRG3_INT	PWRG2_INT	PWRG1_INT
15	0x0F	INT_MASK	Reserved		MASK_TEMP	MASK_LVIN	MASK_PWRG4	MASK_PWRG3	MASK_PWRG2	MASK_PWRG1
16	0x10	Reserved	Reserved							
17	0x11	DEFAULT_SET	DEFAULT_SET[7:0]							

DETAILED REGISTER DESCRIPTIONS

This section describes the bit functions of each register used by the ADP5050. To reset a register, the internal VDD power-on reset signals must be low, unless otherwise noted.

REGISTER 1: PCTRL (CHANNEL ENABLE CONTROL), ADDRESS 0x01

Register 1 is used to enable and disable the operation of each channel. The on or off status of a channel is controlled by the CHx_ON bit in this register and the external hardware enable pin for the channel (logical AND). The default value of the CHx_ON bit, 1, means that the channel enable is controlled by the external hardware enable pin. The channel can be disabled or enabled via the I²C interface only when the ENx pin is high. Pulling the ENx pin low resets the corresponding CHx_ON bit to the default value (1) to allow another valid startup when the ENx pin is high again.

Table 20. Register 1 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			CH5_ON	CH4_ON	CH3_ON	CH2_ON	CH1_ON

Table 21. PCTRL Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:5]	Reserved	R/W	Reserved.
4	CH5_ON	R/W	0 = disable Channel 5 (EN5 pin must be high). 1 = enable Channel 5 (default).
3	CH4_ON	R/W	0 = disable Channel 4 (EN4 pin must be high). 1 = enable Channel 4 (default).
2	CH3_ON	R/W	0 = disable Channel 3 (EN3 pin must be high). 1 = enable Channel 3 (default).
1	CH2_ON	R/W	0 = disable Channel 2 (EN2 pin must be high). 1 = enable Channel 2 (default).
0	CH1_ON	R/W	0 = disable Channel 1 (EN1 pin must be high). 1 = enable Channel 1 (default).

REGISTER 2: VID1 (VID SETTING FOR CHANNEL 1), ADDRESS 0x02

Register 2 is used to set the output voltage for Channel 1.

Table 22. Register 2 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			VID1[4:0]				

Table 23. VID1 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:5]	Reserved	R/W	Reserved.
[4:0]	VID1[4:0]	R/W	These bits set the output voltage for Channel 1. The default value is programmed by factory fuse. 00000 = 0.8 V (adjustable). 00001 = 0.85 V. 00010 = 0.875 V. 00011 = 0.9 V. … 00111 = 1.0 V. … 10011 = 1.3 V. … 11011 = 1.5 V. … 11110 = 1.575 V. 11111 = 1.6 V.

REGISTER 3: VID23 (VID SETTING FOR CHANNEL 2 AND CHANNEL 3), ADDRESS 0x03

Register 3 is used to set the output voltage for Channel 2 and Channel 3.

Table 24. Register 3 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	VID3[2:0]			Reserved	VID2[2:0]		

Table 25. VID23 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	Reserved	R/W	Reserved.
[6:4]	VID3[2:0]	R/W	These bits set the output voltage for Channel 3. The default value is programmed by factory fuse. 000 = 0.8 V (adjustable). 001 = 1.2 V. 010 = 1.3 V. 011 = 1.4 V. 100 = 1.5 V. 101 = 1.6 V. 110 = 1.7 V. 111 = 1.8 V.
3	Reserved	R/W	Reserved.
[2:0]	VID2[2:0]	R/W	These bits set the output voltage for Channel 2. The default value is programmed by factory fuse. 000 = 0.8 V (adjustable). 001 = 3.3 V. 010 = 3.6 V. 011 = 3.9 V. 100 = 4.2 V. 101 = 4.5 V. 110 = 4.8 V. 111 = 5.0 V.

REGISTER 4: VID4 (VID SETTING FOR CHANNEL 4), ADDRESS 0x04

Register 4 is used to set the output voltage for Channel 4.

Table 26. Register 4 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			VID4[4:0]				

Table 27. VID4 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:5]	Reserved	R/W	Reserved.
[4:0]	VID4[4:0]	R/W	These bits set the output voltage for Channel 4. The default value is programmed by factory fuse. 00000 = 0.8 V (adjustable). 00001 = 2.5 V. 00010 = 2.6 V. … 00110 = 3.0 V. … 10000 = 4.0 V. … 11010 = 5.0 V. … 11110 = 5.4 V. 11111 = 5.5 V.

REGISTER 5: DVS_CFG (DVS CONFIGURATION FOR CHANNEL 1 AND CHANNEL 4), ADDRESS 0x05

Register 5 is used to configure dynamic voltage scaling (DVS) for Channel 1 and Channel 4 (see the Dynamic Voltage Scaling (DVS) section).

Table 28. Register 5 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DVS4_ON	DVS4_INTVAL[1:0]		Reserved	DVS1_ON	DVS1_INTVAL[1:0]	

Table 29. DVS_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	Reserved	R/W	Reserved.
6	DVS4_ON	R/W	0 = disable DVS for Channel 4 (default). 1 = enable DVS for Channel 4.
[5:4]	DVS4_INTVAL[1:0]	R/W	These bits configure the DVS interval for Channel 4. 00 = 62.5 µs (default). 01 = 31.2 µs. 10 = 15.6 µs. 11 = 7.8 µs.
3	Reserved	R/W	Reserved.
2	DVS1_ON	R/W	0 = disable DVS for Channel 1 (default). 1 = enable DVS for Channel 1.
[1:0]	DVS1_INTVAL[1:0]	R/W	These bits configure the DVS interval for Channel 1. 00 = 62.5 µs (default). 01 = 31.2 µs. 10 = 15.6 µs. 11 = 7.8 µs.

REGISTER 6: OPT_CFG (FPWM/PSM MODE AND OUTPUT DISCHARGE FUNCTION CONFIGURATION), ADDRESS 0x06

Register 6 is used to configure the operational mode and the discharge switch setting for Channel 1 to Channel 4. The PSMx_ON bit setting for each channel is in effect when the SYNC/MODE pin is high (or when SYNC/MODE is configured as a clock input or output). When the SYNC/MODE pin is low, all channels are forced to work in automatic PWM/PSM mode, and the PSMx_ON settings in this register are ignored. The default value for the output discharge function can be programmed by factory fuse (output discharge function enabled or disabled for all four buck regulators).

Table 30. Register 6 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DSCG4_ON	DSCG3_ON	DSCG2_ON	DSCG1_ON	PSM4_ON	PSM3_ON	PSM2_ON	PSM1_ON

Table 31. OPT_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	DSCG4_ON	R/W	The default value is programmed by factory fuse. 0 = disable output discharge function for Channel 4. 1 = enable output discharge function for Channel 4.
6	DSCG3_ON	R/W	The default value is programmed by factory fuse. 0 = disable output discharge function for Channel 3. 1 = enable output discharge function for Channel 3.
5	DSCG2_ON	R/W	The default value is programmed by factory fuse. 0 = disable output discharge function for Channel 2. 1 = enable output discharge function for Channel 2.
4	DSCG1_ON	R/W	The default value is programmed by factory fuse. 0 = disable output discharge function for Channel 1. 1 = enable output discharge function for Channel 1.
3	PSM4_ON	R/W	This bit is ignored when the SYNC/MODE pin is low. 0 = enable forced PWM mode for Channel 4 (default). 1 = enable automatic PWM/PSM mode for Channel 4.
2	PSM3_ON	R/W	This bit is ignored when the SYNC/MODE pin is low. 0 = enable forced PWM mode for Channel 3 (default). 1 = enable automatic PWM/PSM mode for Channel 3.
1	PSM2_ON	R/W	This bit is ignored when the SYNC/MODE pin is low. 0 = enable forced PWM mode for Channel 2 (default). 1 = enable automatic PWM/PSM mode for Channel 2.
0	PSM1_ON	R/W	This bit is ignored when the SYNC/MODE pin is low. 0 = enable forced PWM mode for Channel 1 (default). 1 = enable automatic PWM/PSM mode for Channel 1.

REGISTER 7: LCH_CFG (SHORT-CIRCUIT LATCH-OFF AND OVERVOLTAGE LATCH-OFF CONFIGURATION), ADDRESS 0x07

Register 7 is used to enable and disable the latch-off function for short-circuit protection (SCP) and overvoltage protection (OVP).

When the SCP or OVP latch-off function is enabled, the CHx_LCH bit in Register 12 is set after an error condition occurs (see the Latch-Off Protection section). The default value for the SCP latch-off and OVP latch-off functions can be programmed by factory fuse (SCP or OVP latch-off function enabled or disabled for all four buck regulators).

Table 32. Register 7 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OVP4_ON	OVP3_ON	OVP2_ON	OVP1_ON	SCP4_ON	SCP3_ON	SCP2_ON	SCP1_ON

Table 33. LCH_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	OVP4_ON	R/W	The default value is programmed by factory fuse. 0 = disable the OVP latch-off function for Channel 4. 1 = enable the OVP latch-off function for Channel 4.
6	OVP3_ON	R/W	The default value is programmed by factory fuse. 0 = disable the OVP latch-off function for Channel 3. 1 = enable the OVP latch-off function for Channel 3.
5	OVP2_ON	R/W	The default value is programmed by factory fuse. 0 = disable the OVP latch-off function for Channel 2. 1 = enable the OVP latch-off function for Channel 2.
4	OVP1_ON	R/W	The default value is programmed by factory fuse. 0 = disable the OVP latch-off function for Channel 1. 1 = enable the OVP latch-off function for Channel 1.
3	SCP4_ON	R/W	The default value is programmed by factory fuse. 0 = disable the SCP latch-off function for Channel 4. 1 = enable the SCP latch-off function for Channel 4.
2	SCP3_ON	R/W	The default value is programmed by factory fuse. 0 = disable the SCP latch-off function for Channel 3. 1 = enable the SCP latch-off function for Channel 3.
1	SCP2_ON	R/W	The default value is programmed by factory fuse. 0 = disable the SCP latch-off function for Channel 2. 1 = enable the SCP latch-off function for Channel 2.
0	SCP1_ON	R/W	The default value is programmed by factory fuse. 0 = disable the SCP latch-off function for Channel 1. 1 = enable the SCP latch-off function for Channel 1.

REGISTER 8: SW_CFG (SWITCHING FREQUENCY AND PHASE SHIFT CONFIGURATION), ADDRESS 0x08

Register 8 is used to configure the switching frequency for Channel 1 and Channel 3 and to configure the phase shift for Channel 2, Channel 3, and Channel 4 with respect to Channel 1 (0°). The default values for the Channel 1 and Channel 3 switching frequencies can be programmed by factory fuse.

Table 34. Register 8 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FREQ3	FREQ1	PHASE4[1:0]		PHASE3[1:0]		PHASE2[1:0]	

Table 35. SW_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	FREQ3	R/W	The default value can be programmed by factory fuse. 0 = switching frequency for Channel 3 is the same as the master frequency set by the RT pin. 1 = switching frequency for Channel 3 is half the master frequency set by the RT pin.
6	FREQ1	R/W	The default value can be programmed by factory fuse. 0 = switching frequency for Channel 1 is the same as the master frequency set by the RT pin. 1 = switching frequency for Channel 1 is half the master frequency set by the RT pin.
[5:4]	PHASE4[1:0]	R/W	These bits configure the phase shift for Channel 4 with respect to Channel 1 (0°). 00 = 0° phase shift. 01 = 90° phase shift. 10 = 180° phase shift (default). 11 = 270° phase shift.
[3:2]	PHASE3[1:0]	R/W	These bits configure the phase shift for Channel 3 with respect to Channel 1 (0°). 00 = 0° phase shift (default). 01 = 90° phase shift. 10 = 180° phase shift. 11 = 270° phase shift.
[1:0]	PHASE2[1:0]	R/W	These bits configure the phase shift for Channel 2 with respect to Channel 1 (0°). 00 = 0° phase shift. 01 = 90° phase shift. 10 = 180° phase shift (default). 11 = 270° phase shift.

REGISTER 9: TH_CFG (TEMPERATURE WARNING AND LOW V_{IN} WARNING THRESHOLD CONFIGURATION), ADDRESS 0x09

Register 9 is used to configure the junction temperature overheat detection threshold and the low input voltage detection threshold. When these thresholds are enabled, the TEMP_INT and LVIN_INT status bits in Register 14 are set if the thresholds are exceeded.

Table 36. Register 9 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TEMP_TH[1:0]		LVIN_TH[3:0]			

Table 37. TH_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:6]	Reserved	R/W	Reserved.
[5:4]	TEMP_TH[1:0]	R/W	These bits set the junction temperature overheat threshold. 00 = temperature warning function disabled (default). 01 = 105°C. 10 = 115°C. 11 = 125°C.
[3:0]	LVIN_TH[3:0]	R/W	These bits set the low input voltage detection threshold. 0000 = 4.2 V (default). 0001 = 4.7 V. 0010 = 5.2 V. 0011 = 5.7 V. 0100 = 6.2 V. 0101 = 6.7 V. 0110 = 7.2 V. 0111 = 7.7 V. 1000 = 8.2 V. 1001 = 8.7 V. 1010 = 9.2 V. 1011 = 9.7 V. 1100 = 10.2 V. 1101 = 10.7 V. 1110 = 11.2 V. 1111 = low input voltage warning function disabled.

REGISTER 10: HICCUP_CFG (HICCUP CONFIGURATION), ADDRESS 0x0A

Register 10 is used to configure the SYNC/MODE pin as a synchronization input or output and to configure hiccup protection for each channel. The default value for hiccup protection can be programmed by factory fuse (hiccup function enabled or disabled for all four buck regulators).

Table 38. Register 10 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC_OUT	Reserved			HICCUP4_OFF	HICCUP3_OFF	HICCUP2_OFF	HICCUP1_OFF

Table 39. HICCUP_CFG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	SYNC_OUT	R/W	The default value can be programmed by factory fuse. 0 = configure the SYNC/MODE pin as a clock synchronization input if a clock is connected (default). 1 = configure the SYNC/MODE pin as a clock synchronization output.
[6:4]	Reserved	R/W	Reserved.
3	HICCUP4_OFF	R/W	The default value can be programmed by factory fuse. 0 = enable hiccup protection for Channel 4. 1 = disable hiccup protection for Channel 4 (short-circuit protection is disabled automatically).
2	HICCUP3_OFF	R/W	The default value can be programmed by factory fuse. 0 = enable hiccup protection for Channel 3. 1 = disable hiccup protection for Channel 3 (short-circuit protection is disabled automatically).
1	HICCUP2_OFF	R/W	The default value can be programmed by factory fuse. 0 = enable hiccup protection for Channel 2. 1 = disable hiccup protection for Channel 2 (short-circuit protection is disabled automatically).
0	HICCUP1_OFF	R/W	The default value can be programmed by factory fuse. 0 = enable hiccup protection for Channel 1. 1 = disable hiccup protection for Channel 1 (short-circuit protection is disabled automatically).

REGISTER 11: PWRGD_MASK (CHANNEL MASK CONFIGURATION FOR PWRGD PIN), ADDRESS 0x0B

Register 11 is used to mask or unmask the power-good status of Channel 1 to Channel 4; when unmasked, a power-good failure on any of these channels triggers the PWRGD pin. The output of the PWRGD pin represents the logical AND of all unmasked PWRGD signals; that is, the PWRGD pin is pulled low by any PWRGD signal failure. There is a 1 ms validation delay time before the PWRGD pin goes high. The default value for the power-good mask configuration can be programmed by factory fuse (mask function enabled or disabled for all four buck regulators).

Table 40. Register 11 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				MASK_CH4	MASK_CH3	MASK_CH2	MASK_CH1

Table 41. PWRGD_MASK Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:4]	Reserved	R/W	Reserved.
3	MASK_CH4	R/W	The default value can be programmed by factory fuse. 0 = mask power-good status of Channel 4. 1 = output power-good status of Channel 4 to the PWRGD pin.
2	MASK_CH3	R/W	The default value can be programmed by factory fuse. 0 = mask power-good status of Channel 3. 1 = output power-good status of Channel 3 to the PWRGD pin.
1	MASK_CH2	R/W	The default value can be programmed by factory fuse. 0 = mask power-good status of Channel 2. 1 = output power-good status of Channel 2 to the PWRGD pin.
0	MASK_CH1	R/W	The default value can be programmed by factory fuse. 0 = mask power-good status of Channel 1. 1 = output power-good status of Channel 1 to the PWRGD pin.

REGISTER 12: LCH_STATUS (LATCH-OFF STATUS READBACK), ADDRESS 0x0C

Register 12 contains latched fault flags for thermal shutdown and channel latch-off caused by an OVP or SCP condition. Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit (provided that the fault no longer persists).

Table 42. Register 12 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			TSD_LCH	CH4_LCH	CH3_LCH	CH2_LCH	CH1_LCH

Table 43. LCH_STATUS Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:5]	Reserved	R/W	Reserved.
4	TSD_LCH	Read/ self-clear	0 = no thermal shutdown has occurred. 1 = thermal shutdown has occurred.
3	CH4_LCH	Read/ self-clear	0 = no short-circuit or overvoltage latch-off has occurred on Channel 4. 1 = short-circuit or overvoltage latch-off has occurred on Channel 4.
2	CH3_LCH	Read/ self-clear	0 = no short-circuit or overvoltage latch-off has occurred on Channel 3. 1 = short-circuit or overvoltage latch-off has occurred on Channel 3.
1	CH2_LCH	Read/ self-clear	0 = no short-circuit or overvoltage latch-off has occurred on Channel 2. 1 = short-circuit or overvoltage latch-off has occurred on Channel 2.
0	CH1_LCH	Read/ self-clear	0 = no short-circuit or overvoltage latch-off has occurred on Channel 1. 1 = short-circuit or overvoltage latch-off has occurred on Channel 1.

REGISTER 13: STATUS_RD (STATUS READBACK), ADDRESS 0x0D

The read-only Register 13 indicates the real-time status of the power-good signals for Channel 1 to Channel 4.

Table 44. Register 13 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				PWRG4	PWRG3	PWRG2	PWRG1

Table 45. STATUS_RD Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:4]	Reserved	R	Reserved.
3	PWRG4	R	0 = Channel 4 power-good status is low (default). 1 = Channel 4 power-good status is high.
2	PWRG3	R	0 = Channel 3 power-good status is low (default). 1 = Channel 3 power-good status is high.
1	PWRG2	R	0 = Channel 2 power-good status is low (default). 1 = Channel 2 power-good status is high.
0	PWRG1	R	0 = Channel 1 power-good status is low (default). 1 = Channel 1 power-good status is high.

REGISTER 14: INT_STATUS (INTERRUPT STATUS READBACK), ADDRESS 0x0E

Register 14 contains the interrupt status for the following events: junction temperature overheat warning, low input voltage warning, and power-good signal failure on Channel 1 to Channel 4.

When any of these unmasked events occur, the $\overline{\text{INT}}$ pin is pulled low to indicate a fault condition. (Masking of these events is configured in Register 15.) To determine the cause of the fault, read this register. Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit or when all ENx pins = 0.

Table 46. Register 14 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TEMP_INT	LVIN_INT	PWRG4_INT	PWRG3_INT	PWRG2_INT	PWRG1_INT

Table 47. INT_STATUS Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:6]	Reserved	R/W	Reserved.
5	TEMP_INT	Read/ self-clear	This bit indicates whether the junction temperature threshold has been exceeded. 0 = junction temperature has not exceeded the threshold. 1 = junction temperature has exceeded the threshold.
4	LVIN_INT	Read/ self-clear	This bit indicates whether the low voltage input threshold has been exceeded. 0 = low voltage input has not fallen below the threshold. 1 = low voltage input has fallen below the threshold.
3	PWRG4_INT	Read/ self-clear	The power-good interrupt is masked when the part is initialized and during a normal shutdown. 0 = no power-good failure has been detected on Channel 4. 1 = power-good failure has been detected on Channel 4.
2	PWRG3_INT	Read/ self-clear	The power-good interrupt is masked when the part is initialized and during a normal shutdown. 0 = no power-good failure has been detected on Channel 3. 1 = power-good failure has been detected on Channel 3.
1	PWRG2_INT	Read/ self-clear	The power-good interrupt is masked when the part is initialized and during a normal shutdown. 0 = no power-good failure has been detected on Channel 2. 1 = power-good failure has been detected on Channel 2.
0	PWRG1_INT	Read/ self-clear	The power-good interrupt is masked when the part is initialized and during a normal shutdown. 0 = no power-good failure has been detected on Channel 1. 1 = power-good failure has been detected on Channel 1.

REGISTER 15: INT_MASK (INTERRUPT MASK CONFIGURATION), ADDRESS 0x0F

Register 15 is used to mask or unmask various warnings for use by the interrupt ($\overline{\text{INT}}$) pin. When any bit in this register is masked, the associated event does not trigger the $\overline{\text{INT}}$ pin.

Table 48. Register 15 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		MASK_TEMP	MASK_LVIN	MASK_PWRG4	MASK_PWRG3	MASK_PWRG2	MASK_PWRG1

Table 49. INT_MASK Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:6]	Reserved	R/W	Reserved.
5	MASK_TEMP	R/W	0 = temperature overheat warning does not trigger the interrupt pin (default). 1 = temperature overheat warning triggers the interrupt pin.
4	MASK_LVIN	R/W	0 = low voltage input warning does not trigger the interrupt pin (default). 1 = low voltage input warning triggers the interrupt pin.
3	MASK_PWRG4	R/W	0 = power-good warning on Channel 4 does not trigger the interrupt pin (default). 1 = power-good warning on Channel 4 triggers the interrupt pin.
2	MASK_PWRG3	R/W	0 = power-good warning on Channel 3 does not trigger the interrupt pin (default). 1 = power-good warning on Channel 3 triggers the interrupt pin.
1	MASK_PWRG2	R/W	0 = power-good warning on Channel 2 does not trigger the interrupt pin (default). 1 = power-good warning on Channel 2 triggers the interrupt pin.
0	MASK_PWRG1	R/W	0 = power-good warning on Channel 1 does not trigger the interrupt pin (default). 1 = power-good warning on Channel 1 triggers the interrupt pin.

REGISTER 17: DEFAULT_SET (DEFAULT RESET), ADDRESS 0x11

The write-only Register 17 is used to reset all registers to their default values.

Table 50. Register 17 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEFAULT_SET[7:0]							

Table 51. DEFAULT_SET Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:0]	DEFAULT_SET[7:0]	W	To reset all registers to their default values, write 0x7F to this register.

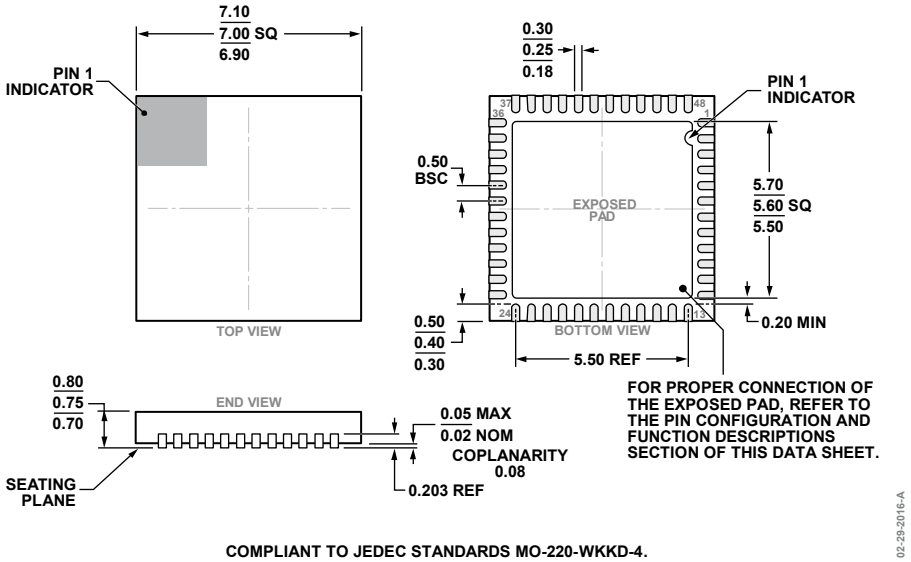
FACTORY DEFAULT OPTIONS

Table 52 lists the factory default options programmed into the ADP5050 when the device is ordered (see the Ordering Guide). To order the device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 52. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 20) Function	PWRGD pin for power-good output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 × switching frequency set by the RT pin
Switching Frequency on Channel 3	1 × switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Overvoltage Latch-Off Function	Disabled for output overvoltage events
I^2C Address	0x48

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4.

Figure 69. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADP5050ACPZ-R7	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
ADP5050-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Table 52 lists the factory default options for the device. To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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