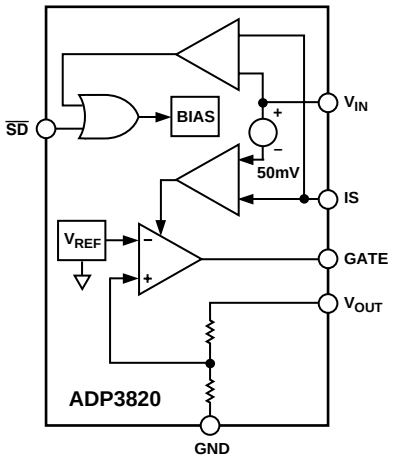
Lithium-Ion Battery Charger

ADP3820

FEATURES
±1% Total Accuracy
630 μA Typical Quiescent Current
Shutdown Current: 1 μA (Typical)
Stable with 10 μF Load Capacitor
4.5 V to 15 V Input Operating Range
Integrated Reverse Leakage Protection
6-Lead SOT-23-6 and 8-Lead SO-8 Packages
Programmable Charge Current
–20°C to +85°C Ambient Temperature Range
Internal Gate-to-Source Protective Clamp

APPLICATIONS
Li-Ion Battery Chargers
Desktop Computers
Hand-Held Instruments
Cellular Telephones
Battery Operated Devices

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3820 is a precision single cell Li-Ion battery charge controller that can be used with an external Power PMOS device to form a two-chip, low cost, low dropout linear battery charger. It is available in two voltage options to accommodate Li-Ion batteries with coke or graphite anodes. The ADP3820's high accuracy (±1%) low shutdown current (1 μA) and easy charge current programming make this device especially attractive as a battery charge controller.

Charge current can be set by an external resistor. For example, 50 mΩ of resistance can be used to set the charge current to 1 A. Additional features of this device include foldback current limit, overload recovery, and a gate-to-source voltage clamp to protect the external MOSFET. The proprietary circuit also minimizes the reverse leakage current from the battery if the input voltage of the charger is disconnected. This feature eliminates the need for an external serial blocking diode.

The ADP3820 operates with a wide input voltage range from 4.5 V to 15 V. It is specified over the industrial temperature range of –20°C to +85°C and is available in the ultrasmall 6-lead surface mount SOT-23-6 and 8-lead SOIC packages.

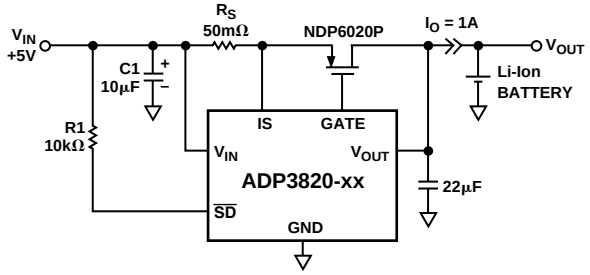


Figure 1. Li-Ion Charger Application Circuit

REV. A

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ADP3820–SPECIFICATIONS[1] (V_{IN} = [V_{OUT} + 1 V] T_A = –20°C to +85°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
INPUT VOLTAGE		V_{IN}	4.5		15	V
OUTPUT VOLTAGE ACCURACY	V_{IN} = V_{OUT} + 1 V to 15 V $V_{\overline{SD}}$ = 2 V	V_{OUT}	–1		+1	%
QUIESCENT CURRENT Shutdown Mode Normal Mode	 $V_{\overline{SD}}$ = 0 V $V_{\overline{SD}}$ = 2 V	 I_{GND} I_{GND}		 1 630	 15 800	 µA µA
GATE TO SOURCE CLAMP VOLTAGE				6	10	V
GATE DRIVE MINIMUM VOLTAGE[2]				0.7		V
GATE DRIVE CURRENT (SINK/SOURCE)			1			mA
GAIN $\left(\frac{\Delta V_{GS}}{\Delta V_{OUT}}\right)$				80		dB
CURRENT LIMIT THRESHOLD VOLTAGE	V_{IN} – V_{IS}		40		75	mV
LOAD REGULATION	I_{OUT} = 10 mA to 1 A, Circuit of Figure 1		–10		+10	mV
LINE REGULATION	V_{IN} = V_{OUT} + 1 V to 15 V I_{OUT} = 0.1 A Circuit of Figure 1 (No Battery)		–10		+10	mV
$\overline{SD}$ INPUT VOLTAGE	V_{IH} V_{IL}	$V_{\overline{SD}}$	2.0		 0.4	V V
$\overline{SD}$ INPUT CURRENT	$V_{\overline{SD}}$ = 0 V to 5 V	$I_{\overline{SD}}$	–15		+15	µA
OUTPUT REVERSE LEAKAGE CURRENT	V_{IN} = Floating	I_{DISCH}		3	5	µA

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
[2]Provided gate-to-source clamp voltage is not exceeded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Voltage, V_{IN} . . . . . +20 V
Enable Input Voltage . . . . . 0.3 V to (V_{IN} + 0.3 V)
Operating Ambient Temperature Range . . . . –20°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
θ_{JA}, SO-8 Package . . . . . 150°C/W
θ_{JA}, SOT-23-6 Package . . . . . 230°C/W
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . 2 kV

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

Model	Voltage Output	Package Option*	Marking Code
ADP3820ART-4.1	4.1 V	RT-6 (SOT-23-6)	BAC
ADP3820ART-4.2	4.2 V	RT-6 (SOT-23-6)	BBC
ADP3820AR-4.1	4.1 V	SO-8	
ADP3820AR-4.2	4.2 V	SO-8	

*SOT = Surface Mount Package. SO = Small Outline.

Contact the factory for availability of other output voltage options.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

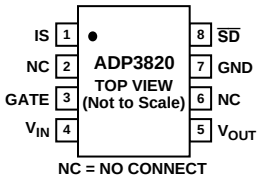


PIN FUNCTION DESCRIPTIONS

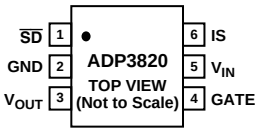
Pin SOT-23-6	Pin SO-8	Name	Function
1	8	$\overline{SD}$	Shutdown. Pulling this pin low will disable the output.
2	7	GND	Device Ground. This pin should be tied to system ground closest to the load.
3	5	V_{OUT}	Output Voltage Sense. This pin is connected to the MOSFET's drain and directly to the load for optimal load regulation. Bypass to ground with a 10 µF or larger capacitor.
4	3	GATE	Gate drive for the external MOSFET.
5	4	V_{IN}	Input Voltage. This is also the positive terminal connection of the current sense resistor.
6	1	IS	Current Sense. Used to sense the input current by monitoring the voltage across the current sense resistor. It is connected to the more negative terminal of the resistor as well as the power MOSFET's source pin. IS pin should be tied to the V_{IN} pin if the current limit feature is not used.
	2, 6	NC	No Connect.

PIN CONFIGURATIONS

SO-8



RT-6 (SOT-23-6)



ADP3820–Typical Performance Characteristics

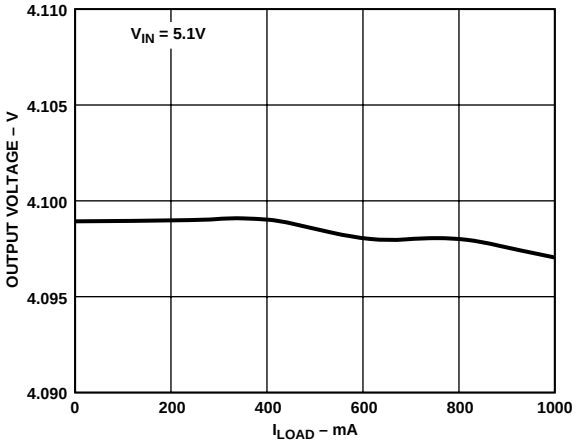


*Figure 2. V_{OUT} vs. I_{LOAD} (V_{IN} = 5.1 V)**

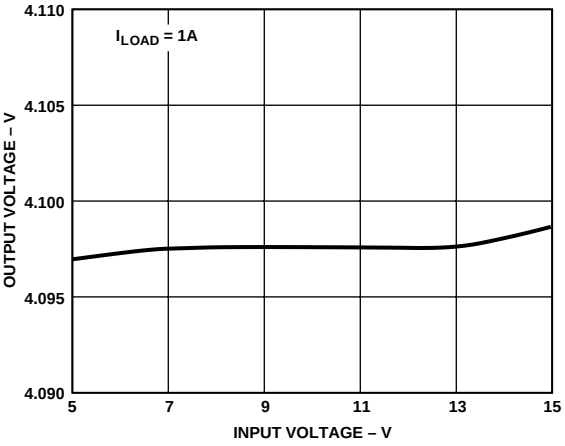


*Figure 3. V_{OUT} vs. V_{IN} (I_{LOAD} = 1 A)**

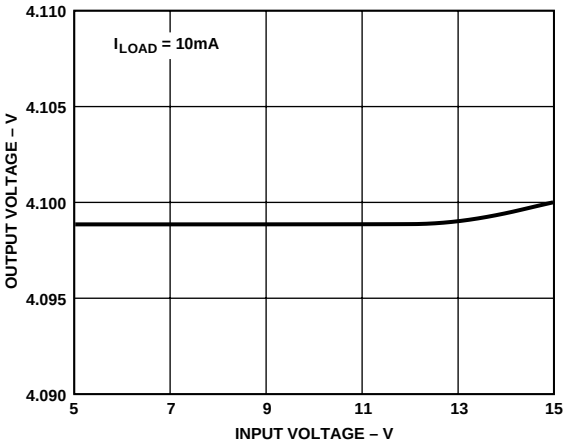


*Figure 4. V_{OUT} vs. V_{IN} (I_{LOAD} = 10 mA)**

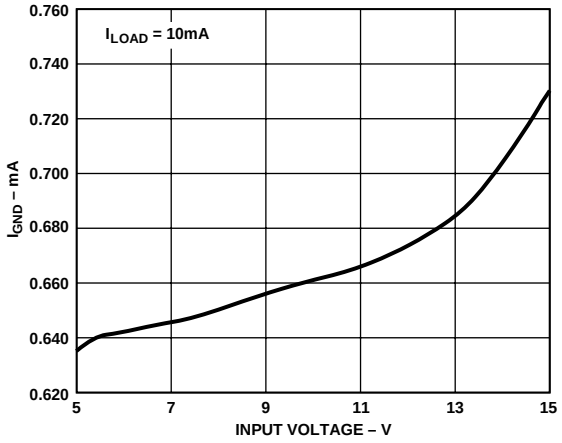


*Figure 5. I_{GND} vs. V_{IN} (I_{LOAD} = 10 mA)**

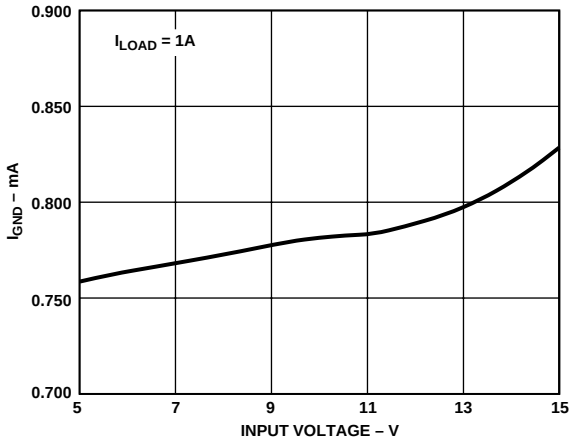


*Figure 6. I_{GND} vs. V_{IN} (I_{LOAD} = 1 A)**

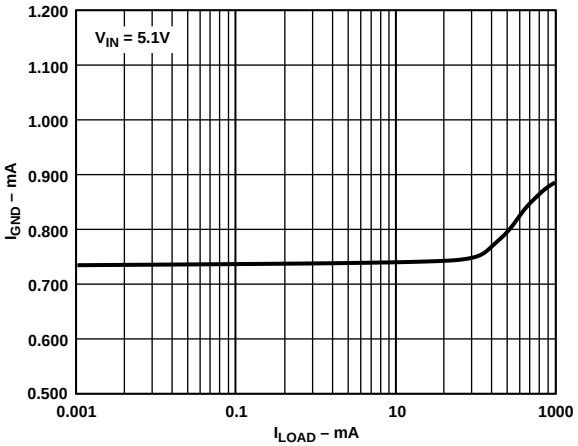


*Figure 7. I_{GND} vs. I_{LOAD} (V_{IN} = 5.1 V)**

*Reference Figure 1.

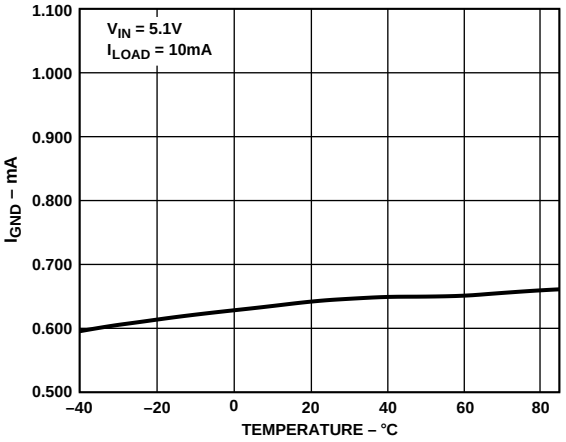


*Figure 8. Quiescent Current vs. Temperature**

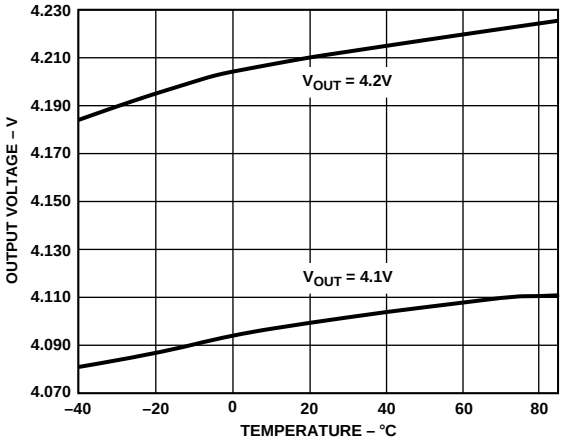


*Figure 11. V_{OUT} vs. Temperature, V_{IN} = 5.1 V, I_{LOAD} = 10 mA**

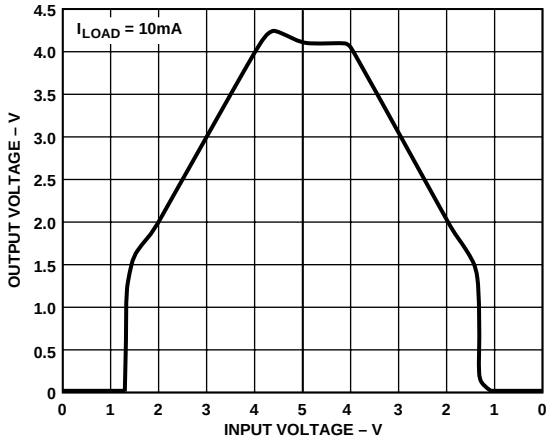


*Figure 9. Power-Up/Power-Down**

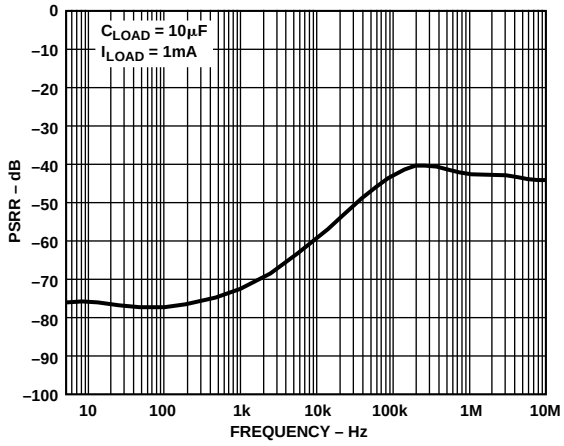


*Figure 12. Ripple Rejection**

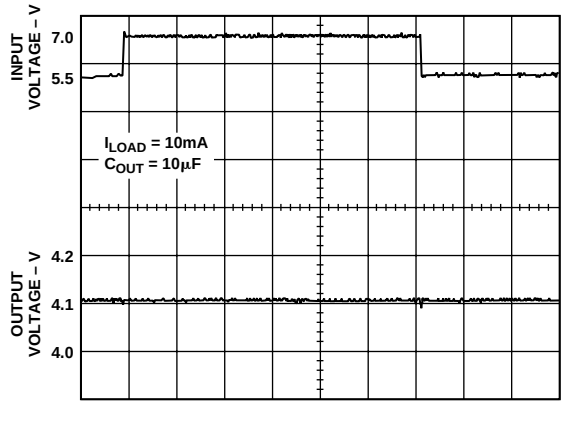


*Figure 10. Line Transient Response (10 μF Output Cap)**

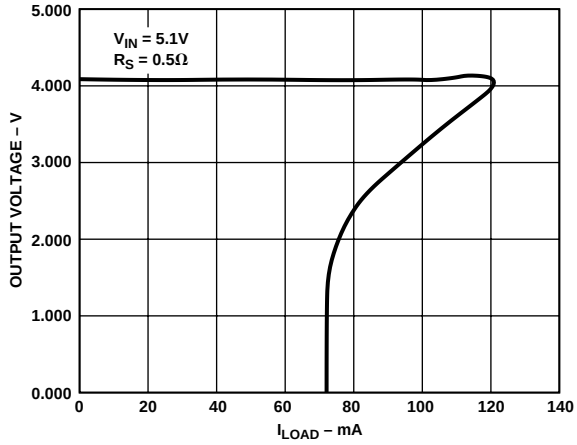


*Figure 13. Current Limit Foldback**

APPLICATION INFORMATION

The ADP3820 is very easy to use. A P-channel power MOSFET and a small capacitor on the output is all that is needed to form an inexpensive Li-Ion battery charger. The advantage of using the ADP3820 controller is that it can directly drive a PMOS FET to provide a regulated output current until the battery is charged. When the specified battery voltage is reached, the charge current is reduced and the ADP3820 maintains the maximum specified battery voltage accurately.

When fully charged, the circuit in Figure 1 works like a well known linear regulator, holding the output voltage within the specified accuracy as needed by single cell Li-Ion batteries. The output is sensed by the V_{OUT} pin. When charging a discharged battery, the circuit maintains a set charging current determined by the current sense resistor until the battery is fully charged, then reduces it to a trickle charge to keep the battery at the specified voltage. The voltage drop across the R_S current sense resistor is sensed by the IS input of the ADP3820. At minimum battery voltage or at shorted battery, the circuit reduces this current (foldback) to limit the dissipation of the FET (see Figure 13). Both the V_{IN} input and V_{OUT} sense pins of the IC need to be bypassed by a suitable bypass capacitor.

A 6 V gate-to-source voltage clamp is provided by the ADP3820 to protect the MOSFET gates at higher source voltages. The ADP3820 also has a TTL $\overline{SD}$ input, which may be connected to the input voltage to enable the IC. Pulling it to low or to ground will disable the FET-drive.

Design Approach

Due to the lower efficiency of Linear Regulator Charging, the most important factor is the thermal design and cost, which is the direct function of the input voltage, output current and thermal impedance between the MOSFET and the ambient cooling air. The worse-case situation is when the battery is shorted since the MOSFET has to dissipate the maximum power.

A tradeoff must be made between the charge current, cost and thermal requirements of the charger. Higher current requires a larger FET with more effective heat dissipation leading to a more expensive design. Lowering the charge current reduces cost by lowering the size of the FET, possibly allowing a smaller package such as SOT-23-6. The following designs consider both options. Furthermore, each design is evaluated under two input source voltage conditions.

Regarding input voltage, there are two options:

A. The input voltage is preregulated, e.g., 5 V ± 10%

B. The input voltage is not a preregulated source, e.g., a wall plug-in transformer with a rectifier and capacitive filter.

Higher Current Option

A. Preregulated Input Voltage (5 V ± 10%)

For the circuit shown in Figure 1, the required θ_{JA} thermal impedance can be calculated as follows: if the FET data sheet allows a max FET junction temperature of T_{JMAX} = 150°C, then at 50°C ambient and at convection cooling, the maximum allowed ΔT junction temperature rise is thus, $T_{JMAX} - T_{AMAX}$ = 150°C – 50°C = 100°C.

The maximum current for a shorted or discharged battery is reduced from the set charge current by a multiplier factor shown in Figure 13 due to the foldback current limiting feature of the ADP3820. This k factor between V_O of 0 V to about 2.5 V is: k ~ 0.65.

$$\theta_{JA} = \Delta T/(I_O \times k \times V_{IN}) = 100/(1 \times 0.65 \times 5) = 30.7\,°C/W$$

This thermal impedance can be realized using the transistor shown in Figure 1 when surface mounted to a 40 × 40 mm double-sided PCB with many vias around the tab of the surface-mounted FET to the backplane of the PCB. Alternatively, a TO-220 packaged FET mounted to a heatsink could be used.

The θ or thermal impedance of a suitable heatsink is calculated below:

$$\theta < (\theta_{JA} - \theta_{JC}) = 30.7 - 2 = +28.7\,°C/W$$

Where the θ_{JC}, or junction-to-case thermal impedance of the FET can be read from the FET data sheet. A low cost such heatsink is type PF430 made by Thermalloy, with a θ = +25.3°C/W.

The current sense resistor for this application can be simply calculated:

$$R_S = V_S/I_O = 0.05/1 = 50\ m\Omega$$

Where V_S is specified on the data sheet as current limit threshold voltage at 40 mV–75 mV. For battery charging applications, it is adequate to use the typical 50 mV midvalue.

B. Nonpreregulated Input Voltage

If the input voltage source is, for example, a rectified and capacitor-filtered secondary voltage of a small wall plug-in transformer, the heatsinking requirement is more demanding. The V_{INMIN} should be specified 5 V, but at the lowest line voltage and full load current. The required thermal impedance can be calculated the same way as above, but here we have to use the maximum output rectified voltage, which can be substantially higher than 5 V, depending on transformer regulation and line voltage variation. For example, if V_{INMAX} is 10 V

$$\theta_{JA} = \Delta T/(I_O \times k \times V_{INMAX}) = 100/(1 \times 0.65 \times 10) = +15.3°C/W$$

The θ suitable heatsink thermal impedance:

$$\theta < \theta_{JA} - \theta_{JC} = 15.3 - 2 = 13.3°C/W$$

A low cost heatsink is Type 6030B made by Thermalloy, with a θ = +12.5°C/W.

Lower Current Option

A. Preregulated Input Voltage (5 V ± 10%)

If lower charging current is allowed, the θ_{JA} value can be increased, and the system cost decreased. The lower cost is assured by using an inexpensive MOSFET with, for example, a NDT452P in a SOT-23-6 package mounted on a small 40 × 40 mm area on double-sided PCB. This provides a convection cooled thermal impedance of θ_{JA} = +55°C/W, presuming many vias are used around the FET to the backplane. Allowing a maximum FET junction temperature of +150°C, at +50°C ambient, and at convection cooling the maximum allowed heat rise is thus 150°C–50°C = 100°C.

The maximum foldback current allowed:

$$I_{FB} = \Delta T/(\theta \times V_{IN}) = 100/(55 \times 5) = 0.33\ A$$

Thus the full charging current:

$$I_{OUTMAX} = I_{FB}/k = 0.5\ A$$

k is calculated in the above example.

The current sense resistor for this application:

$$R_S = V_S/I_O = 0.05/0.5 = 100\ m\Omega$$

FET Selection

The type and size of the pass transistor are determined by the threshold voltage, input-output voltage differential and load current. The selected PMOS must satisfy the physical and thermal design requirements. To ensure that the maximum V_{GS} provided by the controller will turn on the FET at worst case conditions, (i.e., temperature and manufacturing tolerances) the maximum available V_{GS} must be determined. Maximum V_{GS} is calculated as follows:

$$V_{GS} = V_{IN} - V_{BE} - I_{OUTMAX} \times R_S$$

where

I_{OUTMAX} = Maximum Output Current
R_S = Current Sense Resistor
V_{BE} ~ 0.7 V (Room Temperature)
~ 0.5 V (Hot)
~ 0.9 V (Cold)

For example:

$$V_{IN} = 5\ V, \text{ and } I_{OUTMAX} = 1\ A,$$

$$V_{GS} = 5\ V - 0.7\ V - 1\ A \times 50\ m\Omega = 4.25\ V$$

If V_{GS} < 5 V, logic level FET should be considered.
If V_{GS} > 5 V, either logic level or standard MOSFET can be used.

The difference between V_{IN} and V_O (V_{DS}) must exceed the voltage drop due to the sense resistor plus the ON-resistance of the FET at the maximum charge current. The selected MOSFET must satisfy these criteria; otherwise, a different pass device should be used.

$$V_{DS} = V_{IN} - V_O = 5\ V - 4.2\ V = 0.8\ V$$

The maximum $R_{DS(ON)}$ required at the available gate drive (V_{DR}) and Drain-to-Source voltage (V_{DS}) is:

$$R_{DS(ON)} = V_{DS}/I_{OUTMAX}$$

From the Drain-to Source current vs. Drain-to-Source voltage vs. gate drive graph off the MOSFET data sheet, it can be determined if the above calculated $R_{DS(ON)}$ is higher than the graph indicates. However, the value read from the MOSFET data sheet graph must be adjusted based on the junction temperature of the MOSFET. This adjustment factor can be obtained from the normalized $R_{DS(ON)}$ vs. junction temperature graph in the MOSFET data sheet.

External Capacitors

The ADP3820 is stable with or without a battery load, and virtually any good quality output filter capacitors can be used (anyCAP™), independent of the capacitor's minimum ESR (Effective Series Resistance) value. The actual value of the capacitor and its associated ESR depends on the g_m and capacitance of the external PMOS device. A 10 µF tantalum or aluminum electrolytic capacitor at the output is sufficient to ensure stability for up to a 10 A output current.

Shutdown Mode

Applying a TTL high signal to the $\overline{SD}$ pin or tying it to the input pin will enable the output. Pulling this pin low or tying it to ground will disable the output. In shutdown mode, the controller's quiescent current is reduced to less than 1 µA.

Gate-to-Source Clamp

A 6 V gate-to-source voltage clamp is provided by the ADP3820 to protect most MOSFET gates in the event the $V_{IN} > V_{GS}$ allowed and the output is suddenly shorted to ground. This allows use of the new, low $R_{DS(ON)}$ MOSFETs.

Short Circuit Protection

The power FET is protected during short circuit conditions with a foldback type of current limiting that significantly reduces the current. See Figure 13 for foldback current limit information.

Current Sense Resistor

Current limit is achieved by setting an appropriate current sense resistor (R_S) across the current limit threshold voltage. Current limit sense resistor, R_S, is calculated as shown above. Proper derating is advised to select the power dissipation rating of the resistor.

The simplest and cheapest sense resistor for high current applications, (i.e., Figure 1) is a PCB trace. However, the temperature dependence of the copper trace and the thickness tolerances of the trace must be considered in the design. The resistivity of copper has a positive temperature coefficient of +0.39%/°C. Copper's Tempco, in conjunction with the proportional-to-absolute temperature (±0.3%) current limit voltage, can provide an accurate current limit. Table I provides the typical resistance values for PCB copper traces. Alternately, an appropriate sense resistor, such as surface mount sense resistors, available from KRL, can be used.

Table I. Printed Circuit Copper Resistance

Conductor Thickness	Conductor Width/Inch	Resistance mΩ/In
1/2oz/ft² (18 µm)	0.025	39.3
	0.050	19.7
	0.100	9.83
	0.200	4.91
	0.500	1.97
1oz/ft² (35 µm)	0.025	19.7
	0.050	9.83
	0.100	4.91
	0.200	2.46
	0.500	0.98
2oz/ft² (70 µm)	0.025	9.83
	0.050	4.91
	0.100	2.46
	0.200	1.23
	0.500	0.49
3oz/ft² (106 µm)	0.025	6.5
	0.050	3.25
	0.100	1.63
	0.200	0.81
	0.500	0.325

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PCB Layout Issues

For optimum voltage regulation, place the load as close as possible to the device's V_{OUT} and GND pins. It is recommended to use dedicated PCB traces to connect the MOSFET's drain to the positive terminal and GND to the negative terminal of the load to avoid voltage drops along the high current carrying PCB traces.

If PCB layout is used as heatsink, adding many vias around the power FET helps conduct more heat from the FET to the backplane of the PCB, thus reducing the maximum FET junction temperature.

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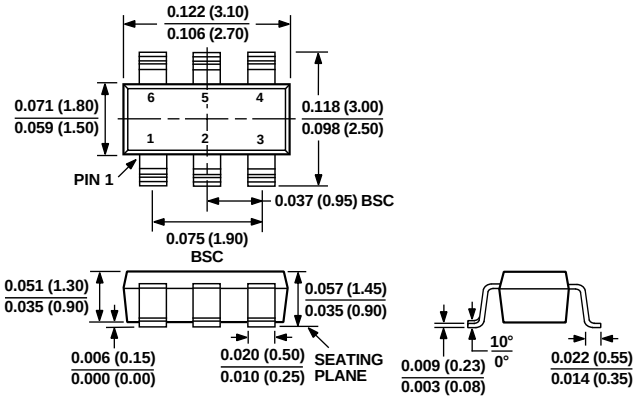
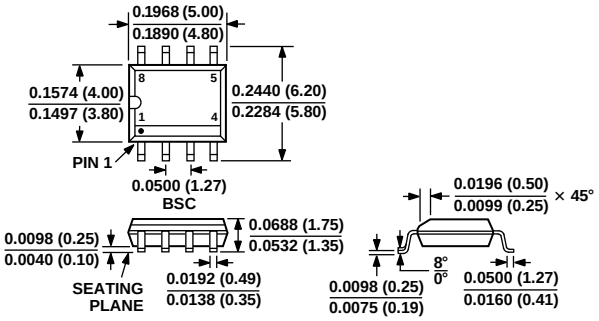
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Plastic Surface Mount Package
RT-6 (SOT-23-6)



8-Lead Narrow Body Package
SO-8



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