GSM Power Management System

ADP3522

FEATURES
Handles all GSM Baseband Power Management
6 LDOs Optimized for Specific GSM Subsystems
Li-Ion Battery Charge Function
Optimized for the AD20msp430 Baseband Chipset
Reduced Package Size: 5 mm × 5 mm LFCSP-32

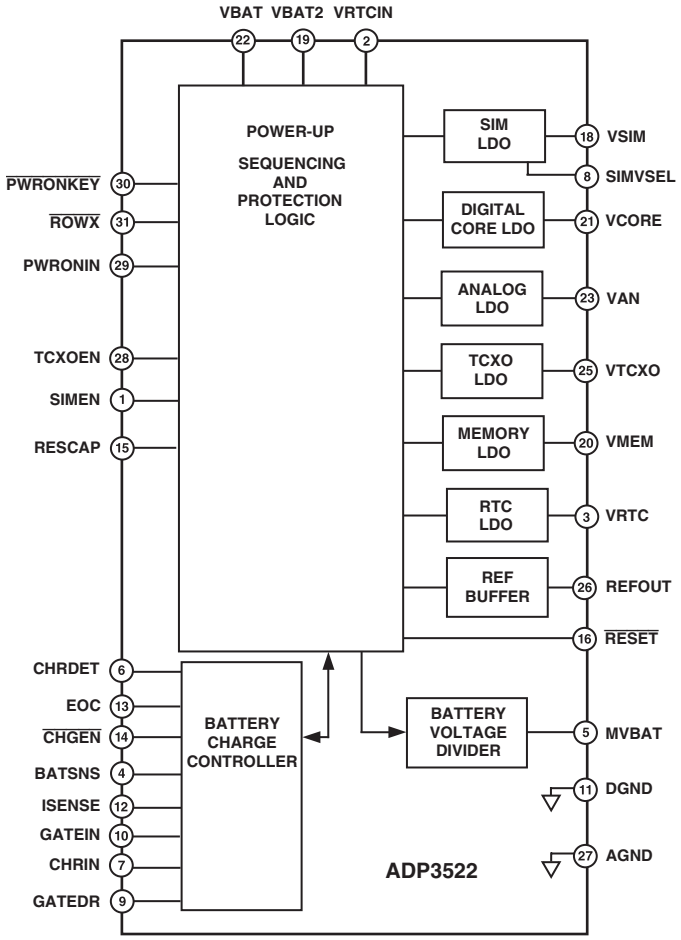
APPLICATIONS
GSM/GPRS Handsets

GENERAL DESCRIPTION

The ADP3522 is a multifunction power system chip optimized for GSM/GPRS handsets, especially those based on the Analog Devices AD20msp430 system solution with 1.8 V digital baseband processors, such as the AD6525, AD6526, and AD6528. It contains six LDOs, one to power each of the critical GSM subblocks. Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm. The charge circuit maintains low current charging during the initial charge phase and provides an end of charge (EOC) signal when a Li-Ion battery is being charged. This product also meets the market trend of reduced size with a new LFCSP package. Its footprint is only 5 mm × 5 mm and yet offers excellent thermal performance due to the exposed die attached paddle.

The ADP3522 is specified over the temperature range of –20°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADP3522–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

(–20°C ≤ T_A ≤ +85°C, VBAT = VBAT2 = 3 V–5.5 V, CVSIM = CVCORE = CVAN = CVMEM = 2.2 µF, VTCXO = 0.22 µF, CVRTC = 0.1 µF, CVBAT = 10 µF, minimum loads applied on all outputs, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHUTDOWN SUPPLY CURRENT	ICC					
VBAT ≤ 2.5 V (Deep Discharged Lockout Active)		VBAT = VBAT2 = 2.3 V		15	40	µA
2.5 V < VBAT ≤ 3.2 V (UVLO Active)		VBAT = VBAT2 = 3.0 V		30	55	µA
VBAT > 3.2 V		VBAT = VBAT2 = 4.0 V		45	80	µA
OPERATING GROUND CURRENT	IGND	VBAT = 3.6 V				
VSIM, VCORE, VMEM, VRTC On		Minimum Loads		225	300	µA
All LDOs On		Minimum Loads		345	450	µA
All LDOs On		Maximum Loads		1.0	3.0	% of Max Load
UVLO ON THRESHOLD	VUVLO	Rising Edge		3.2	3.3	V
UVLO HYSTERESIS				200		mV
DEEP DISCHARGED LOCKOUT ON THRESHOLD	VDDLO	Falling Edge		2.4	2.75	V
DEEP DISCHARGED LOCKOUT HYSTERESIS				100		mV
INPUT HIGH VOLTAGE	V_{IH}					
PWRONIN			1.0			V
TCXOEN, SIMEN, $\overline{\text{CHGEN}}$, GATEIN, SIMVSEL			1.5			V
INPUT LOW VOLTAGE (PWRONIN, TCXOEN, SIMEN, $\overline{\text{CHGEN}}$, SIMVSEL)	V_{IL}				0.3	V
PWRONIN Pin Pull-Down Resistor	R_{PD}		200	1000	5000	kΩ
INPUT HIGH BIAS CURRENT (TCXOEN, SIMEN, $\overline{\text{CHGEN}}$, SIMVSEL)	I_{IH}				1.0	µA
INPUT LOW BIAS CURRENT (PWRONIN, TCXOEN, SIMEN, $\overline{\text{CHGEN}}$, SIMVSEL)	I_{IL}		–1.0			µA
$\overline{\text{PWRONKEY}}$ INPUT HIGH VOLTAGE	V_{IH}		0.7 × VBAT			V
$\overline{\text{PWRONKEY}}$ INPUT LOW VOLTAGE	V_{IL}				0.3 × VBAT	V
$\overline{\text{PWRONKEY}}$ INPUT PULL-UP RESISTANCE TO VBAT			70	100	130	kΩ
THERMAL SHUTDOWN THRESHOLD[2]				160		°C
THERMAL SHUTDOWN HYSTERESIS				45		°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$\overline{\text{ROWX}}$ CHARACTERISTICS						
$\overline{\text{ROWX}}$ Output Low Voltage	V_{OL}	$\overline{\text{PWRONKEY}}$ = Low I_{OL} = 200 µA			0.4	V
$\overline{\text{ROWX}}$ Output High Leakage Current	I_{IH}	$\overline{\text{PWRONKEY}}$ = High V(ROWX) = 5 V			1	µA
SIM CARD LDO (VSIM)						
Output Voltage	VSIM	Line, Load, Temperature SIMVSEL = Low	1.70	1.80	1.90	V
Output Voltage	VSIM	Line, Load, Temperature SIMVSEL = High	2.80	2.85	2.92	V
Line Regulation	ΔVSIM			2		mV
Load Regulation	ΔVSIM	50 µA ≤ I_{LOAD} ≤ 20 mA VBAT = 3.6 V		2		mV
Output Capacitor Required for Stability	C_O		2.2			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV, I_{LOAD} = 20 mA, VSIM = 2.85 V		35	100	mV
DIGITAL CORE LDO (VCORE)						
Output Voltage	VCORE	Line, Load, Temperature	1.75	1.80	1.85	V
Line Regulation	ΔVCORE			2		mV
Load Regulation	ΔVCORE	50 µA ≤ I_{LOAD} ≤ 100 mA VBAT = 3.6 V		8		mV
Output Capacitor Required for Stability	C_O		2.2			µF
RTC LDO REAL-TIME CLOCK LDO/ COIN CELL CHARGER (VRTC)						
Maximum Output Voltage	VRTC	1 µA ≤ I_{LOAD} ≤ 10 µA	1.86	1.95	2.0	V
Maximum Output Current		VRTC = 0.5 V		4.0		mA
Off Reverse Input Current	I_L	VRTC = 1.90 V, VBAT = 1.70 V, T_A = 25°C			0.5	µA
Output Capacitor Required for Stability	C_O		0.1			µF
ANALOG LDO (VAN)						
Output Voltage	VAN	Line, Load, Temperature	2.50	2.55	2.60	V
Line Regulation	ΔVAN			2		mV
Load Regulation	ΔVAN	50 µA ≤ I_{LOAD} ≤ 180 mA, VBAT = 3.6 V		11		mV
Output Capacitor Required for Stability	C_O		2.2			µF
Ripple Rejection	ΔVBAT/ ΔVAN[3]	f = 217 Hz (t = 4.6 ms) VBAT = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 180 mA VBAT = 3.6 V		80		µV rms
Dropout Voltage		V_O = $V_{INITIAL}$ – 100 mV, I_{LOAD} = 180 mA		160	400	mV

ELECTRICAL CHARACTERISTICS[1]

(–20°C ≤ T_A ≤ +85°C, VBAT = VBAT2 = 3 V–5.5 V, CVSIM = CVCORE = CVAN = CVMEM = 2.2 μF, VTCXO = 0.22 μF, CVRTC = 0.1 μF, CVBAT = 10 μF, minimum loads applied on all outputs, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TCXO LDO (VTCXO)						
Output Voltage	VTCXO	Line, Load, Temperature	2.711	2.75	2.789	V
Line Regulation	ΔVTCXO			2		mV
Load Regulation	ΔVTCXO	50 μA ≤ I_{LOAD} ≤ 20 mA, VBAT = 3.6 V		2		mV
Output Capacitor Required for Stability	C_O		0.22			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 20 mA		160	300	mV
Ripple Rejection	ΔVBAT/ ΔVTCXO	f = 217 Hz (t = 4.6 ms) VBAT = 3.6 V	65			dB
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz I_{LOAD} = 20 mA, VBAT = 3.6 V		80		μV rms
MEMORY LDO (VMEM)						
Output Voltage-3	VMEM	Line, Load, Temperature	2.740	2.80	2.850	V
Output Voltage-1.8	VMEM	Line, Load, Temperature	1.80	1.85	1.90	V
Line Regulation	ΔVMEM			2		mV
Load Regulation	ΔVMEM	50 μA < I_{LOAD} < 150 mA VBAT = 3.6 V		12		mV
Output Capacitor Required for Stability	C_O		2.2			μF
Dropout Voltage-3		V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 150 mA		160	360	mV
REFOUT						
Output Voltage	VREFOUT	Line, Load, Temperature	1.19	1.21	1.23	V
Line Regulation	ΔVREFOUT	Min Load		0.2		mV
Load Regulation	ΔVREFOUT	0 μA < I_{LOAD} < 50 μA VBAT = 3.6 V		0.5		mV
Ripple Rejection	ΔVBAT/ ΔVREFOUT	f = 217 Hz (t = 4.6 ms)	65	75		dB
Maximum Capacitive Load	C_O		100			pF
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz		40		μV rms
RESET GENERATOR ($\overline{\text{RESET}}$)						
Output High Voltage	V_{OH}	I_{OH} = +500 μA	V_{MEM} – 0.25			V
Output Low Voltage	V_{OL}	I_{OL} = –500 μA			0.25	V
Output Current	I_{OL}/I_{OH}	V_{OL}= 0.25 V, V_{OH} = V_{MEM} – 0.25 V		1		mA
Delay Time per Unit Capacitance Applied to RESCAP Pin	t_D		0.6	1.2	2.4	ms/nF
BATTERY VOLTAGE DIVIDER						
Divider Ratio	BATSNS/ MVBAT	TCXOEN = High	2.32	2.35	2.37	
Divider Impedance at MVBAT	Z_O		59.5	85	110	kΩ
Divider Leakage Current		TCXOEN = Low			1	μA
Divider Resistance		TCXOEN = High	215	300	385	kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BATTERY CHARGER						
Charger Output Voltage	BATSNS	4.35 V ≤ CHRIN ≤ 10 V[3] $\overline{CHGEN}$ = Low, No Load	4.150	4.200	4.250	V
		CHRIN = 10 V $\overline{CHGEN}$ = Low, No Load 0°C < T_A < 50°C	4.155		4.250	V
Load Regulation	ΔBATSNS	CHRIN = 5 V 0 ≤ CHRIN – ISENSE < Current Limit Threshold $\overline{CHGEN}$ = Low			15	mV
CHRDET On Threshold	CHRIN – VBAT		30	90	150	mV
CHRDET Hysteresis				40		mV
CHRDET Off Delay[4]		CHRIN < VBAT		6		ms/nF
CHRIN Supply Current		CHRIN = 5 V		0.6		mA
Current Limit Threshold	CHRIN – ISENSE					
High Current Limit (UVLO Not Active)		CHRIN = 5 V DC VBAT = 3.6 V $\overline{CHGEN}$ = Low	142	160	190	mV
		CHRIN = 5 V DC VBAT = 3.6 V $\overline{CHGEN}$ = Low 0°C < T_A < 50°C	149	160	180	mV
Low Current Limit (UVLO Active)		VBAT = 2 V $\overline{CHGEN}$ = Low CHRIN = 5 V – 10 V		20	35	mV
ISENSE Bias Current				200		µA
EOC Signal Threshold	CHRIN – ISENSE	CHRIN = 5 V DC VBAT > 4.0 V $\overline{CHGEN}$ = Low		14	35	mV
EOC Reset Threshold	VBAT	$\overline{CHGEN}$ = Low	3.82	3.96	4.10	V
GATEDR Transition Time	t_R, t_F	CHRIN = 5 V VBAT > 3.6 V $\overline{CHGEN}$ = High, C_L = 2 nF	0.1		1	µs
GATEDR High Voltage	V_{OH}	CHRIN = 5 V VBAT = 3.6 V $\overline{CHGEN}$ = High GATEIN = High I_{OH} = –1 mA	4.5			V
GATEDR Low Voltage	V_{OL}	CHRIN = 5 V VBAT = 3.6 V $\overline{CHGEN}$ = High GATEIN = Low I_{OL} = 1 mA			0.5	V
Output High Voltage (EOC, CHRDET)	V_{OH}	I_{OH} = –250 µA	V_{MEM} – 0.25			V
Output Low Voltage (EOC, CHRDET)	V_{OL}	I_{OL} = 250 µA			0.25	V

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]This feature is intended to protect against catastrophic failure of the device. Maximum allowed operating junction temperature is 125°C. Operation beyond 125°C could cause permanent damage to the device.
[3]No isolation diode is present between the charger input and the battery.
[4]Delay set by external capacitor on the RESCAP pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

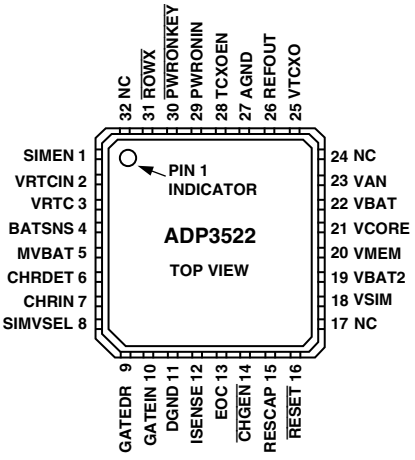
Voltage on Any Pin with Respect to
Any GND Pin . . . . . –0.3 V to +10 V
Voltage on Any Pin May Not Exceed VBAT, with the Following Exceptions: CHRIN, BASE, ISENSE
Storage Temperature Range . . . . . –65°C to +150°C
Operating Ambient Temperature Range . . . . . –20°C to +85°C
Maximum Junction Temperature . . . . . 125°C
θ_{JA}, Thermal Impedance (LFCSP 5 mm × 5 mm)
4-Layer JEDEC PCB . . . . . 32°C/W
2-Layer SEMI PCB . . . . . 108°C/W
Lead Temperature Range (Soldering, 60 sec.) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ORDERING GUIDE

Model	Memory LDO Output	Temperature Range	Package Option
ADP3522ACP-3	2.80 V	–20°C to +85°C	CP-32
ADP3522ACP-1.8	1.80 V	–20°C to +85°C	CP-32

PIN CONFIGURATION



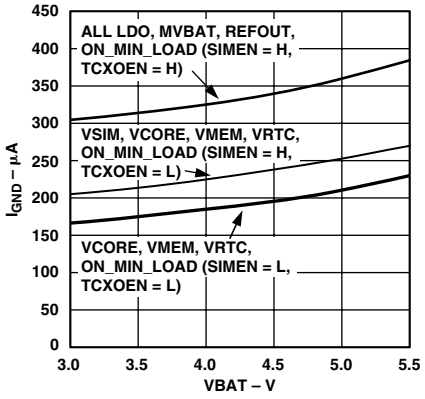
PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	SIMEN	SIM LDO Enable
2	VRTCIN	RTC LDO Input Voltage
3	VRTC	Real-Time Clock Supply/ Coin Cell Battery Charger
4	BATSNS	Battery Voltage Sense Input
5	MVBAT	Divided Battery Voltage Output
6	CHRDET	Charge Detect Output
7	CHRIN	Charger Input Voltage
8	SIMVSEL	Programs VSIM Output; Low: 1.8 V
9	GATEDR	Charger Drive Output
10	GATEIN	Microprocessor Charger Gate Control Input
11	DGND	Digital Ground
12	ISENSE	Charge Current Sense Input
13	EOC	End of Charge Output
14	$\overline{\text{CHGEN}}$	Charge Enable Control Input
15	RESCAP	Reset Delay Time
16	$\overline{\text{RESET}}$	Main Reset, Open Drain
17, 24, 32	NC	No Connection
18	VSIM	SIM LDO Output
19	VBAT2	Battery Input Voltage 2
20	VMEM	Memory LDO Output
21	VCORE	Digital Core LDO Output
22	VBAT	Battery Input Voltage
23	VAN	Analog LDO Output
25	VTCXO	TCXO LDO Output
26	REFOUT	Output Reference
27	AGND	Analog Ground
28	TCXOEN	TCXO LDO Enable and MVBAT Enable
29	PWRONIN	Power On/Off Signal from Microprocessor
30	$\overline{\text{PWRONKEY}}$	Power On/Off Key
31	$\overline{\text{ROWX}}$	Power Key Interface Output

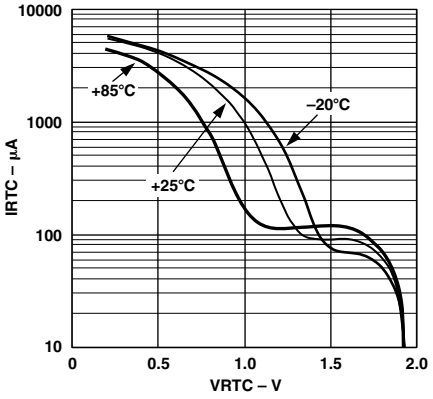
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3522 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

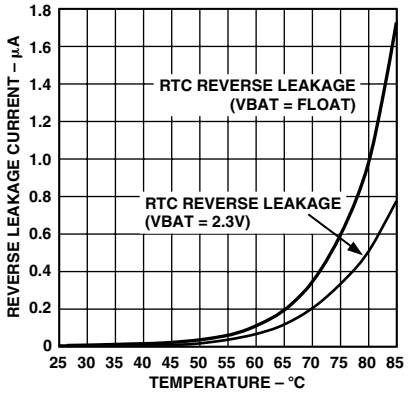




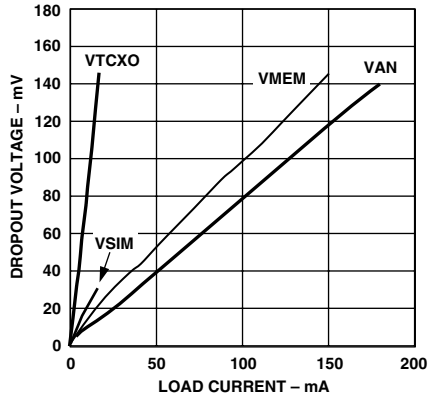
TPC 1. Ground Current vs. Battery Voltage



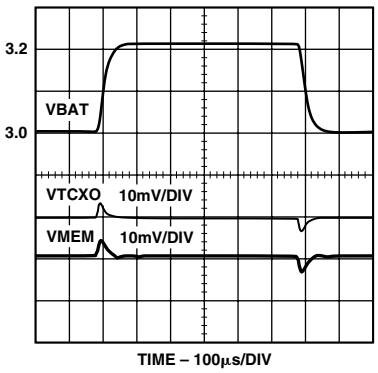
TPC 2. RTC I/V Characteristic



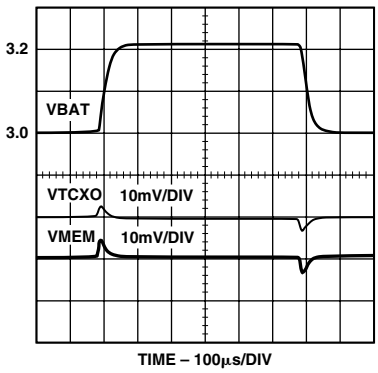
TPC 3. VRTC Reverse Leakage Current vs. Temperature



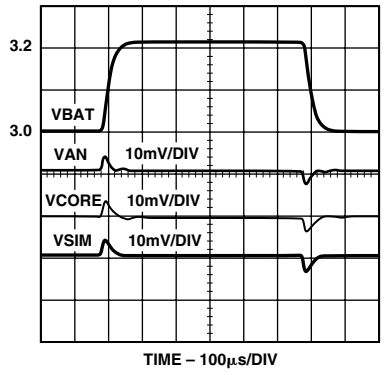
TPC 4. Dropout Voltage vs. Load Current



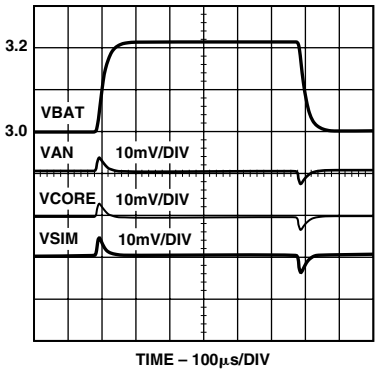
TPC 5. Line Transient Response, Minimum Loads



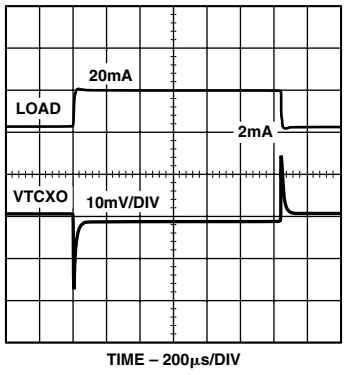
TPC 6. Line Transient Response, Maximum Loads



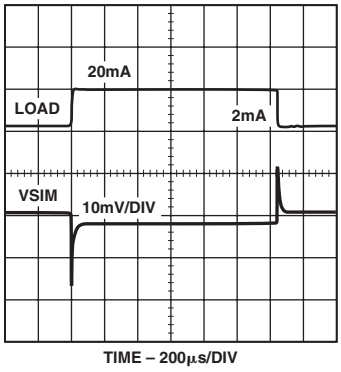
TPC 7. Line Transient Response, Minimum Loads



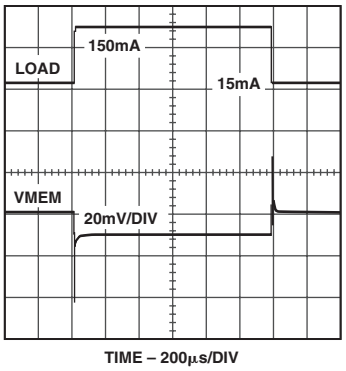
TPC 8. Line Transient Response, Maximum Loads



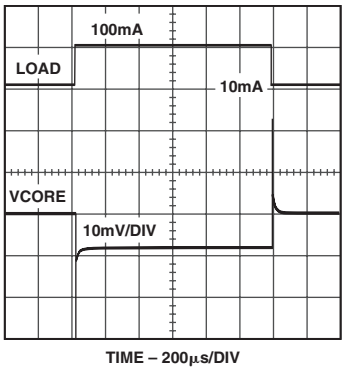
TPC 9. VTCXO Load Step



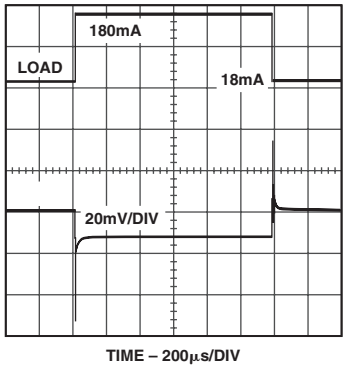
TPC 10. VSIM Load Step



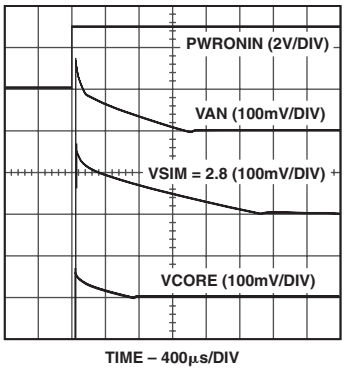
TPC 11. VMEM Load Step



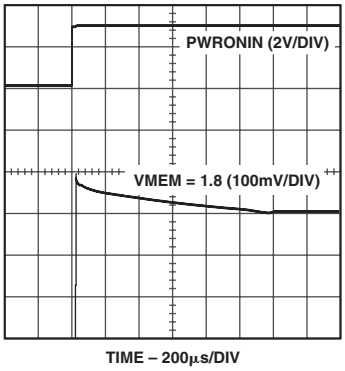
TPC 12. VCORE Load Setup



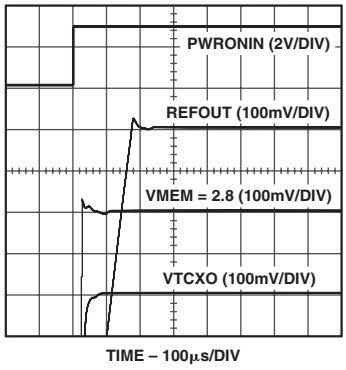
TPC 13. VAN Load Step



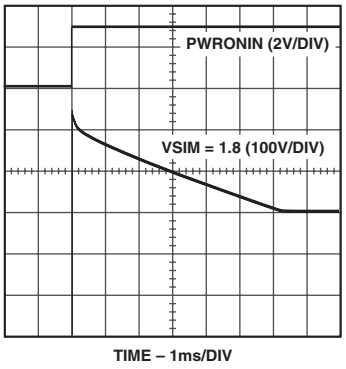
TPC 14. Turn On Transient by PWRONIN, Minimum Load (Part 1)



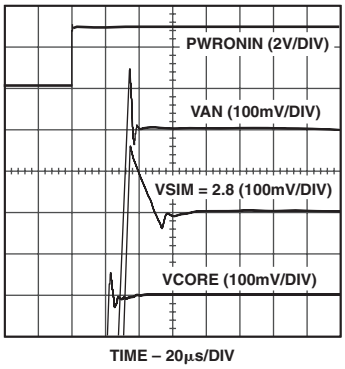
TPC 15. Turn On Transient by PWRONIN, Minimum Load (Part 2)



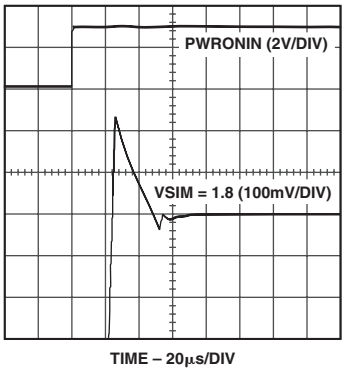
TPC 16. Turn On Transient by PWRONIN, Minimum Load (Part 3)



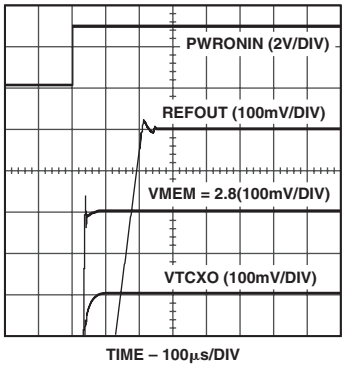
TPC 17. Turn On Transient by PWRONIN, Minimum Load (Part 4)



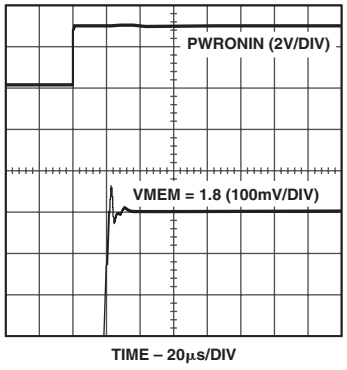
TPC 18. Turn On Transient by PWRONIN, Maximum Load (Part 1)



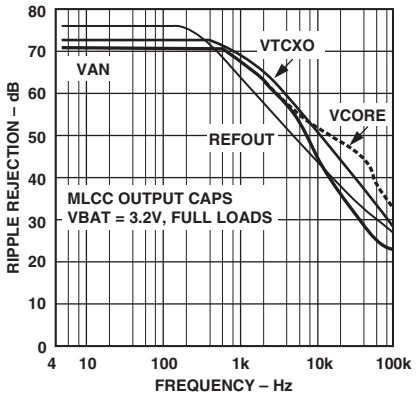
TPC 19. Turn On Transient by PWRONIN, Maximum Load (Part 2)



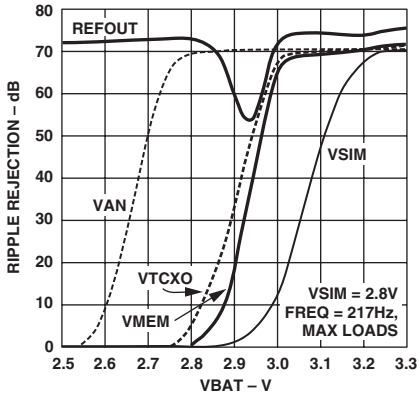
TPC 20. Turn On Transient by PWRONIN, Maximum Load (Part 3)



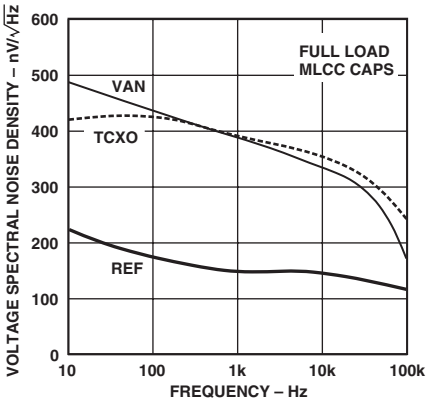
TPC 21. Turn On Transient by PWRONIN, Maximum Load (Part 4)



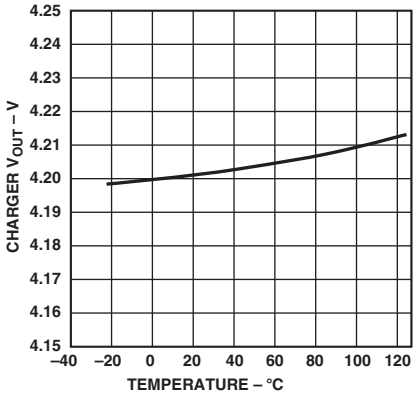
TPC 22. Ripple Rejection vs. Frequency



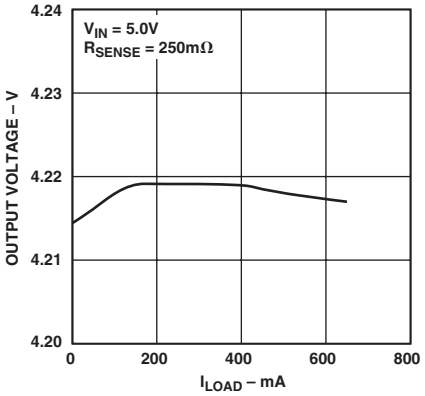
TPC 23. Ripple Rejection vs. Battery Voltage



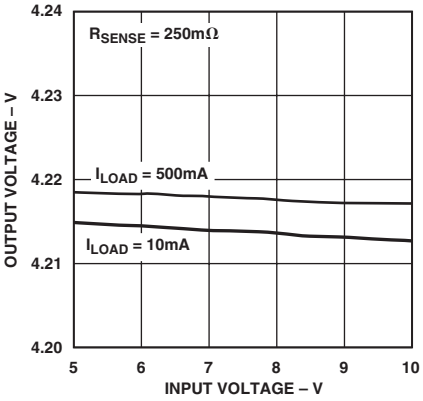
TPC 24. Output Noise Density



TPC 25. Charger V_{OUT} vs. Temperature, V_{IN} = 5.0 V, I_{LOAD} = 10 mA



TPC 26. Charger V_{OUT} vs. I_{LOAD} (V_{IN} = 5.0 V)



TPC 27. Charger V_{OUT} vs. V_{IN}

Table I. LDO Control Logic

STATE NO. PHONE STATUS	DDLO	UVLO	CHRDET	$\overline{\text{PWRONKEY}}$	PWRONIN	TCXOEN	SIMEN	VSIM	VCORE	VMEM	VRTC	VAN	VTCXO	REFOUT	MVBAT
State No. 1 Battery Deep Discharged	L	X	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
State No. 2 Phone Off	H	L	X	X	X	X	X	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
State No. 3 Phone Off, Turn-On Allowed	H	H	L	H	L	X	X	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
State No. 4 Charger Applied	H	H	H	X	X	X	L	OFF	ON	ON	ON	ON	ON	ON	ON*
State No. 5 Phone Turned On by User Key	H	H	X	L	X	X	L	OFF	ON	ON	ON	ON	ON	ON	ON*
State No. 6 Deep Sleep	H	H	L	H	H	L	H	ON	ON	ON	ON	OFF	OFF	OFF	OFF
State No. 7 Active	H	H	L	H	H	H	H	ON	ON	ON	ON	ON	ON	ON	ON
State No. 8 Reset SIM Card	H	H	L	H	H	H	L	OFF	ON	ON	ON	ON	ON	ON	ON

*The state of MVBAT is determined by TCXOEN. When TCXOEN is high, MVBAT is ON.

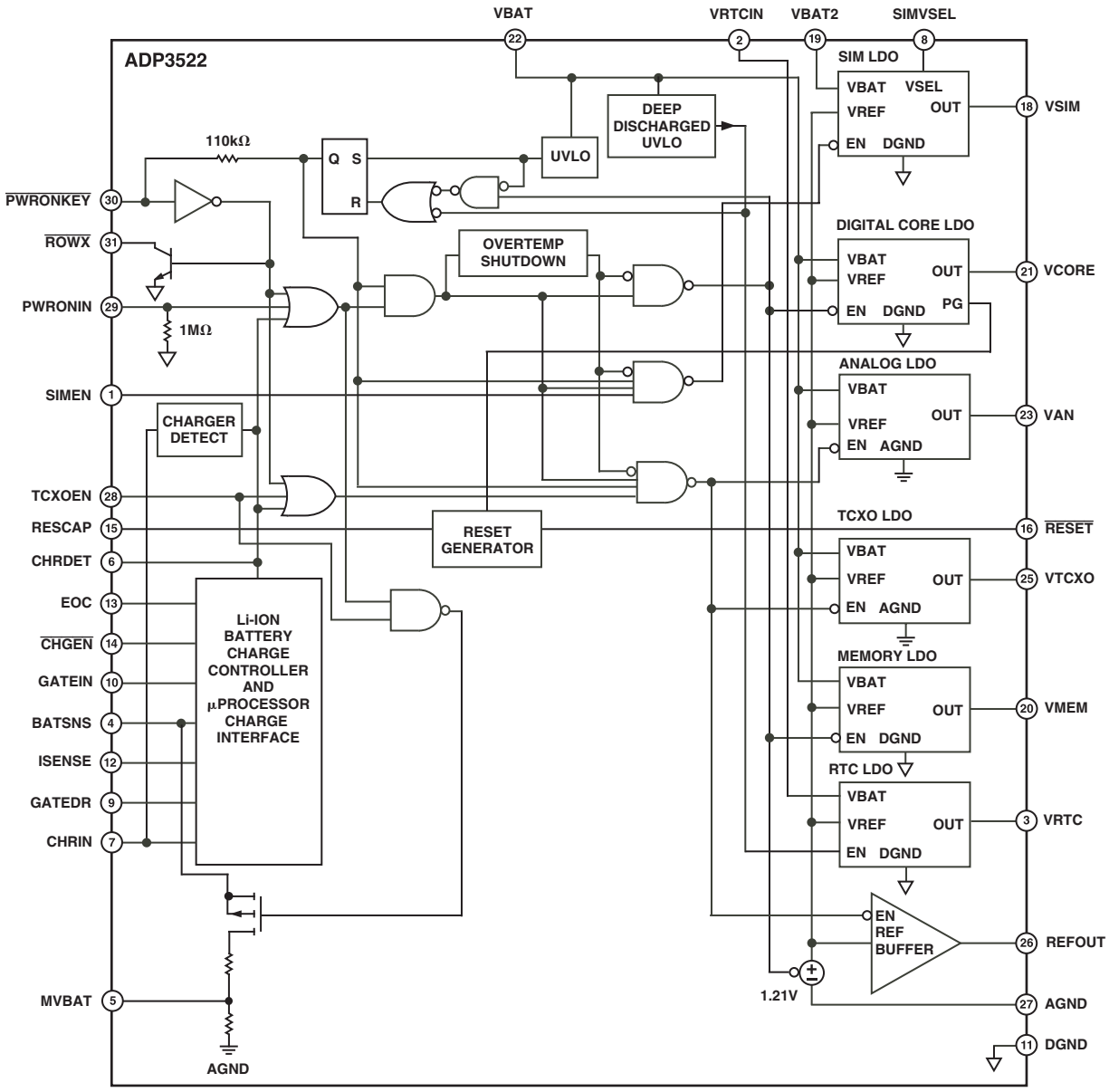


Figure 1. Functional Block Diagram

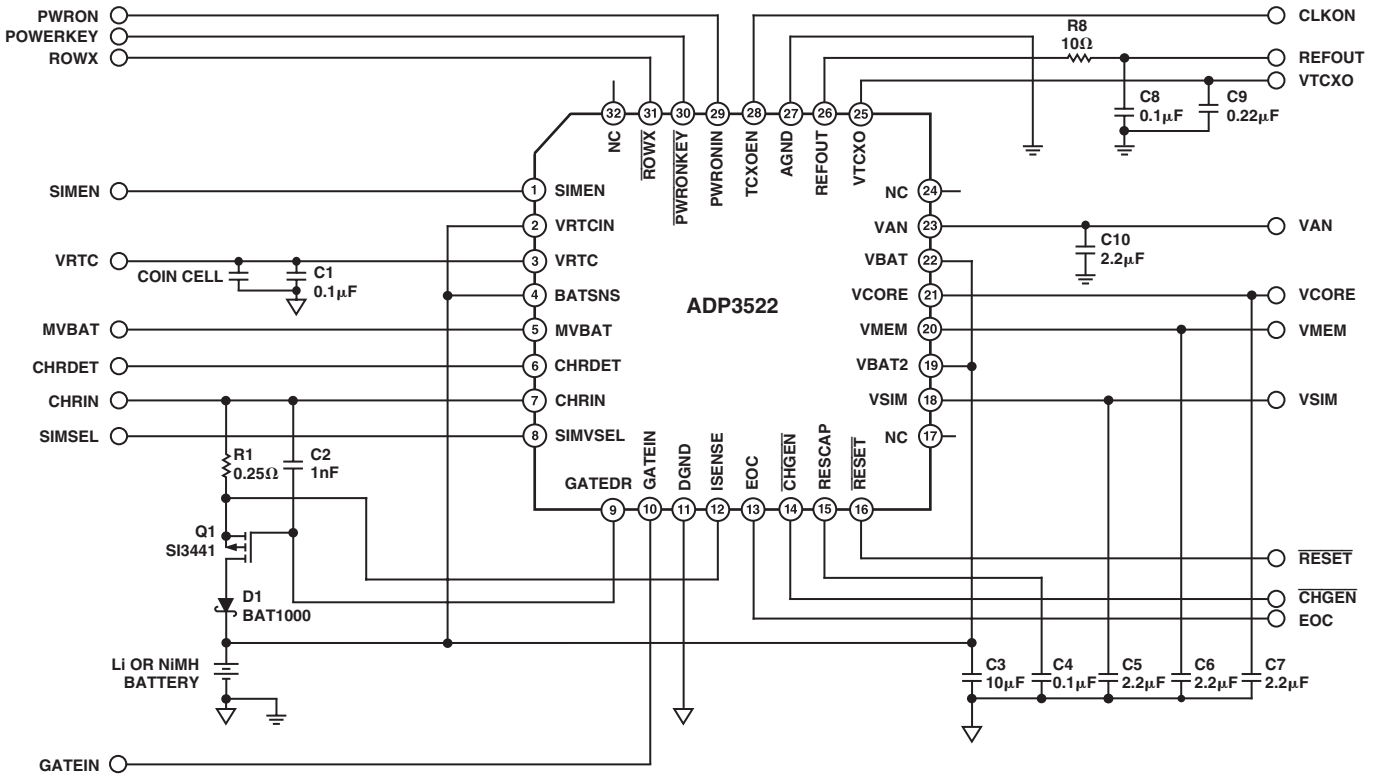


Figure 2. Typical Application Circuit

THEORY OF OPERATION

The ADP3522 is a power management chip optimized for use with GSM baseband chipsets in handset applications. Figure 1 shows a block diagram of the ADP3522. The ADP3522 contains several blocks, such as:

- Six low dropout regulators (SIM, core, analog, crystal oscillator, memory, real-time clock)
- Reset generator
- Buffered precision reference
- Lithium ion charge controller and processor interface
- Power on/off logic
- Undervoltage lockout
- Deep discharge lockout

These functions have traditionally been done either as a discrete implementation or as a custom ASIC design. The ADP3522 combines the benefits of both worlds by providing an integrated standard product where every block is optimized to operate in a GSM environment while maintaining a cost competitive solution.

Figure 2 shows the external circuitry associated with the ADP3522. Only a minimal number of support components are required.

Input Voltage

The input voltage range of the ADP3522 is 3 V to 5.5 V and is optimized for a single Li-Ion cell or three NiMH cells. The type of battery, the SIM LDO output voltage, and the memory LDO output voltage will all affect the amount of power that the ADP3522 needs to dissipate. The thermal impedance of the CSP package is 32°C/W for a JEDEC standard 4-layer board.

The end of charge voltage for high capacity NiMH cells can be as high as 5.5 V. This results in a worst-case power dissipation for the ADP3522-1.8 to be as high as 1.6 W for NiMH cells. The power dissipation for the ADP3522-3 is slightly lower at 1.45 W.

A fully charged Li-Ion battery is 4.25 V, where the ADP3522-3 can dissipate a maximum power of 0.85 W. However, the ADP3522-1.8 can have a maximum dissipation of 1.0 W.

High battery voltages normally occur when the battery is being charged and the handset is not in conversation mode. In this mode, there is a relatively light load on the LDOs. The worst-case power dissipation should be calculated based on the actual load currents and voltages used.

Figure 3 shows the maximum power dissipation as a function of the input voltage. Figure 4 shows the maximum allowable power dissipation as a function of the ambient temperature.

Low Dropout Regulators (LDOs)

The ADP3522 high performance LDOs are optimized for their given functions by balancing quiescent current, dropout voltage, regulation, ripple rejection, and output noise. 2.2 µF tantalum or MLCC ceramic capacitors are recommended for use with the core, memory, SIM, and analog LDOs. A 0.22 µF capacitor is recommended for the TCXO LDO.

Digital Core LDO (VCORE)
The digital core LDO supplies the baseband circuitry in the handset (baseband processor and baseband converter). The LDO has been optimized for very low quiescent current at light loads as this LDO is on whenever the handset is switched on.

Memory LDO (VMEM)
The memory LDO supplies the system memory as well as the subsystems of the baseband processor including memory IO, display, and melody interfaces. It is capable of delivering up to 150 mA of current and is available for either 1.8 V or 3 V based systems. The LDO has also been optimized for low quiescent current and will power up at the same time as the core LDO.

Analog LDO (VAN)
This LDO has the same features as the core LDO. It has furthermore been optimized for good low frequency ripple rejection for use with the baseband converter sections in order to reject the ripple coming from the RF power amplifier. VAN is rated to 180 mA, which is sufficient to supply the analog section of the baseband converter, such as the AD6521, as well as the microphone and speaker.

TCXO LDO (VTCXO)
The TCXO LDO is intended as a supply for a temperature compensated crystal oscillator, which needs its own ultralow noise supply. VTCXO is rated for 20 mA of output current and is turned on along with the analog LDO when TCXOEN is asserted. Note that the ADP3522 has been optimized for use with the AD6534 (Othello One™).

RTC LDO (VRTC)
The RTC LDO is capable of charging rechargeable Lithium or capacitor-type backup coin cells to run the real-time clock module. The RTC LDO supplies current both for charging the coin cell and for the RTC module. In addition, it features a very low quiescent current since this LDO is running all the time, even when the handset is switched off. It also has reverse current protection with low leakage, which is needed when the main battery is removed and the coin cell supplies the RTC module.

SIM LDO (VSIM)
The SIM LDO generates the voltage needed for 1.8 V or 3 V SIMs. It is rated for 20 mA of supply current and can be controlled completely independently of the other LDOs.

Applying a low to SIMEN shuts down the SIM LDO. A discharge circuit is active when SIMEN is low. This pulls the SIM LDO's output down when the LDO is disabled.

SIMVSEL allows the SIM LDO to be programmed for either 1.8 V or 2.8 V. Asserting a high on SIMVSEL sets the output for 2.8 V.

SIMEN and SIMVSEL allow the baseband processor to properly sequence the SIM supply when determining which type of SIM module is present.

Reference Output (REFOUT)
The reference output is a low noise, high precision reference with a guaranteed accuracy of 1.5% overtemperature. The maximum output current of the REFOUT supply is limited to 50 μA.

Power ON/OFF
The ADP3522 handles all issues regarding the powering ON and OFF of the handset. It is possible to turn on the ADP3522 in three different ways:

- Pulling the $\overline{\text{PWRONKEY}}$ low
- Pulling the PWRONIN high
- CHRIN exceeds CHRDET threshold

Pulling the $\overline{\text{PWRONKEY}}$ low is the normal way of turning on the handset. This will turn on all the LDOs, except the SIM LDO, as long as the $\overline{\text{PWRONKEY}}$ is held low. When the VCORE LDO comes into regulation, the $\overline{\text{RESET}}$ timer is started. After timing out, the $\overline{\text{RESET}}$ pin goes high, allowing the baseband processor to start up. With the baseband processor running, it can poll the $\overline{\text{ROWX}}$ pin of the ADP3522 to determine if the $\overline{\text{PWRONKEY}}$ has been depressed and pull PWRONIN high. Once the PWRONIN is taken high, the $\overline{\text{PWRONKEY}}$ can be released. Note that by monitoring the $\overline{\text{ROWX}}$ pin, the baseband processor can detect a second $\overline{\text{PWRONKEY}}$ and press and turn the LDOs off in an orderly manner. In this way, the $\overline{\text{PWRONKEY}}$ can be used for ON/OFF control.

Pulling the PWRONIN pin high is how the alarm in the real-time clock module will turn the handset on. Asserting PWRONIN will turn the core and memory LDOs on, starting up the baseband processor.

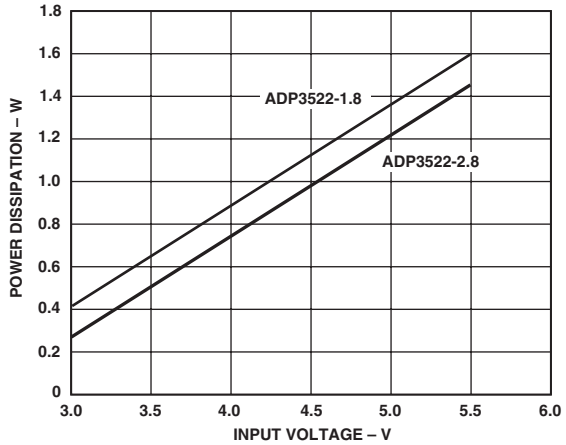


Figure 3. Power Dissipation vs. Input Voltage

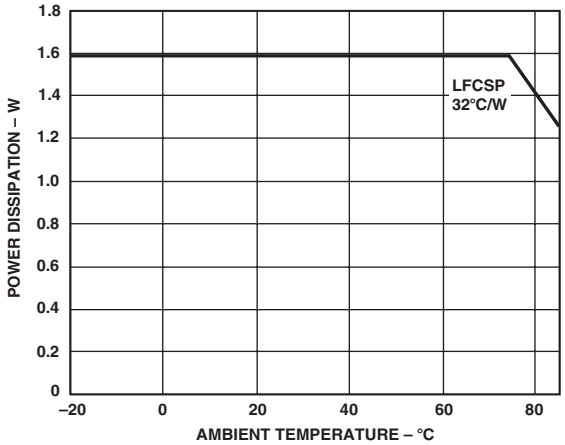


Figure 4. Allowable Package Power Dissipation vs. Temperature

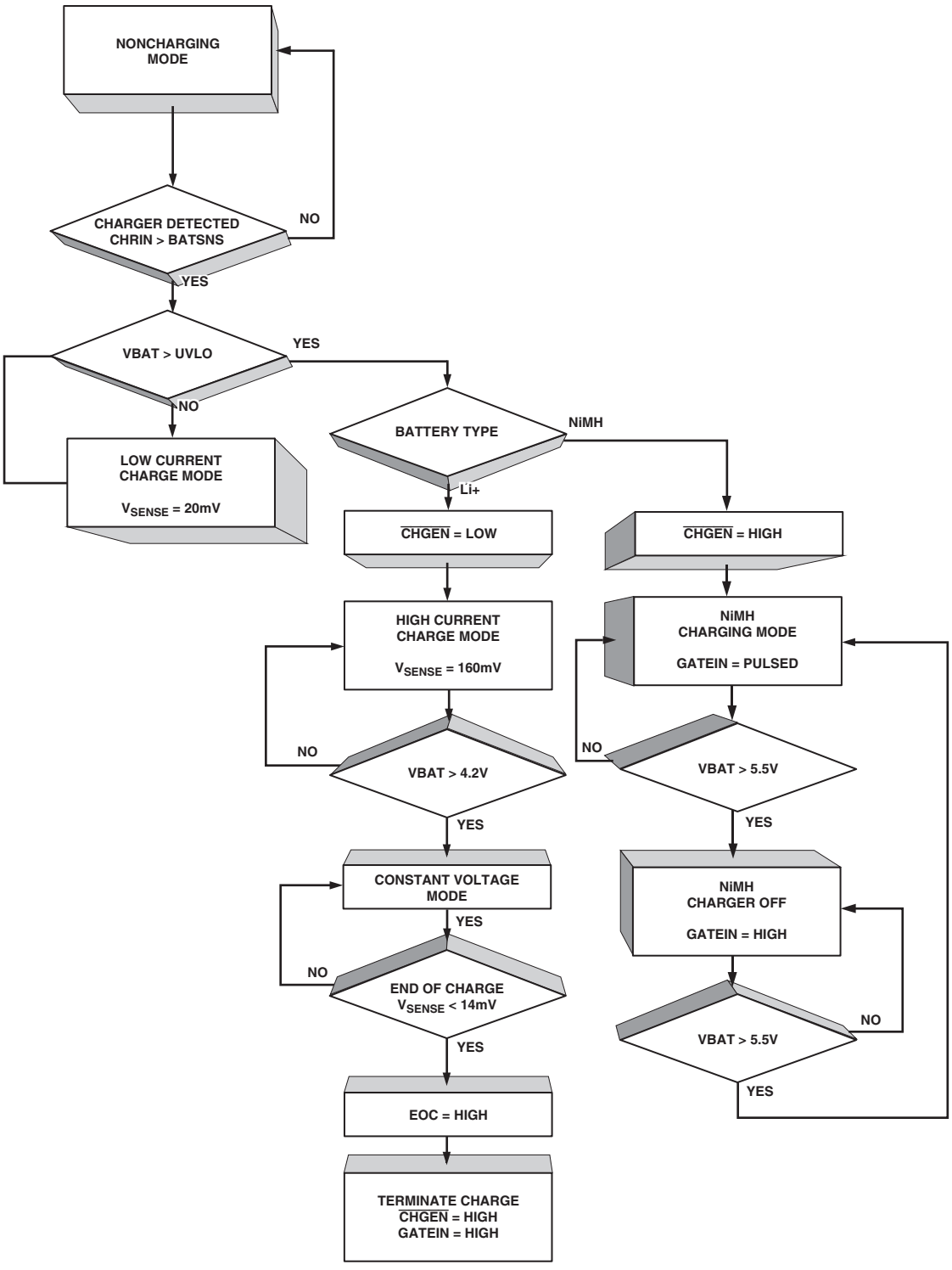


Figure 5. Battery Charger Flow Chart

Applying an external charger can also turn the handset on. This will turn on all the LDOs, except the SIM LDO, again starting up the baseband processor. Note that if the battery voltage is below the undervoltage lockout threshold, applying the adapter will not start up the LDOs.

Deep Discharge Lockout (DDLO)
The DDLO block in the ADP3522 shuts down the handset in the event that the software fails to turn off the phone when the battery voltage drops below 2.9 V to 3.0 V. The DDLO will shut down the handset when the battery falls below 2.4 V to prevent further discharge and damage to the battery.

The DDLO will also shut down the RTC LDO when the main battery is removed. This will prevent reverse current from discharging the backup coin cell.

Undervoltage Lockout (UVLO)
The UVLO function in the ADP3522 prevents startup when the initial voltage of the battery is below the 3.2 V threshold. If the battery voltage is this low with no load, there is insufficient capacity left to run the handset. When the battery is greater than 3.2 V, such as inserting a fresh battery, the UVLO comparator trips, and the threshold is reduced to 3.0 V. This allows the handset to start normally until the battery decays to below 3.0 V.

Once the system is started and the core and memory LDOs are up and running, the UVLO function is entirely disabled. The ADP3522 is then allowed to run until the battery voltage reaches the DDLO threshold, typically 2.4 V. Normally, the battery voltage is monitored by the baseband processor, which usually shuts the phone off at a battery voltage of around 3.0 V.

If the handset is off and the battery voltage drops below 3.0 V, the UVLO circuit disables startup and puts the ADP3522 into UVLO shutdown mode. In this mode, the ADP3522 draws very low quiescent current, typically 30 μA. In DDLO mode, the ADP3522 draws 15 μA of quiescent current. NiMH batteries can reverse polarity if the 3-cell battery voltage drops below 3.0 V, which will degrade the batteries' performance. Lithium ion batteries will lose their capacity if overdischarged repeatedly, so minimizing the quiescent currents helps prevent battery damage.

RESET
The ADP3522 contains a reset circuit that is active both at power-up and power-down. The $\overline{\text{RESET}}$ pin is held low at initial power-up. An internal power good signal is generated by the core LDO when its output is up, starting the reset delay timer. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.2\frac{ms}{nF} \times C_{RESCAP} \quad (1)$$

At power-off, $\overline{\text{RESET}}$ will be kept low to prevent any baseband processor starts.

Overtemperature Protection
The maximum die temperature for the ADP3522 is 125°C. If the die temperature exceeds 160°C, the ADP3522 will disable all the LDOs except the RTC LDO. The LDOs will not be re-enabled before the die temperature is below 125°C, regardless of the state of $\overline{\text{PWRONKEY}}$, PWRONIN, and CHRDET. This ensures that the handset will always power off before the ADP3522 exceeds its absolute maximum thermal ratings.

Battery Charging
The ADP3522 battery charger can be used with lithium ion (Li+) and nickel metal hydride (NiMH) batteries. The charger initialization, trickle charging, and Li+ charging are implemented in hardware. Battery type determination and NiMH charging must be implemented in software.

The charger block works in three different modes:

1. Low current (trickle) charging
2. Lithium ion charging
3. Nickel metal hydride charging

See Figure 5 for the charger flow chart.

Charge Detection
The ADP3522 charger block has a detection circuit that determines if an adapter has been applied to the CHRIN pin. If the adapter voltage exceeds the battery voltage by 100 mV, the CHRDET output will go high. If the adapter is then removed and the voltage at the CHRIN pin drops to only 50 mV above the BATSNS pin, CHRDET goes low. The CHRDET signal is not asserted if the battery voltage is below the UVLO threshold.

Trickle Charging
When the battery voltage is below the UVLO threshold, the charge current is set to the low current limit, or about 10% of the full charge current. The low current limit is determined by the voltage developed across the current sense resistor. Therefore, the trickle charge current can be calculated by

$$I_{CHR(TRICKLE)} = \frac{20\,mV}{R_{SENSE}} \quad (2)$$

Trickle charging is performed for deeply discharged batteries to prevent undue stress on either the battery or the charger. Trickle charging will continue until the battery voltage exceeds the UVLO threshold.

Once the UVLO threshold has been exceeded, the charger will switch to the default charge mode, the LDOs will start up, and the baseband processor will start to run. The processor must then poll the battery to determine which chemistry is present and set the charger to the proper mode. Control of the charge mode, Li+ or NiMH, is determined by the $\overline{\text{CHGEN}}$ input.

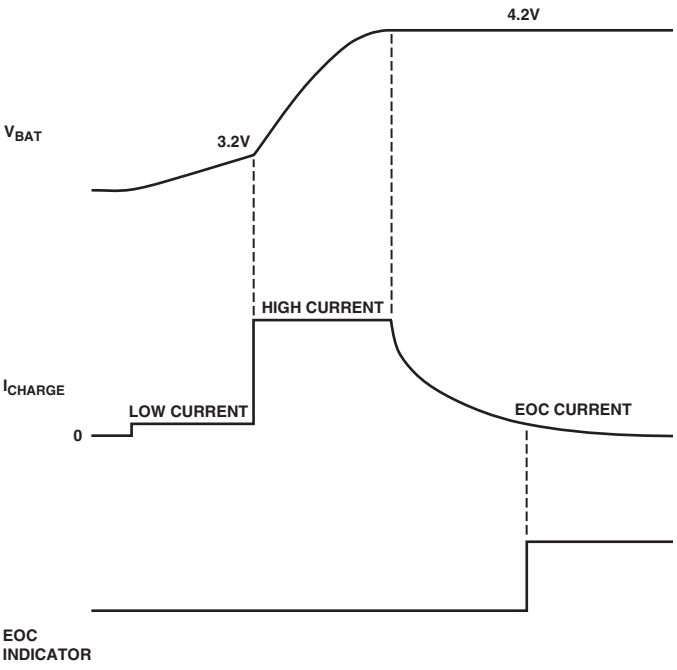


Figure 6. Lithium Ion Charging Diagram

Lithium Ion Charging

For lithium ion charging, the $\overline{\text{CHGEN}}$ input must be low. This allows the ADP3522 to continue charging the battery at the full current. The full charge current can be calculated by using

$$I_{CHR(FULL)} = \frac{160\,mV}{R_{SENSE}} \quad (3)$$

If the voltage at BATSNS is below the charger's output voltage of 4.2 V, the battery will continue to charge in the constant current mode. If the battery has reached the final charge voltage, a constant voltage is applied to the battery until the charge current has reduced to the charge termination threshold. The charge termination threshold is determined by the voltage across the sense resistor. If the battery voltage is above 4.0 V and the voltage across the sense resistor has dropped to 14 mV, then an end of charge signal is generated—the EOC output goes high (see Figure 6).

The baseband processor can either let the charger continue to charge the battery for an additional amount of time or terminate the charging. To terminate the charging, the processor must pull the GATEIN pin high and the $\overline{\text{CHGEN}}$ pin high.

NiMH Charging

For NiMH charging, the processor must pull the $\overline{\text{CHGEN}}$ pin high. This disables the internal Li+ mode control of the gate drive pin. The gate drive must now be controlled by the baseband processor. By pulling GATEIN high, the GATEDR pin is driven high, turning the PMOS off. By pulling the GATEIN pin low, the GATEDR pin is driven low, and the PMOS is turned on. So, by pulsing the GATEIN input, the processor can charge a NiMH battery. Note that when charging NiMH cells, a current limited adapter is required.

During the PMOS off periods, the battery voltage needs to be monitored through the MVBAT pin. The battery voltage is continually polled until the final battery voltage is reached. Then the charge can either be terminated or the frequency of the pulsing reduced. An alternative method of determining the end of charge is to monitor the temperature of the cells and terminate the charging when a rapid rise in temperature is detected.

Battery Voltage Monitoring

The battery voltage can be monitored at MVBAT during charging and discharging to determine the condition of the battery. An internal resistor divider can be connected to BATSNS when both the digital and analog baseband sections are powered up. To enable MVBAT, both PWRONIN and TCXOEN must be high.

The ratio of the voltage divider is selected so that the 2.4 V maximum input of the AD6521's auxiliary ADC will correspond with the maximum battery voltage of 5.5 V. The divider will be disconnected from the battery when the baseband sections are powered down.

APPLICATION INFORMATION

Input Capacitor Selection

For the input (VBAT, VBAT2, and VRTCIN) of the ADP3522, a local bypass capacitor is recommended; use a 10 μF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size but may not be cost effective. A lower cost alternative may be to use a 10 μF tantalum capacitor with a small (1 μF to 2 μF) ceramic in parallel.

Separate inputs for the SIM LDO and the RTC LDO are supplied for additional bypassing or filtering. The SIM LDO has VBAT2 as its input and the RTC LDO has VRTCIN.

LDO Capacitor Selection

The performance of any LDO is a function of the output capacitor. The core, memory, SIM, and analog LDOs require a 2.2 μF capacitor and the TCXO LDO requires a 0.22 μF capacitor. Larger values may be used, but the overshoot at startup will increase slightly. If a larger output capacitor is desired, be sure to check that the overshoot and settling time are acceptable for the application.

All the LDOs are stable with a wide range of capacitor types and ESR (anyCAP® technology). The ADP3522 is stable with extremely low ESR capacitors (ESR ~ 0) such as multilayer ceramic capacitors (MLCC), but care should be taken in their selection. Note that the capacitance of some capacitor types shows wide variations over temperature or with dc voltage. A good quality dielectric, X7R or better, capacitor is recommended.

The RTC LDO can have a rechargeable coin cell or an electric double-layer capacitor as a load, but an additional 0.1 μF ceramic capacitor is recommended for stability and best performance.

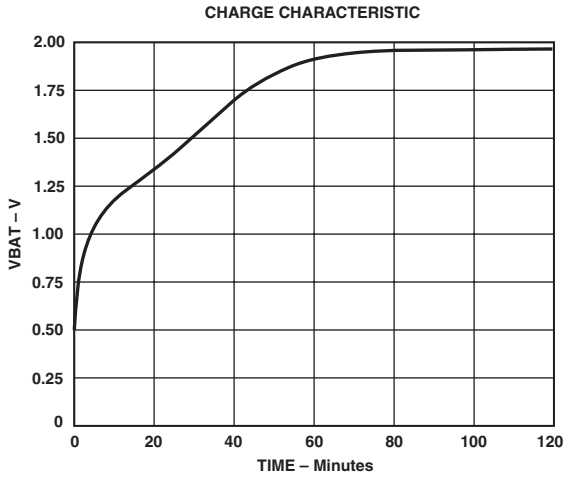


Figure 7. Kanebo PAS621 Charge Characteristic

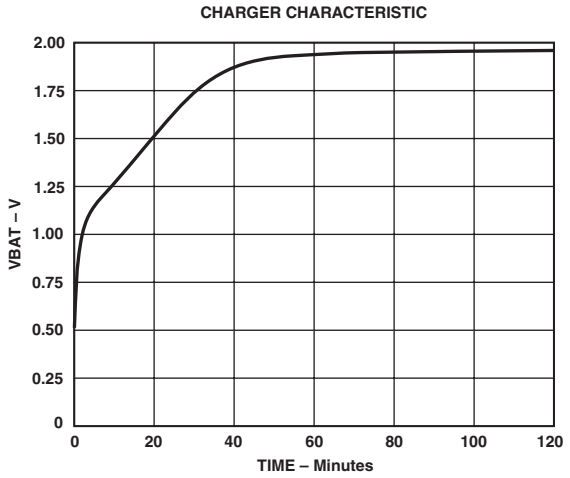


Figure 8. Panasonic EECEM0E204A Charge Characteristic

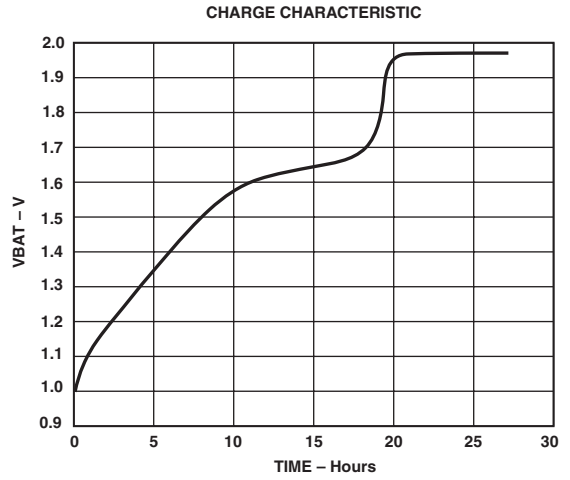


Figure 9. Maxell TC614 Charge Characteristic

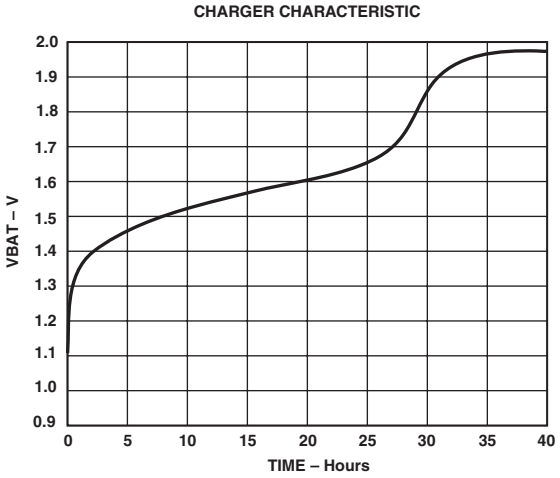


Figure 10. Seiko TS621 Charge Characteristic

RTC Backup Coin Cell Selection

The choice of the backup cell is based upon size, cost, and capacity. It must be able to support the RTC module's current requirement and voltage range, as well as handle the charge current supplied by the ADP3522 (see TPC 2). Check with the coin cell vendor if the ADP3522's charge current profile is acceptable.

Some suitable coin cells are the electric double layer capacitors available from Kanebo (PAS621), Seiko (XC621), or Panasonic (EECEM0E204A). They have a small physical size (6.8 mm diameter) and a nominal capacity of 0.2 F to 0.3 F, giving hours of backup time. Rechargeable lithium coin cells, such as the TC614 from Maxell or the TS621 from Seiko, are also small in size but have higher capacity than the double layer capacitors, resulting in longer backup times. Typical charge curves for each cell type are shown in Figures 7 through 10. Note that the rechargeable lithium type coin cells generally come precharged from the vendor.

$\overline{\text{RESET}}$ Capacitor Selection

$\overline{\text{RESET}}$ is held low at power up. An internal power-good signal starts the reset delay when the core LDO is up. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.2\frac{ms}{nF} \times C_{RESCAP} \quad (4)$$

A 100 nF capacitor will produce a 120 ms reset delay. The current capability of $\overline{\text{RESET}}$ is minimal (a few hundred nA) when VCORE is off to minimize power consumption. When VCORE is on, $\overline{\text{RESET}}$ is capable of driving 500 µA.

Setting the Charge Current

The ADP3522 is capable of charging both lithium ion and NiMH batteries. For NiMH batteries, the charge current is limited by the adapter. For lithium ion batteries, the charge

current is programmed by selecting the sense resistor, R1 (see Figure 2).

The lithium ion charge current is calculated using

$$I_{CHR} = \frac{V_{SENSE}}{R1} = \frac{160\,mV}{R1} \quad (5)$$

where V_{SENSE} is the high current limit threshold voltage. Or if the charge current is known, $R1$ can be found:

$$R1 = \frac{V_{SENSE}}{I_{CHR}} = \frac{160\,mV}{I_{CHR}} \quad (6)$$

Similarly the trickle charge current and the end of charge current can be calculated:

$$I_{TRICKLE} = \frac{V_{SENSE}}{R1} = \frac{20\,mV}{R1} \quad (7)$$

$$I_{EOC} = \frac{V_{SENSE}}{R1} = \frac{14\,mV}{R1} \quad (8)$$

Example: Assume an 800 mA-H capacity lithium ion battery and a 1 C charge rate. $R1$ = 200 mΩ. Then $I_{TRICKLE}$ = 100 mA and I_{EOC} = 70 mA.

Appropriate sense resistors are available from the following vendors:

- Vishay Dale
- IRC
- Panasonic

Charger FET Selection

The type and size of the pass transistor is determined by the threshold voltage, input-output voltage differential, and charge current. The selected PMOS must satisfy the physical, electrical, and thermal design requirements.

To ensure proper operation, the minimum VGS the ADP3522 can provide must be enough to turn on the FET. The available gate drive voltage can be estimated using the following:

$$V_{GS} = V_{ADAPTER(MIN)} - V_{GATEDR} - V_{SENSE} \quad (9)$$

where

$V_{ADAPTER(MIN)}$ is the minimum adapter voltage.

V_{GATEDR} is the gate drive "low" voltage, 0.5 V.

V_{SENSE} is the maximum high current limit threshold voltage.

The difference between the adapter voltage ($V_{ADAPTER}$) and the final battery voltage (V_{BAT}) must exceed the voltage drop due to the blocking diode, the sense resistor, and the on resistance of the FET at maximum charge current.

$$V_{DS} = V_{ADAPTER} - V_{DIODE} - V_{SENSE} - V_{BAT} \quad (10)$$

Then the $R_{DS(ON)}$ of the FET can be calculated:

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} \quad (11)$$

The thermal characteristics of the FET must be considered next. The worst-case dissipation can be determined using:

$$P_{DISS} = V_{ADAPTER(MAX)} - V_{DIODE} - V_{SENSE} - UVLO \times I_{CHR} \quad (12)$$

It should be noted that the adapter voltage can be either preregulated or nonregulated. In the preregulated case, the difference between the maximum and minimum adapter voltage is probably not significant. In the unregulated case, the adapter voltage can have a wide range specified. However, the maximum voltage specified is usually with no load applied. So, the worst-case power dissipation calculation will often lead to an overspecified pass device. In either case, it is best to determine the load characteristics of the adapter to optimize the charger design.

For example:

$V_{ADAPTER(MIN)}$ = 5.0 V

$V_{ADAPTER(MAX)}$ = 6.5 V

V_{DIODE} = 0.5 V at 800 mA

V_{GATEDR} = 0.5 V

V_{SENSE} = 160 mV

V_{GS} = 5 V – 0.5 V – 0.160 V = 4.3 V. So choose a low threshold voltage FET.

$$V_{DS} = V_{ADAPTER(MIN)} - V_{DIODE} - V_{SENSE} - V_{BAT} \quad (13)$$

$$V_{DS} = 5\,V - 0.5\,V - 0.160\,V - 4.2\,V = 140\,mV$$

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} = \frac{140\,mV}{800\,mA} = 175\,m\Omega \quad (14)$$

$$P_{DISS} = (V_{ADAPTER(MAX)} - V_{DIODE} - V_{SENSE} - UVLO) \times I_{CHR} \quad (15)$$

$$P_{DISS} = (6.5\,V - 0.5\,V - 0.160\,V - 3.2\,V) \times 0.8\,A = 2.1\,W$$

Appropriate PMOS FETs are available from the following vendors:

- Siliconix
- IR
- Fairchild

Charger Diode Selection

The diode, D1, shown in Figure 2 is used to prevent the battery from discharging through the PMOS' body diode into the charger's internal bias circuits. A Schottky diode is recommended to minimize the voltage difference from the charger to the battery and the power dissipation. Choose a diode with a current rating high enough to handle the battery charging current and a voltage rating greater than VBAT. The blocking diode is required for both lithium and nickel battery types.

Printed Circuit Board Layout Considerations
Use the following general guidelines when designing printed circuit boards:

1. Connect the battery to the VBAT, VBAT2, and VRTCIN pins of the ADP3522. Locate the input capacitor as close to the pins as possible.
2. VAN and VTCXO output capacitors should be returned to AGND.
3. VCORE, VMEM, and VSIM output capacitors should be returned to DGND.
4. Split the ground connections. Use separate traces or planes for the analog, digital, and power grounds and tie them together at a single point, preferably close to the battery return.
5. Run a separate trace from the BATSNS pin to the battery to prevent voltage drop error in the MVBAT measurement.
6. Kelvin connect the charger's sense resistor by running separate traces to the CHRIN pin and ISENSE pin. Make sure the traces are terminated as close to the resistor's body as possible.
7. Use the best industry practice for thermal considerations during the layout of the ADP3522 and charger components. Careful use of copper area, weight, and multilayer construction all contribute to improved thermal performance.

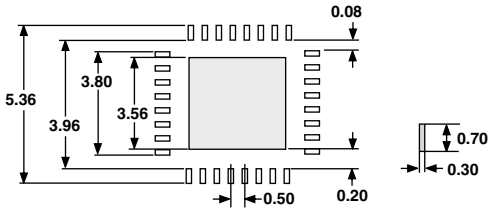
LFCSP Layout Considerations
The CSP package has an exposed die paddle on the bottom that efficiently conducts heat to the PCB. In order to achieve the optimum performance from the CSP package, special consideration must be given to the layout of the PCB. Use the following layout guidelines for the CSP package:

1. The pad pattern is given in Figure 11. The pad dimension should be followed closely for reliable solder joints while maintaining reasonable clearances to prevent solder bridging.
2. The thermal pad of the CSP package provides a low thermal impedance path (approximately 15°C/W) to the PCB. Therefore, the PCB must be properly designed to effectively conduct the heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. See Figure 12 for the recommended via pattern. Note that the via diameter is small. This is to prevent the solder from flowing through the via and leaving voids in the thermal pad solder joint.

   Note that the thermal pad is attached to the die substrate; the thermal planes that the vias attach the package to must be electrically isolated or connected to VBAT. **Do NOT connect the thermal pad to ground**.
3. The solder mask opening should be about 120 microns (4.7 mils) larger than the pad size resulting in a minimum 60 microns (2.4 mils) clearance between the pad and the solder mask.
4. The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm.

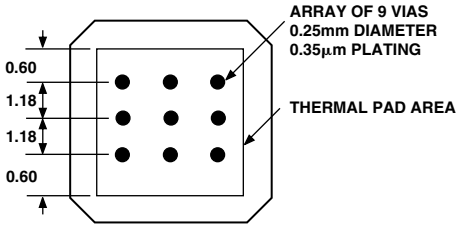
   The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the large size of the thermal pad, eliminating voids may not be possible. Also, if the solder paste coverage is too large, solder joint defects may occur. Therefore, it is recommended to use multiple small openings over a single big opening in designing the paste mask. The recommended paste mask pattern is given in Figure 13. This pattern will result in about 80% coverage, which should not degrade the thermal performance of the package significantly.
5. The recommended paste mask stencil thickness is 0.125 mm. A laser cut stainless steel stencil with trapezoidal walls should be used.

   A "No Clean," Type 3 solder paste should be used for mounting the LFCSP package. Also, a nitrogen purge during the reflow process is recommended.
6. The package manufacturer recommends that the reflow temperature should not exceed 220°C and the time above liquids is less than 75 seconds. The preheat ramp should be 3°C/second or lower. The actual temperature profile depends on the board's density and must be determined by the assembly house as to what works best.



Dimensions shown in millimeters

Figure 11. 5 mm × 5 mm LFCSP Pad Pattern



Dimensions shown in millimeters

Figure 12. 5 mm × 5 mm LFSCP Via Pattern

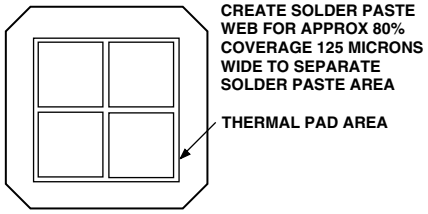
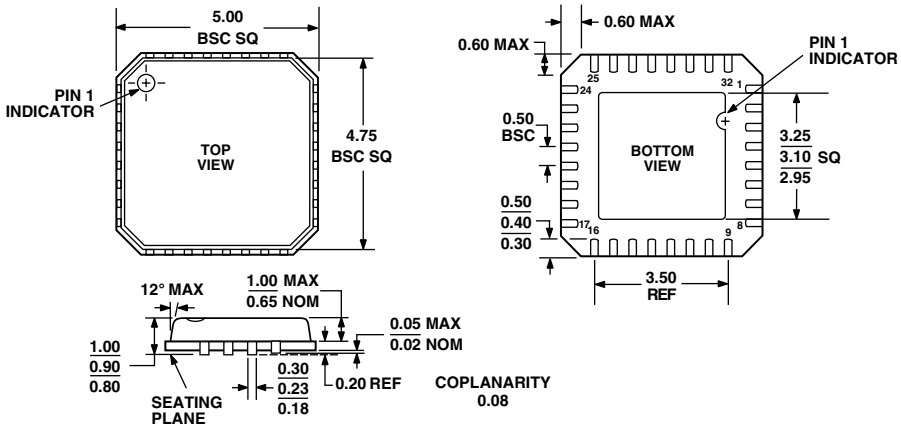


Figure 13. 5 mm × 5 mm LFSCP Solder Paste Mask Pattern

C03535–0–2/03(0)

OUTLINE DIMENSIONS

32-Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

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