Configurable, Dual 2 A/Single 4 A, Synchronous Step-Down DC-to-DC Regulator

ADP2114

FEATURES

Configurable 2 A/2 A or 3 A/1 A dual output load combinations or 4 A combined single output
High efficiency: up to 95%
Input voltage V_{IN}: 2.75 V to 5.5 V
Selectable fixed output: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V or adjustable output voltage to 0.6 V minimum
±1.5% accurate reference voltage
Selectable switching frequency: 300 kHz, 600 kHz, 1.2 MHz or synchronized from 200 kHz to 2 MHz
Optimized gate slew rate for reduced EMI
External synchronization input or internal clock output
Dual-phase, 180° phase shifted PWM channels
Current mode for fast transient response
Pulse skip under light load or forced PWM operation
Input undervoltage lockout (UVLO)
Independent enable inputs and PGOOD outputs
Overcurrent and thermal overload protection
Externally programmable soft start
32-lead 5 mm × 5 mm LFCSP package

APPLICATIONS

Point of load regulation
Telecommunications and networking systems
Consumer electronics
Industrial and Instrumentation
Medical

GENERAL DESCRIPTION

The ADP2114 is a versatile, synchronous step-down, switching regulator that satisfies a wide range of customer point-of-load requirements. The two PWM channels can be configured to deliver independent outputs at 2 A and 2 A (or 3 A/1 A) or can be configured as a single interleaved output capable of delivering 4 A. The two PWM channels are 180° phase shifted to reduce input ripple current and to reduce input capacitance.

The ADP2114 provides high efficiency and operates at switching frequencies of up to 2 MHz. At light loads, the ADP2114 can be set to operate in pulse skip mode for higher efficiency or in forced PWM mode to reduce EMI.

The ADP2114 is designed with an optimized gate slew rate to reduce EMI emissions, allowing it to power sensitive, high performance signal chain circuits. The switching frequency can be set to 300 kHz, 600 kHz, or 1.2 MHz and can be synchronized to an external clock that minimizes the system noise. The bidirectional synchronization pin is also configurable as a 90° out-of-phase output clock, providing the possibility for a stackable multiphase power solution.

TYPICAL APPLICATION CIRCUIT

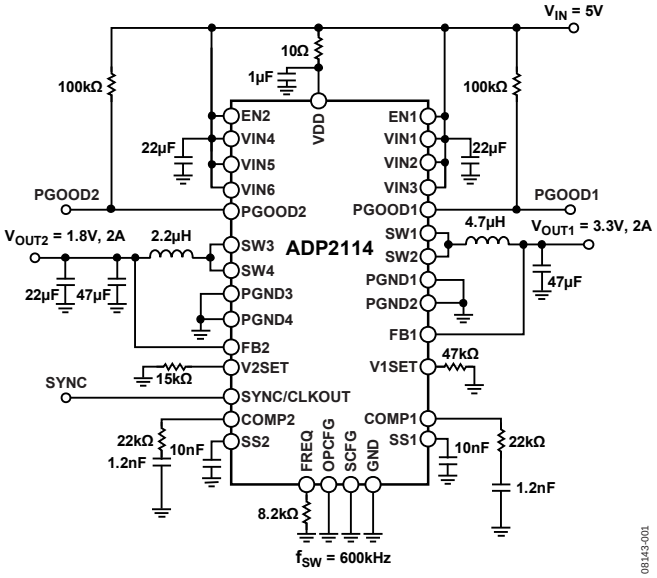

Figure 1.

The ADP2114 input voltage range is from 2.75 V to 5.5 V, and it converts to fixed outputs of 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V that can be set independently for each channel using external resistors. Using a resistor divider, it is also possible to set the output voltage as low as 0.6 V. The ADP2114 operates over the −40°C to +125°C junction temperature range.

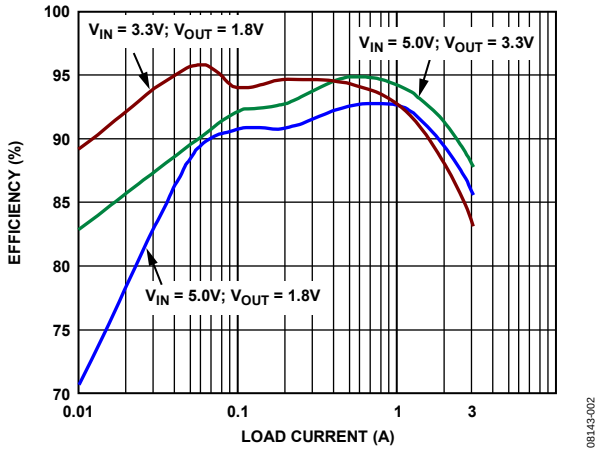

Figure 2. Typical Efficiency vs. Load Current

Rev. 0
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REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

If unspecified, VDD = VINx = EN1 = EN2 = 5.0 V. The minimum and maximum specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_J = 25°C. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VDD Bias Voltage	VDD		2.75		5.5	V
Undervoltage Lockout Threshold	UVLO	V_{DD} rising		2.65	2.75	V
		V_{DD} falling	2.35	2.47		
Undervoltage Lockout Hysteresis				0.18		V
Quiescent Current	IDD_{Ch1}	EN1 = VDD = 5 V, EN2 = GND, V_{FB1} = VDD, OPCFG = GND		1.7	2.5	mA
	IDD_{Ch2}	EN2 = VDD = 5V, EN1 = GND, V_{FB2} = VDD, OPCFG = GND		1.7	2.5	mA
	$IDD_{Ch1+Ch2}$	EN1 = EN2 = VDD = 5 V, V_{FB2} = V_{FB1} = VDD, OPCFG = GND		3.0	4.0	mA
Shutdown Current	IDD_{SD}	EN1 = EN2 = GND, VDD = VINx = 2.75 V to 5.5 V, T_J = −40°C to +115°C		1.0	10	µA
ERROR INTEGRATOR (OTA)						
FB1, FB2 Input Bias Current	I_{FB}	Adjustable output, V_{FBx} = 0.6 V, V1SET, V2SET = VDD or via 82 kΩ to GND		1	65	nA
		Fixed output; V_{FBx} = 1.2 V, V1SET, V2SET via 4.7 kΩ to GND		11	15	µA
Transconductance	g_M			550		µA/V
COMPx VOLTAGE RANGE						
COMPx Zero-Current Threshold	$V_{COMP, ZCT}$	Guaranteed by design		1.12		V
COMPx Clamp High Voltage	$V_{COMP, HI}$	VDD = VINx = 2.75 V to 5.5 V		2.36	2.45	V
COMPx Clamp Low Voltage	$V_{COMP, LO}$	VDD = VINx = 2.75 V to 5.5 V	0.65	0.70		V
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	V_{FB}	Adjustable output, T_J = 25°C, V1SET, V2SET = VDD or via 82 kΩ to GND	0.597	0.600	0.603	V
		Adjustable output, T_J = −40°C to +125°C, V1SET, V2SET = VDD or via 82 kΩ to GND	0.594	0.600	0.606	V
	$V_{FB\ ERROR}$	Fixed output, T_J = 25°C, V1SET, V2SET = GND or via 4.7 kΩ, 8.2 kΩ, 15 kΩ, 27 kΩ, 47 kΩ to GND	−1.0		+1.0	%
		Fixed output, T_J = −40°C to +125°C, V1SET, V2SET = GND or via 4.7 kΩ, 8.2 kΩ, 15 kΩ, 27 kΩ, 47 kΩ to GND	−1.5		+1.5	%
Line Regulation		VDD = VINx = 2.75 V to 5.5 V		0.05		%/V
Load Regulation		VDD = VINx = 2.75 V to 5.5 V		0.03		%/A
OSCILLATOR		All oscillator parameters provided for VDD = 2.75 V to 5.5 V				
Switching Frequency	f_{SW}	FREQ tied to GND	255	300	345	kHz
		FREQ via 8.2 kΩ to GND	510	600	690	kHz
		FREQ via 27 kΩ to GND	1020	1200	1380	kHz
SYNC Frequency Range	f_{SYNC}	$f_{SYNC} = 2 \times f_{SW}$				
		FREQ tied to GND	400		1000	kHz
		FREQ via 8.2 kΩ to GND	800		2000	kHz
		FREQ via 27 kΩ to GND	1600		4000	kHz
SYNC Input Pulse Width			100			ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYNC Pin Capacitance to GND	C_{SYNC}			5		pF
SYNC Input Logic Low	V_{IL_SYNC}				0.8	V
SYNC Input Logic High	V_{IH_SYNC}		2.0			V
Phase Shift Between Channels				180		Degrees
CLKOUT Frequency	f_{CLKOUT}	$f_{CLKOUT} = 2 \times f_{SW}$				
		FREQ tied to GND	510	600	690	kHz
		FREQ via 8.2 kΩ to GND	1020	1200	1380	kHz
		FREQ via 27 kΩ to GND	2040	2400	2760	kHz
CLKOUT Positive Pulse Time	t_{CLKOUT}		100			ns
CLKOUT Rise or Fall Time		C_{CLKOUT} = 20 pF		10		ns
CURRENT LIMIT		All current limit parameters provided for VDD = VINx = 2.75 V to 5.5 V				
Peak Output Current Limit, Channel 1	I_{LIMIT1}	OPCFG tied to GND or via 4.7 kΩ to GND	2.4	3.3	4.0	A
		OPCFG via 8.2 kΩ or 15 kΩ to GND	3.5	4.5	5.3	A
Peak Output Current Limit, Channel 2	I_{LIMIT2}	OPCFG tied to GND or via 4.7 kΩ to GND	2.4	3.3	4.0	A
		OPCFG via 8.2 kΩ or 15 kΩ to GND	1.2	1.9	2.6	A
Current Sense Amplifier Gain	G_{CS}			4		A/V
Hiccup Time		f_{SW} = 300 kHz	10	13.6	17	ms
Number of Cumulative Current Limit Cycles to Go into Hiccup				8		Cycles
SWITCH NODE CHARACTERISTICS						
High-Side, P-Channel $R_{DS\ ON}$[1]		VDD = VINx = 3.3 V		68		mΩ
		VDD = VINx = 5.0 V		52		mΩ
Low-Side, N-Channel $R_{DS\ ON}$[1]		VDD = VINx = 3.3 V		32		mΩ
		VDD = VINx = 5.0 V		27		mΩ
SWx Minimum On Time	$SW_{ON\ MIN}$	VDD = VINx = 2.75 V to 5.5 V		107		ns
SWx Minimum Off Time	$SW_{OFF\ MIN}$	VDD = VINx = 5.5 V		192		ns
		VDD = VINx = 2.75 V		255		ns
SWx Maximum Leakage Current		VDD = VINx = 2.75 V to 5.5 V; ENx = GND, T_J = −40°C to +115°C		0.1	15	µA
ENABLE INPUT						
EN1, EN2 Logic Low Level	EN_{LOW}	VDD = VINx = 2.75 V to 5.5 V			0.8	V
EN1, EN2 Logic High Level	EN_{HI}	VDD = VINx = 2.75 V to 5.5 V	2			V
EN1, EN2 Input Leakage Current	I_{EN_LEAK}	VDD = VINx = ENx = 2.75 V to 5.5 V, T_J = −40°C to +115°C		0.1	1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			150		°C
Thermal Shutdown Hysteresis				25		°C
SOFT START						
SS1, SS2 Pin Current	I_{SS1}, I_{SS2}	VDD = VINx = 2.75 V to 5.5 V; V_{SS} = 0 V	4.8	6.0	7.8	µA
Soft Start Threshold Voltage	V_{SS_THRESH}	VDD = VINx = 2.75 V to 5.5 V		0.65		V
Soft Start Pull-Down Current		VDD = VINx = 2.75 V to 5.5 V; EN = GND	0.5			mA
POWER GOOD		All power good parameters provided for VDD = VINx = 2.75 V to 5.5 V				
Overvoltage PGOODx Rising Threshold[2]				116		%
Overvoltage PGOODx Falling Threshold[2]			100	108	114	%
Undervoltage PGOODx Rising Threshold[2]			85	92	97	%
Undervoltage PGOODx Falling Threshold[2]				84		%
PGOODx Delay				50		µs
PGOODx Leakage Current		V_{PGOODx} = VDD		0.1	1	µA
PGOODx Low Saturation Voltage		I_{PGOODx} = 1 mA		50	110	mV

[1] Pin-to-pin measurements.
[2] The thresholds are expressed in percentage terms of the nominal output voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDD to GND	−0.3 V to +6 V
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6 to PGND1, PGND2, PGND3, PGND4	−0.3 V to +6 V
EN1, EN2, SCFG, FREQ, FB1, FB2, SYNC/CLKOUT, PGOOD1, PGOOD2, V1SET, V2SET, COMP1, COMP2, SS1, SS2 to GND	−0.3 V to (VDD + 0.3 V)
FB1, FB2 to GND	−0.3V to +3.6V
SW1, SW2, SW3, SW4 to PGND1, PGND2, PGND3, PGND4	−0.3 V to (VDD + 0.3 V)
PGND1, PGND2, PGND3, PGND4 to GND	±0.3 V
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6 to VDD	±0.3 V
θ_{JA}, JEDEC 1S2P PCB, Natural Convection	34°C/W
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature (10 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

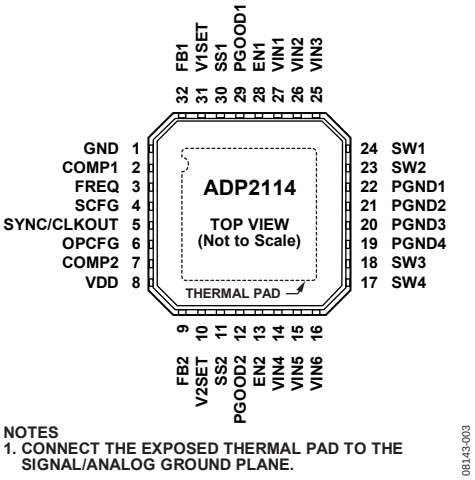

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground for the Internal Analog and Digital Circuits. Connect GND to the signal/analog ground plane before connecting to the power ground.
2	COMP1	Error Amplifier Output for Channel 1. Connect a series RC network from COMP1 to GND to compensate for Channel 1. For multiphase operation, tie COMP1 and COMP2 together.
3	FREQ	Frequency Select Input. Connect this pin through a resistor to GND to set the appropriate switching frequency (see Table 5).
4	SCFG	Synchronization Configuration Input. SCFG configures the SYNC/CLKOUT pin as an input or output. Tie this pin to VDD to configure SYNC/CLKOUT as an output. Tie this pin to GND to configure SYNC/CLKOUT as an input.
5	SYNC/CLKOUT	This is a configurable bidirectional pin (configured with the SCFG pin—see the Pin 4 description for details). When SYNC/CLKOUT is an output, a buffered clock of twice the switching frequency with a phase shift of 90° is available on this pin. When configured as an input, this pin accepts an external clock to which the converters are synchronized. The frequency select resistor, mentioned in the description of Pin 3, must be selected close to the expected switching frequency for stable operation.
6	OPCFG	Operation Configuration Input. Connect this pin through a resistor to GND to set the system mode of operation according to Table 7. This pin can be used to select a peak current limit for each power channel and enable or disable the pulse skip mode.
7	COMP2	Error Amplifier Output for Channel 2. Connect a series RC network from COMP2 to GND to compensate the Channel 2. Tie COMP1 and COMP2 together for multiphase configuration.
8	VDD	Power Supply Input. The power source for the ADP2114 internal circuitry. Connect VDD and VINx with a 10 Ω resistor as close as possible to the ADP2114. Bypass VDD to GND with a 1 µF or greater capacitor.
9	FB2	Feedback Voltage Input for Channel 2. For the fixed output voltage option, connect FB2 to V_{OUT2}. For the adjustable output voltage option, connect this pin to a resistor divider between V_{OUT2} and GND. The reference voltage for the adjustable output voltage option is 0.6 V. With multiphase configurations, connect FB2 to FB1 and then connect them to V_{OUT}.
10	V2SET	Output Voltage Set Pin for Channel 2. Connect this pin through a resistor to GND or tie to VDD to select a fixed output voltage option (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V) or an adjust output voltage for V_{OUT2}. See Table 4 for output voltage selection.
11	SS2	Soft Start Input for Channel 2. Place a capacitor from SS2 to GND to set the soft start period. A 10 nF capacitor sets a 1 ms soft start period. For multiphase configuration, connect SS2 to SS1.
12	PGOOD2	Open-Drain Power Good Output for Channel 2. Place a 100 kΩ pull-up resistor to VDD or any other voltage ≤ 5.5 V; PGOOD2 pulls low when Channel 2 is out of regulation.
13	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 converter and drive EN2 low to turn off Channel 2. Tie EN2 to VDD for startup with VDD. With multiphase configuration, tie EN2 to EN1.

Pin No.	Mnemonic	Description
14	VIN4	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
15	VIN5	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
16	VIN6	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
17	SW4	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 2. Tie SW3 to SW4 and then connect the output LC filter between SW and the output voltage.
18	SW3	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 2. Tie SW3 to SW4 and then connect the output LC filter between SW and the output voltage.
19	PGND4	Power Ground. Source of the low-side internal power MOSFET of Channel 2.
20	PGND3	Power Ground. Source of the low-side internal power MOSFET of Channel 2.
21	PGND2	Power Ground. Source of the low-side internal power MOSFET of Channel 1.
22	PGND1	Power Ground. Source of the low-side internal power MOSFET of Channel 1.
23	SW2	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 1. Tie SW1 to SW2 and connect the output LC filter between SW and the output voltage.
24	SW1	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 1. Tie SW1 to SW2 and connect the output LC filter between SW and the output voltage.
25	VIN3	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
26	VIN2	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
27	VIN1	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
28	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 converter and drive EN1 low to turn off Channel 1. Tie EN1 to VDD for startup with VDD. With multiphase configurations, connect EN1 to EN2.
29	PGOOD1	Open-Drain Power Good Output for Channel 1. Place a 100 kΩ pull-up resistor to VDD or any other voltage ≤ 5.5 V; PGOOD1 pulls low when Channel 1 is out of regulation.
30	SS1	Soft Start Input for Channel 1. Place a capacitor from SS1 to GND to set the soft start period. A 10 nF capacitor sets a 1 ms soft start period. For multiphase configuration, connect SS1 to SS2.
31	V1SET	Output Voltage Set Pin for Channel 1. Connect this pin through a resistor to GND or tie to VDD to select a fixed output voltage option (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V) or an adjustable output voltage for V_{OUT1}. See Table 4 for output voltage selection.
32	FB1	Feedback Voltage Input for Channel 1. For the fixed output voltage option, connect FB1 to V_{OUT1}. For the adjusted output voltage option, connect this pin to a resistor divider between V_{OUT1} and GND. With multiphase configurations, connect FB1 to FB2 and then connect them to V_{OUT}.
	EPAD (EP)	Exposed Thermal Pad. Connect to the signal/analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

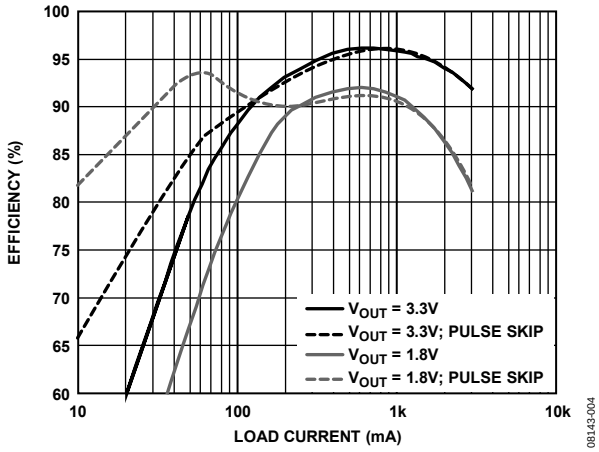

Figure 4. Channel 1 Efficiency vs. Load, V_{IN} = 5 V and f_{sw} = 300 kHz; V_{OUT} = 3.3 V, Inductor Cooper Bussmann DR1050-8R2-R, 8.2 µH, 15 mΩ; V_{OUT} = 1.8 V, Inductor TOKO FDV0620-4R7M, 4.7 µH, 53 mΩ

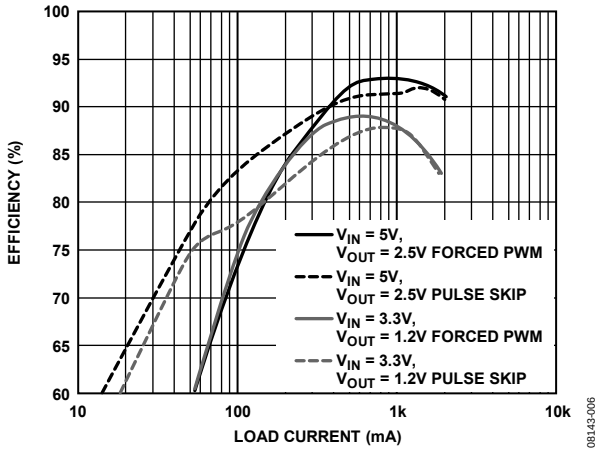

Figure 6. Efficiency vs. Load at f_{SW} = 1.2 MHz; Inductor TOKO FDV0620-1R0M, 1.0 µH, 14 mΩ

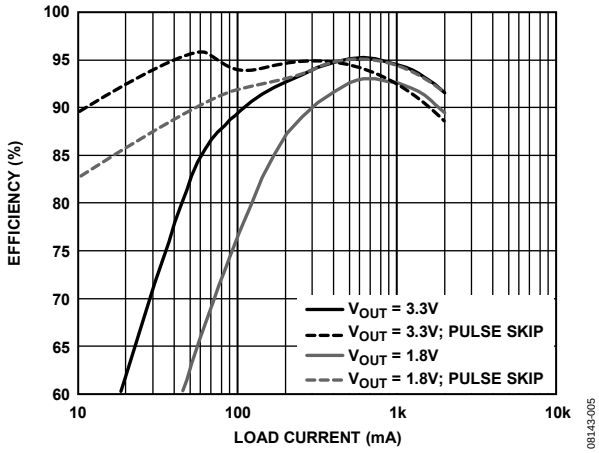

Figure 5. Channel 2 Efficiency vs. Load, V_{IN} = 5 V and f_{SW} = 600 kHz; V_{OUT} = 3.3 V, Inductor TOKO FDV0620-4R7M, 4.7 µH, 53 mΩ; V_{OUT} = 1.8 V, Inductor TOKO FDV0620-2R2M, 2.2 µH, 30 mΩ

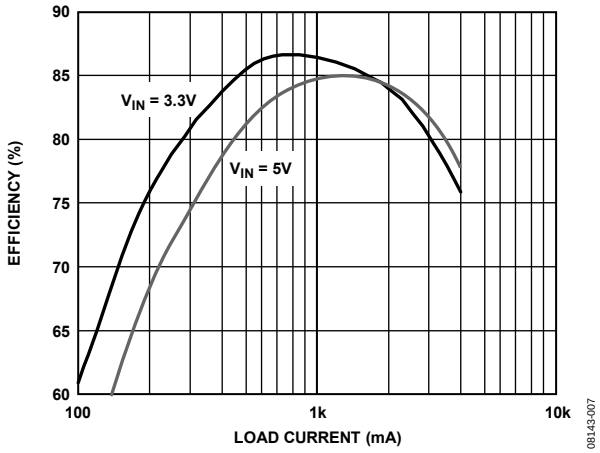

Figure 7. Efficiency Combined Dual-Phase Output, V_{OUT} = 0.8 V and f_{SW} = 1.2 MHz; Inductor TOKO FDV0620-1R0M, 1.0 µH, 14 mΩ

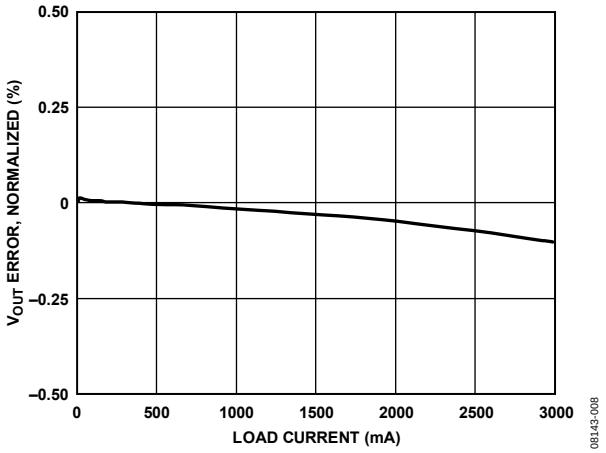

Figure 8. Load Regulation, Channel 1: V_{IN} = 5 V, f_{SW} = 600 kHz, and T_A = 25°C

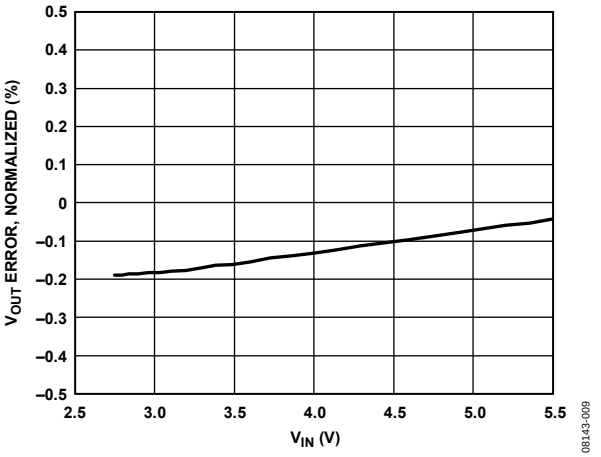

Figure 9. Line Regulation, Channel 1: Load Current = 3 A and f_{SW} = 600 kHz

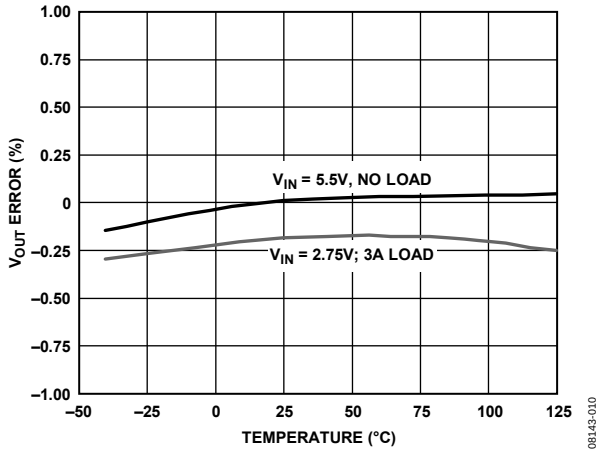

Figure 10. Output Voltage vs. Temperature, Channel 1: V_{OUT} = 0.6 V and f_{SW} = 600 kHz

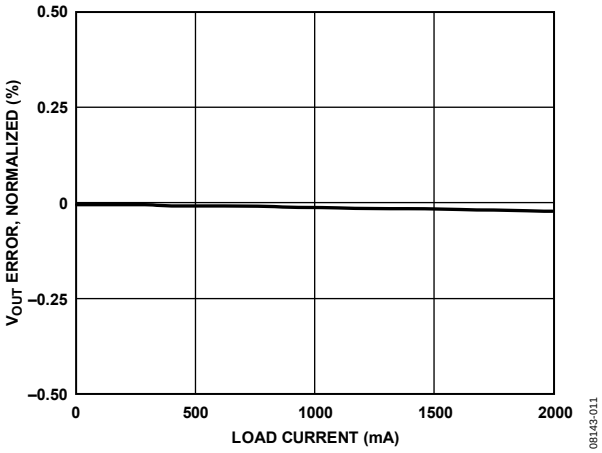

Figure 11. Load Regulation, Channel 2: V_{IN} = 5 V, f_{SW} = 300 kHz, and T_A = 25°C

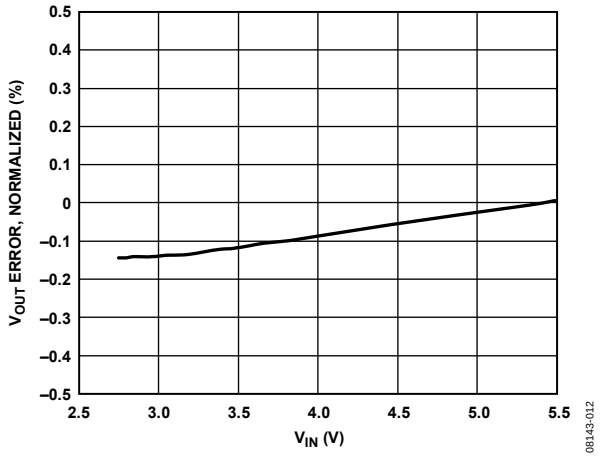

Figure 12. Line Regulation, Channel 2: Load Current = 1 A and f_{SW} = 600 kHz

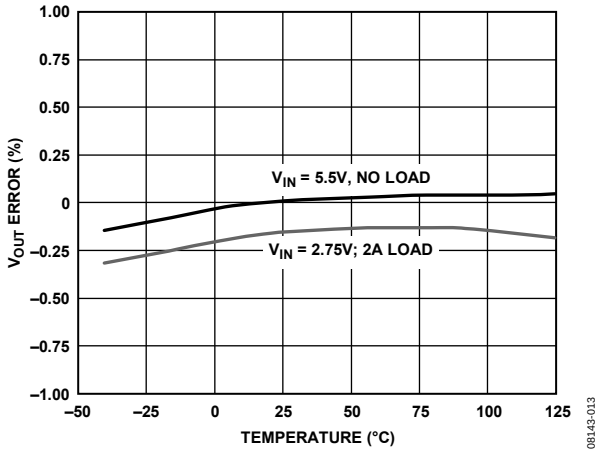

Figure 13. Output Voltage vs. Temperature, Channel 2: V_{OUT} = 1.5 V and f_{SW} = 600 kHz

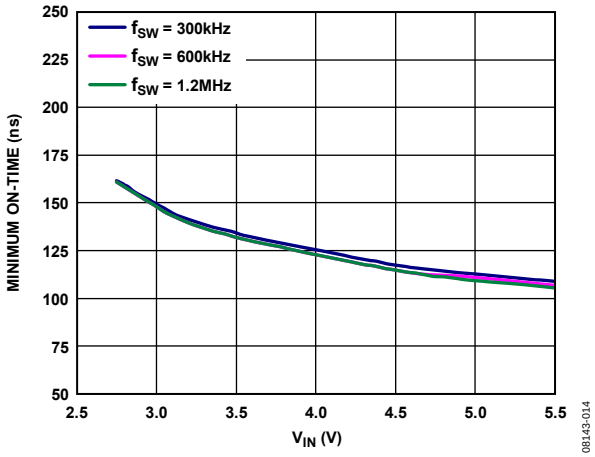

Figure 14. Minimum On-Time, Open Loop, Includes Dead Time

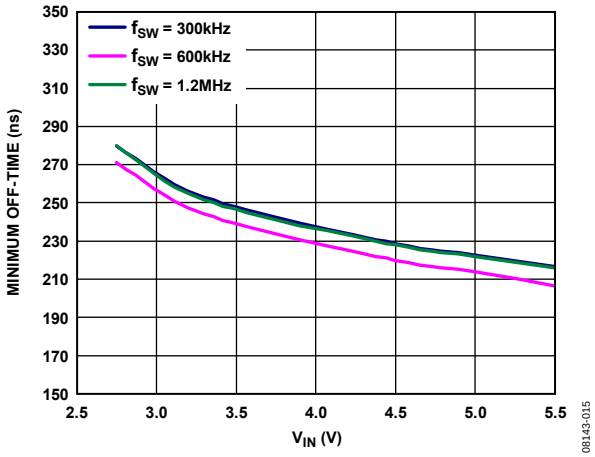

Figure 15. Minimum Off-Time, Open Loop, Includes Dead Time

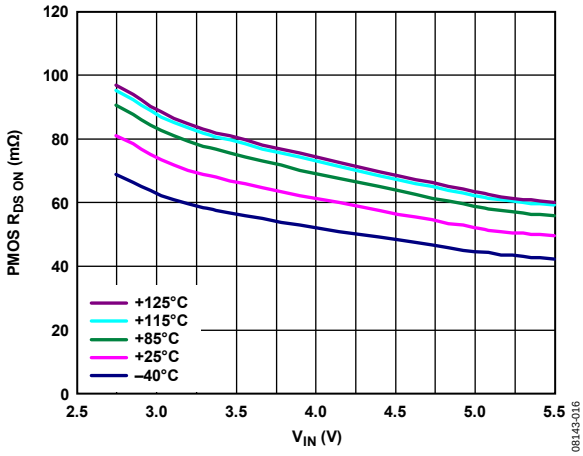

Figure 16. High-Side PMOS Resistance vs. Input Voltage, Includes Bond Wires

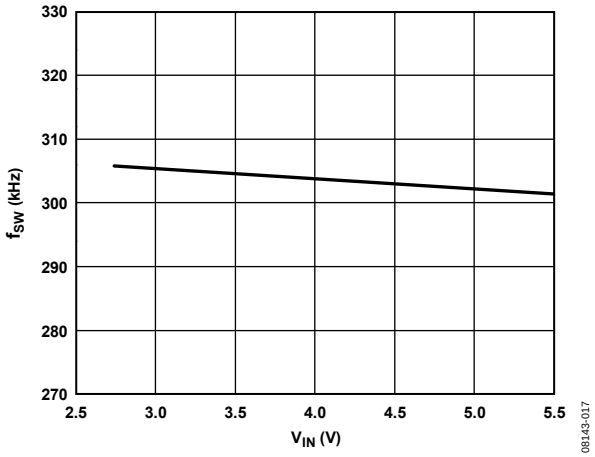

Figure 17. Switching Frequency vs. Input Voltage, f_{SW} = 300 kHz

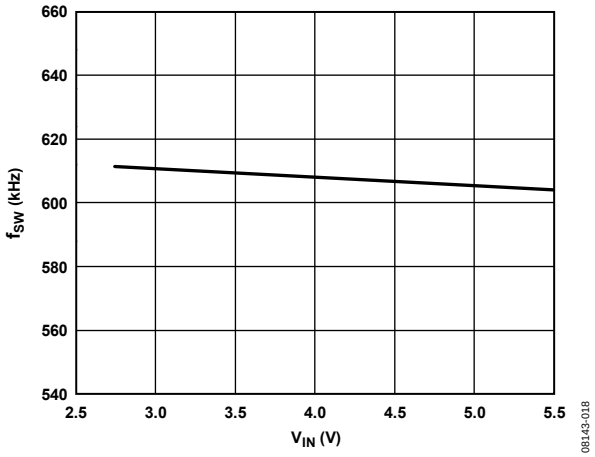

Figure 18. Switching Frequency vs. Input Voltage, f_{SW} = 600 kHz

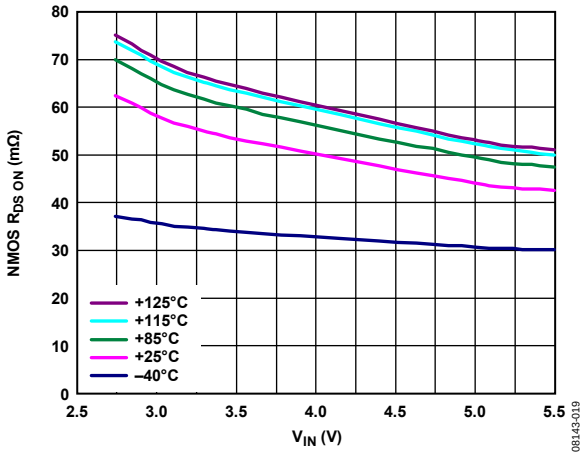

Figure 19. Low-Side NMOS Resistance vs. Input Voltage, Includes Bond Wires

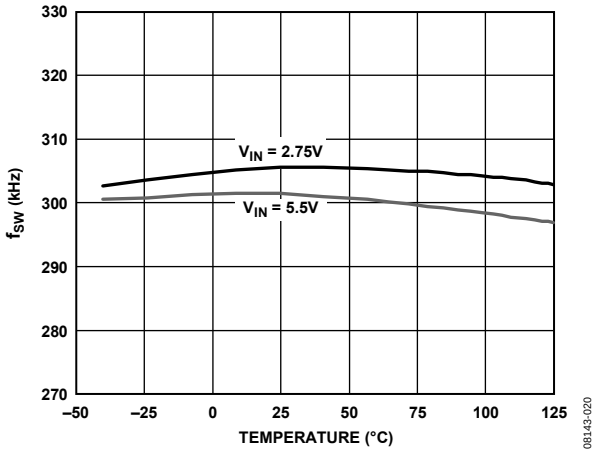

Figure 20. Switching Frequency vs. Temperature, f_{SW} = 300 kHz

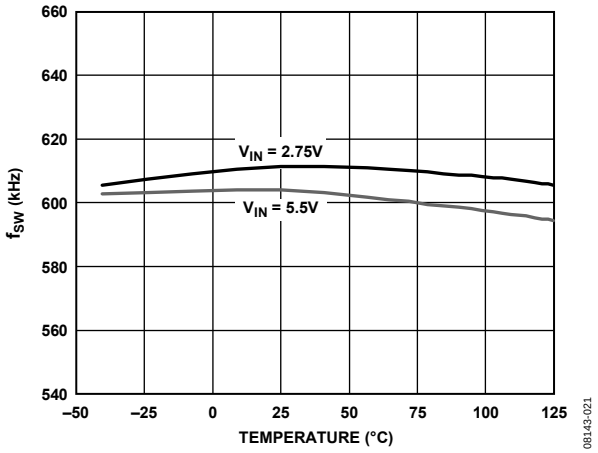

Figure 21. Switching Frequency vs. Temperature, f_{SW} = 600 kHz

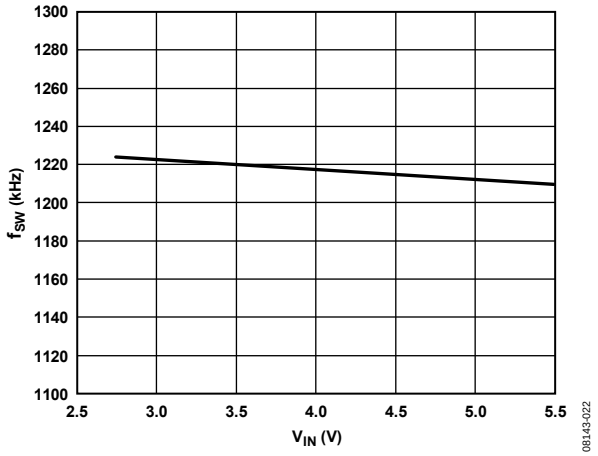

Figure 22. Switching Frequency vs. Input Voltage, f_{SW} = 1.2 MHz

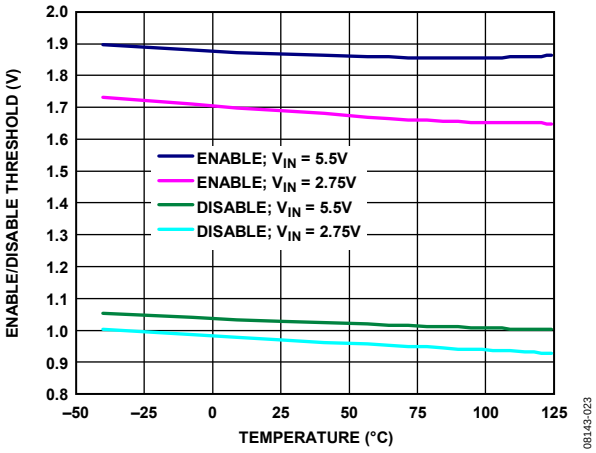

Figure 23. Enable/Disable Threshold vs. Temperature

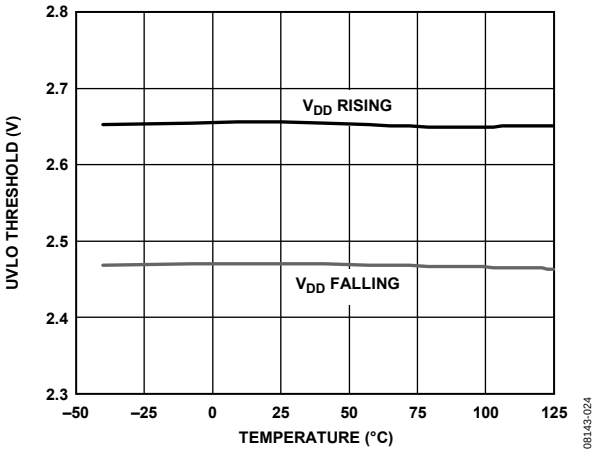

Figure 24. UVLO Threshold vs. Temperature

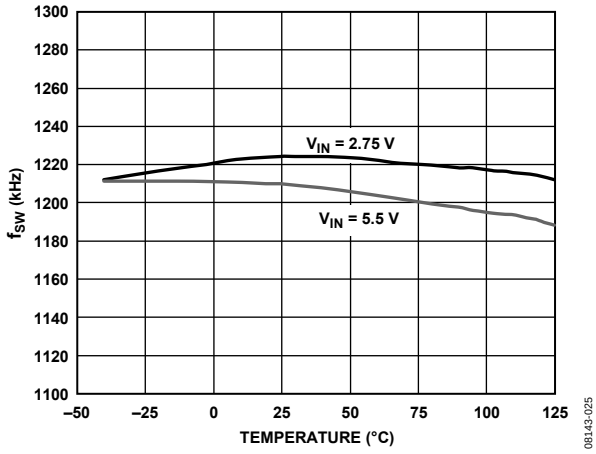

Figure 25. Switching Frequency vs. Temperature, f_{SW} = 1.2 MHz

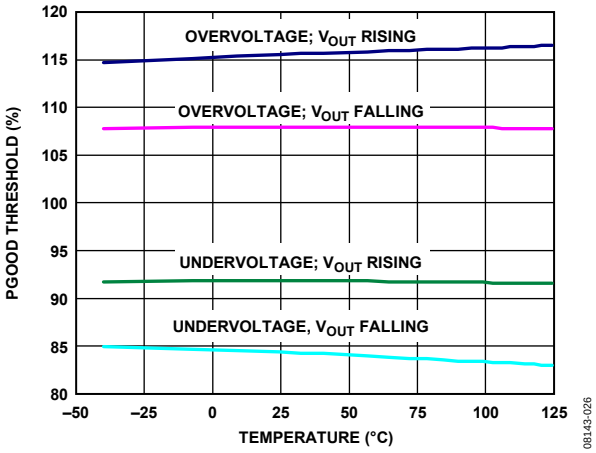

Figure 26. PGOOD Threshold vs. Temperature

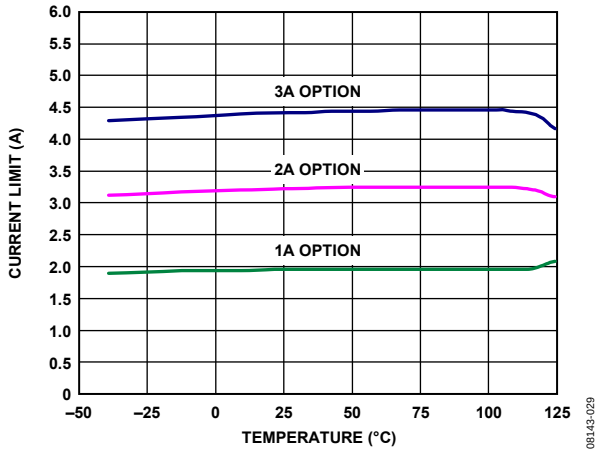

Figure 29. Peak Current Limit vs. Temperature, V_{IN} = 5 V

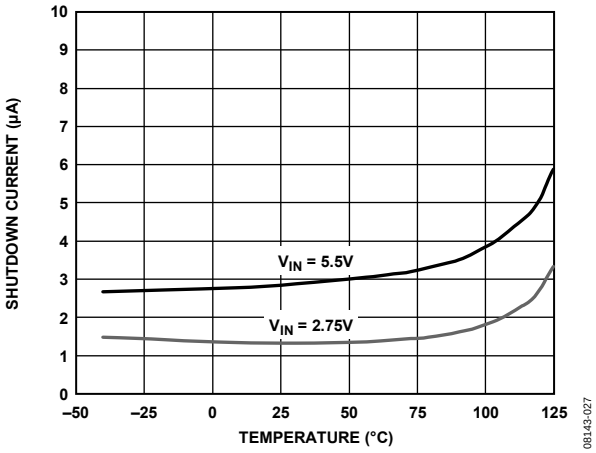

Figure 27. Shutdown Current vs. Temperature

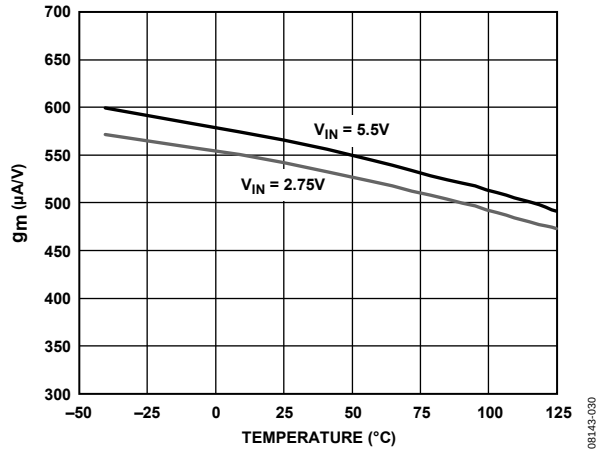

Figure 30. g_M vs. Temperature

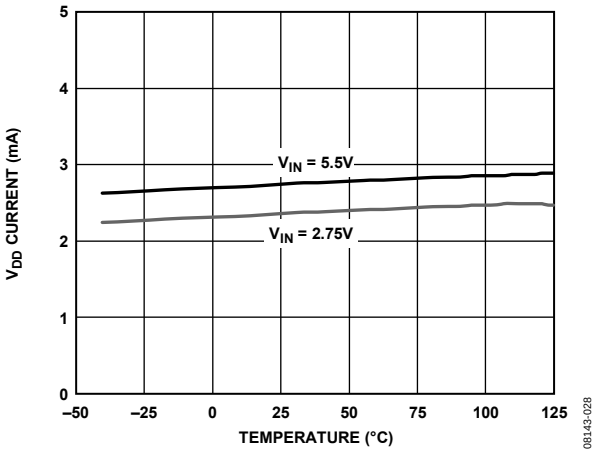

Figure 28. VDD Input Current vs. Temperature (Not Switching)

SUPPLY CURRENT

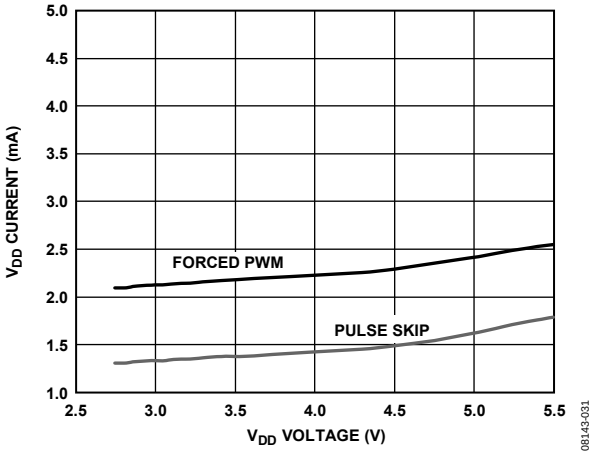

Figure 31. V_{DD} Supply Current, No Load, Channel 1: V_{OUT} = 1.5 V, Channel 2 Off, f_{SW} = 1.2 MHz

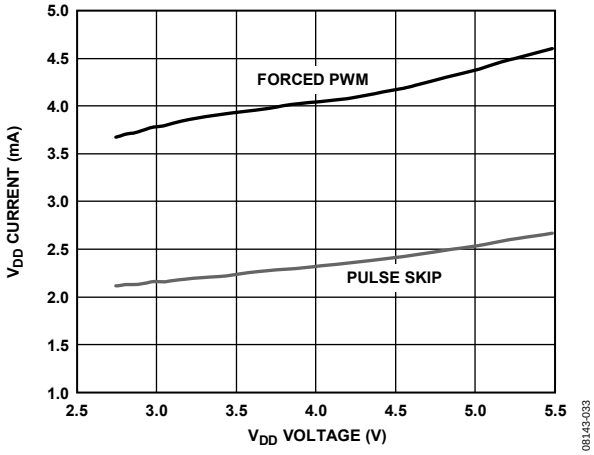

Figure 33. V_{DD} Supply Current, No Load, Channel 1: V_{OUT} = 1.5 V, Channel 2: V_{OUT} = 0.8 V, f_{SW} = 1.2 MHz

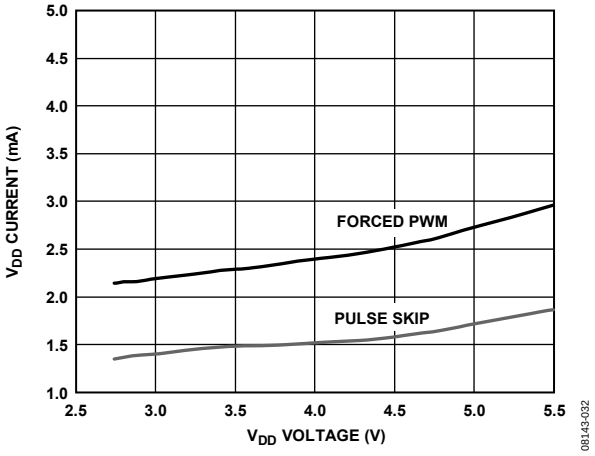

Figure 32. V_{DD} Supply Current, No Load, Channel 2: V_{OUT} = 0.8 V, Channel 1 Off, f_{SW} = 1.2 MHz

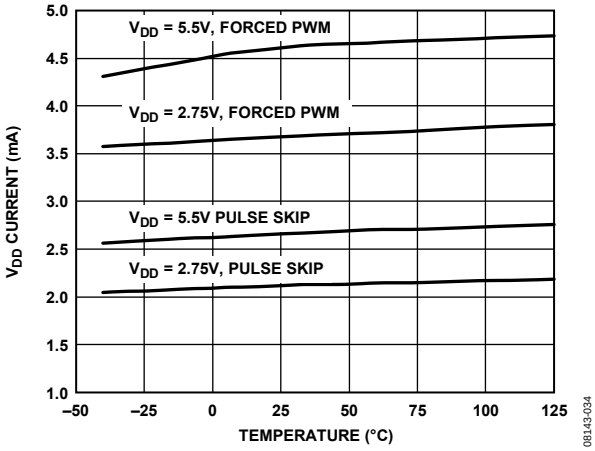

Figure 34. V_{DD} Supply Current vs. Temperature, Channel 1: V_{OUT} = 1.5 V, Channel 2: V_{OUT} = 0.8 V, f_{SW} = 1.2 MHz

LOAD TRANSIENT RESPONSE

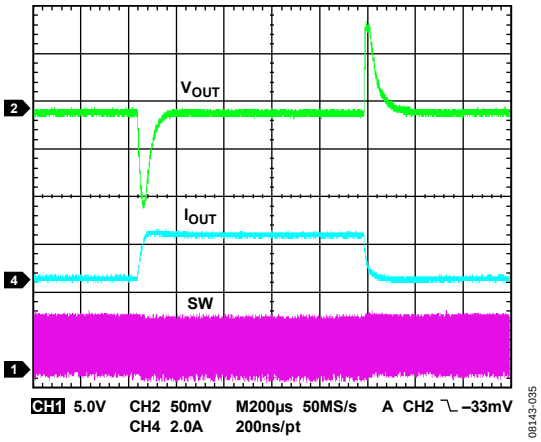

Figure 35. Channel 1: V_{IN} = 5 V, V_{OUT} = 3.3V, f_{SW} = 600 kHz; Forced PWM (See Table 12 for the Circuit Details)

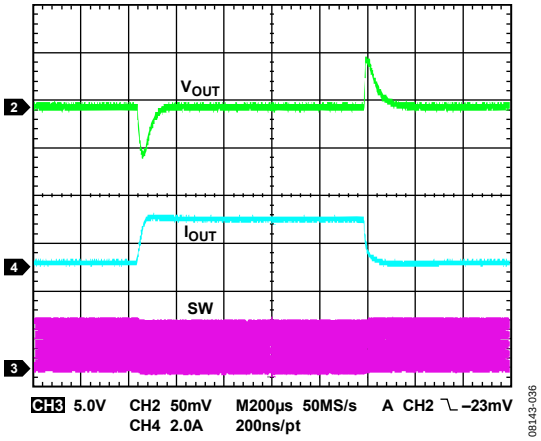

Figure 36. Channel 2: V_{IN} = 5 V, V_{OUT} = 1.8 V, f_{SW} = 600 kHz; Forced PWM (See Table 12 for the Circuit Details)

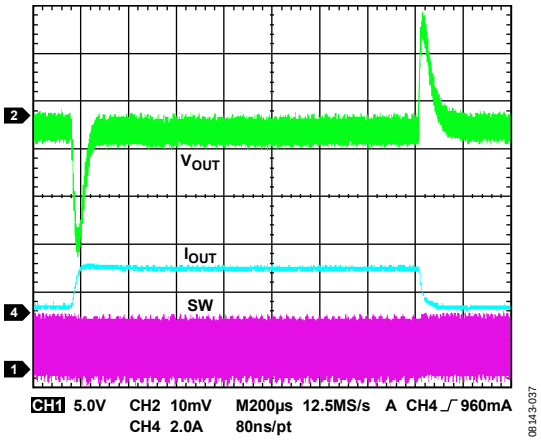

Figure 37. Channel 1: V_{IN} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 1.2 MHz; Forced PWM (See Table 12 for the Circuit Details)

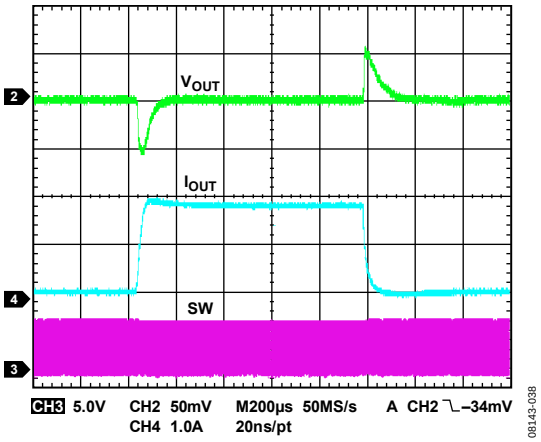

Figure 38. Channel 2: V_{IN} = 5 V, V_{OUT} = 1.8 V, f_{SW} = 600 kHz; Pulse Skip (See Table 12 for the Circuit Details)

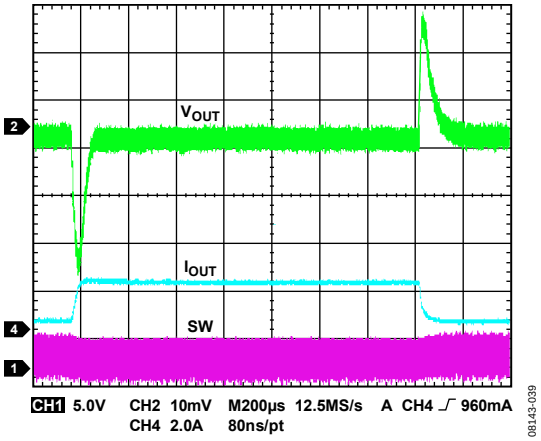

Figure 39. Channel 1: V_{IN} = 3.3 V, V_{OUT} = 1.2 V, f_{SW} = 1.2 MHz; Forced PWM (See Table 12 for the Circuit Details)

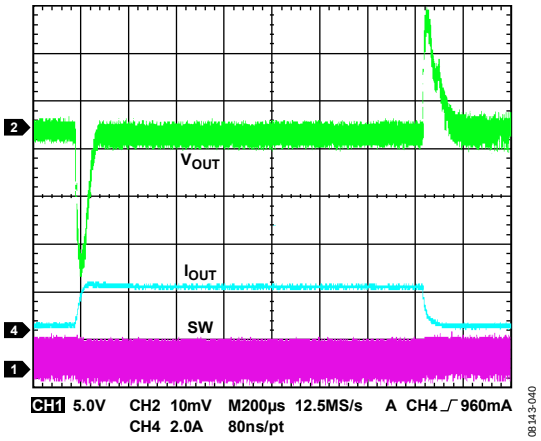

Figure 40. Channel 1: V_{IN} = 3.3 V, V_{OUT} = 1.2 V, f_{SW} = 1.2 MHz; Pulse Skip (See Table 12 for the Circuit Details)

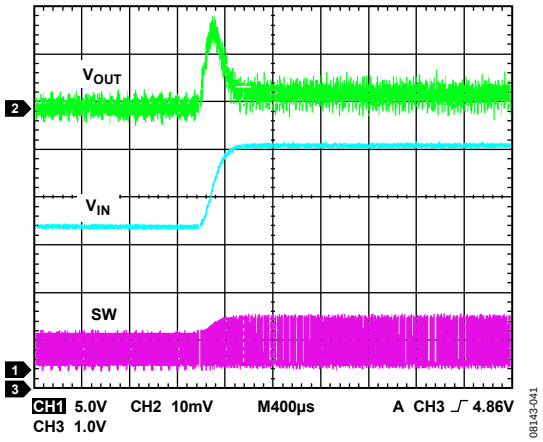

Figure 41. 3.3 V to 5 V Line Transient, V_{OUT} = 1.5 V, Load = 1 A f_{SW} = 1.2 MHz, Pulse Skip Enabled

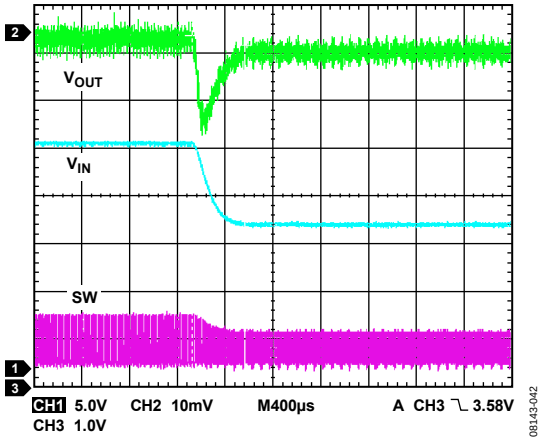

Figure 42. 5 V to 3.3 V Line Transient, V_{OUT} = 1.5 V, Load = 1 A f_{SW} = 1.2 MHz, Pulse Skip Enabled

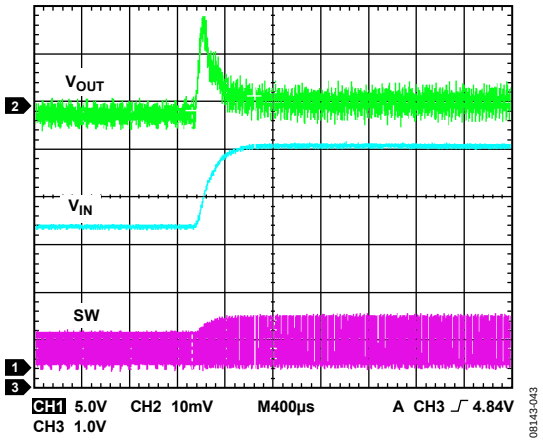

Figure 43. 3.3 V to 5 V Line Transient, V_{OUT} = 1.5 V, Load = 1 A f_{SW} = 1.2 MHz, Forced PWM

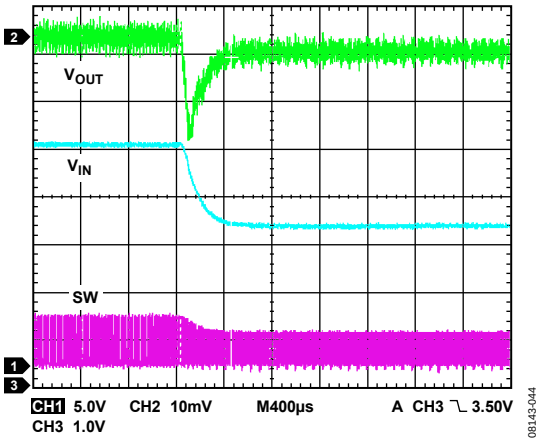

Figure 44. 5 V to 3.3 V Line Transient, V_{OUT} = 1.5 V, Load = 1 A f_{SW} = 1.2 MHz, Forced PWM

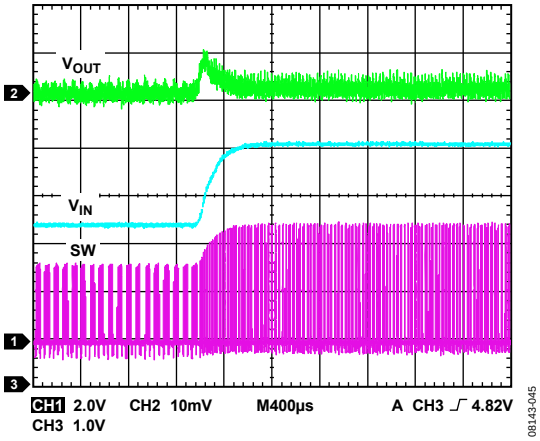

Figure 45. 3.3 V to 5 V Line Transient, V_{OUT} = 0.6 V, Load = 1 A f_{SW} = 600 kHz, Pulse Skip Enabled

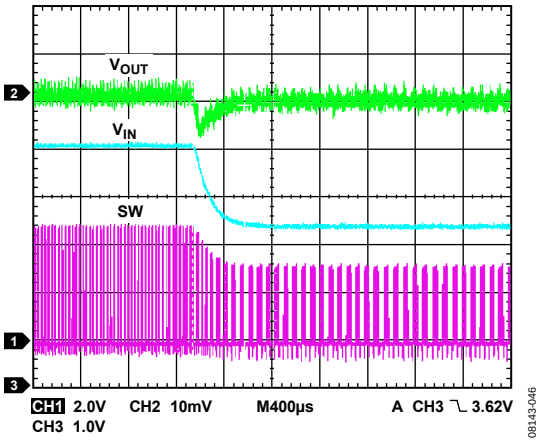

Figure 46. 5 V to 3.3 V Line Transient, V_{OUT} = 0.6 V, Load = 1 A f_{SW} = 600 kHz, Pulse Skip Enabled

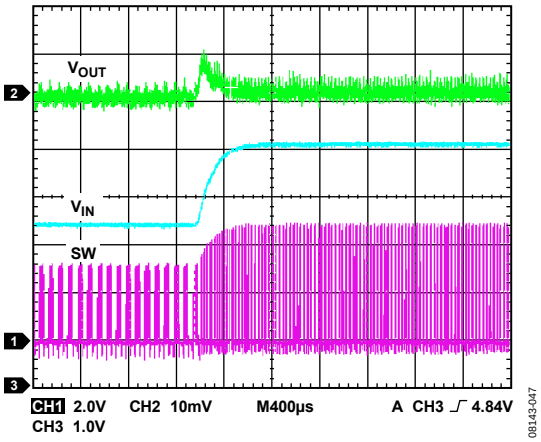

Figure 47. 3.3 V to 5 V Line Transient, V_{OUT} = 0.6 V, Load = 1 A f_{SW} = 600 kHz, Forced PWM

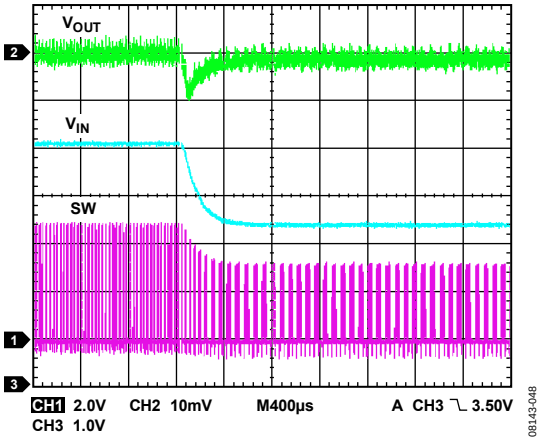

Figure 48. 5 V to 3.3 V Line Transient, V_{OUT} = 0.6 V, Load = 1 A f_{SW} = 600 kHz, Forced PWM

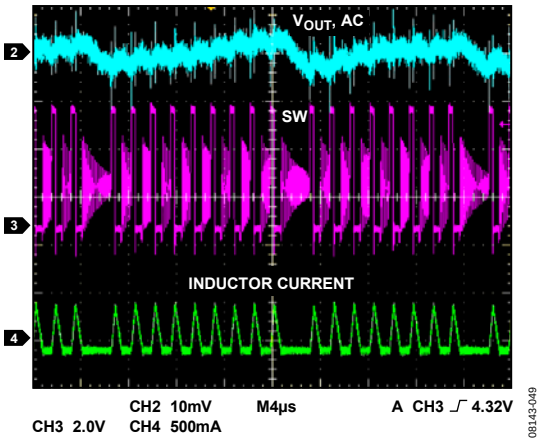

Figure 49. Pulse Skip Mode, 110 mA Load

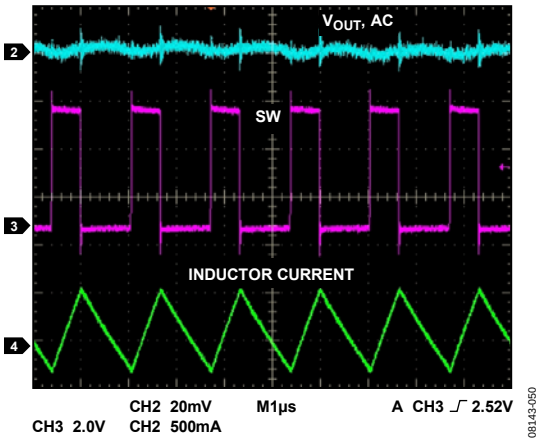

Figure 50. Forced PWM Mode, CCM Operation, 200 mA Load, f_{SW} = 600 kHz

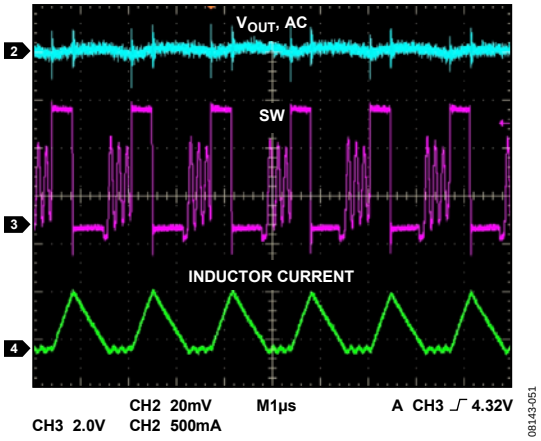

Figure 51. Pulse Skip Enabled, DCM Operation, 200 mA Load, f_{SW} = 600 kHz

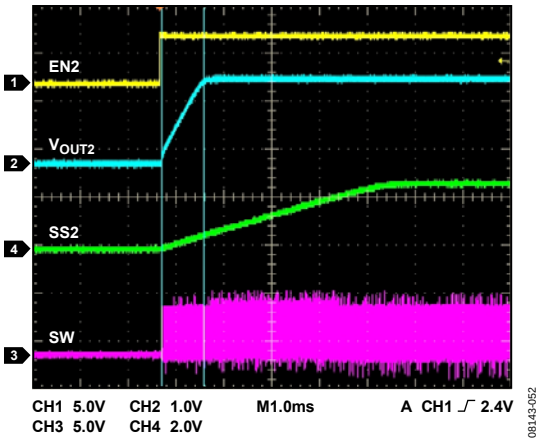

Figure 52. Soft Start, Channel 2 V_{OUT} = 1.8 V, $C_{SS}2$ = 10 nF

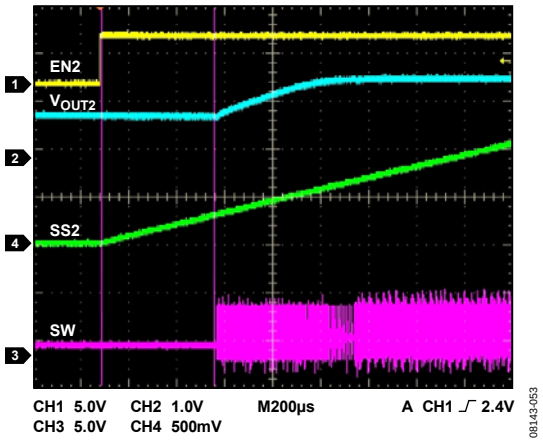

Figure 53. Start with Precharged Output

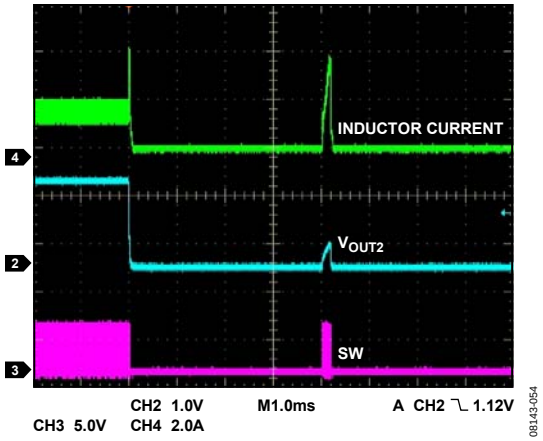

Figure 54. Current Limit Entry, Channel 2 V_{OUT} = 1.8 V, 2 A Configuration, f_{SW} = 600 kHz

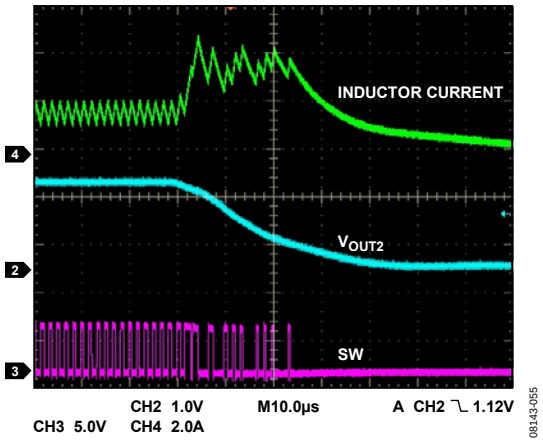

Figure 55. Current Limit Entry (Zoomed In), Channel 2 V_{OUT} = 1.8 V, 2 A Configuration, f_{SW} = 600 kHz

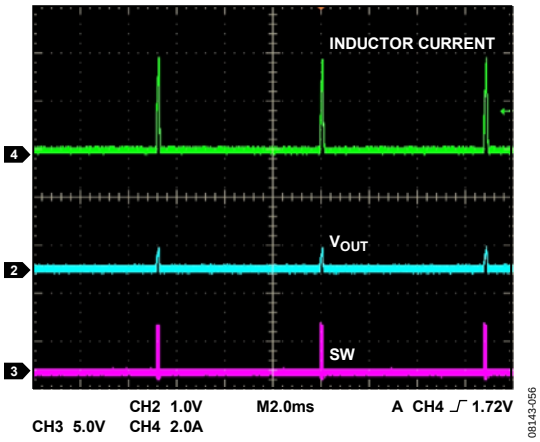

Figure 56. Hiccup Mode, f_{SW} = 600 kHz, 6.8 ms Hiccup Cycle

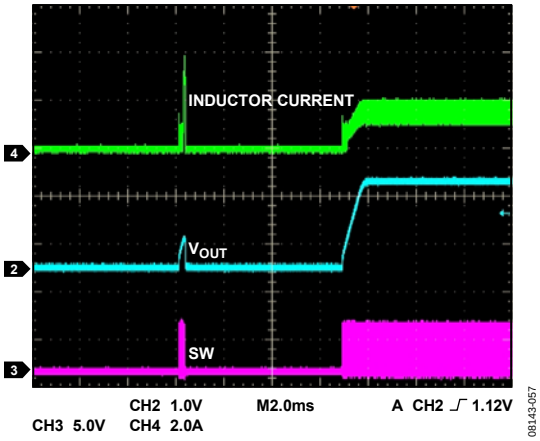

Figure 57. Exit Hiccup Mode, Channel 2 V_{OUT} = 1.8 V, f_{SW} = 600 kHz

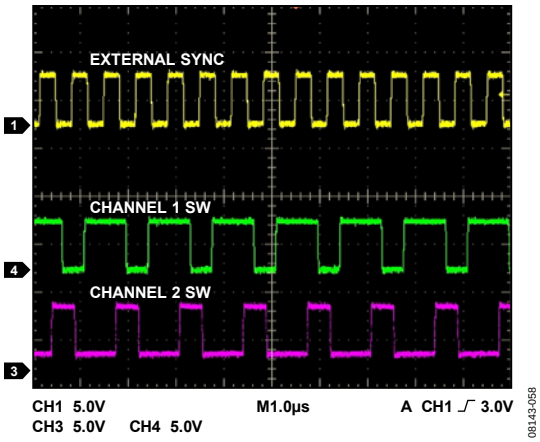

Figure 58. External Synchronization, f_{SYNC} = 1.5 MHz, f_{SW} = 750 kHz

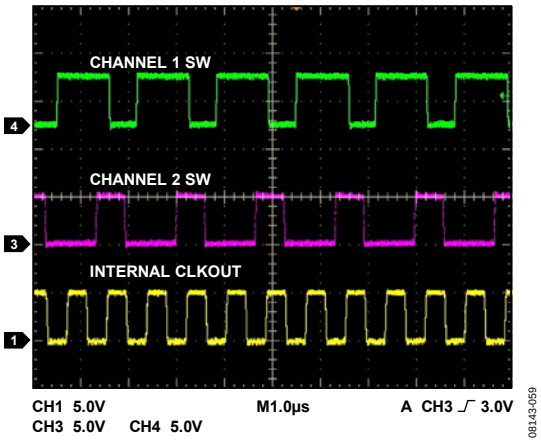

Figure 59. Internal Clock Out, f_{SW} = 600 kHz, f_{CLKOUT} = 1.2 MHz

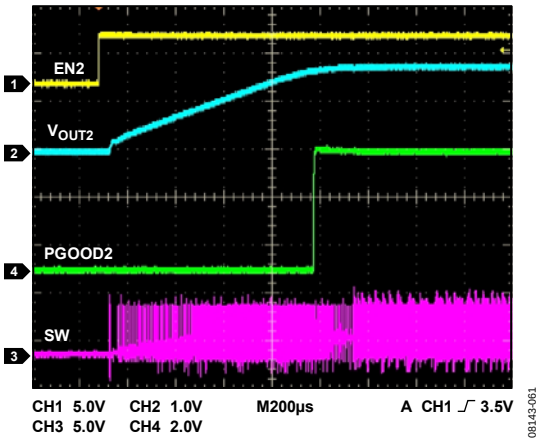

Figure 61. Power Good Signal

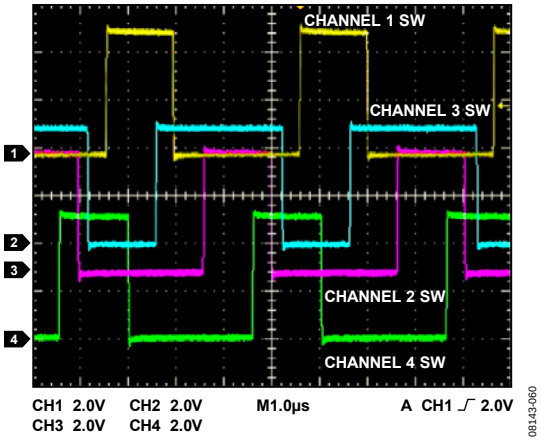

Figure 60. 4-Channel Operation, Two ADP2114s, One Synchronizes Another, 90° Phase-Shifted Switch Nodes

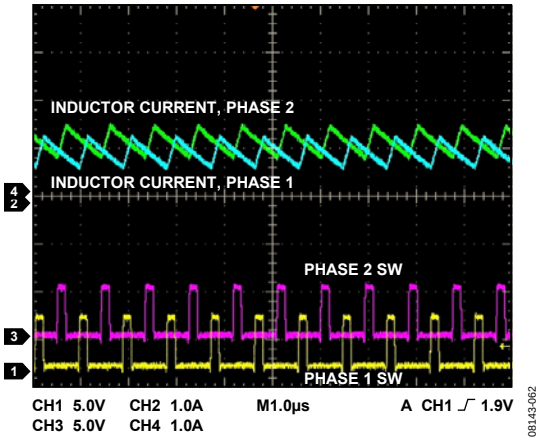

Figure 62. Combined Dual-Phase Output Operation, V_{OUT} = 1.2 V, f_{SW} = 1.1 MHz, 4 A Load

BODE PLOTS

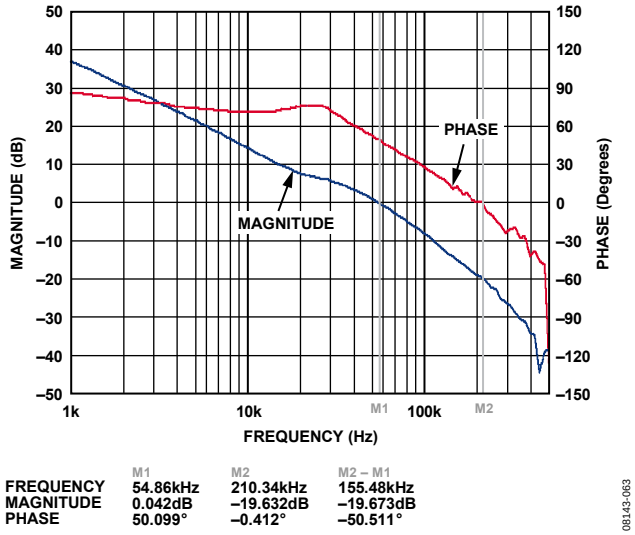

Figure 63. V_{IN} = 5 V, V_{OUT} = 3.3 V, Load = 2 A, f_{SW} = 600 kHz, Crossover Frequency (f_{CO}) = 55 kHz; Phase Margin 50° (See Table 12 for the Circuit Details)

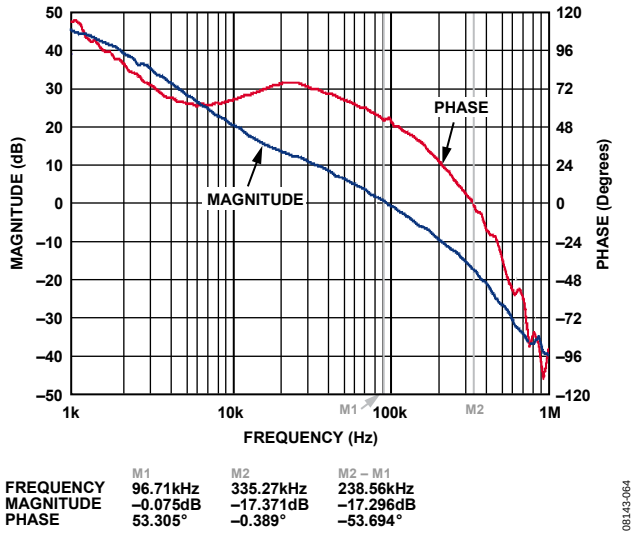

Figure 64. V_{IN} = 5 V, V_{OUT} = 1.2 V, Load = 2 A, f_{SW} = 1.2 MHz, Crossover Frequency (f_{CO}) = 97 kHz; Phase Margin 53° (See Table 12 for the Circuit Details)

SIMPLIFIED BLOCK DIAGRAM

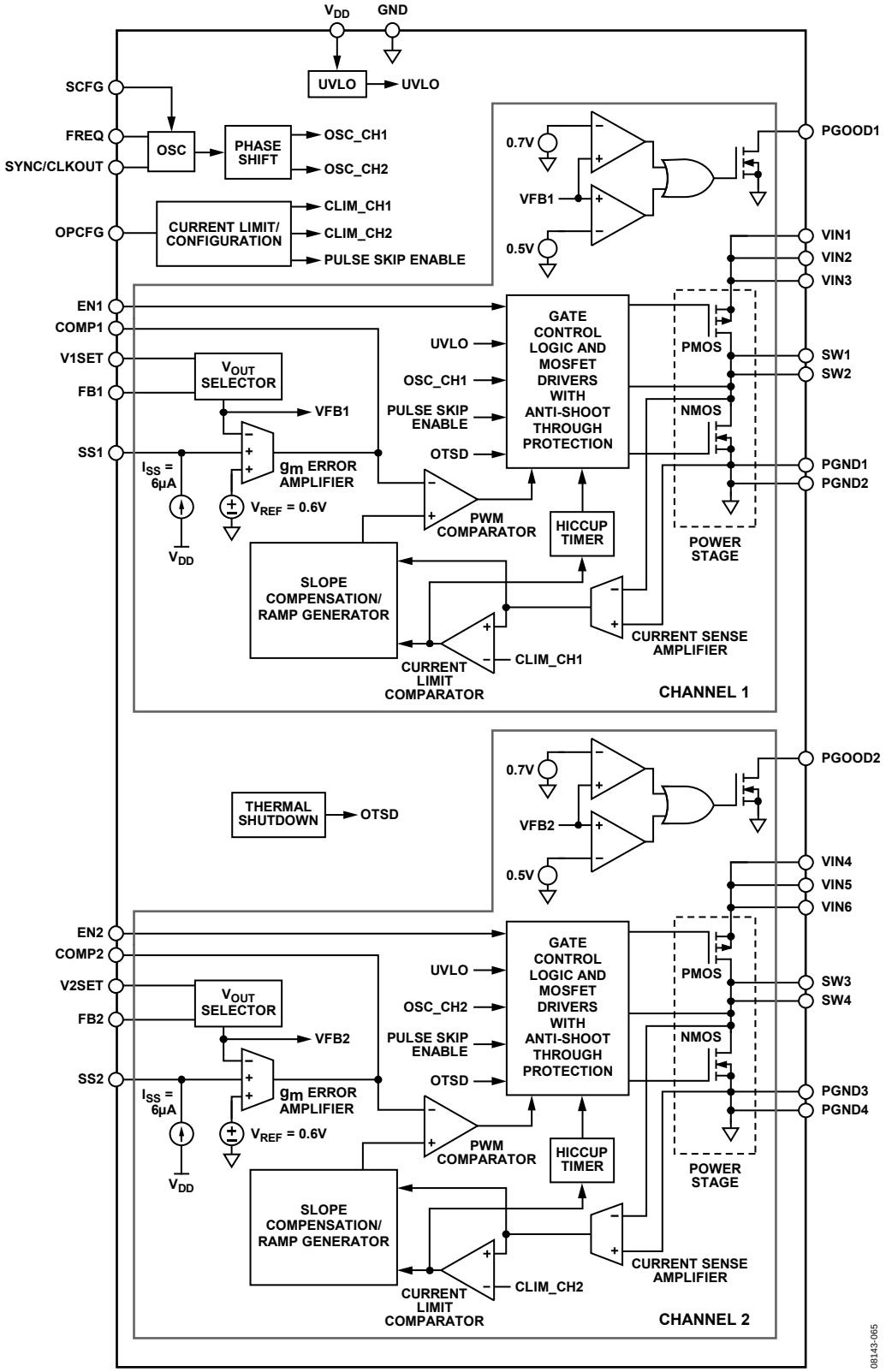

Figure 65. Simplified Block Diagram

THEORY OF OPERATION

The ADP2114 is a high efficiency, dual, fixed switching frequency, synchronous step-down, dc-to-dc converter with flex mode architecture, which is the Analog Devices, Inc., proprietary version of its peak current mode control architecture. The device operates over an input voltage range of 2.75 V to 5.5 V. Each output channel provides an adjustable output down to 0.6 V and delivers up to 2 A of load current. When both the output channels are tied together, they operate 180° out of phase to deliver up to 4 A of load current. The integrated high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET yield high efficiency at medium to heavy loads. Pulse skip mode is available for improved efficiency at light loads. With its high switching frequency (up to 2 MHz) and its integrated power switches, the ADP2114 has been optimized to deliver high performance in a small size for power management solutions.

The ADP2114 also includes undervoltage lockout (UVLO) with hysteresis, soft start, and power good, as well as protection features such as output short-circuit protection and thermal shutdown. The output voltages, current limits, switching frequency, pulse skip operation, and soft start time are externally programmable with tiny resistors and capacitors.

CONTROL ARCHITECTURE

The ADP2114 consists of two step-down, dc-to-dc converters that deliver regulated output voltages, V_{OUT1} and V_{OUT2} (see Figure 1), by modulating the duty cycle at which the internal high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET are switched on and off. In steady-state operation, the output voltage, V_{OUT}, is sensed on the feedback pin, FB1 (FB2), and attenuated in proportion to the selected output voltage on the V1SET (V2SET) pin. An error amplifier integrates the error between the feedback voltage and the reference voltage (V_{REF} = 0.6 V) to generate an error voltage at the COMP1 (COMP2) pin. The valley inductor current is sensed by a current-sense amplifier when the low-side, N-channel MOSFET is on. An internal oscillator turns off the low-side, N-channel MOSFET and turns on the high-side, P-channel MOSFET at a fixed switching frequency. When the high,-side P-channel MOSFET is enabled, the valley inductor current information is added to an emulated ramp signal and compared to the error voltage by the PWM comparator. The output of the PWM comparator modulates the duty cycle by adjusting the trailing edge of the PWM pulse that switches the power devices. Slope compensation is programmed internally into the emulated ramp signal and automatically selected, depending on the V_{IN}, V_{OUT}, and switching frequency. This prevents subharmonic oscillations on the inductor current for greater than 50% duty-cycle operation.

Control logic with the antishoot-through circuit monitor and adjust the low-side and high-side driver outputs to ensure break-before-make switching. This monitoring and control prevents crossconduction between the internal high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO threshold is 2.65 V when VDD is increasing and 2.47 V when VDD is decreasing. The 180 mV hysteresis prevents the converter from turning off and on repeatedly during a slow voltage transition on VDD close to the 2.75 V minimum operational level due to changing load conditions.

ENABLE/DISABLE CONTROL

The EN1 and EN2 pins are used to independently enable or disable Channel 1 and Channel 2, respectively. Drive ENx high to turn on the corresponding channel of ADP2114. Drive ENx low to turn off the corresponding channel of ADP2114, reducing input current below 1 μA. To force a channel to start automatically when input power is applied, connect the corresponding ENx to VDD. When shut down, the ADP2114 channels discharge the soft start capacitor, causing a new soft start cycle every time the converters are re-enabled.

SOFT START

The ADP2114 soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during startup. Soft start begins after the undervoltage lockout threshold is exceeded and the enable pin, EN1 (EN2), is pulled high above 2.0 V. External capacitors to ground are required on both the SS1 and SS2 pins. Each regulating channel has its own soft start circuit. When the converter powers up and is enabled, the internal 6 μA current source charges the external soft start capacitor, establishing a voltage ramp slope at the SS1 (SS2) pin, as shown in Figure 66. The soft start time period ends when the soft start ramp voltage exceeds the internal reference of 0.6 V.

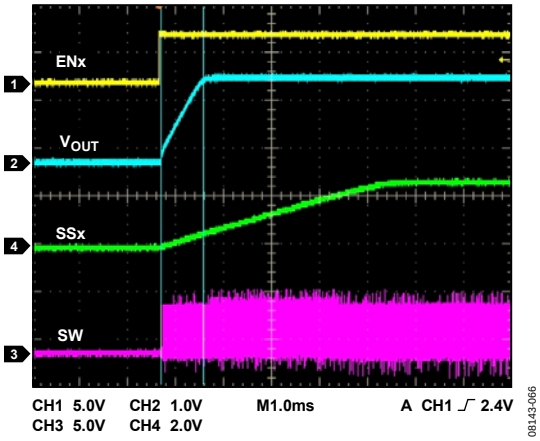

Figure 66. Soft Start

The capacitance value of the soft start capacitor defines the soft start time, t_{SS}, based on

$$\frac{V_{REF}}{t_{SS}} = \frac{I_{SS}}{C_{SS}} \quad (1)$$

where:
V_{REF} is the internal reference voltage, 0.6 V.
I_{SS} is the soft start current, 6 µA.
C_{SS} is the soft start capacitor value.

If the output voltage V_{OUT1} (V_{OUT2}) is precharged prior to enabling Channel 1 (Channel 2), the control logic prevents inductor current reversal by holding the power MOSFETs off until the soft start voltage ramp at SS1 (SS2) reaches the precharged output voltage on V_{FB1} (V_{FB2}), see Figure 67.

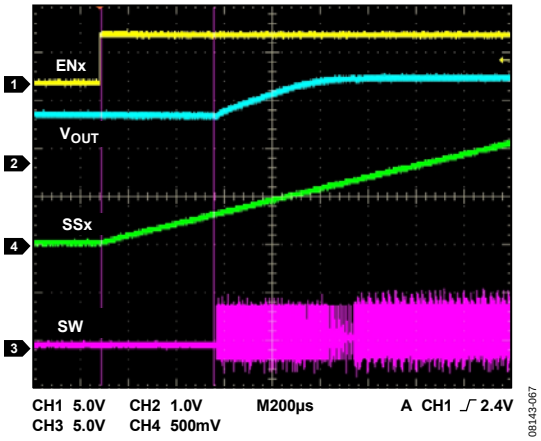

Figure 67. Start with a Precharged Load

POWER GOOD

The ADP2114 features open-drain, power-good outputs (PGOOD1 and PGOOD2) that indicate when the converter output voltage is within regulation. The power good signal transitions low immediately when the corresponding channel is disabled.

The power good circuitry monitors the output voltage on the FB1 (FB2) pin and compares it to the rising and falling thresholds shown in Table 1. If the output voltage, $V_{OUT}1$ ($V_{OUT}2$), exceeds the typical rising limit of 116% of the target output voltage, $V_{OUT}1_{SET}$ ($V_{OUT}2_{SET}$), the PGOOD1 (PGOOD2) pin pulls low. The PGOOD1 (PGOOD2) pin continues to pull low until the output voltage recovers down to 108% (typical) of the target value.

If the output voltage drops below 84% of the target output voltage, the corresponding PGOOD1 (PGOOD2) pin pulls low. The PGOOD1 (PGOOD2) pin continues to pull low until the output voltage rises to within 92% of the target output voltage. The PGOOD1 (PGOOD2) pin then releases and signals the return of the output voltage within the power good window.

The power good thresholds are shown in Figure 68. The PGOOD1 and PGOOD2 outputs also sink current if an overtemperature condition is detected. Use these outputs as logical power good signals by connecting the pull-up resistors from PGOOD1 (PGOOD2) to VDD. If the power good function is not used, the pins can be left floating.

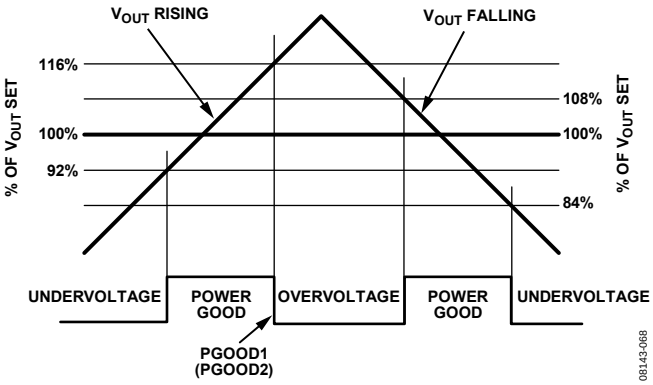

Figure 68. PGOOD1 and PGOOD2 Thresholds

PULSE SKIP MODE

The ADP2114 has built-in, pulse skip circuitry that turns on during light loads, switching only as necessary to maintain the output voltage within regulation. This allows the converter to maintain high efficiency during light load operation by reducing the switching losses. The pulse skip mode can be selected by configuring the OPCFG pin according to Table 7. In pulse skip mode, when the output voltage dips below regulation, the ADP2114 enters PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

If the converter is configured to operate in forced PWM mode (by selecting that configuration on the OPCFG pin), the device operates with a fixed switching frequency, even at light loads.

HICCUP MODE CURRENT LIMIT

The ADP2114 features a hiccup mode current limit implementation. When the peak inductor current exceeds the preset current limit for more than eight consecutive clock cycles, the hiccup mode current limit condition occurs. The channel then goes to sleep for 6.8 ms (at a 600 kHz switching frequency), which is enough time for the output to discharge and the average power dissipation to reduce. It then wakes up with a soft start period (see Figure 69). If the current limit condition is triggered again, the channel goes to sleep and wakes up after 6.8 ms. The current limits for the two channels are programmed by configuring the OPCFG pin (see Table 7). For the 2 A/2 A option, the output current limit is set to 3.3 A per output. For the 3 A/1 A option, the current limits are set to 4.5 A and 1.9 A for V_{OUT1} and V_{OUT2}, respectively.

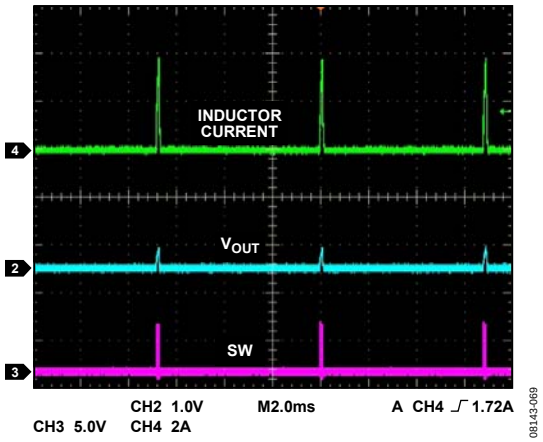

Figure 69. Hiccup Mode

THERMAL OVERLOAD PROTECTION

The ADP2114 has an internal temperature sensor that monitors the junction temperature. High current going into the switches or a hot printed circuit board (PCB) can cause the junction temperature of the ADP2114 to rise rapidly. When the junction temperature reaches approximately 150°C, the ADP2114 goes into thermal shutdown and the converter is turned off. When the junction temperature drops below 125°C, the ADP2114 resumes normal operation after the soft start sequence.

MAXIMUM DUTY CYCLE OPERATION

As the input voltage drops and approaches the output voltage, the ADP2114 smoothly transitions to maximum duty cycle operation, maintaining the low-side, N-channel MOSFET switch on for the minimum off time. In maximum duty cycle operation, the output voltage dips below regulation because the output voltage is the product of the input voltage and the maximum duty cycle limitation. The maximum duty cycle limit is a function of the switching frequency and the input voltage, as shown in Figure 72.

SYNCHRONIZATION

The ADP2114 can be synchronized to an external clock such that the two channels operate at a switching frequency that is half the input synchronization clock. The SYNC/CLKOUT pin can be configured as an input SYNC pin or an output CLKOUT pin through the SCFG pin, as shown in Table 6. Through the input SYNC pin, the ADP2114 can be synchronized to an external clock such that the two channels switch at half the external clock, 180° out of phase. Through the output CLKOUT pin, the ADP2114 provides an output clock that is twice the switching frequency of the channels and 90° out of phase. Therefore, a single ADP2114 configured for the CLKOUT option acts as the master converter and provides an external clock for all other dc-to-dc converters (including other ADP2114s). These other converters are configured as slaves that accept an external clock and synchronize to it. This clock distribution approach synchronizes all dc-to-dc converters in the system and prevents beat harmonics that can lead to EMI issues.

The ADP2114 has been optimized to power high performance signal chain circuits. The slew rate of the switch node is controlled by the size of the driver devices. Fast slewing of the switch node is desirable to minimize transition losses but can lead to serious EMI issues due to parasitic inductance. Therefore, the slew rate of the drivers has been optimized such that the ADP2114 can match the performance of the low dropout regulators in supplying sensitive signal chain circuits while providing excellent power efficiency.

CONVERTER CONFIGURATION

SELECTING THE OUTPUT VOLTAGE

To set the output voltage, V_{OUT1} (V_{OUT2}), select one of the six fixed voltages, as shown in Table 4, by connecting the V1SET (V2SET) pin to GND through an appropriate value resistor (see Figure 70). V1SET and V2SET set the voltage output levels for Channel 1 and Channel 2, respectively. The feedback pin FB1 (FB2) should be directly connected to V_{OUT1} (V_{OUT2}).

Table 4. Output Voltage Programming

R_{V1SET} (Ω) ± 5%	V_{OUT1} (V)	R_{V2SET} (Ω) ± 5%	V_{OUT2} (V)
0 to GND	0.8	0 to GND	0.8
4.7 k to GND	1.2	4.7 k to GND	1.2
8.2 k to GND	1.5	8.2 k to GND	1.5
15 k to GND	1.8	15 k to GND	1.8
27 k to GND	2.5	27 k to GND	2.5
47 k to GND	3.3	47 k to GND	3.3
82 k to GND	0.6 to <1.6 (adjustable)	82 k to GND	0.6 to <1.6 (adjustable)
0 to VDD	1.6 to 3.3 (adjustable)	0 to VDD	1.6 to 3.3 (adjustable)

If the required output voltage V_{OUT1} (V_{OUT2}) is in the adjustable range, from 0.6 V to less than 1.6 V, connect V1SET (V2SET) through an 82 kΩ resistor to GND. For the adjustable output voltage range of 1.6 V to 3.3 V, tie V1SET (V2SET) to VDD (see Table 4). The adjustable output voltage of ADP2114 is externally set by a resistive voltage divider from the output voltage to the feedback pin (see Figure 71). The ratio of the resistive voltage divider sets the output voltage, while the absolute value of those resistors sets the divider string current. For lower divider string currents, the small 10 nA (0.1 µA maximum) FB bias current should be taken into account when calculating the resistor values. The FB bias current can be ignored for a higher divider string current; however, this degrades efficiency at very light loads.

To limit output voltage accuracy degradation due to FB bias current to less than 0.05% (0.5% maximum), ensure that the divider string current is greater than 20 µA. To calculate the desired resistor values, first determine the value of the bottom divider string resistor, R1, by

$$R1 = V_{REF}/I_{STRING} \quad (2)$$

where:
V_{REF} is 0.6 V, the internal reference.
I_{STRING} is the resistor divider string current.

When R1 is determined, calculate the value of the top resistor, R2, by

$$R2 = R1\left[\frac{V_{OUT} - V_{REF}}{V_{REF}}\right] \quad (3)$$

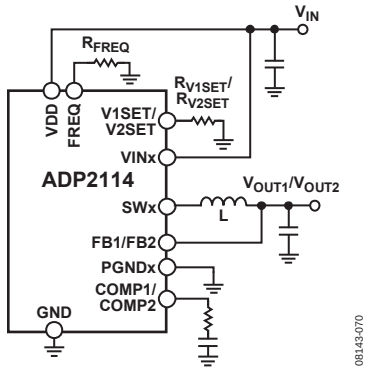

Figure 70. Configuration for Fixed Outputs

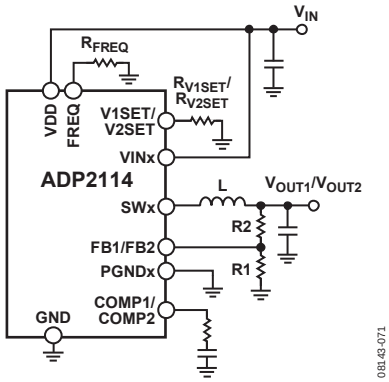

Figure 71. Configuration for Adjustable Outputs

SETTING THE OSCILLATOR FREQUENCY

The ADP2114 channels can be set to operate in one of the three preset switching frequencies: 300 kHz, 600 kHz, or 1.2 MHz. For 300 kHz operation, connect the FREQ pin to GND. For 600 kHz or 1.2 MHz operation, connect a resistor between the FREQ pin and GND, as shown in Table 5.

Table 5. Oscillator Frequency Setting

R_{FREQ} (Ω) ± 5%	f_{SW} (kHz)
0 to GND	300
8.2 k to GND	600
27 k to GND	1200

Choice of the switching frequency depends on the required dc-to-dc conversion ratio and is limited by the minimum and maximum controllable duty cycle shown on Figure 72. This is due to the requirement of minimum on and minimum off times for current sensing and robust operation. The choice of switching frequency is also determined by the need for small external components. For small, area limited power solutions, use of higher switching frequencies is recommended.

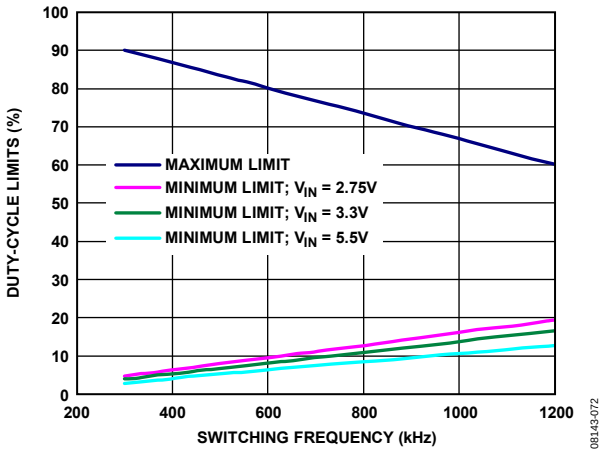

Figure 72. Duty Cycle Working Limits

For single output, multiphase applications that operate at close to 50% duty cycle, it is recommended to use the 1.2 MHz switching frequency to minimize crosstalk between the phases.

SYNCHRONIZATION AND CLKOUT

The ADP2114 can be configured to output an internal clock or synchronize to an external clock at the STNC/CLKOUT pin. The SYNC/CLKOUT pin is a bidirectional pin configured by the SCFG pin, as shown in Table 6.

Table 6. SYNC/CLKOUT Configuration Setting

SCFG	SYNC/CLKOUT
GND	Input
VDD	Output

The converter switching frequency, f_{SW}, is half of the synchronization frequency f_{SYNC}/f_{CLKOUT} as shown in Equation 4, irrespective of whether SYNC/CLKOUT is configured as an input or output.

$$f_{SYNC}/f_{CLKOUT} = 2 \times f_{SW} \quad (4)$$

An external clock can be applied to the SYNC/CLKOUT pin when configured as an input to synchronize multiple ADP2114s to the same external clock. The f_{SYNC} range is 400 kHz to 4 MHz, which produces f_{SW} in the 200 kHz to 2 MHz range. See Figure 73 for an illustration.

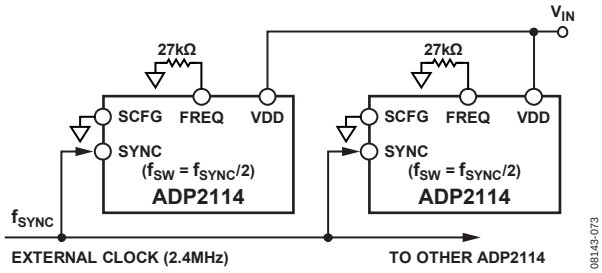

Figure 73. Synchronization with External Clock (f_{SW} = 1.2 MHz in This Case)

When synchronizing to an external clock, the switching frequency f_{SW} must be set close to half of the expected external clock frequency by appropriately terminating the FREQ pin as shown in Table 5.

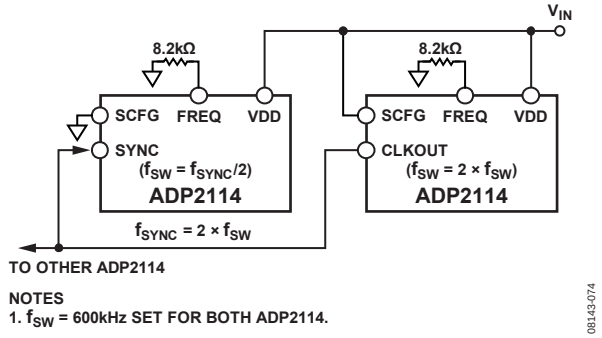

Figure 74. ADP2114 to SYNC with Another ADP2114 (Note that the SCFG of the master is tied to VDD.)

The ADP2114 can also be configured to output a clock signal on the SYNC/CLKOUT pin to synchronize multiple ADP2114s to it (see Figure 74). The CLKOUT signal is 90° phase shifted to the internal clock of the channels so that the master ADP2114 and the slave channels are out of phase (see Figure 75 for additional information).

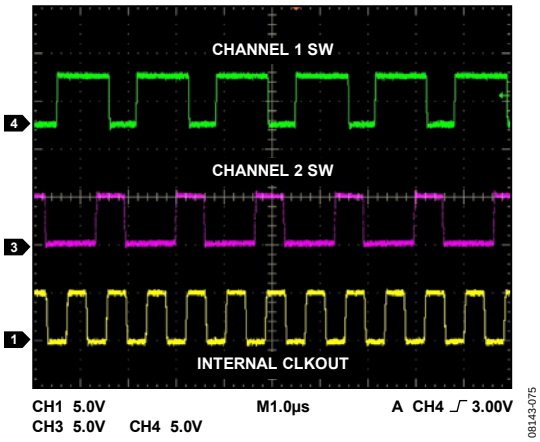

Figure 75. CLKOUT Waveforms

OPERATION MODE CONFIGURATION

The dual-channel ADP2114 can be configured to one of the four modes of operation by connecting the OPCFG pin as shown in Table 7. This configuration sets the current limit for each channel and enables or disables the transition to pulse skip mode at light loads.

In the dual-phase configuration, the outputs of the two channels are connected together, and they generate a single dc output voltage, V_{OUT}. For this single combined dual-phase output, only Mode 2 in the OPCFG options can be used. In this mode, the error amplifiers of both phases are used. The feedback pins (FB1 and FB2) are tied together, the compensation pins (COMP1 and COMP2) are tied together, the soft start pins (SS1 and SS2) are tied together, and the enable pins (EN1 and EN2) are tied together.

In addition, if the power-good feature is used, combine PGOOD1 and PGOOD2 and connect them to VDD through a single pull-up resistor.

When the ADP2114 is synchronized to an external clock, the converters always operate in fixed frequency CCM, and they do not enter into pulse skip mode at light loads. In this case, when configuring the OPCFG pin, choose forced PWM mode.

Table 7. Current Limit Operation Mode and Configuration

		Maximum Output Current	Peak Current Limit	
Mode	**R_{OPCFG} (Ω) ± 5%**	**I_{OUT1} (A)/I_{OUT2} (A)**	**I_{LIMIT1} (A)/I_{LIMIT2} (A)**	**Power Savings at Light Load**
1	0 to GND	2/2	3.3/3.3	Pulse skip enabled
2	4.7 k to GND	2/2	3.3/3.3	Forced PWM
3	8.2 k to GND	3/1	4.5/1.9	Pulse skip enabled
4	15 k to GND	3/1	4.5/1.9	Forced PWM

EXTERNAL COMPONENTS SELECTION

INPUT CAPACITOR SELECTION

The input current to a buck converter is pulsating in nature. The current is zero when the high-side switch is off and approximately equal to the load current when it is on. Because this occurs at reasonably high frequencies (300 kHz to 1.2 MHz), the input bypass capacitor ends up supplying most of the high frequency current (ripple current), allowing the input power source to supply only the average (dc) current. The input capacitor needs a sufficient ripple current rating to handle the input ripple as well as an ESR that is low enough to mitigate the input voltage ripple. For the ADP2114, place a 22 µF, 6.3 V, X5R ceramic capacitor close to the VINx pin for each channel. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

VDD RC FILTER

It is recommended to apply the input power, V_{IN}, to the VDD pin through a low-pass RC filter, as shown on Figure 76. Connecting a 10 Ω resistor in series with V_{IN} and a 1 µF, 6.3 V, X5R (or X7R) ceramic capacitor between VDD and GND creates a 16 kHz (−3 dB) low-pass filter that effectively attenuates voltage glitches on the input power rail caused by the switching regulator. This provides a clean power supply to the internal, sensitive, analog and digital circuits in the ADP2114, ensuring robust operation.

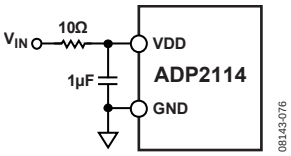

Figure 76. Low-Pass Filter at VDD

INDUCTOR SELECTION

The high switching frequency of ADP2114 allows for minimal output voltage ripple even with small inductors. The sizing of the inductor is a trade-off between efficiency and transient response. A small inductor leads to larger inductor current ripple that provides excellent transient response but degrades efficiency. Due to the high switching frequency of ADP2114, shielded ferrite core inductors are recommended for their low core losses and low EMI.

As a guideline, the inductor peak-to-peak current ripple, ΔI_L, is typically set to 1/3 of the maximum load current for optimal transient response and efficiency.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \approx \frac{I_{LOAD(MAX)}}{3}$$

$$\Rightarrow L_{IDEAL} = \frac{3 \times V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN} \times I_{LOAD(MAX)}} \quad (5)$$

where:
V_{IN} is the input voltage on the VINx terminal.
V_{OUT} is the desired output voltage.
f_{SW} is the converter switching frequency.

The internal slope compensation introduces additional limitations on the optimal inductor value for stable operation because the internal ramp is scaled for each V_{OUT} setting. The limits for different V_{IN}, V_{OUT}, and f_{SW} combinations are listed in Table 8.

Table 8. Minimum and Maximum Inductor Values

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	Min L (µH)	Max L (µH)
300	5	3.3	6.8	10
300	5	2.5	5.6	15
300	3.3	2.5	5.6	6.8
300	5	1.8	4.7	12
300	3.3	1.8	4.7	8.2
300	5	1.5	2.2	12
300	3.3	1.5	2.2	8.2
300	5	1.2	2.2	10
300	3.3	1.2	2.2	8.2
300	5	0.8	1.5	6.8
300	3.3	0.8	1.5	6.8
600	5	3.3	3.3	4.7
600	5	2.5	3.3	6.8
600	3.3	2.5	3.3	3.3
600	5	1.8	2.2	6.8
600	3.3	1.8	2.2	3.3
600	5	1.5	1.5	5.6
600	3.3	1.5	1.5	4.7
600	5	1.2	1.5	4.7
600	3.3	1.2	1.5	3.3
600	5	0.8	1.0	3.3
600	3.3	0.8	1.0	3.3
1200	5	2.5	1.0	3.3
1200	5	1.8	1.0	3.3
1200	3.3	1.8	1.0	2.2
1200	5	1.5	0.8	2.2
1200	3.3	1.5	0.8	2.2
1200	5	1.2	0.8	2.2
1200	3.3	1.2	0.8	2.2
1200	5	0.8	0.47	1.5
1200	3.3	0.8	0.47	1.5

To avoid saturation, the rated current of the inductor has to be larger than the maximum peak inductor I_{L_PEAK} current given by

$$I_{L_PEAK} = I_{LOAD_MAX} + \frac{\Delta I_L}{2} \quad (6)$$

where:
I_{LOAD_MAX} is the maximum dc load current.
ΔI_L is the inductor ripple current (peak to peak).

The ADP2114 can be configured in either a 2 A/2 A or a 3 A/1 A current limit configuration and, therefore, the current limit thresholds for the two channels are different in each setting. The inductor chosen for each channel must have at least the peak output current limit of the IC in each case for robust operation during short-circuit conditions. The following inductors are recommended:

- From 0.47 µH to 4.7 µH, the TOKO D53LC and FDV0620 series
- From 4.7 µH to 12 µH, the Cooper Bussman DR1050 series and the Wurth Elektronik WE-PDF series.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. The ADP2114 is designed for operation with small ceramic output capacitors that have low ESR and ESL; therefore, comfortably able to meet tight output voltage ripple specifications. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics. The minimum output capacitance, C_{OUT_MIN}, is determined by Equation 7 and Equation 8.

For acceptable maximum output voltage ripple,

$$\Delta V_{RIPPLE} \cong \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT_MIN}} \right) \quad (7)$$

Therefore,

$$C_{OUT_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)} \quad (8)$$

where:
ΔV_{RIPPLE} is allowable peak-to-peak output voltage ripple in volts.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the capacitor in ohms.
f_{SW} is the converter switching frequency in Hertz.

If there is a step load, choose the output capacitor value based on the value of the step load. For the maximum acceptable output voltage droop/overshoot caused by the step load,

$$C_{OUT_MIN} \cong \Delta I_{OUT_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right) \quad (9)$$

where:
ΔI_{OUT_STEP} is the load step value in amperes.
f_{SW} is the switching frequency in Hertz.
ΔV_{DROP} is the maximum allowable output voltage droop/overshoot in volts for the load step.

Note that the previous equations are approximations and are based on following assumptions:

- The inductor value is based on the peak-to-peak current being 30% of the maximum load current.
- Voltage drops across the internal MOSFET switches and across the dc resistance of the inductor are ignored.
- In Equation 9, it is assumed that it takes up to three switching cycles until the loop adjusts the inductor current in response to the load step.

Select the largest output capacitance given by Equation 8 and Equation 9. While choosing the actual type of ceramic capacitor for the output filter of the converter, pick one with a nominal capacitance that is 20% to 30% larger than the calculated value because the effective capacitance decreases with larger dc voltages. In addition, the rated voltage of the capacitor must be higher than the output voltage of the converter.

Recommended input and output ceramic capacitors include

- Murata GRM21BR61A106KE19L, 10 µF, 10 V, X5R, 0805
- TDK C2012X5R0J226M, 22 µF, 6.3 V, X5R, 0805
- Panasonic ECJ-4YB0J476M, 47 µF, 6.3 V, X5R, 1210
- Murata GRM32ER60J107ME20L, 100 µF, 6.3 V, X5R, 1210

CONTROL LOOP COMPENSATION

The ADP2114 uses a peak, current mode control architecture for excellent load and line transient response. The external voltage loop is compensated by a transconductance amplifier with a simple external RC network between the COMP1 (COMP2) pin and GND, as shown in Figure 77.

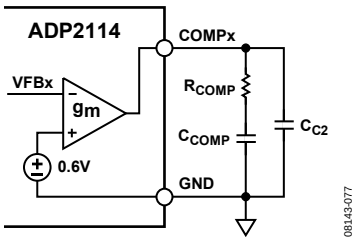

Figure 77. Compensation Components

The basic control loop block diagram is shown in Figure 78.

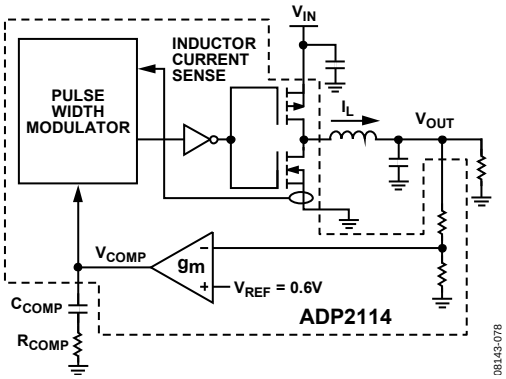

Figure 78. Basic Control Block Diagram

The blocks and components shown enclosed within the dashed line in Figure 78 are embedded inside each channel of the ADP2114.

The control loop can be broken down into the following three sections:

- V_{OUT} to V_{COMP}
- V_{COMP} to I_L
- I_L to V_{OUT}

Correspondingly, there are three transfer functions:

$$\frac{V_{COMP}(s)}{V_{OUT}(s)} = \frac{V_{REF}}{V_{OUT}} \times g_m \times Z_{COMP}(s) \quad (10)$$

$$\frac{I_L(s)}{V_{COMP}(s)} = G_{CS} \quad (11)$$

$$\frac{V_{OUT}(s)}{I_L(s)} = Z_{FILT}(s) \quad (12)$$

where:
g_m is the transconductance of the error amplifier, 550 µs.
G_{CS} is the current sense gain, 4 A/V.
V_{OUT} is the output voltage of the converter.
V_{REF} is the internal reference voltage of 0.6 V.
$Z_{COMP}(s)$ is the impedance of the RC compensation network that forms a pole at origin and a zero as expressed in Equation 13.

$$Z_{COMP}(s) = \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times C_{COMP}} \quad (13)$$

$Z_{FILT}(s)$ is the impedance of the output filter and is expressed as

$$Z_{FILT}(s) = \frac{R_{LOAD}}{1 + s \times R_{LOAD} \times C_{OUT}} \quad (14)$$

where s is angular frequency that can be written as s = 2πf.

The overall loop gain, H(s), is obtained by multiplying the three transfer functions previously mentioned as follows:

$$H(s) = g_M \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILT}(s) \quad (15)$$

When the switching frequency (f_{SW}), output voltage (V_{OUT}), output inductor (L), and output capacitor (C_{OUT}) values are selected, the unity crossover frequency of 1/12 (approximately) the switching frequency can be targeted.

At the crossover frequency, the gain of the open-loop transfer function is unity. This yields Equation 16 for the compensation network impedance at the crossover frequency.

$$Z_{COMP}(f_{CROSS}) = \frac{2 \times \pi \times f_{CROSS} \times C_{OUT}}{g_m \times G_{CS}} \times \frac{V_{OUT}}{V_{REF}} \quad (16)$$

To ensure that there is sufficient phase margin at the crossover frequency, place the compensator zero at 1/8 of the crossover frequency, as shown in Equation 17.

$$f_{ZERO} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \approx \frac{f_{CROSS}}{8} \quad (17)$$

Solving Equation 16 and Equation 17 simultaneously yields the value for the compensation resistor and compensation capacitor, as shown in Equation 18 and Equation 19.

$$R_{COMP} = 0.9 \times \left(\frac{(2\pi)F_{CROSS}}{G_m G_{CS}} \right) \times \left(\frac{C_{OUT} V_{OUT}}{V_{REF}} \right) \quad (18)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{ZERO} \times R_{COMP}} \quad (19)$$

The capacitor C_{C2} (as shown in Figure 77) forms a pole with the compensation resistor, R_{COMP}, in the feedback loop to ensure that the loop gain keeps rolling off well beyond the unity-gain crossover frequency. The value of C_{C2}, if used, is typically set to 1/40 of the compensation capacitor, C_{COMP}.

DESIGN EXAMPLE

The external component selection procedure from the Control Loop Compensation section is used for this design example.

Table 9. 2-Channel Step-Down DC-to-DC Converter Requirements

Parameter	Specification	Additional Requirements
Input Voltage, V_{IN}	5.0 V ±10%	None
Channel 1, V_{OUT1}	3.3 V, 2 A, 1% V_{OUT} ripple (p-p)	Maximum load step: 1 A to 2 A, 5% droop maximum
Channel 2, V_{OUT2}	1.8 V, 2 A, 1% V_{OUT} ripple (p-p)	Maximum load step: 1 A to 2 A, 5% droop maximum
Pulse-Skip Feature	Enabled	None

CHANNEL 1 CONFIGURATION AND COMPONENTS SELECTION

Complete the following steps to configure Channel 1:

1. For the target output voltage, V_{OUT} = 3.3 V, connect the V1SET pin through a 47 kΩ resistor to GND (see Table 4). Because one of the fixed output voltage options is chosen, the feedback pin (FB1) must be directly connected to the output of Channel 1, V_{OUT1}.
2. Estimate the duty-cycle, D, range. Ideally,

$$D = \frac{V_{OUT}}{V_{IN}} \tag{20}$$

That gives the duty cycle for the 3.3 V output voltage and the nominal input voltage of D_{NOM} = 0.66 at V_{IN} = 5.0 V.

The minimum duty cycle, D_{MIN}, for the maximum input voltage (10% above the nominal) is D_{MIN} = 0.60 at V_{IN} maximum = 5.5 V

The maximum duty cycle, D_{MAX}, for the minimum input voltage (10% less than nominal) is D_{MAX} = 0.73 at V_{IN} minimum = 4.5 V.

However, the actual duty cycle is larger than the calculated values to compensate for the power losses in the converter. Therefore, add 5% to 7% at the maximum load.

Based on the estimated duty-cycle range, choose the switching frequency according to the minimum and maximum duty-cycle limitations, as shown in Figure 72.

For the Channel 1 V_{IN} = 5 V and V_{OUT} = 3.3 V combination, choose f_{SW} = 600 kHz with a maximum duty cycle of 0.8. This frequency option provides the smallest sized solution. If a higher efficiency is required, choose the 300 kHz option. However, the PCB footprint area of the converter will be larger because of the bigger inductor and output capacitors.

3. Select the inductor by using Equation 5.

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In Equation 5, V_{IN} = 5 V, V_{OUT} = 3.3 V, $\Delta I_L = 0.3 \times I_L$ = 0.6 A, and f_{SW} = 600 kHz, which results in L = 3.11 µH.

Therefore, when L = 3.3 µH (the closest standard value) in Equation 3, ΔI_L = 0.566 A.

Although the maximum output current required is 2 A, the maximum peak current is 3.3 A under the current limit condition (see Table 7). Therefore, the inductor should be rated for 3.3 A of peak current and 3 A of average current for reliable circuit operation.

4. Select the output capacitor by using Equation 8 and Equation 9.

$$C_{OUT_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)}$$

$$C_{OUT_MIN} \cong \Delta I_{OUT_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right)$$

Equation 8 is based on the output ripple (ΔV_{RIPPLE}), and Equation 9 is for capacitor selection based on the transient load performance requirements that allow, in this case, 5% maximum deviation. As previously mentioned, perform these calculations and choose whatever equation yields the larger capacitor size.

In this case, the following values are substituted for the variables in Equation 8 and Equation 9:

ΔI_L = 0.566 A

f_{SW} = 600 kHz

ΔV_{RIPPLE} = 33 mV (1% of 3.3 V)

ESR = 3 mΩ (typical for ceramic capacitors)

ΔI_{OUT_STEP} = 1 A

ΔV_{DROOP} = 0.165 V (5% of 3.3 V)

The output ripple based calculation (see Equation 8) dictates that C_{OUT} = 4.0 µF, whereas the transient load based calculation (see Equation 9) dictates that C_{OUT} = 30 µF. To meet both requirements, choose the latter. As previously mentioned in the Control Loop Compensation section, the capacitor value reduces with applied dc bias; therefore, select a higher value. In this case, the next higher value is 47 µF with a minimum voltage rating of 6.3 V.

5. Calculate the feedback loop, compensation component values by using Equation 15.

$$H(s) = g_M \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILT}(s)$$

In this case, the following values are substituted for the variables in Equation 18:

g_m = 550 µs

G_{CS} = 4A/V

V_{REF} = 0.6 V

V_{OUT} = 3.3 V

C_{OUT} = 0.8 × 47 µF (capacitance derated by 20% to account for dc bias).

From Equation 18,

R_{COMP} = 27 kΩ.

Substituting R_{COMP} in Equation 19 yields C_{COMP} = 1000 pF.

Table 10. Channel 1 Circuit Settings

Circuit Parameter	Setting	Value
Output Voltage, V_{OUT}	Step 1	3.3 V
Reference Voltage, V_{REF}	Fixed, typical	0.6 V
Error Amp Transconductance, g_m	Fixed, typical	550 µs
Current Sense Gain, C_{CS}	Fixed, typical	4 A/V
Switching Frequency, f_{SW}	Step 2	600 kHz
Crossover Frequency, f_C	1/12 f_{SW}	50 kHz
Zero Frequency, f_{ZERO}	1/8 f_{CROSS}	6.25 kHz
Output Inductor, L_{OUT}	Step 3	3.3 µH
Output Capacitor, C_{OUT}	Step 4	47 µF, 6.3 V
Compensation Resistor, R_{COMP}	Equation 18	27 kΩ
Compensation Capacitor, C_{COMP}	Equation 19	1000 pF

CHANNEL 2 CONFIGURATION AND COMPONENTS SELECTION

Complete the following steps to configure Channel 2:

1. For the target output voltage, V_{OUT} = 1.8 V, connect the V2SET pin through a 15 kΩ resistor to GND (see Table 4). Because one of the fixed output voltage options is chosen, the feedback pin (FB2) must be directly connected to the output of Channel 2, V_{OUT2}.
2. Estimate the duty-cycle, D, range (see Equation 20). Ideally,

$$D = \frac{V_{OUT}}{V_{IN}}$$

That gives the duty cycle for the 1.8 V output voltage and the nominal input voltage of D_{NOM} = 0.36 at V_{IN} = 5.0 V.

The minimum duty cycle for the maximum input voltage (10% above the nominal) is D_{MIN} = 0.33 at V_{IN} maximum = 5.5 V.

The maximum duty cycle for the minimum input voltage (10% less than nominal) is D_{MAX} = 0.4 at V_{IN} minimum = 4.5 V.

However, the actual duty cycle is larger than the calculated values to compensate for the power losses in the converter. Therefore, add 5% to 7% at the maximum load.

The switching frequency (f_{SW}) of 600 kHz, which is chosen based on the Channel 1 requirements, meets the duty cycle ranges that have been previously calculated. Therefore, this switching frequency is acceptable.

3. Select the inductor by using Equation 5.

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In Equation 5, V_{IN} = 5 V, V_{OUT} = 1.8 V, $\Delta I_L = 0.3 \times I_L$ = 0.6 A, and f_{SW} = 600 kHz, which results in L = 2.9 µH.

Therefore, when L = 3.3 µH (the closest standard value) in Equation 3, ΔI_L = 0.582 A.

Although the maximum output current required is 2 A, the maximum peak current is 3.3 A under the current limit condition (see Table 7). Therefore, the inductor should be rated for 3.3 A of peak current and 3 A of average current for reliable circuit operation under all conditions.

4. Select the output capacitor by using Equation 8 and Equation 9.

$$C_{OUT_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)}$$

$$C_{OUT_MIN} \cong \Delta I_{OUT_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right)$$

Equation 8 is based on the output ripple (ΔV_{RIPPLE}), and Equation 9 is for capacitor selection based on the transient load performance requirements that allow, in this case, 5% maximum deviation. As mentioned earlier, perform these calculations and choose whatever equation yields the larger capacitor size.

In this case, the following values are substituted for the variables in Equation 8 and Equation 9:

ΔI_L = 0.582 A

f_{SW} = 600 kHz

ΔV_{RIPPLE} = 18 mV (1% of 1.8 V)

ESR = 3 mΩ (typical for ceramic capacitors)

ΔI_{OUT_STEP} = 1 A

ΔV_{DROOP} = 0.09 V (5% of 1.8 V)

The output ripple based calculation (see Equation 8) dictates that C_{OUT} = 7.7 µF, whereas the transient load based calculation (see Equation 9) dictates that C_{OUT} = 55 µF. To meet both requirements, choose the latter. As previously mentioned in the Control Loop Compensation section, the capacitor value reduces with applied dc bias; therefore, select a higher value. In this case, choose a 47 µF/6.3 V capacitor and a 22 µF/6.3 V capacitor in parallel to meet the requirements.

5. Calculate the feedback loop, compensation component values by using Equation 15.

$$H(s) = g_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILT}(s)$$

In this case, the following values are substituted for the variables in Equation 18:

g_m = 550 µs

G_{CS} = 4

V_{REF} = 0.6 V

V_{OUT} = 1.8 V

C_{OUT} = 0.8 × (47+22) µF (capacitance derated by 20% to account for dc bias).

From Equation 18,

R_{COMP} = 22 kΩ.

Substituting R_{COMP} in Equation 19 yields C_{COMP} = 1100 pF.

Table 11. Channel 2 Circuit Settings

Circuit Parameter	Setting	Value
Output Voltage, V_{OUT}	Nominal	1.8 V
Reference Voltage, V_{REF}	Typical	0.6 V
Error Amp Transconductance, g_m	Typical	550 µs
Current Sense Gain, C_{CS}	Typical	4 A/V
Switching Frequency, f_{SW}	Step 2	600 kHz
Crossover Frequency, f_{CROSS}	1/12 f_{SW}	50 kHz
Zero Frequency, f_{ZERO}	1/8 f_{CROSS}	6.25 kHz
Output Inductor, L_{OUT}	Step 3	3.3 µF
Output Capacitors, C_{OUT}	Step 4	47 µF + 22 µF
Compensation Resistor, R_{COMP}	Equation 18	22 kΩ
Compensation Capacitor, C_{COMP}	Equation 19	1100 pF

SYSTEM CONFIGURATION

Complete the following steps to further configure the ADP2114 for this design example:

1. Set the switching frequency (f_{SW}) = 600 kHz (see Table 5) by connecting the FREQ pin through an 8.2 kΩ resistor to GND.
2. Tie SCFG to VDD and use the CLKOUT signal to synchronize other converters on the same board with the ADP2114.
3. Tie OPCFG to GND for 2 A/2 A maximum output current operation and to enable pulse skip mode at light load conditions (see Table 7).

A schematic of the ADP2114 as configured in the design example described in this section is shown in Figure 79.

Table 12 provides the recommended inductor, output capacitor, and compensation component values for a set of popular input and output voltage combinations.

Table 12. Selection Table of L, C_{OUT}, and Compensation Values

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	Maximum Load (A)	L (µH)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (pF)
300	5	3.3	2.0	6.8	69 (47 + 22)	20	2400
300	5	2.5	2.0	6.8	100	22	2400
300	5	1.8	2.0	6.8	147 (100 + 47)	22	2400
300	5	1.2	2.0	4.7	200 (2 × 100)	20	2400
600	5	3.3	2.0	3.3	47	27	1000
600	5	2.5	2.0	3.3	57 (47 + 10)	24	1100
600	5	1.8	2.0	3.3	69 (47 + 22)	22	1100
600	5	1.2	2.0	2.2	100	20	1200
1200	5	2.5	2.0	1.8	32 (22 + 10)	27	470
1200	5	1.8	2.0	1.8	44 (2 × 22)	27	470
1200	5	1.2	2.0	1.2	57 (47 + 10)	24	510
1200	5	0.8	2.0	1.0	100	27	470

APPLICATION CIRCUITS

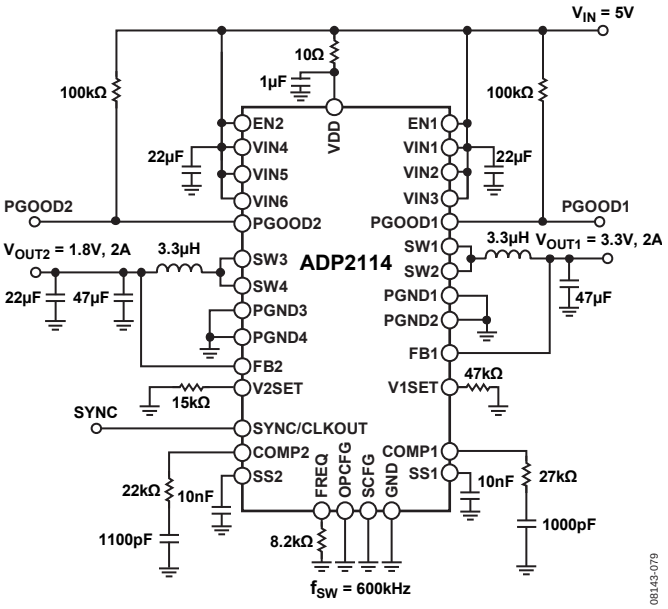

Figure 79. Application Circuit for 2 A/2 A Outputs

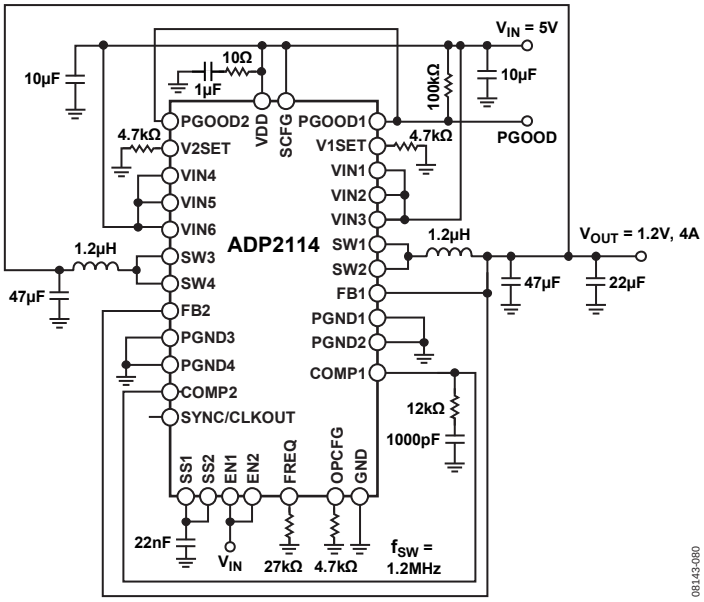

Figure 80. Application Circuit for a Single 4 A Output

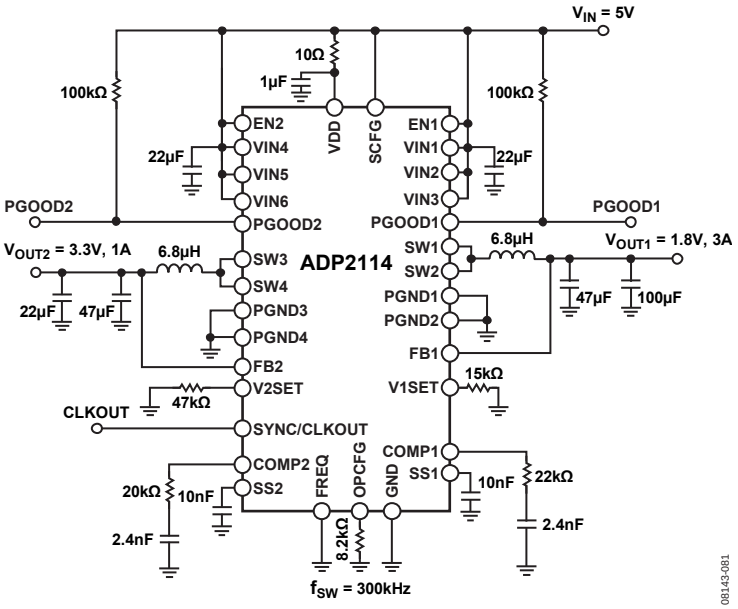

Figure 81. Application Circuit for 3 A/1 A Outputs

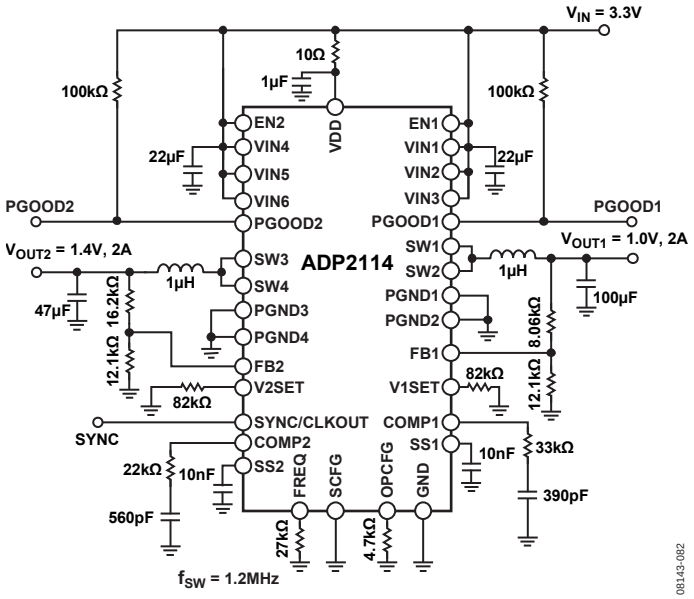

Figure 82. Application Circuit for Adjustable Outputs

POWER DISSIPATION, THERMAL CONSIDERATIONS

Power dissipated by the ADP2114 dual switching regulator is a major factor that affects the efficiency of the two dc-to-dc converters. The efficiency is given by

$$Efficiency = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (21)$$

where:
P_{IN} is the input power.
P_{OUT} is the output power.
Power loss is given by $P_{LOSS} = P_{IN} - P_{OUT}$.

The power loss of the step-down dc-to-dc converter is approximated by

$$P_{LOSS} = P_D + P_L \quad (22)$$

where:
P_D is the power dissipation on the ADP2114.
P_L is the inductor power losses.

The inductor losses are estimated (without core losses) by

$$P_L \cong I_{OUT}^2 \times DCR_L \quad (23)$$

where:
I_{OUT} is the dc load current.
DCR_L is the inductor series resistance.

The ADP2114 power dissipation, P_D, includes the power switch conductive losses, the switch losses, and the transition losses of each channel.

The power switch conductive losses are due to the output current, I_{OUT}, flowing through the PMOSFET and the NMOSET power switches that have internal resistance, R_{DSON}. The amount of conductive power loss is found by

$$P_{COND} = [R_{DSON\text{-}P} \times D + R_{DSON\text{-}N} \times (1 - D)] \times I_{OUT}^2 \quad (24)$$

where the duty-cycle, D, = V_{OUT}/V_{IN}.

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by

$$P_{SW} = (C_{GATE\text{-}P} + C_{GATE\text{-}N}) \times V_{IN}^2 \times f_{SW} \quad (25)$$

where:
$C_{GATE\text{-}P}$ is the PMOSFET gate capacitance.
$C_{GATE\text{-}N}$ is the NMOSFET gate capacitance.

Transition losses occur because the P-channel power MOSFET cannot be turned on or off instantaneously. The amount of transition loss is calculated by

$$P_{TRAN} = V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (26)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SW. In the ADP2114, the rise and fall times of the switching node are in the order of 5 ns.

The power dissipated by the regulator increases the die junction temperature, T_J, above the ambient temperature, T_A.

$$T_J = T_A + T_R \quad (27)$$

where the temperature rise, T_R, is proportional to the power dissipation in the package, P_D.

The proportionality coefficient is defined as the thermal resistance from the junction of the die to the ambient temperature.

$$T_R = \theta_{JA} \times P_D \quad (28)$$

where θ_{JA} is the junction-ambient thermal resistance (34°C/W for the JEDEC 1S2P board, see Table 2).

When designing an application for a particular ambient temperature range, calculate the expected ADP2114 power dissipation (P_D) due to conductive, switching, and transition losses of both channels by using Equation 24, Equation 25, and Equation 26 and estimate the temperature rise by using Equation 27 and Equation 28. The reliable operation of the two converters can be achieved only if the estimated die junction temperature of the ADP2114 (Equation 27) is less than 125°C. Therefore, at higher ambient temperatures, reduce the power dissipation of the system. Figure 83 provides the power derating for the elevated ambient temperature at different air flow conditions. The area below the curves is the safe operation area for ADP2114 dual regulators.

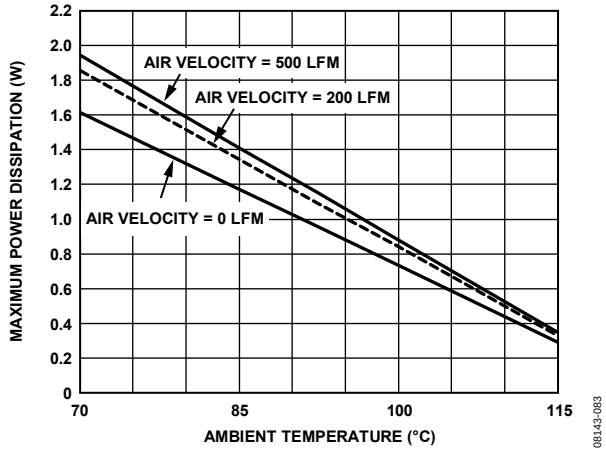

Figure 83. Power Dissipation Derating (JEDEC 1S2P Board)

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential in obtaining the best performance from each channel of the ADP2114. Poor circuit layout degrades the output ripple and regulation, as well as the EMI and electromagnetic compatibility performance. For optimum layout, refer to the following guidelines:

- Use separate analog and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground references of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed pad of the ADP2114.
- Place the input capacitor of each channel as close to the VINx pins as possible and connect the other end to the closest power ground plane.
- For low noise and better transient performance, a filter is recommended between VINx and VDD. Place a 1 µF, 10 Ω low-pass input filter between the VDD pin and the VINx pins, as close to the GND pin as possible.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from C_{IN} through L, C_{OUT}, and the power ground plane back to C_{IN} as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane. In addition, make the high current path from the PGNDx pin through L and C_{OUT} back to the power ground plane as short as possible. To do this, ensure that the PGNDx pin of the ADP2114 is tied to the PGND plane as close as possible to the input and output capacitors (see Figure 84).
- Connect the ADP2114 exposed pad to a large copper plane to maximize its power dissipation capability. Thermal conductivity can be obtained using the method described in JEDEC specification JESD51-7.
- Place the feedback resistor divider network as close as possible to the FBx pin to prevent noise pickup. Try to minimize the length of the trace connecting the top of the feedback resistor divider to the output while keeping away from the high current traces and the switch node, SWx, that can lead to noise pickup. To reduce noise pickup, place an analog ground plane on either side of the FBx trace and make it as small as possible to reduce the parasitic capacitance pickup.

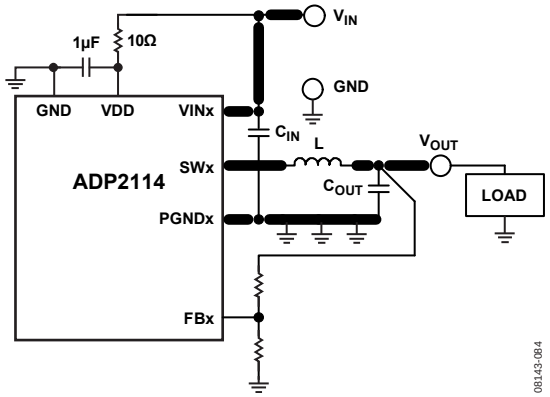

Figure 84. High Current Traces in the PCB Circuit

OUTLINE DIMENSIONS

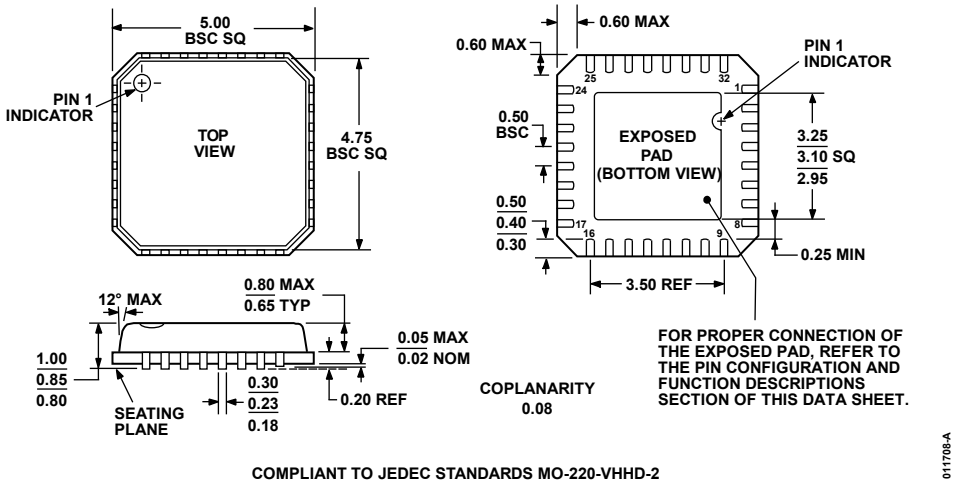

Figure 85. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option	Ordering Quantity
ADP2114ACPZ-R7[2]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2	1,500
ADP2114-2PH-EVALZ[2]		Single output, dual-phase interleaved, 1.2 V at 4 A, 1.2 MHz switching frequency, forced PWM		
ADP2114-EVALZ[2]		Dual output, 3.3 V at 2 A and 1.8 V at 2 A, 600 kHz switching frequency, pulse skip enabled		

[1] Operating junction temperature is −40°C to +125°C.
[2] Z = RoHS Compliant Part.

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