Logic Controlled, High-Side Power Switch with Reverse Current Blocking

ADP195

FEATURES

- Low RDS_{ON} of 65 mΩ @ 1.8 V
- Low input voltage range: 1.1 V to 3.6 V
- >1 A continuous operating current @ 85°C
- Built-in level shift for control logic that can be operated by 1.2 V logic
- Low 10 µA (maximum) ground current @ 3.6 V
- Low 1 µA (typical) ground current @ 1.8 V
- Low 4 µA (maximum) reverse current @ 3.6 V
- Reverse current blocking
- Ultralow shutdown current: <0.7 µA
- Ultrasmall 1.0 mm × 1.0 mm, 4-ball, 0.5 mm pitch WLCSP

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment

TYPICAL APPLICATIONS CIRCUIT

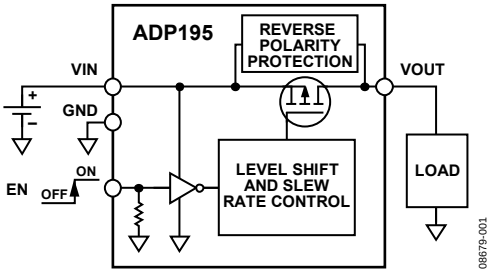

Figure 1.

GENERAL DESCRIPTION

The ADP195 is a high-side load switch designed for operation between 1.1 V to 3.6 V and protected against reverse current flow from output to input. This load switch provides power domain isolation helping extended power domain isolation. The device contains a low on-resistance, P-channel MOSFET that supports over 500 mA of continuous current and minimizes power loss. The low 10 µA of quiescent current and ultralow shutdown current make the ADP195 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP195 compatible with many processors and GPIO controllers.

In addition to operating performance, the ADP195 occupies minimal printed circuit board (PCB) space with an area of less than 1.0 mm^2 and a height of 0.60 mm.

It is available in an ultrasmall 1 mm × 1 mm, 4-ball, 0.5 mm pitch WLCSP.

Rev. 0
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REVISION HISTORY

3/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{OUT} = 200 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.1		3.6	V
EN INPUT						
EN Input Threshold	V_{IH}	1.1 V ≤ V_{IN} < 1.8 V, T_J = −40°C to +85°C	0.29		1.0	V
		1.8 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +85°C	0.45		1.2	
EN Input Pull-Down Current	I_{EN}	V_{IN} = 1.8 V		500		nA
V_{IN} Shutdown Current		V_{EN} = 0 V, V_{IN} = 0 V, V_{OUT} = 3.6 V		−10		nA
REVERSE BLOCKING						
V_{OUT} Current		V_{EN} = 0 V, V_{IN} = 0 V, V_{OUT} = 3.6 V		4		µA
Hysteresis		$\lvert V_{IN} - V_{OUT} \rvert$		75		mV
CURRENT						
Ground Current	I_{GND}	V_{OUT} = 0, includes V_{EN} pull-down and reverse blocking bias current, V_{IN} = 3.6 V, T_J = −40°C to +85°C			10	µA
		V_{OUT} = 0, includes V_{EN} pull-down and reverse blocking bias current, V_{IN} = 1.8 V		1		µA
Off State Current	I_{OFF}	V_{EN} = GND (includes reverse blocking bias current), V_{OUT} = 0 V		0.7		µA
		V_{EN} = GND, T_J = −40°C to +85°C, V_{OUT} = 0 V			5	µA
V_{IN} to V_{OUT} RESISTANCE	RDS_{ON}					
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 3.6 V		0.050		Ω
		V_{IN} = 2.5 V, I_{LOAD} = 200 mA, V_{EN} = 2.5 V		0.055		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.8 V		0.065		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.8 V, T_J = −40°C to +85°C			0.095	Ω
		V_{IN} = 1.5 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		0.075		Ω
		V_{IN} = 1.2 V, I_{LOAD} = 200 mA, V_{EN} = 1.2 V		0.100		Ω
V_{OUT} TURN-ON DELAY TIME						
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 1.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.8 V, C_{LOAD} = 1 µF		5		µs
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 3.6 V, C_{LOAD} = 1 µF		1.5		µs

TIMING DIAGRAM

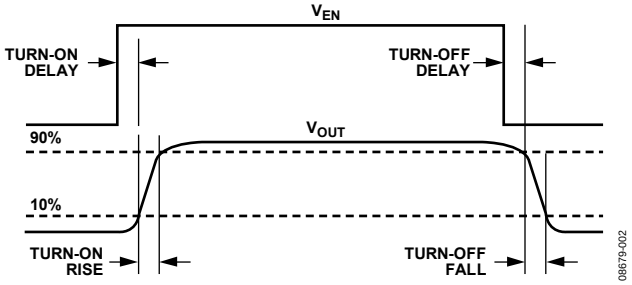

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +4.0 V
VOUT to GND	−0.3 V to V_{IN}
EN to GND	−0.3 V to +4.0 V
Continuous Drain Current	
T_A = 25°C	±2 A
T_A = 85°C	±1.1 A
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Typical Ψ_{JB} Values

Package	Ψ_{JB}	Unit
4-Ball WLCSP	58.4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

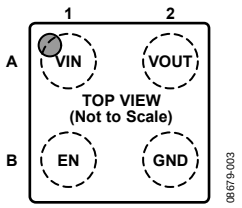

Figure 3. 4-Ball WLCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Input Voltage.
A2	VOUT	Output Voltage.
B1	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

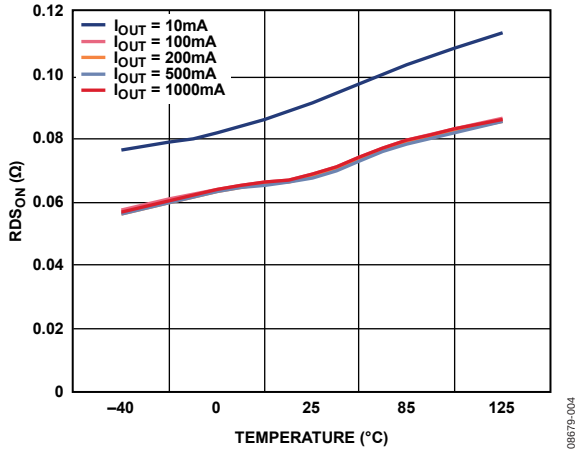

Figure 4. RDS_{ON} vs. Temperature

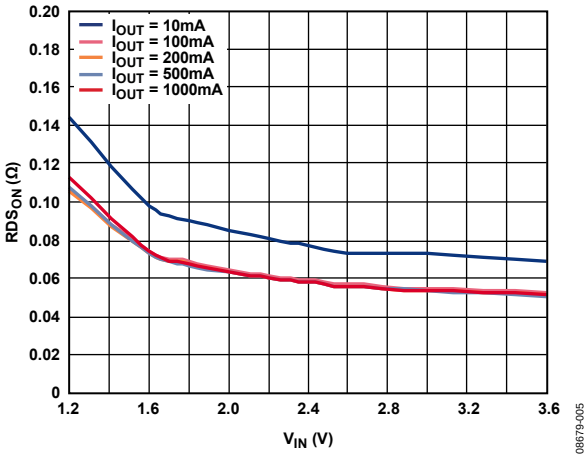

Figure 5. RDS_{ON} vs. Input Voltage (V_{IN})

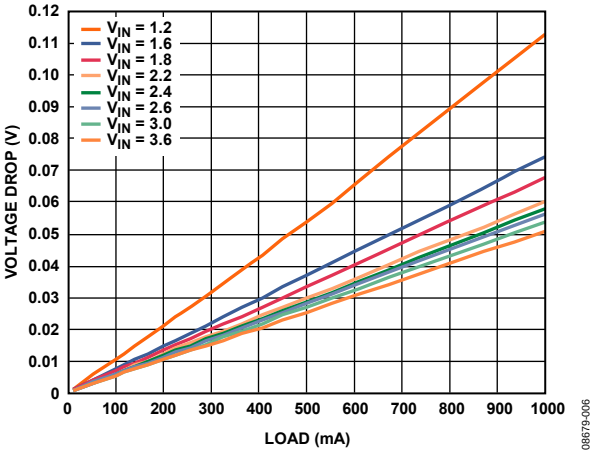

Figure 6. Voltage Drop vs. Load Current

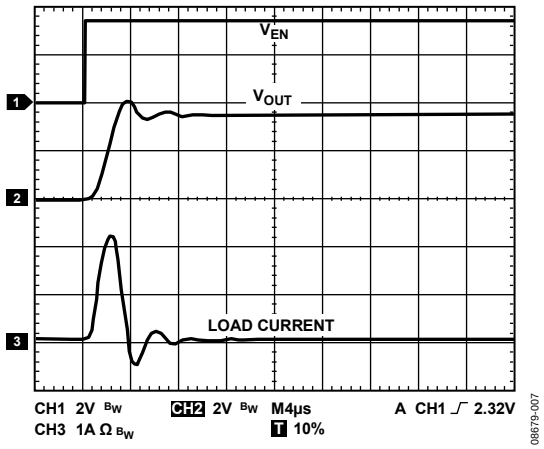

Figure 7. Typical Rise Time and Inrush Current, V_{IN} = 3.6 V, No Load

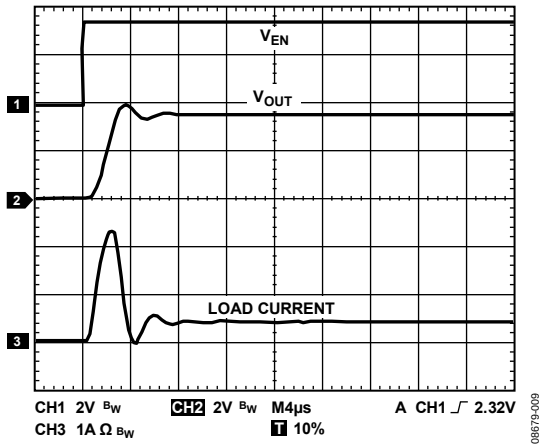

Figure 8. Typical Rise Time and Inrush Current, V_{IN} = 3.6 V, Load = 200 mA

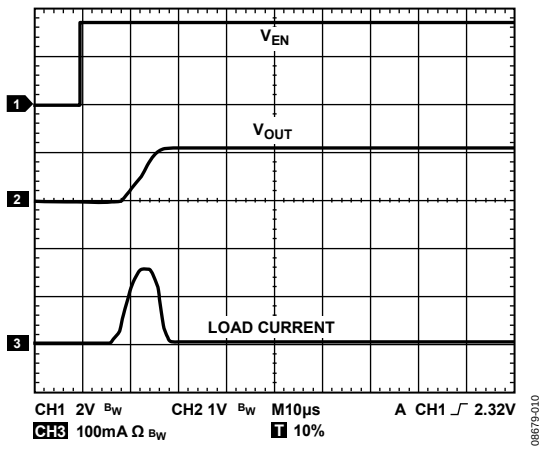

Figure 9. Typical Rise Time and Inrush Current, V_{IN} = 1.2 V, No Load

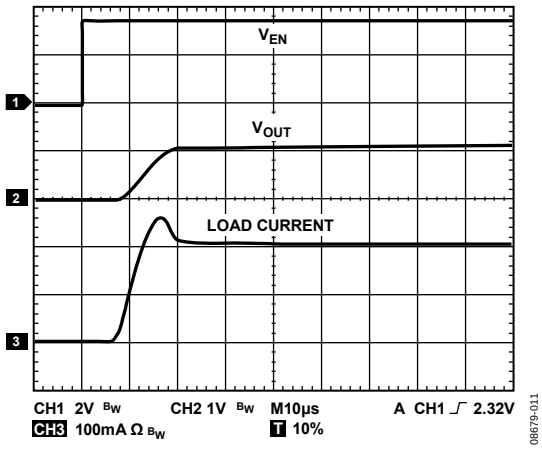

Figure 10. Typical Rise Time and Inrush Current, V_{IN} = 1.2 V, Load = 200 mA

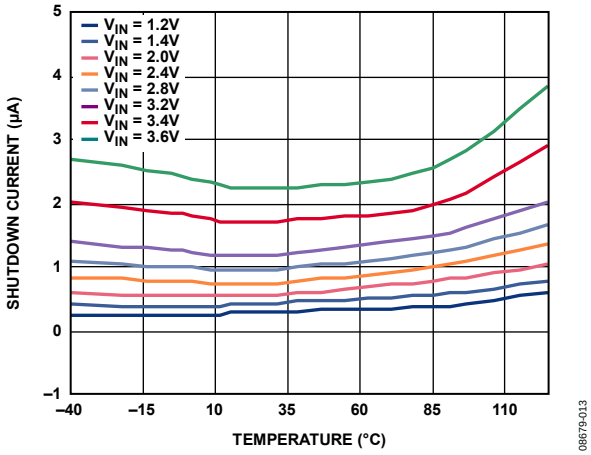

Figure 13. Shutdown Current vs. Temperature

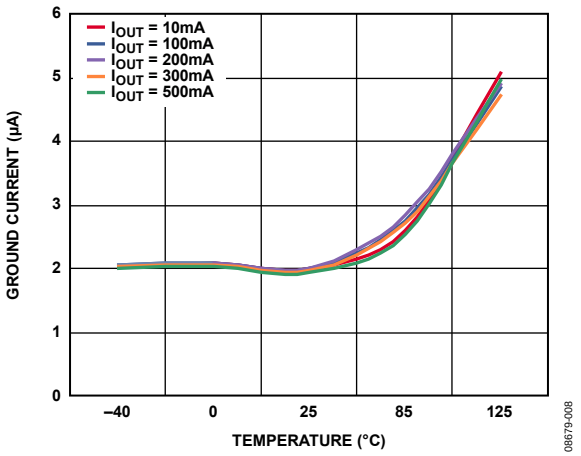

Figure 11. Ground Current vs. Temperature

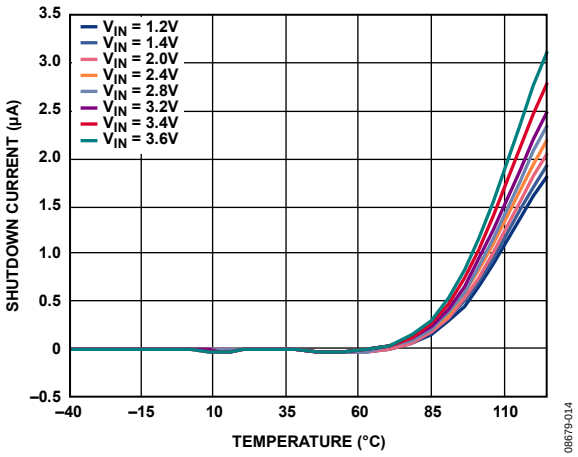

Figure 14. Reverse Input Shutdown Current vs. Temperature

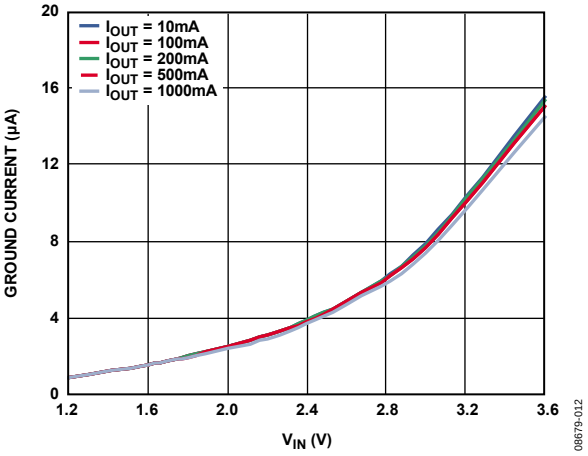

Figure 12. Ground Current vs. Input Voltage (V_{IN})

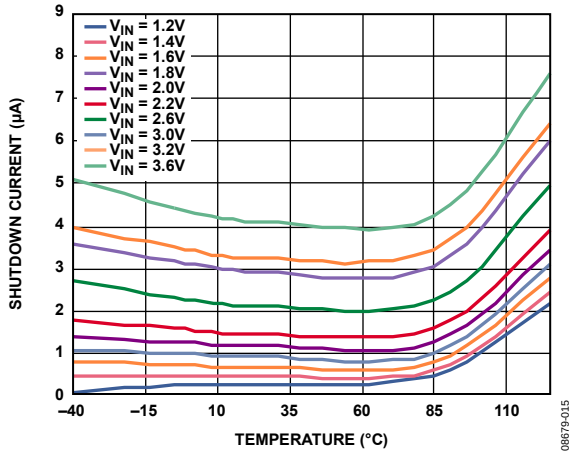

Figure 15. Reverse Output Shutdown Current vs. Temperature

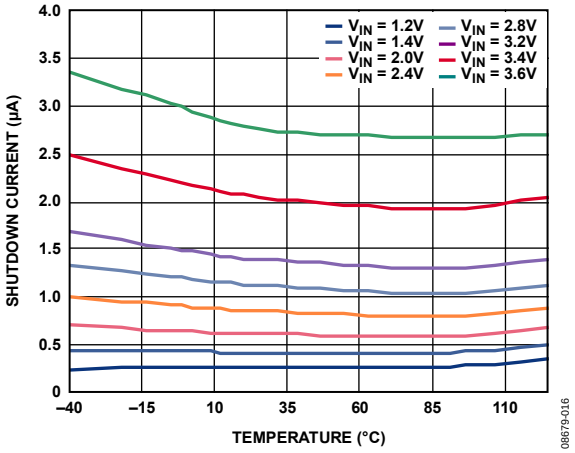

Figure 16. Reverse Shutdown Current vs. Temperature

THEORY OF OPERATION

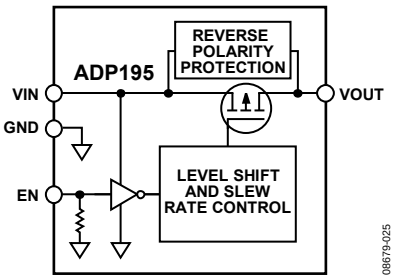

Figure 17. Functional Block Diagram

The ADP195 is a high-side PMOS load switch. It is designed for supply operation between 1.1 V to 3.6 V. The PMOS load switch is designed for low on resistance, 65 mΩ at V_{IN} = 1.8 V and supports greater than 1 A of continuous current. It is a low quiescent current device with a nominal 4 MΩ pull-down resistor on its enable pin (EN). The packaging is a space-saving 1.0 mm × 1.0 mm, 4-ball WLCSP.

APPLICATIONS INFORMATION

GROUND CURRENT

The major source for ground current in the ADP195 is an internal 4 MΩ pull-down on the enable pin. Figure 18 shows the typical ground current when $V_{EN} = V_{IN}$ and varies from 1.2 V to 3.6 V.

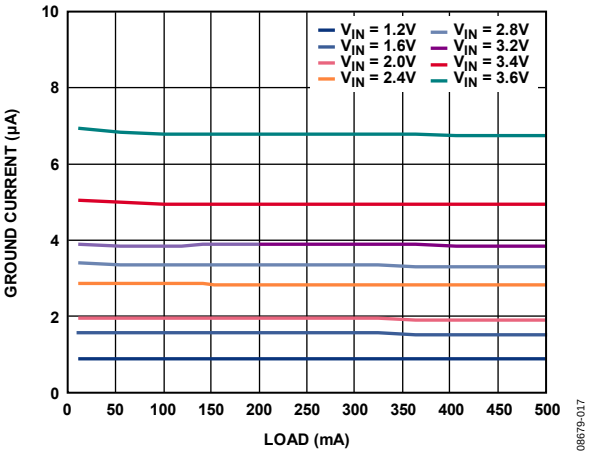

Figure 18. Ground Current vs. Load Current

As shown in Figure 19, an increase in quiescent current can occur when $V_{EN} \neq V_{IN}$. This is caused by the CMOS logic nature of the level shift circuitry as it translates an V_{EN} signal ≥ 1.2 V to a logic high. This increase is a function of the $V_{IN} - V_{EN}$ delta.

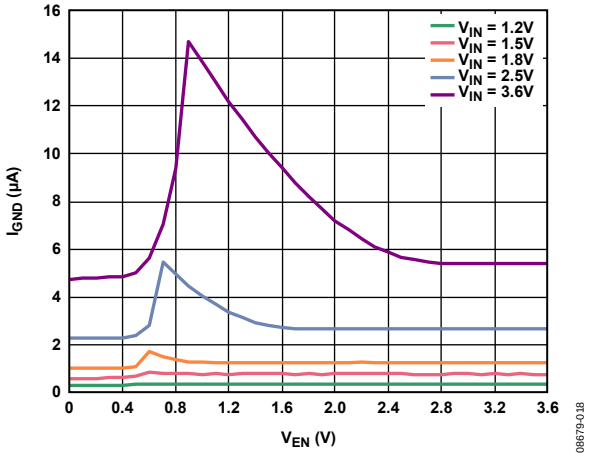

Figure 19. Typical Ground Current when $V_{EN} \neq V_{IN}$

ENABLE FEATURE

The ADP195 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 20, when a rising voltage on V_{EN} crosses the active threshold, V_{OUT} turns on. When a falling voltage on V_{EN} crosses the inactive threshold, V_{OUT} turns off.

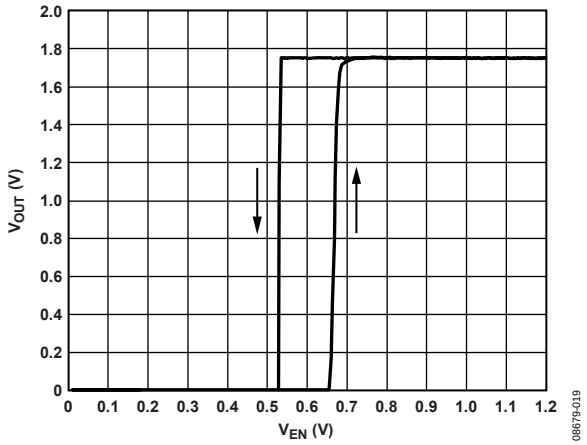

Figure 20. Typical EN Operation

As shown in Figure 20, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with the changing input voltage. Figure 21 shows the typical EN active/inactive thresholds when the input voltage varies from 1.2 V to 3.6 V.

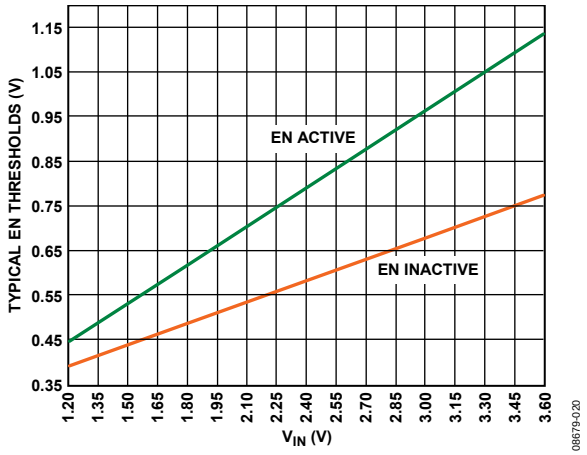

Figure 21. Typical EN Thresholds vs. Input Voltage (V_{IN})

TIMING

Turn-on delay is defined as the delta between the time that V_{EN} reaches >1.2 V until V_{OUT} rises to ~10% of its final value. The ADP195 includes circuitry to have typical 5 µs turn-on delay at 3.6 V V_{IN} to limit the V_{IN} inrush current. As shown in Figure 22, the turn-on delay is dependent on the input voltage.

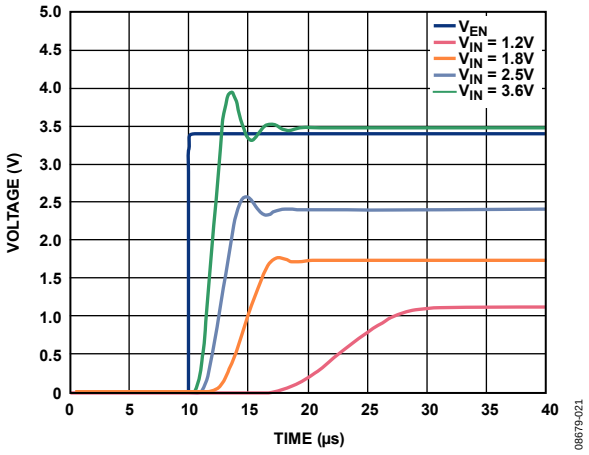

Figure 22. Typical Turn-On Delay Time with Varying Input Voltage

The rise time is defined as the delta between the time from 10% to 90% of V_{OUT} reaching its final value. It is dependent on the RC time constant where C = load capacitance (C_{LOAD}) and R = $RDS_{ON}||R_{LOAD}$. Because RDS_{ON} is usually smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. An input or load capacitor is not needed for the ADP195; however, capacitors can be used to suppress noise on the board. If significant load capacitance is connected, inrush current is a concern.

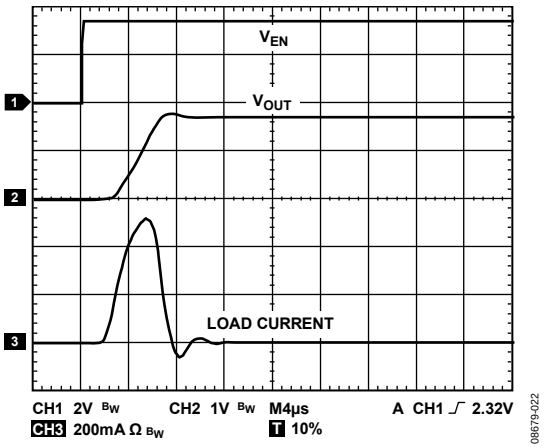

Figure 23. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 1.8 V, No Load

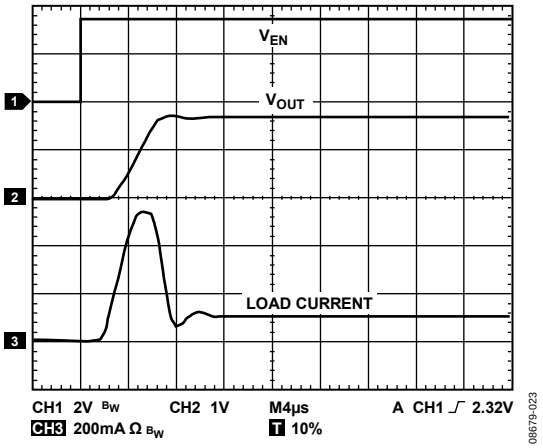

Figure 24. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 1.8 V, Load = 200 mA

The turn-off time is defined as the delta between the time from 90% to 10% of V_{OUT} reaching its final value. It is also dependent on the RC time constant.

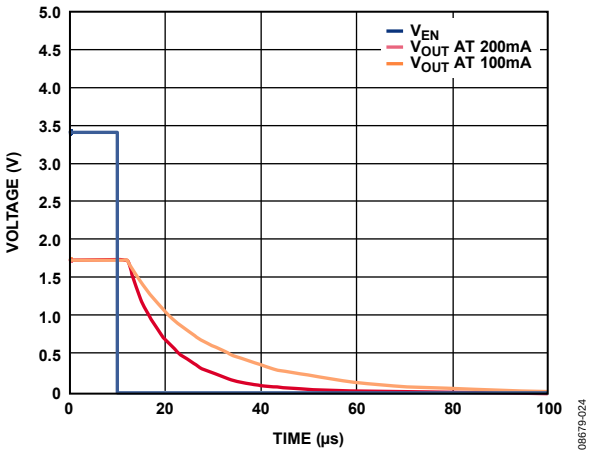

Figure 25. Typical Turn-Off Time

OUTLINE DIMENSIONS

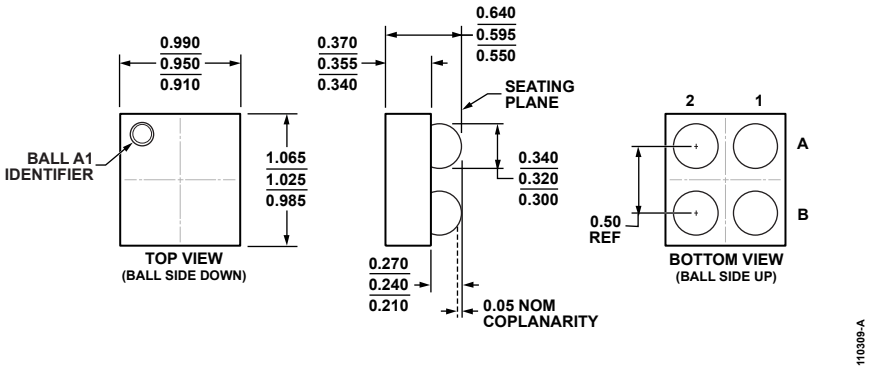

Figure 26. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP195ACBZ-R7	−40°C to +85°C	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-4	5Y

[1] Z = RoHS Compliant Part.

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