500 mA, Low Dropout, CMOS Linear Regulator

ADP1715/ADP1716

FEATURES

- Maximum output current: 500 mA
- Input voltage range: 2.5 V to 5.5 V
- Low shutdown current: <1 µA
- Low dropout voltage:
  - 250 mV @ 500 mA load
  - 50 mV @ 100 mA load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: ±3%
- 16 fixed output voltage options with soft start:
  - 0.75 V to 3.3 V (ADP1715)
- Adjustable output voltage option: 0.8 V to 5.0 V
  - (ADP1715 Adjustable)
- 16 fixed output voltage options with tracking:
  - 0.75 V to 3.3 V (ADP1716)
- Stable with small 2.2 µF ceramic output capacitor
- Excellent load/line transient response
- Current limit and thermal overload protection
- Logic controlled enable
- 8-lead thermally enhanced MSOP package

APPLICATIONS

- Notebook computers
- Memory components
- Telecommunications equipment
- Network equipment
- DSP/FPGA/µP supplies
- Instrumentation equipment/data acquisition systems

TYPICAL APPLICATION CIRCUITS

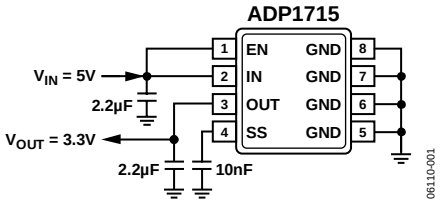


Figure 1. ADP1715 with Fixed Output Voltage, 3.3 V

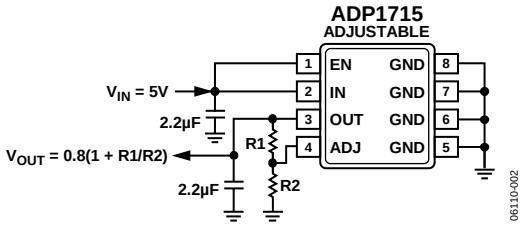


Figure 2. ADP1715 with Adjustable Output Voltage, 0.8 V to 5.0 V

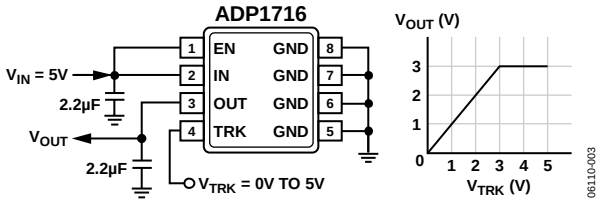


Figure 3. ADP1716 with Output Voltage Tracking

GENERAL DESCRIPTION

The ADP1715/ADP1716 are low dropout, CMOS linear regulators that operate from 2.5 V to 5.5 V and provide up to 500 mA of output current. Using an advanced proprietary architecture, they provide high power supply rejection and achieve excellent line and load transient response with just a small 2.2 µF ceramic output capacitor.

Three versions of this part are available, one with fixed output voltage options and variable soft start (ADP1715), one with adjustable output voltage and fixed soft start (ADP1715 Adjustable), and one with voltage tracking in fixed output voltage options (ADP1716). The fixed output voltage options are internally set to one of sixteen values between 0.75 V and 3.3 V; the adjustable output voltage can be set to any value between 0.8 V and 5.0 V by an external voltage divider connected from OUT to ADJ. The variable soft start uses an external capacitor at SS to control the output voltage ramp. Tracking limits the output voltage to the at-or-below voltage at the TRK pin.

The ADP1715/ADP1716 are available in 8-lead thermally enhanced MSOP packages, making them not only a very compact solution but also providing excellent thermal performance for applications requiring up to 500 mA of output current in a small, low profile footprint.

Rev. 0
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REVISION HISTORY

9/06—Rev. 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 100 µA		65		µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			100	µA
		I_{OUT} = 100 mA		160		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			220	µA
		100 µA < I_{OUT} < 500 mA, T_J = −40°C to +125°C			650	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
FIXED OUTPUT VOLTAGE ACCURACY (ADP1715 and ADP1716 ONLY)	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		I_{OUT} = 10 mA to 500 mA	−2		+2	%
		100 µA < I_{OUT} < 500 mA, T_J = −40°C to +125°C	−3		+3	%
ADJUSTABLE OUTPUT VOLTAGE ACCURACY (ADP1715 ADJUSTABLE)[1]	V_{OUT}	I_{OUT} = 10 mA	0.792	0.8	0.808	V
		I_{OUT} = 10 mA to 500 mA	0.784		0.816	V
		100 µA < I_{OUT} < 500 mA, T_J = −40°C to +125°C	0.776		0.824	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.15		+0.15	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 500 mA		0.002		%/mA
		I_{OUT} = 10 mA to 500 mA, T_J = −40°C to +125°C			0.004	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 3.3 V		50		mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 3.3 V, T_J = −40°C to +125°C			100	mV
		I_{OUT} = 500 mA, V_{OUT} ≥ 3.3 V		250	300	mV
		I_{OUT} = 500 mA, V_{OUT} ≥ 3.3 V, T_J = −40°C to +125°C			400	mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.3 V		60		mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.3 V, T_J = −40°C to +125°C			100	mV
		I_{OUT} = 500 mA, 2.5 V ≤ V_{OUT} < 3.3 V		320	400	mV
		I_{OUT} = 500 mA, 2.5 V ≤ V_{OUT} < 3.3 V, T_J = −40°C to +125°C			500	mV
START-UP TIME[4]	$T_{START-UP}$					
ADP1715 Adjustable and ADP1716				100		µs
ADP1715 with External Soft Start		C_{SS} = 10 nF		7.3		ms
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		550	750	1200	mA
THERMAL SHUTDOWN THRESHOLD	TS_{SD}	T_J rising		150		°C
THERMAL SHUTDOWN HYSTERESIS	TS_{SD-HYS}			15		°C
SOFT-START SOURCE CURRENT (ADP1715 WITH EXTERNAL SOFT START)	$SS_{I-SOURCE}$	SS = GND	0.7	1.2	1.7	µA
V_{OUT} to V_{TRK} ACCURACY (ADP1716)	$V_{TRK-ERROR}$	0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT(NOM)}$), $V_{OUT(NOM)}$ ≤ 1.8 V, T_J = −40°C to +125°C	−50		+50	mV
		0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT(NOM)}$), $V_{OUT(NOM)}$ > 1.8 V, T_J = −40°C to +125°C	−100		+100	mV
EN INPUT LOGIC HIGH	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.8			V
EN INPUT LOGIC LOW	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN INPUT LEAKAGE CURRENT	$V_{I-LEAKAGE}$	EN = IN or GND		0.1	1	µA
ADJ INPUT BIAS CURRENT (ADP1715 ADJUSTABLE)	ADJ_{I-BIAS}			30	100	nA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 0.75 V		125		µVrms
		10 Hz to 100 kHz, V_{OUT} = 3.3 V		450		µVrms
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{OUT} = 0.75 V		67		dB
		1 kHz, V_{OUT} = 3.3 V		53		dB

[1] Accuracy when OUT is connected directly to ADJ. When OUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.

[2] Based on an end-point calculation using 10 mA and 500 mA loads. See Figure 8 for typical load regulation performance for loads less than 10 mA.

[3] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.

[4] Start-up time is defined as the time between the rising edge of EN to OUT being at 95% of its nominal value.

[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	–0.3 V to +6 V
OUT to GND	–0.3 V to IN
EN to GND	–0.3 V to +6 V
SS/ADJ/TRK to GND	–0.3 V to +6 V
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead MSOP	118	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

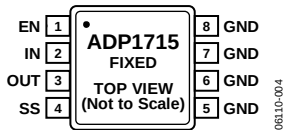


Figure 4. 8-Lead MSOP (RM-Suffix)

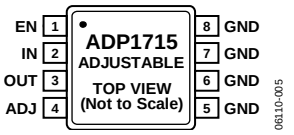


Figure 5. 8-Lead MSOP (RM-Suffix)

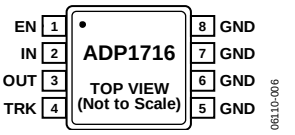


Figure 6. 8-Lead MSOP (RM-Suffix)

Table 4. Pin Function Descriptions

ADP1715 Fixed Pin No.	ADP1715 Adjustable Pin No.	ADP1716 Pin No.	Mnemonic	Description
1	1	1	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
2	2	2	IN	Regulator Input Supply. Bypass IN to GND with a 2.2 µF or greater capacitor.
3	3	3	OUT	Regulated Output Voltage. Bypass OUT to GND with a 2.2 µF or greater capacitor.
4			SS	Soft Start. A capacitor connected to this pin determines the soft-start time.
	4		ADJ	Adjust. A resistor divider from OUT to ADJ sets the output voltage.
		4	TRK	Track. The output will follow the voltage placed on the TRK pin. (See the Theory of Operation section for a more detailed description.)
5, 6, 7, 8	5, 6, 7, 8	5, 6, 7, 8	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, I_{OUT} = 10 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

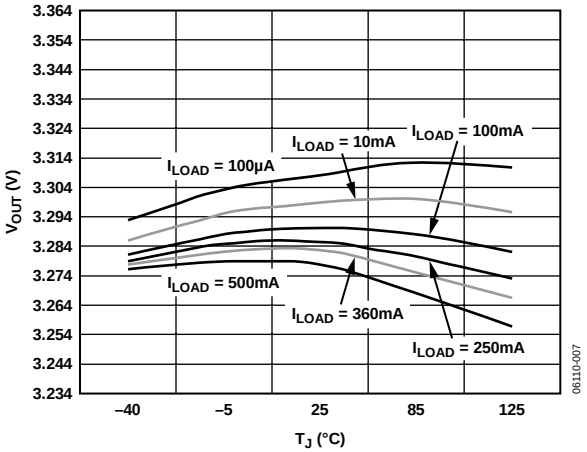


Figure 7. Output Voltage vs. Junction Temperature

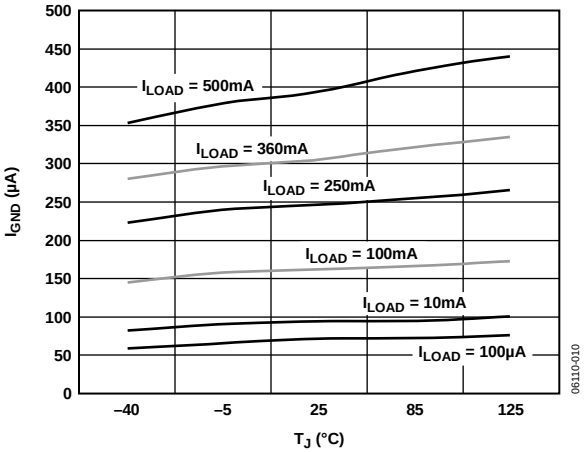


Figure 10. Ground Current vs. Junction Temperature

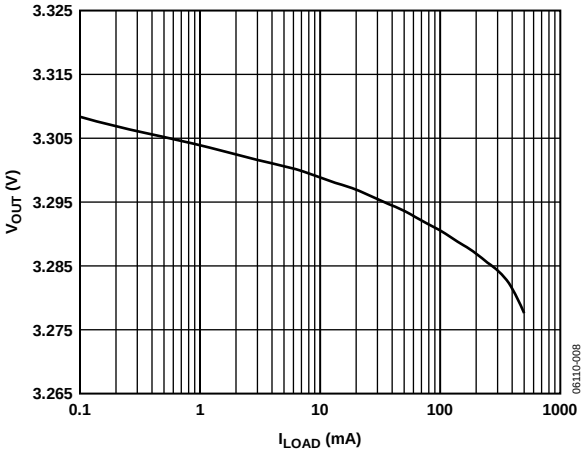


Figure 8. Output Voltage vs. Load Current

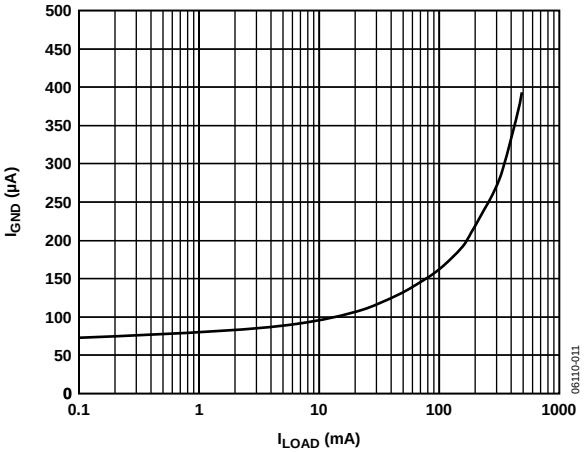


Figure 11. Ground Current vs. Load Current

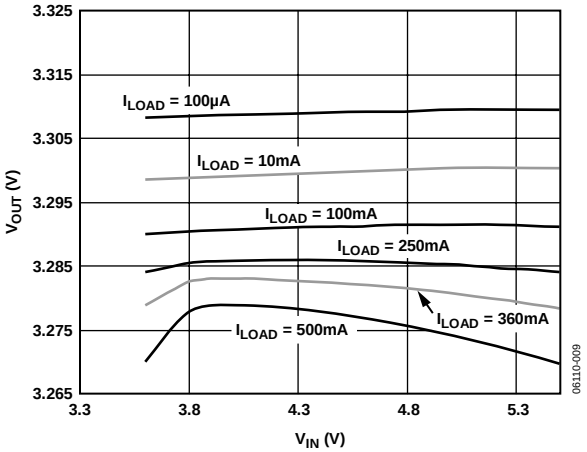


Figure 9. Output Voltage vs. Input Voltage

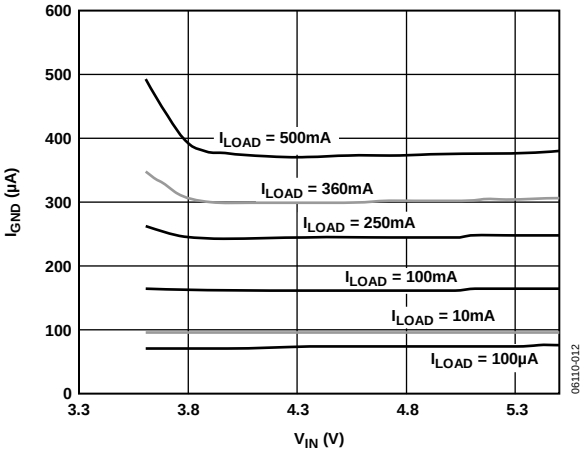


Figure 12. Ground Current vs. Input Voltage

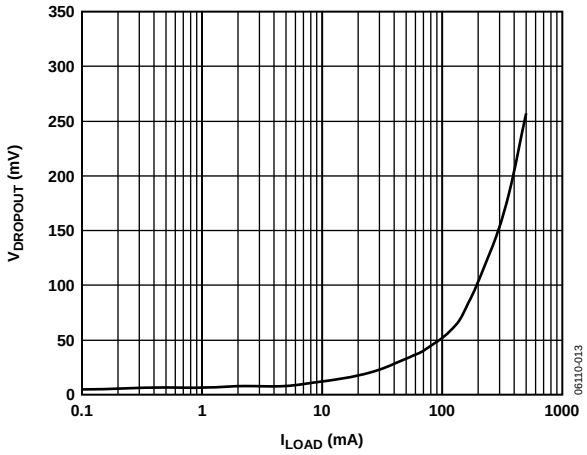


Figure 13. Dropout Voltage vs. Load Current

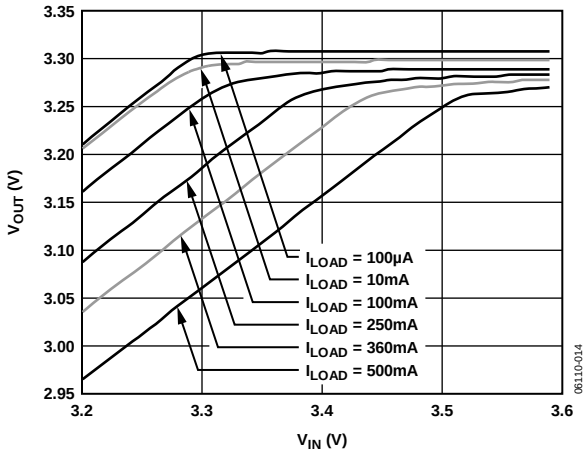


Figure 14. Output Voltage vs. Input Voltage (in Dropout)

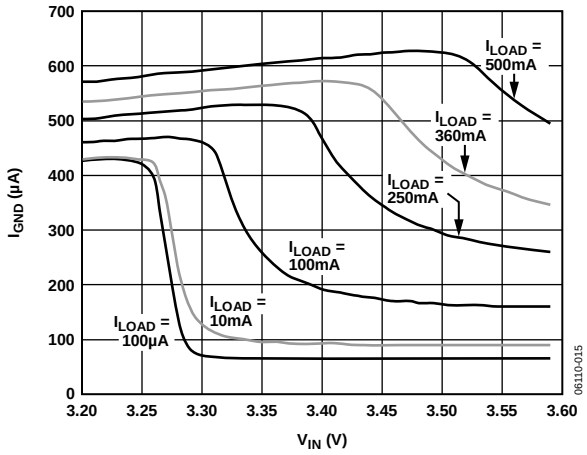


Figure 15. Ground Current vs. Input Voltage (in Dropout)

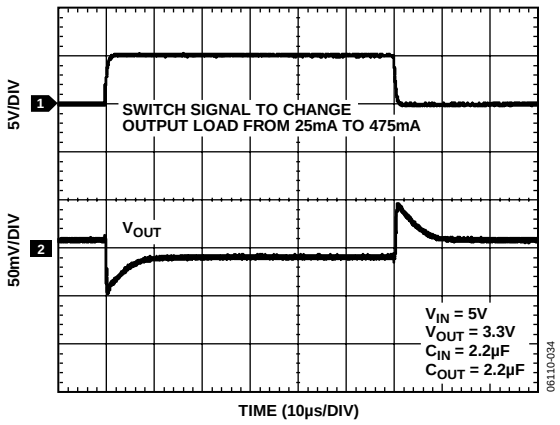


Figure 16. Load Transient Response

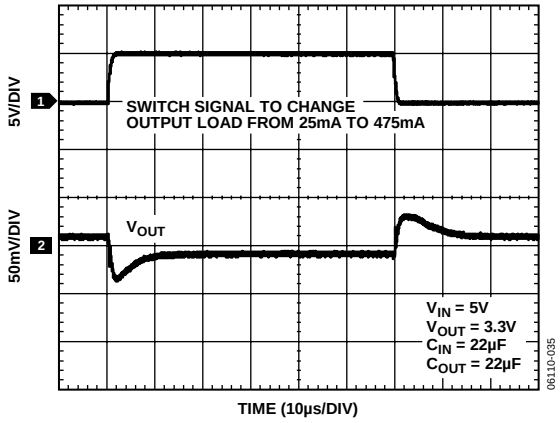


Figure 17. Load Transient Response

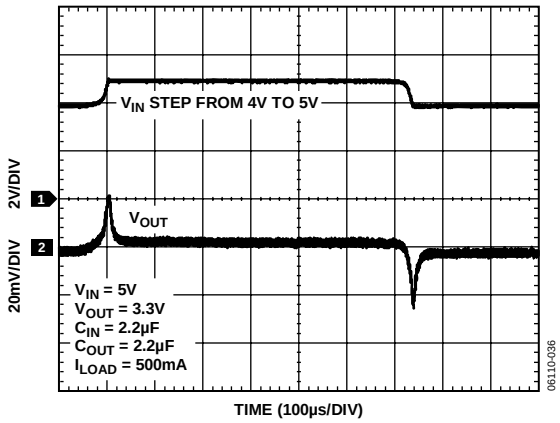


Figure 18. Line Transient Response

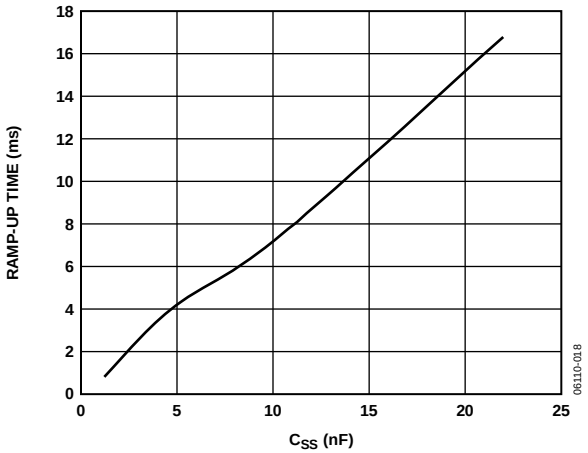


Figure 19. Output Voltage Ramp-Up Time vs. Soft-Start Capacitor Value

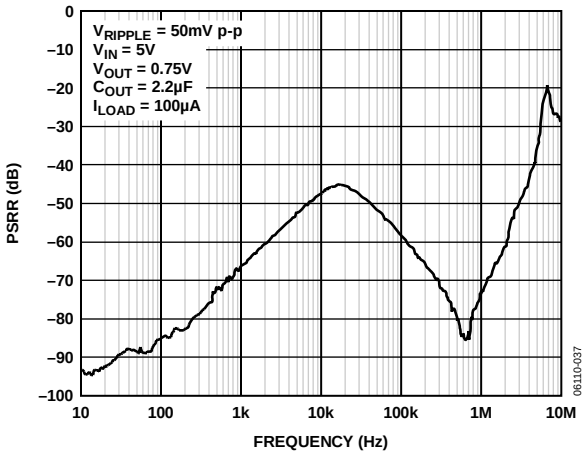


Figure 20. Power Supply Rejection Ratio vs. Frequency

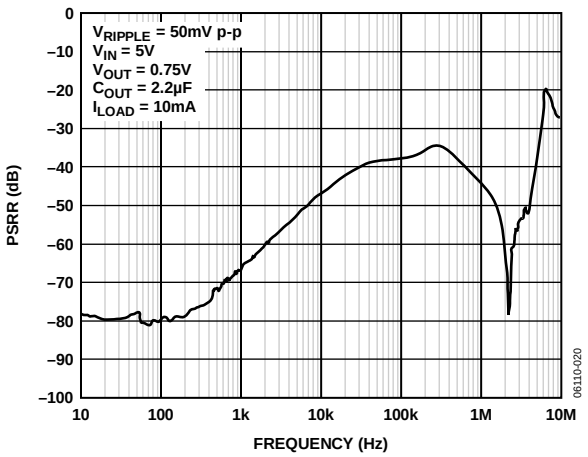


Figure 21. Power Supply Rejection Ratio vs. Frequency

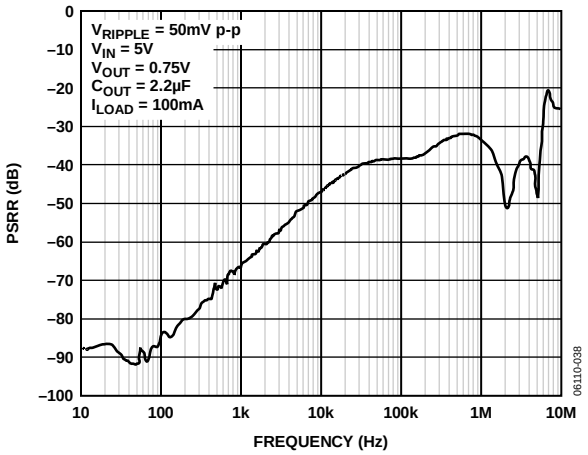


Figure 22. Power Supply Rejection Ratio vs. Frequency

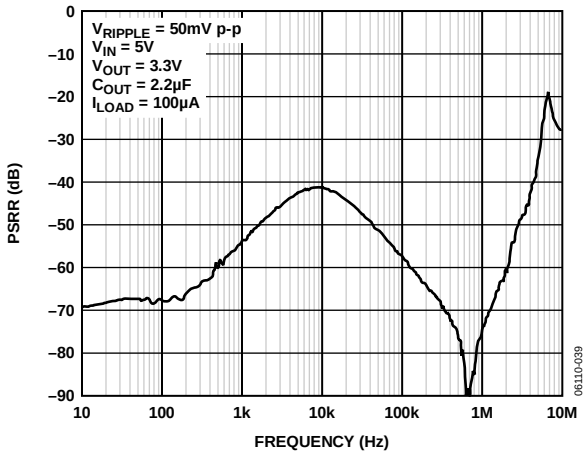


Figure 23. Power Supply Rejection Ratio vs. Frequency

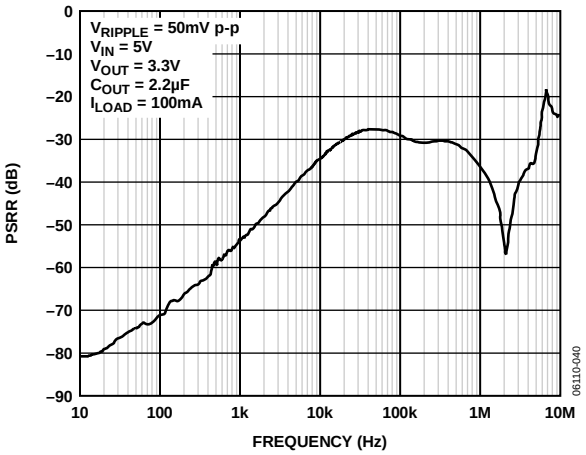


Figure 25. Power Supply Rejection Ratio vs. Frequency

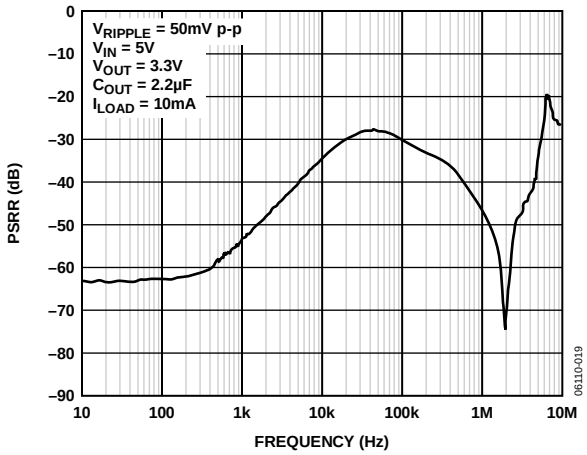


Figure 24. Power Supply Rejection Ratio vs. Frequency

THEORY OF OPERATION

The ADP1715/ADP1716 are low dropout, CMOS linear regulators that use an advanced, proprietary architecture to provide high power supply rejection ratio (PSRR) and excellent line and load transient response with just a small 2.2 µF ceramic output capacitor. Both devices operate from a 2.5 V to 5.5 V input rail and provide up to 500 mA of output current. Supply current in shutdown mode is typically 100 nA.

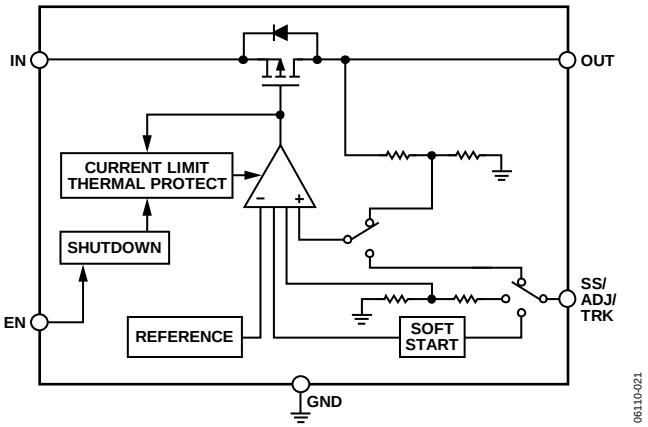


Figure 26. Internal Block Diagram

Internally, the ADP1715/ADP1716 consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP1715 is available in two versions, one with fixed output voltage options and one with an adjustable output voltage. The fixed output voltage options are set internally to one of sixteen values between 0.75 V and 3.3 V, using an internal feedback network. The adjustable output voltage can be set to between 0.8 V and 5.0 V by an external voltage divider connected from OUT to ADJ. The fixed output version of ADP1715 allows for connection of an external soft-start capacitor, which controls the output voltage ramp during startup. The ADP1716 features a track pin and is available with fixed output voltage options. All devices are controlled by an enable pin (EN).

SOFT-START FUNCTION (ADP1715)

For applications that require a controlled startup, the ADP1715 provides a programmable soft-start function. Programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement soft start, connect a small ceramic capacitor from SS to GND. Upon startup, a 1.2 µA current source charges this capacitor. The ADP1715 start-up output voltage is limited by the voltage at SS, providing a smooth ramp up to the nominal output voltage. The soft-start time is calculated by

$$T_{SS} = V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

where:

T_{SS} is the soft-start period.
V_{REF} is the 0.8 V reference voltage.
C_{SS} is the soft-start capacitance from SS to GND.
I_{SS} is the current sourced from SS (1.2 µA).

When the ADP1715 is disabled (using EN), the soft-start capacitor is discharged to GND through an internal 100 Ω resistor.

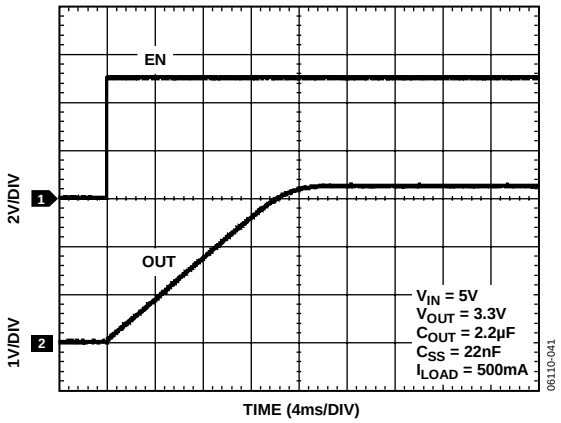


Figure 27. OUT Ramp-Up with External Soft-Start Capacitor

The ADP1715 adjustable version and the ADP1716 have no pins for soft start, so the function is switched to an internal soft-start capacitor. This sets the soft-start ramp-up period to approximately 24 µs. For the worst-case output voltage of 5 V, using the suggested 2.2 µF output capacitor, the resulting input inrush current is approximately 460 mA, which is less than the maximum 500 mA load current.

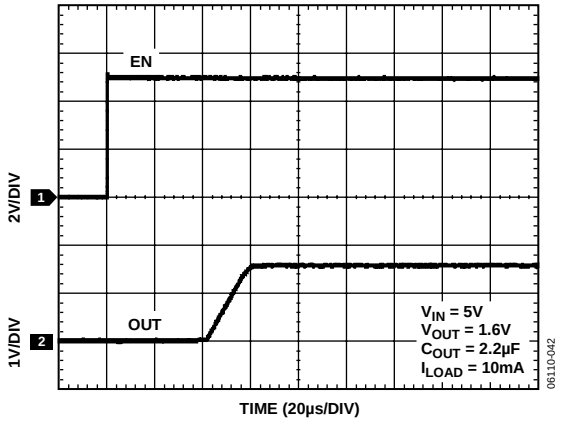


Figure 28. OUT Ramp-Up with Internal Soft-Start

ADJUSTABLE OUTPUT VOLTAGE (ADP1715 ADJUSTABLE)

The ADP1715 adjustable version can have its output voltage set over a 0.8 V to 5.0 V range. The output voltage is set by connecting a resistive voltage divider from OUT to ADJ. The output voltage is calculated using the equation

$$V_{OUT} = 0.8\ V\ (1 + R1/R2) \quad (2)$$

where:

R1 is the resistor from OUT to ADJ.
R2 is the resistor from ADJ to GND.

The maximum bias current into ADJ is 100 nA, so for less than 0.5% error due to the bias current, use values less than 60 kΩ for R2.

TRACK MODE (ADP1716)

The ADP1716 includes a tracking mode feature. As shown in Figure 29, if the voltage applied at the TRK pin is less than the nominal output voltage, OUT is equal to the voltage at TRK. Otherwise, OUT regulates to its nominal output value.

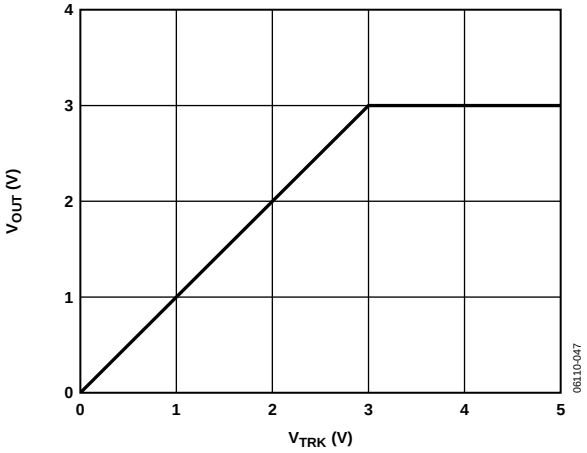


Figure 29. ADP1716 Output Voltage vs. Tracking Voltage with Nominal Output Voltage Set to 3 V

For example, consider an ADP1716 with a nominal output voltage of 3 V. If the voltage applied to its TRK pin is greater than 3 V, OUT maintains a nominal output voltage of 3 V. If the voltage applied to TRK is reduced below 3 V, OUT tracks this voltage. OUT can track the TRK pin voltage from the nominal value all the way down to 0 V. A voltage divider is present from TRK to the error amplifier input with a divider ratio equal to the divider from OUT to the error amplifier. This sets the output voltage equal to the tracking voltage. Both divider ratios are set by post-package trim, depending on the desired output voltage.

ENABLE FEATURE

The ADP1715/ADP1716 use the EN pin to enable and disable the OUT pin under normal operating conditions. As shown in Figure 30, when a rising voltage on EN crosses the active threshold, OUT turns on. When a falling voltage on EN crosses the inactive threshold, OUT turns off.

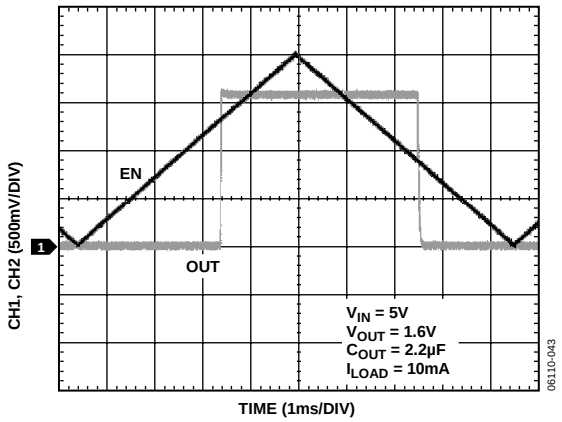


Figure 30. ADP1715 Adjustable Typical EN Pin Operation

As can be seen, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the IN voltage. Therefore, these thresholds vary with changing input voltage. Figure 31 shows typical EN active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

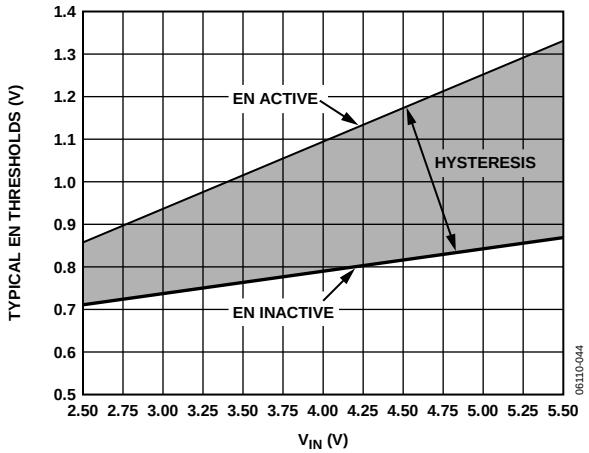


Figure 31. Typical EN Pin Thresholds vs. Input Voltage

APPLICATION INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1715/ADP1716 are designed for operation with small, space-saving ceramic capacitors, but they will function with most commonly used capacitors as long as care is taken about the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure stability of the ADP1715/ADP1716. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1715/ADP1716 to large changes in load current. Figure 32 and Figure 33 show the transient responses for output capacitance values of 2.2 µF and 22 µF.

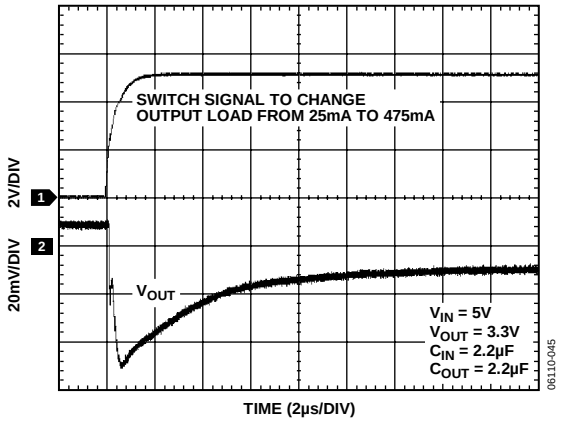


Figure 32. Output Transient Response

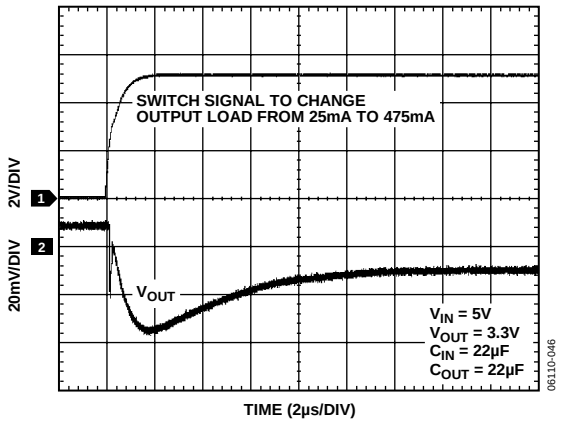


Figure 33. Output Transient Response

Input Bypass Capacitor

Connecting a 2.2 µF capacitor from the IN pin to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces, or high source impedance, is encountered. If greater than 2.2 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1715/ADP1716, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1715/ADP1716 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP1715/ADP1716 are designed to current limit when the output load reaches 750 mA (typical). When the output load exceeds 750 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first the ADP1715/ADP1716 will current limit, so that only 750 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown will activate, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 750 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 750 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation should be externally limited so junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1715/ADP1716 should not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user

should be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered to on the PCB. Table 5 shows typical θ_{JA} values of the 8-lead thermally enhanced MSOP package for various PCB copper sizes.

Table 5.

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	118
100	99
300	77
500	75
700	74

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP1715/ADP1716 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

where:

T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (4)$$

where:

I_{LOAD} is the load current.
I_{GND} is ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (5)$$

As shown in Equation 5, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. The following figures show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

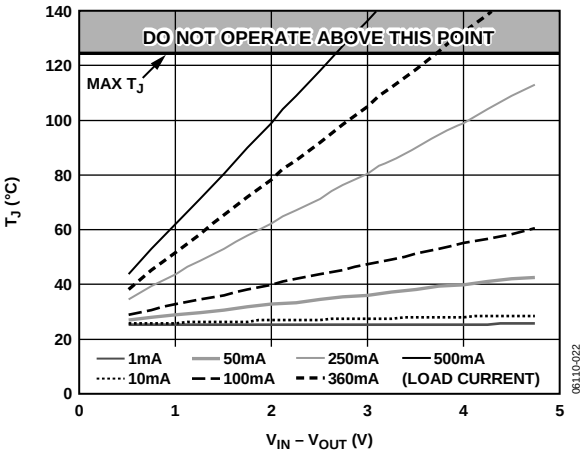


Figure 34. 700 mm² of PCB Copper, T_A = 25°C

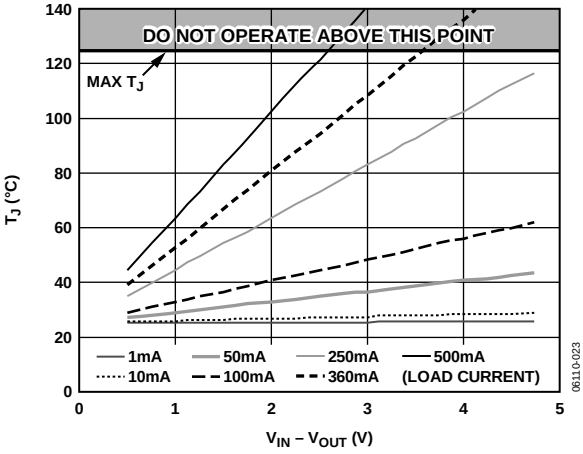


Figure 35. 300 mm² of PCB Copper, T_A = 25°C

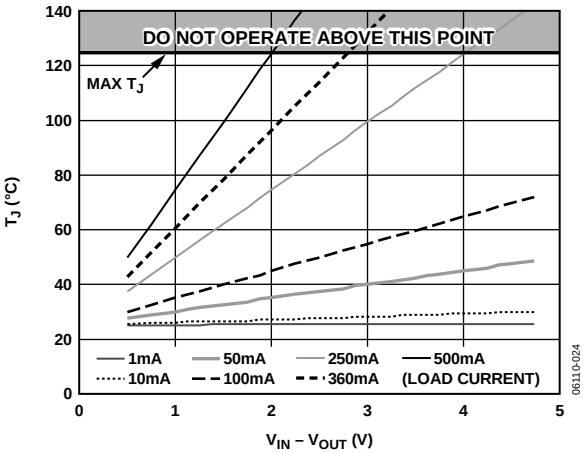


Figure 36. 100 mm² of PCB Copper, T_A = 25°C

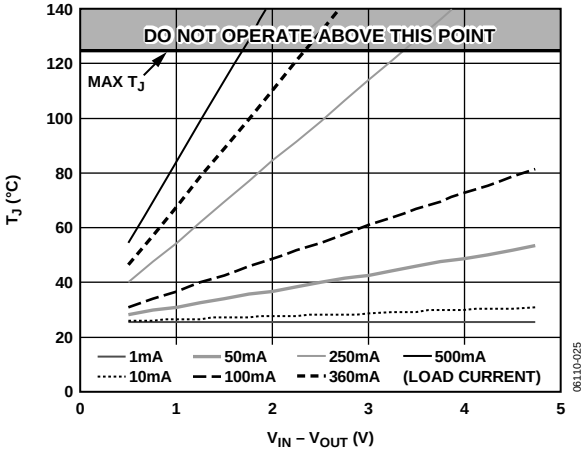


Figure 37. 0 mm² of PCB Copper, T_A = 25°C

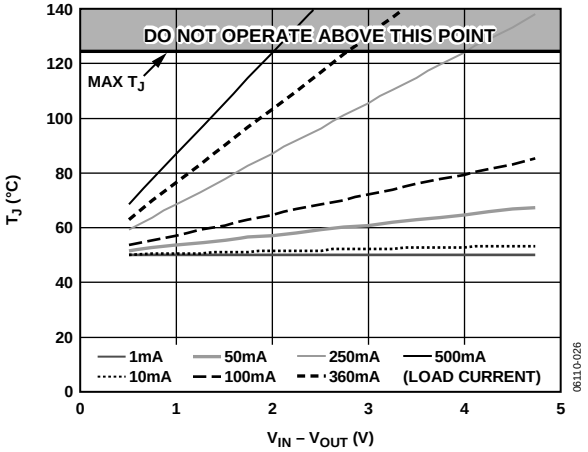


Figure 38. 700 mm² of PCB Copper, T_A = 50°C

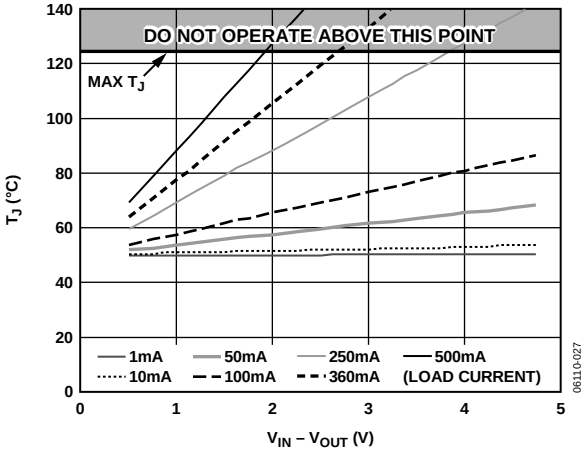


Figure 39. 300 mm² of PCB Copper, T_A = 50°C

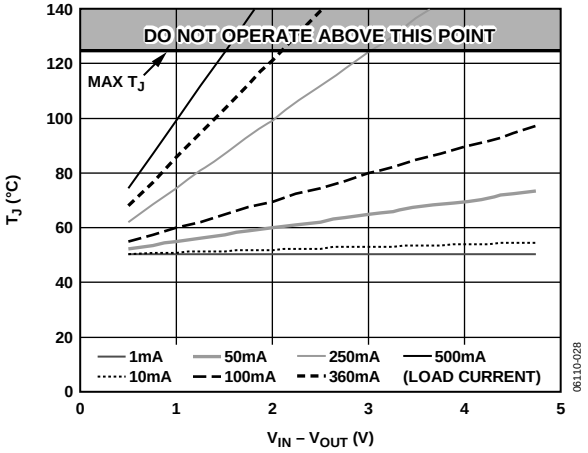


Figure 40. 100 mm² of PCB Copper, T_A = 50°C

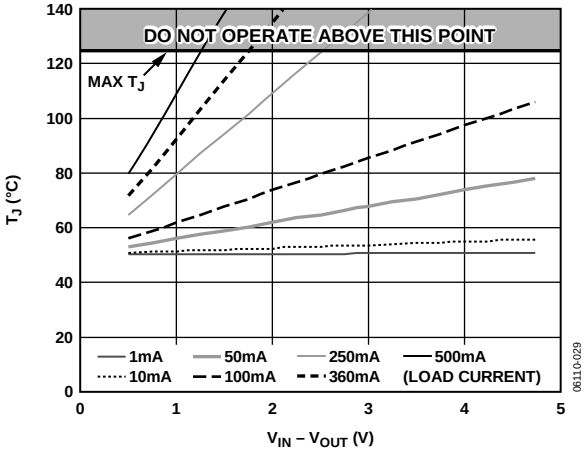


Figure 41. 0 mm² of PCB Copper, T_A = 50°C

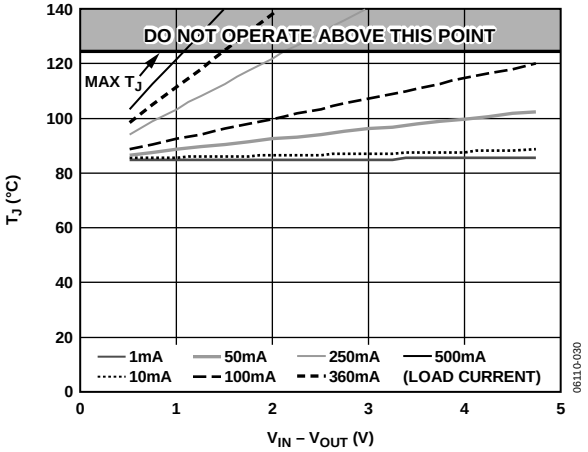


Figure 42. 700 mm² of PCB Copper, T_A = 85°C

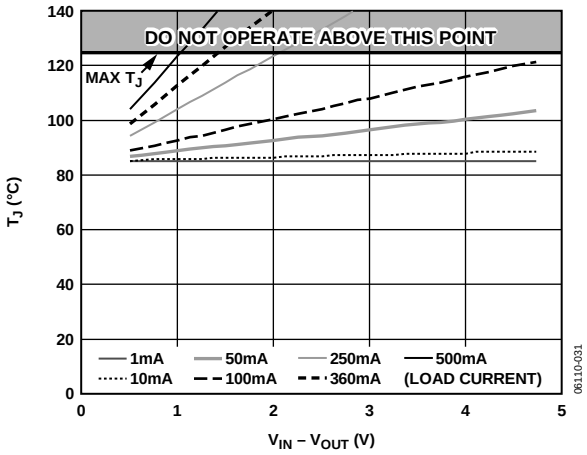


Figure 43. 300 mm² of PCB Copper, T_A = 85°C

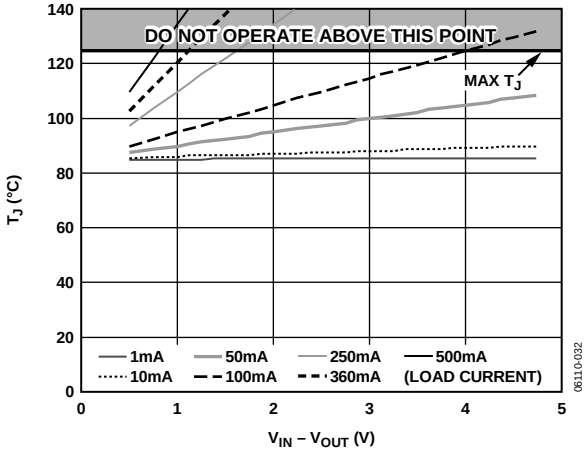


Figure 44. 100 mm² of PCB Copper, T_A = 85°C

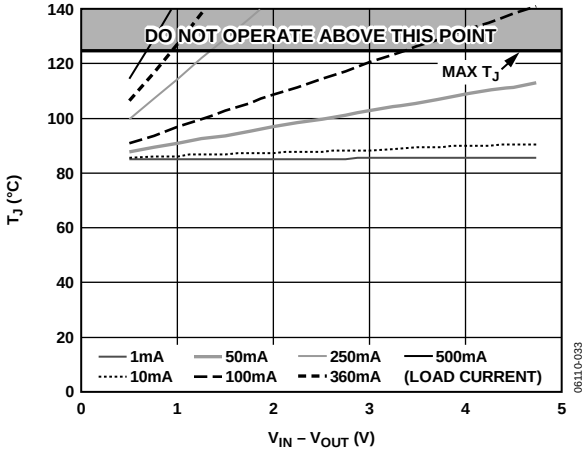


Figure 45. 0 mm² of PCB Copper, T_A = 85°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The 8-lead MSOP package has the four GND pins fused together internally, which enhances its thermal characteristics. Heat dissipation from the package is increased by connecting as much copper as possible to the four GND pins of the ADP1715/ADP1716. From Table 5 it can be seen that a point of diminishing returns eventually is reached, beyond which an increase in the copper size does not yield additional heat dissipation benefits.

Figure 46 shows a typical layout for the ADP1715/ADP1716. The four GND pins are connected to a large copper pad. If a second layer is available, multiple vias can be used to connect them, increasing the overall copper area. The input capacitor should be placed as close as possible to the IN and GND pins. The output capacitor should be placed as close as possible to the OUT and GND pins. 0603 or 0402 size capacitors and resistors should be used to achieve the smallest possible footprint solution on boards where area is limited.

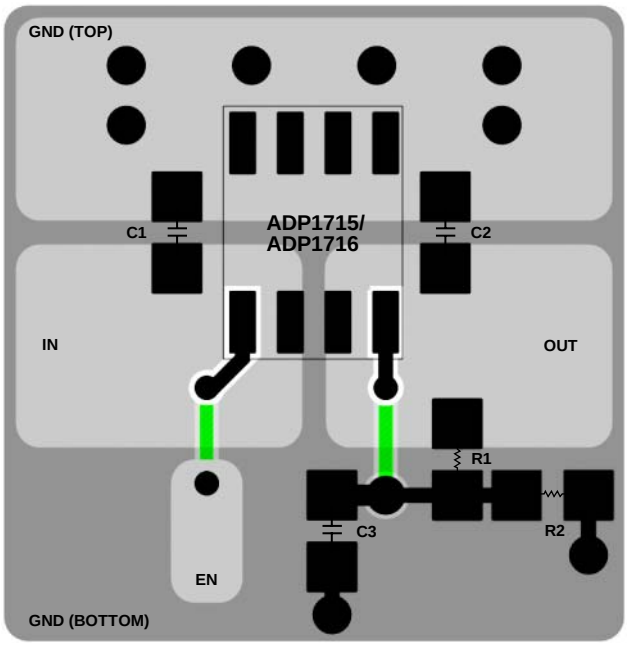
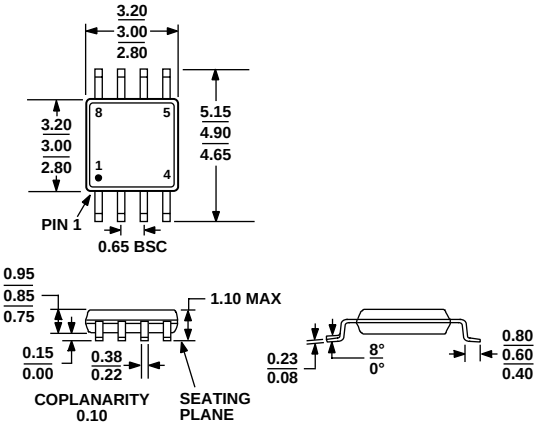


Figure 46. Example PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 47. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions show in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1715ARMZ-0.75R7[1]	–40°C to +125°C	0.75	8-Lead MSOP	RM-8	L29
ADP1715ARMZ-0.8-R7[1]	–40°C to +125°C	0.80	8-Lead MSOP	RM-8	L2A
ADP1715ARMZ-0.85R7[1]	–40°C to +125°C	0.85	8-Lead MSOP	RM-8	L2C
ADP1715ARMZ-0.9-R7[1]	–40°C to +125°C	0.90	8-Lead MSOP	RM-8	L2D
ADP1715ARMZ-0.95R7[1]	–40°C to +125°C	0.95	8-Lead MSOP	RM-8	L2E
ADP1715ARMZ-1.0-R7[1]	–40°C to +125°C	1.00	8-Lead MSOP	RM-8	L2F
ADP1715ARMZ-1.05R7[1]	–40°C to +125°C	1.05	8-Lead MSOP	RM-8	L2G
ADP1715ARMZ-1.1-R7[1]	–40°C to +125°C	1.10	8-Lead MSOP	RM-8	L2H
ADP1715ARMZ-1.15R7[1]	–40°C to +125°C	1.15	8-Lead MSOP	RM-8	L2J
ADP1715ARMZ-1.2-R7[1]	–40°C to +125°C	1.20	8-Lead MSOP	RM-8	L2K
ADP1715ARMZ-1.3-R7[1]	–40°C to +125°C	1.30	8-Lead MSOP	RM-8	L32
ADP1715ARMZ-1.5-R7[1]	–40°C to +125°C	1.50	8-Lead MSOP	RM-8	L2L
ADP1715ARMZ-1.8-R7[1]	–40°C to +125°C	1.80	8-Lead MSOP	RM-8	L3R
ADP1715ARMZ-2.5-R7[1]	–40°C to +125°C	2.50	8-Lead MSOP	RM-8	L33
ADP1715ARMZ-3.0-R7[1]	–40°C to +125°C	3.00	8-Lead MSOP	RM-8	L34
ADP1715ARMZ-3.3-R7[1]	–40°C to +125°C	3.30	8-Lead MSOP	RM-8	L35
ADP1715ARMZ-R7[1]	–40°C to +125°C	0.8 to 5.0	8-Lead MSOP	RM-8	L3K
ADP1716ARMZ-0.75R7[1]	–40°C to +125°C	0.75	8-Lead MSOP	RM-8	L2N
ADP1716ARMZ-0.8-R7[1]	–40°C to +125°C	0.80	8-Lead MSOP	RM-8	L2P
ADP1716ARMZ-0.85R7[1]	–40°C to +125°C	0.85	8-Lead MSOP	RM-8	L2Q
ADP1716ARMZ-0.9-R7[1]	–40°C to +125°C	0.90	8-Lead MSOP	RM-8	L2R
ADP1716ARMZ-0.95R7[1]	–40°C to +125°C	0.95	8-Lead MSOP	RM-8	L2S
ADP1716ARMZ-1.0-R7[1]	–40°C to +125°C	1.00	8-Lead MSOP	RM-8	L2T
ADP1716ARMZ-1.05R7[1]	–40°C to +125°C	1.05	8-Lead MSOP	RM-8	L3D
ADP1716ARMZ-1.1-R7[1]	–40°C to +125°C	1.10	8-Lead MSOP	RM-8	L2U
ADP1716ARMZ-1.15R7[1]	–40°C to +125°C	1.15	8-Lead MSOP	RM-8	L2 V
ADP1716ARMZ-1.2-R7[1]	–40°C to +125°C	1.20	8-Lead MSOP	RM-8	L2W
ADP1716ARMZ-1.3-R7[1]	–40°C to +125°C	1.30	8-Lead MSOP	RM-8	L2X
ADP1716ARMZ-1.5-R7[1]	–40°C to +125°C	1.50	8-Lead MSOP	RM-8	L2Y
ADP1716ARMZ-1.8-R7[1]	–40°C to +125°C	1.80	8-Lead MSOP	RM-8	L31
ADP1716ARMZ-2.5-R7[1]	–40°C to +125°C	2.50	8-Lead MSOP	RM-8	L37
ADP1716ARMZ-3.0-R7[1]	–40°C to +125°C	3.00	8-Lead MSOP	RM-8	L38
ADP1716ARMZ-3.3-R7[1]	–40°C to +125°C	3.30	8-Lead MSOP	RM-8	L39

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

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