# 1.2 MHz DC-to-DC Step-Up Switching Converter

# ADP1610

## FEATURES

**Fully integrated 1.2 A, 0.2 Ω, power switch**
**Pin-selectable 700 kHz or 1.2 MHz PWM frequency**
**92% efficiency**
**Adjustable output voltage up to 12 V**
**3% output regulation accuracy**
**Adjustable soft start**
**Input undervoltage lockout**
**MSOP 8-lead package**

## APPLICATIONS

**TFT LC bias supplies**
**Portable applications**
**Industrial/instrumentation equipment**

## GENERAL DESCRIPTION

The ADP1610 is a dc-to-dc step-up switching converter with an integrated 1.2 A, 0.2 Ω power switch capable of providing an output voltage as high as 12 V. With a package height of less than 1.1 mm, the ADP1610 is optimal for space-constrained applications such as portable devices or thin film transistor (TFT) liquid crystal displays (LCDs).

The ADP1610 operates in pulse-width modulation (PWM) current mode with up to 92% efficiency. Adjustable soft start prevents inrush currents at startup. The pin-selectable switching frequency and PWM current mode architecture allow excellent transient response, easy noise filtering, and the use of small, cost-saving external inductors and capacitors.

The ADP1610 is offered in the RoHS compliant 8-lead MSOP and operates over the temperature range of −40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM

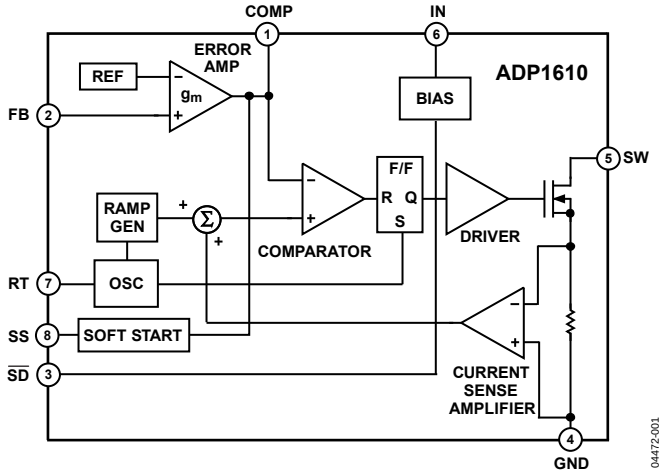



*Figure 1.*

**Rev. A**

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## REVISION HISTORY

**9/08—Rev. 0 to Rev. A**

Changes to Table 4 ... 11
Changes to Table 5 ... 14

**10/04—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{IN}$ = 3.3 V, $T_A$ = −40°C to +85°C, unless otherwise noted. All limits at temperature extremes are guaranteed by correlation and characterization using standard statistical quality control (SQC), unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY | | | | | | |
| Input Voltage | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Quiescent Current | | | | | | |
| Nonswitching State | $I_Q$ | $V_{FB}$ = 1.3 V, RT = $V_{IN}$ | | 390 | 600 | µA |
| Shutdown | $I_{Q\overline{SD}}$ | $V_{\overline{SD}}$ = 0 V | | 0.01 | 10 | µA |
| Switching State[1] | $I_{QSW}$ | $F_{SW}$ = 1.23 MHz, no load | | 1 | 2 | mA |
| OUTPUT | | | | | | |
| Output Voltage | $V_{OUT}$ | | $V_{IN}$ | | 12 | V |
| Load Regulation | | $I_{LOAD}$ = 10 mA to 150 mA, $V_{OUT}$ = 10 V | | 0.05 | | mV/mA |
| Overall Regulation | | Line, load, temperature | | ±3 | | % |
| REFERENCE | | | | | | |
| Feedback Voltage | $V_{FB}$ | | 1.212 | 1.230 | 1.248 | V |
| Line Regulation | | $V_{IN}$ = 2.5 V to 5.5 V | −0.15 | | +0.15 | %/V |
| ERROR AMPLIFIER | | | | | | |
| Transconductance | $g_m$ | ΔI = 1 µA | | 100 | | µA/V |
| Voltage Gain | $A_V$ | | | 60 | | dB |
| FB Input Bias Current | | $V_{FB}$ = 1.23 V | | 10 | | nA |
| SWITCH | | | | | | |
| SW On Resistance | $R_{ON}$ | $I_{SW}$ = 1.0 A | | 200 | 400 | mΩ |
| SW Leakage Current | | $V_{SW}$ = 12 V | | 0.01 | 20 | µA |
| Peak Current Limit[2] | $I_{CLSET}$ | | | 2.0 | | A |
| OSCILLATOR | | | | | | |
| Oscillator Frequency | $f_{OSC}$ | RT = GND | 0.49 | 0.7 | 0.885 | MHz |
| | | RT = IN | 0.89 | 1.23 | 1.6 | MHz |
| Maximum Duty Cycle | $D_{MAX}$ | COMP = open, $V_{FB}$ = 1 V, RT = GND | 78 | 83 | 90 | % |
| SHUTDOWN | | | | | | |
| Shutdown Input Voltage Low | $V_{IL}$ | Nonswitching state | | | 0.6 | V |
| Shutdown Input Voltage High | $V_{IH}$ | Switching state | 2.2 | | | V |
| Shutdown Input Bias Current | $I_{\overline{SD}}$ | $V_{\overline{SD}}$ = 3.3 V | | 0.01 | 1 | µA |
| SOFT START | | | | | | |
| SS Charging Current | | $V_{SS}$ = 0 V | | 3 | | µA |
| UNDERVOLTAGE LOCKOUT[3] | | | | | | |
| UVLO Threshold | | $V_{IN}$ rising | 2.2 | 2.4 | 2.5 | V |
| UVLO Hysteresis | | | | 220 | | mV |

[1] This parameter specifies the average current while switching internally and with SW (Pin 5) floating.
[2] Guaranteed by design and not fully production tested.
[3] Guaranteed by characterization.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| IN, COMP, $\overline{SD}$, SS, RT, FB to GND | −0.3 V to +6 V |
| SW to GND | 14 V |
| RMS SW Pin Current | 1.2 A |
| Operating Ambient Temperature Range | −40°C to +85°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| $\theta_{JA}$, Two Layers | 206°C/W |
| $\theta_{JA}$, Four Layers | 142°C/W |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

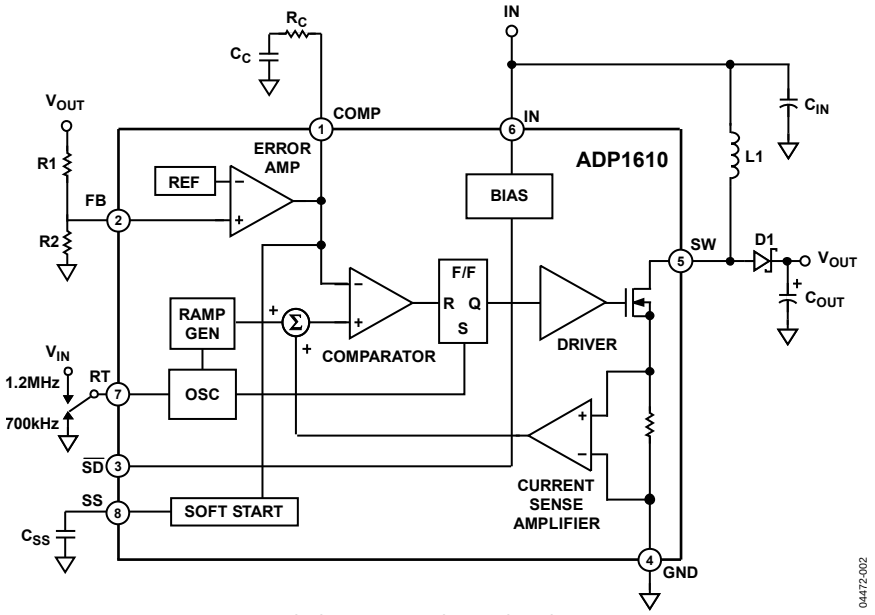



*Figure 2. Block Diagram and Typical Application Circuit*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

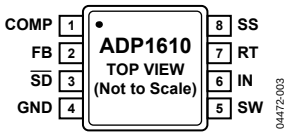



*Figure 3. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | COMP | Compensation Input. Connect a series resistor-capacitor network from COMP to GND to compensate the regulator. |
| 2 | FB | Output Voltage Feedback Input. Connect a resistive voltage divider from the output voltage to FB to set the regulator output voltage. |
| 3 | $\overline{SD}$ | Shutdown Input. Drive $\overline{SD}$ low to shut down the regulator; drive $\overline{SD}$ high to turn it on. |
| 4 | GND | Ground. |
| 5 | SW | Switching Output. Connect the power inductor from the input voltage to SW and connect the external rectifier from SW to the output voltage to complete the step-up converter. |
| 6 | IN | Main Power Supply Input. IN powers the ADP1610 internal circuitry. Connect IN to the input source voltage. Bypass IN to GND with a 10 µF or greater capacitor as close to the ADP1610 as possible. |
| 7 | RT | Frequency Setting Input. RT controls the switching frequency. Connect RT to GND to program the oscillator to 700 kHz, or connect RT to IN to program the oscillator to 1.2 MHz. |
| 8 | SS | Soft Start Timing Capacitor Input. A capacitor from SS to GND brings up the output slowly at power-up. |

# TYPICAL PERFORMANCE CHARACTERISTICS

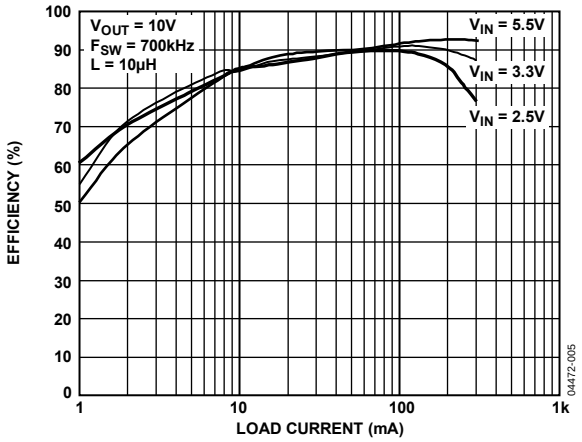



Figure 4. Output Efficiency vs. Load Current

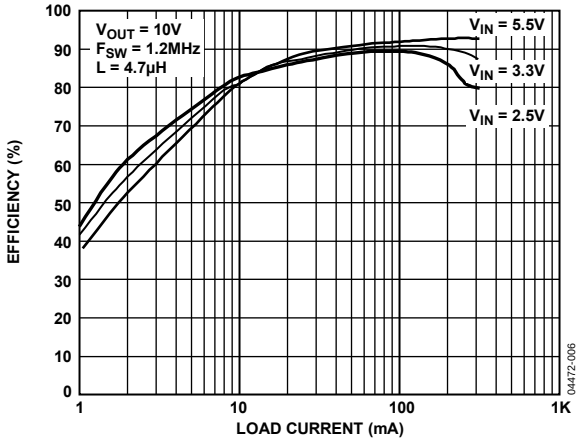



Figure 5. Output Efficiency vs. Load Current

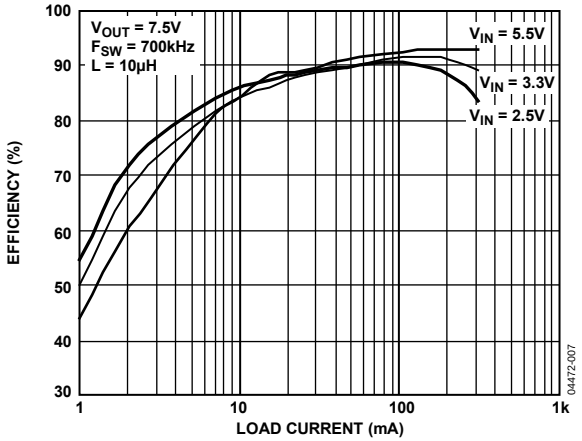



Figure 6. Output Efficiency vs. Load Current

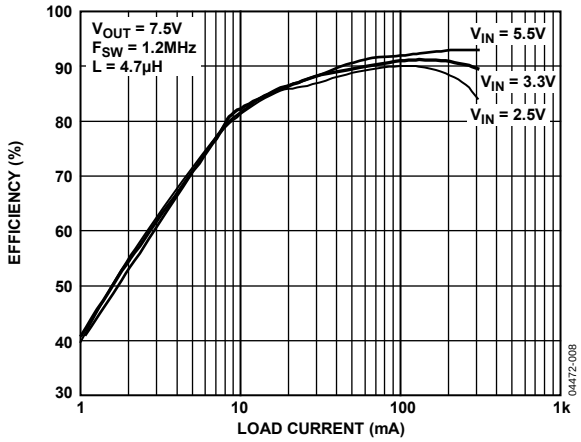



Figure 7. Output Efficiency vs. Load Current

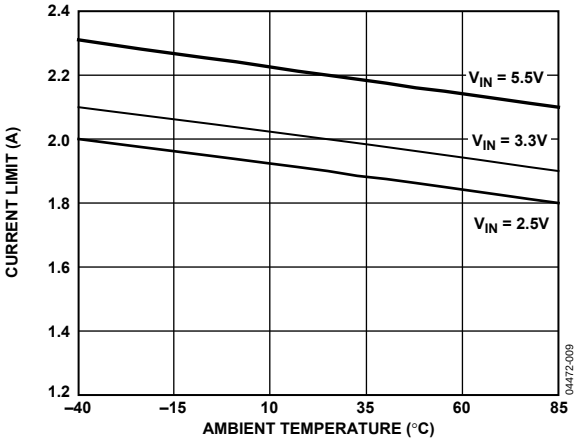



Figure 8. Current Limit vs. Ambient Temperature, $V_{OUT}$ = 10 V

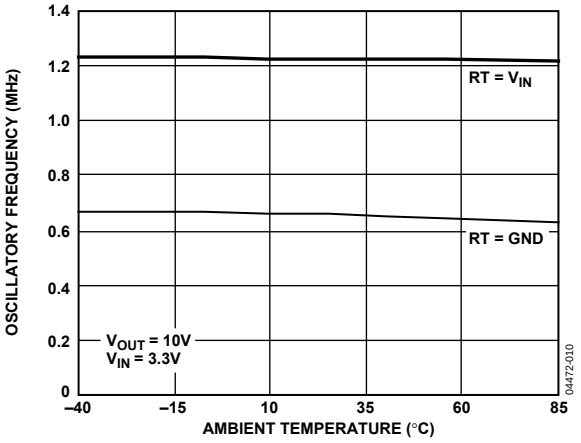



Figure 9. Oscillatory Frequency vs. Ambient Temperature

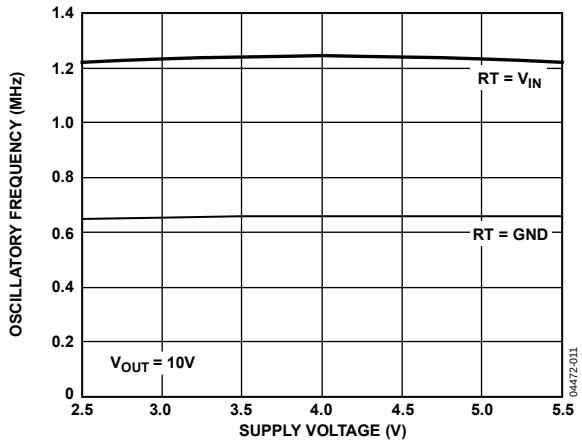



Figure 10. Oscillatory Frequency vs. Supply Voltage

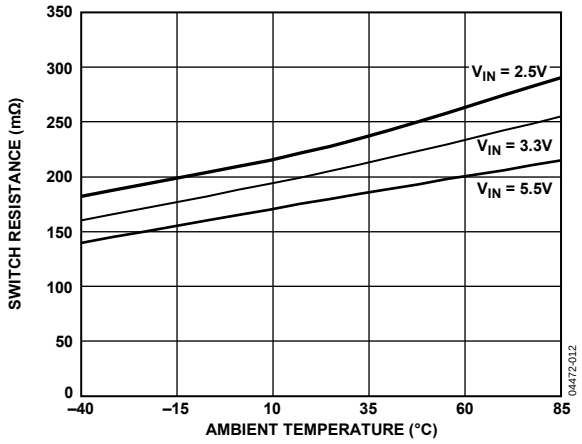



Figure 11. Switch Resistance vs. Ambient Temperature

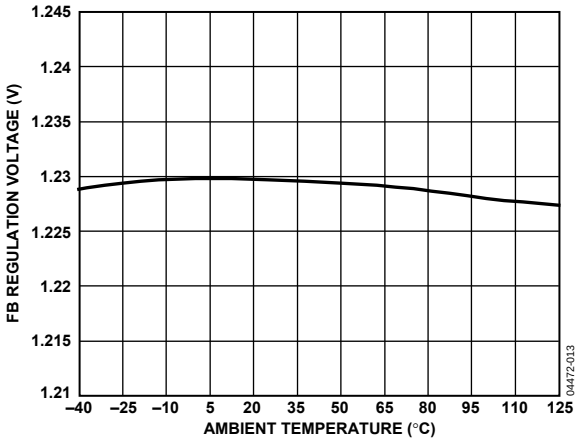



Figure 12. FB Regulation Voltage vs. Ambient Temperature

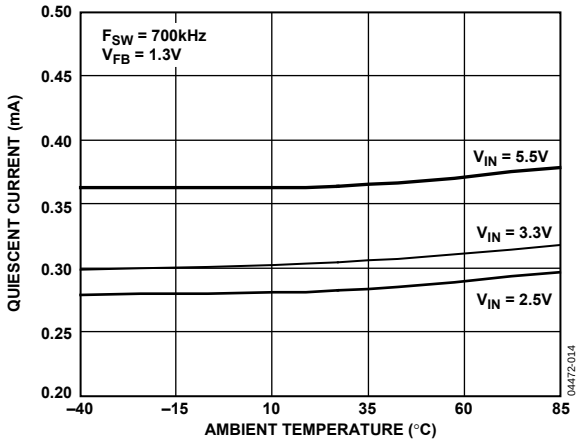



Figure 13. Quiescent Current vs. Ambient Temperature

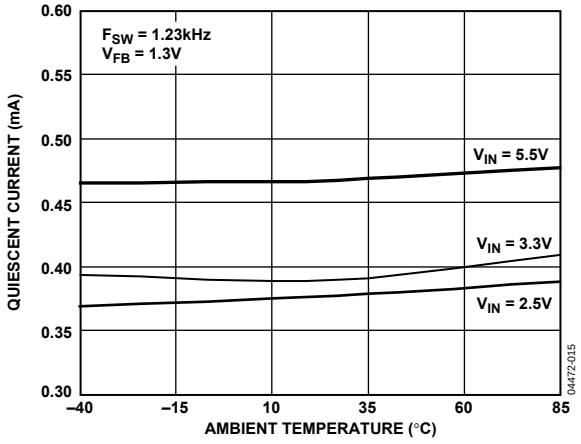



Figure 14. Quiescent Current vs. Ambient Temperature

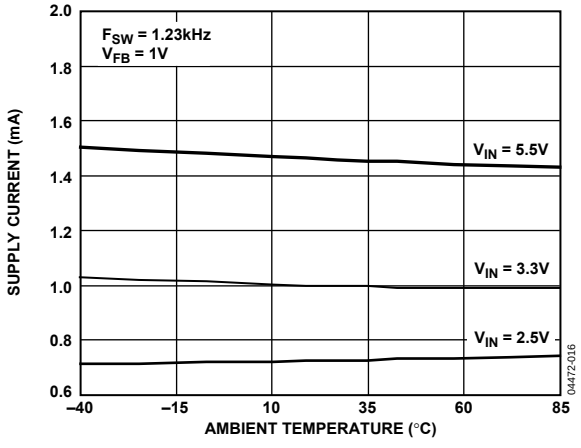



Figure 15. Supply Current vs. Ambient Temperature

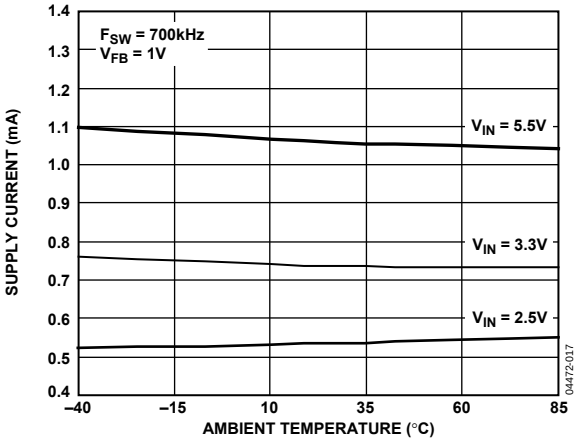



*Figure 16. Supply Current vs. Ambient Temperature*

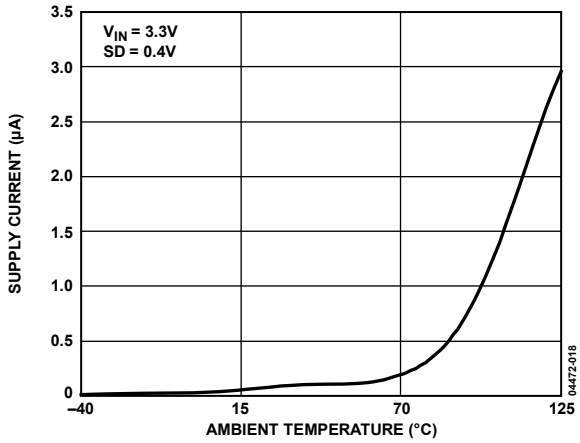



*Figure 17. Supply Current in Shutdown vs. Ambient Temperature*

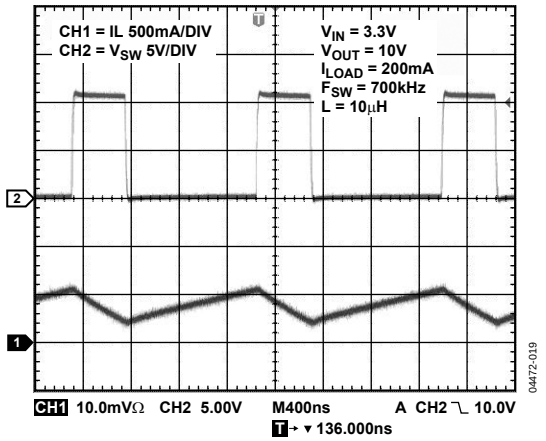



*Figure 18. Switching Waveform in Continuous Conduction*

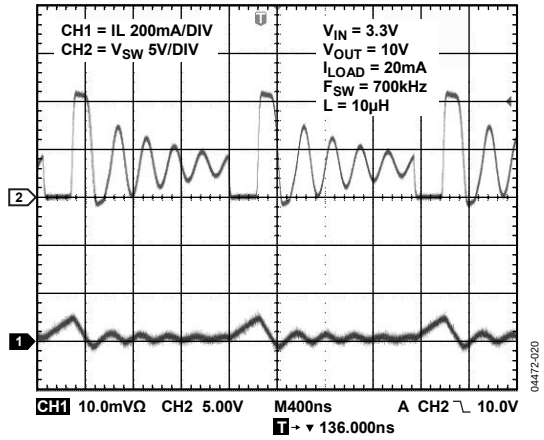



*Figure 19. Switching Waveform in Discontinuous Conduction*

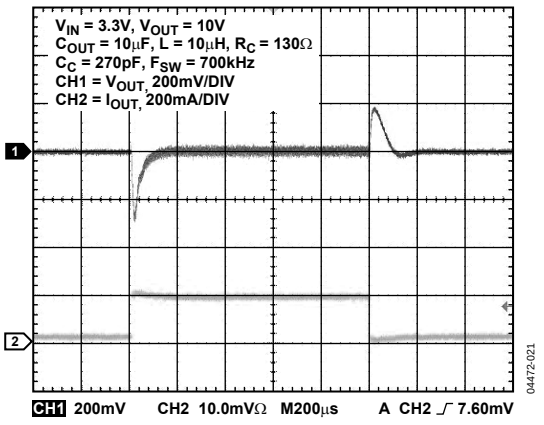



*Figure 20. Load Transient Response, 700 kHz , $V_{OUT}$ = 10 V*

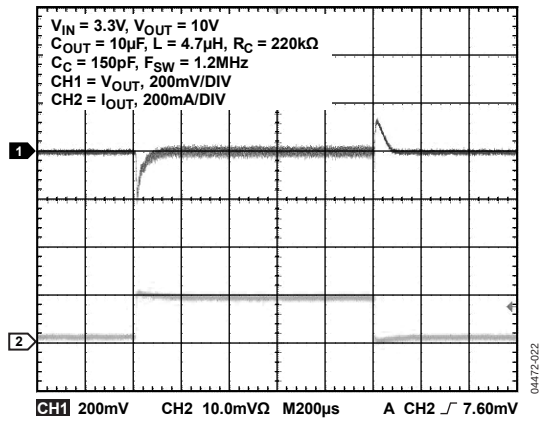



*Figure 21. Load Transient Response, 1.2 MHz, $V_{OUT}$ = 10 V*

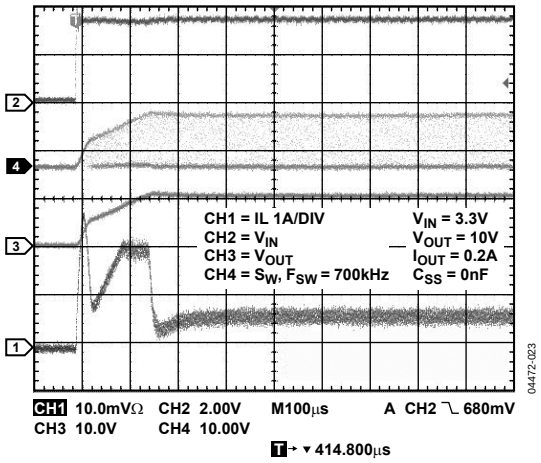



*Figure 22. Start-Up Response from $V_{IN}$, SS = 0 nF*

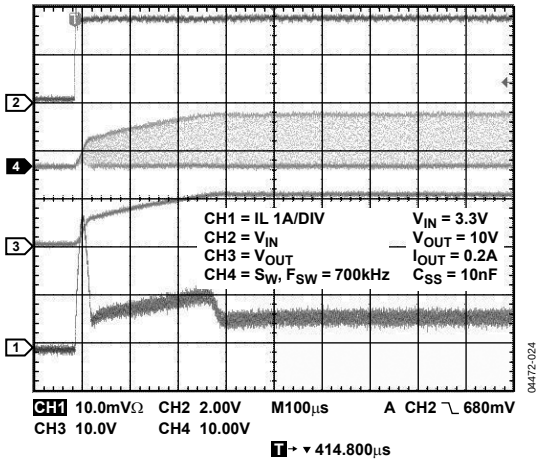



*Figure 23. Start-Up Response from $V_{IN}$, SS = 10 nF*

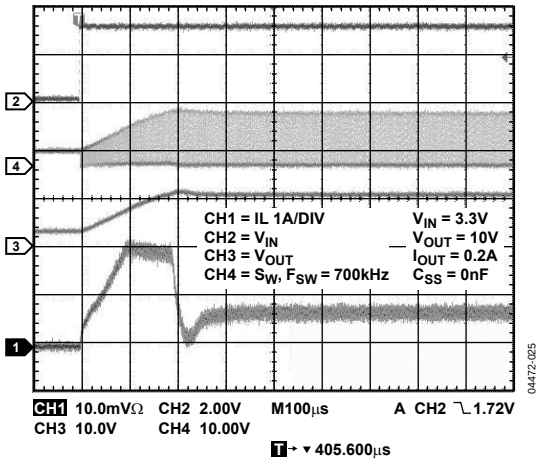



*Figure 24. Start-Up Response from Shutdown, SS = 0 nF*

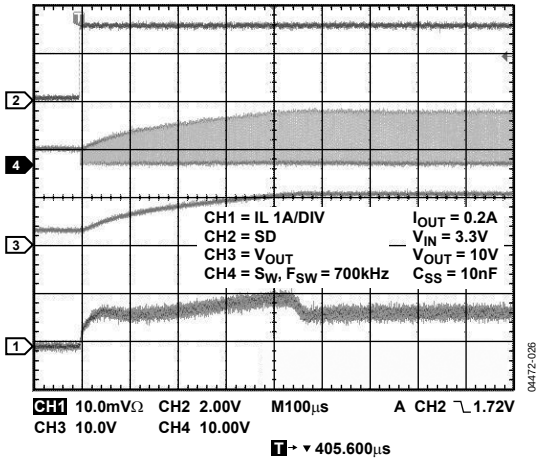



*Figure 25. Start-Up Response from Shutdown, SS = 10 nF*

# THEORY OF OPERATION

The ADP1610 current mode step-up switching converter converts a 2.5 V to 5.5 V input voltage up to an output voltage as high as 12 V. The 1.2 A internal switch allows a high output current, and the high 1.2 MHz switching frequency allows tiny external components. The switch current is monitored on a pulse-by-pulse basis to limit it to 2 A.

## CURRENT MODE PWM OPERATION

The ADP1610 uses current mode architecture to regulate the output voltage. The output voltage is monitored at FB through a resistive voltage divider. The voltage at FB is compared to the internal 1.23 V reference by the internal transconductance error amplifier to create an error current at COMP. A series resistor capacitor at COMP converts the error current to a voltage. The switch current is internally measured and added to the stabilizing ramp. The resulting sum is compared to the error voltage at COMP to control the PWM modulator. This current mode regulation system allows fast transient response, while maintaining a stable output voltage. By selecting the proper resistor capacitor network from COMP to GND, the regulator response is optimized for a wide range of input voltages, output voltages, and load conditions.

## FREQUENCY SELECTION

The frequency of the ADP1610 is selectable to operate at either 700 kHz to optimize the regulator for high efficiency or at 1.2 MHz for small external components. Connect RT to IN for 1.2 MHz operation, or connect RT to GND for 700 kHz operation. To achieve the maximum duty cycle, which may be required for converting a low input voltage to a high output voltage, use the lower 700 kHz switching frequency.

## SOFT START

To prevent input inrush current at startup, connect a capacitor from SS to GND to set the soft start period. When the ADP1610 is in shutdown ($\overline{SD}$ is at GND) or the input voltage is below the 2.4 V undervoltage lockout voltage, SS is internally shorted to GND to discharge the soft start capacitor. When the ADP1610 is turned on, SS sources 3 µA to the soft start capacitor at startup. As the soft start capacitor charges, it limits the voltage at COMP. Because of the current mode regulator, the voltage at COMP is proportional to the switch peak current, and, therefore, the input current. By slowly charging the soft start capacitor, the input current ramps slowly to prevent the current from overshooting excessively at startup.

## ON/OFF CONTROL

The $\overline{SD}$ input turns the ADP1610 regulator on or off. Drive $\overline{SD}$ low to turn off the regulator and reduce the input current to 10 nA. Drive $\overline{SD}$ high to turn on the regulator.

When the dc-to-dc step-up switching converter is turned off, there is a dc path from the input to the output through the inductor and output rectifier. This causes the output voltage to remain slightly below the input voltage by the forward voltage of the rectifier, preventing the output voltage from dropping to zero when the regulator is shut down. Figure 28 shows the application circuit to disconnect the output voltage from the input voltage at shutdown.

## SETTING THE OUTPUT VOLTAGE

The ADP1610 features an adjustable output voltage range of $V_{IN}$ to 12 V. The output voltage is set by the resistive voltage divider (R1 and R2 in Figure 2) from the output voltage ($V_{OUT}$) to the 1.230 V feedback input at FB. To calculate the output voltage use the following equation:

$$V_{OUT} = 1.23 \times (1 + R1/R2) \quad (1)$$

To prevent output voltage errors due to the 10 nA FB input bias current, an R2 resistance of 10 kΩ or less is to be used. Choose R1 based on the following equation:

$$R1 = R2 \times \left( \frac{V_{OUT} - 1.23}{1.23} \right) \quad (2)$$

## INDUCTOR SELECTION

The inductor is an essential part of the step-up switching converter. It stores energy during the on-time, and transfers that energy to the output through the output rectifier during the off-time. Use inductance in the range of 1 µH to 22 µH. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current at approximately 30% of the maximum dc input current typically yields an optimal compromise.

For determining the inductor ripple current, the input ($V_{IN}$) and output ($V_{OUT}$) voltages determine the switch duty cycle (D) by the following equation:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

**Table 4. Recommended Capacitor and Inductor Manufacturers**

| Vendor | Part | L (µH) | C (µF)/Rating (V) | Maximum DC Current | Maximum DCR (mΩ) | Height (mm) | Comments |
|---|---|---|---|---|---|---|---|
| Sumida | CMD4D11-2R2MC | 2.2 | | 0.95 | 116 | 1.2 | |
| | CMD4D11-4R7MC | 4.7 | | 0.75 | 216 | 1.2 | |
| | CDRH4D28-100 | 10 | | 1.00 | 128 | 3.0 | |
| | CDRH5D18-220 | 22 | | 0.80 | 290 | 2.0 | |
| | CR43-4R7 | 4.7 | | 1.15 | 109 | 3.5 | |
| | CR43-100 | 10 | | 1.04 | 182 | 3.5 | |
| Coilcraft | DS1608-472 | 4.7 | | 1.40 | 60 | 2.9 | |
| | DS1608-103 | 10 | | 1.00 | 75 | 2.9 | |
| Toko | D52LC-4R7M | 4.7 | | 1.14 | 87 | 2.0 | |
| | D52LC-100M | 10 | | 0.76 | 150 | 2.0 | |
| Murata | GRM32ER61A226KE20L | | 22/10 | | | | Used only for 3.3 V input and 5 V output |
| | GRM31CR61E106KA12L | | 10/25 | | | | Used for 9 V, 10 V, and 12 V outputs |
| | GRM31CR61A106KA01L | | 10/10 | | | | Used for inputs and outputs of 5 V |
| | GRM31CR71E475KA88L | | 4.7/25 | | | | |

Using the duty cycle and switching frequency ($F_{SW}$), the on-time is calculated using the following equation:

$$t_{ON} = \frac{D}{f_{SW}} \quad (4)$$

The inductor ripple current ($\Delta I_L$) in steady state is calculated using the following equation:

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L} \quad (5)$$

The inductance value (L) is calculated using the following equation:

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L} \quad (6)$$

The peak inductor current (the maximum input current plus half the inductor ripple current) must be less than the rated saturation current of the inductor. Likewise, the maximum rated rms current of the inductor must be greater than the maximum dc input current to the regulator.

For duty cycles greater than 50%, which occur with input voltages greater than one-half the output voltage, slope compensation is required to maintain stability of the current-mode regulator. For stable current-mode operation, ensure that the selected inductance is equal to or greater than $L_{MIN}$ using the following equation:

$$L > L_{MIN} = \frac{V_{OUT} - V_{IN}}{1.8\,\text{A} \times f_{SW}} \quad (7)$$

## CHOOSING THE INPUT AND OUTPUT CAPACITORS

The ADP1610 requires input and output bypass capacitors to supply transient currents while maintaining constant input and output voltage. To prevent noise at the ADP1610 input, a low ESR (equivalent series resistance), 10 µF or greater input capacitor is to be used. Place the capacitor between IN and GND as close to the ADP1610 as possible. Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor as close to the ADP1610 as possible.

The output capacitor maintains the output voltage and supplies current to the load while the ADP1610 switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferred.

The input bypass capacitor limits the high frequency impedance of the input voltage source. The value of this capacitor may need to be increased if the wire length from the input voltage source to the applications board is longer than 18" to optimize the transient performance.

For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated using the following equation. Because the capacitor discharges during the on-time ($t_{ON}$), the charge removed from the capacitor ($Q_C$) is the load current multiplied by the on-time. The output voltage ripple ($\Delta V_{OUT}$) is

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_L \times t_{ON}}{C_{OUT}} \quad (8)$$

where:
$C_{OUT}$ is the output capacitance.
$I_L$ is the average inductor current.

$$t_{ON} = \frac{D}{F_{SW}} \quad (9)$$

and

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (10)$$

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_L \times (V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times \Delta V_{OUT}} \quad (11)$$

The following are recommended capacitor manufacturers:

- AVX
- Kyocera
- Murata
- Sanyo
- Taiyo–Yuden
- TDK

## DIODE SELECTION

The output rectifier conducts the inductor current to the output capacitor and load while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. For this reason, Schottky rectifiers are recommended. The following are recommended Schottky diode manufacturers:

- ON Semiconductor
- Diodes, Inc.

However, for high voltage, high temperature applications, where the Schottky rectifier reverse leakage current becomes significant and can degrade efficiency, use an ultrafast junction diode.

Make sure that the diode is rated to handle the average output load current. Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle. The minimum duty cycle of the ADP1610 is calculated by the following equations:

$$D_{MIN} = \frac{V_{OUT} - V_{IN-MAX}}{V_{OUT}} \quad (12)$$

where $V_{IN-MAX}$ is the maximum input voltage.

## LOOP COMPENSATION

The ADP1610 uses external components to compensate the regulator loop, allowing optimization of the loop dynamics for a given application.

The step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right-half plane zero. The right-half plane zero is determined by the following equation:

$$F_Z(RHP) = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{R_{LOAD}}{2\pi \times L} \quad (13)$$

where:
$F_Z(RHP)$ is the right-half plane zero.
$R_{LOAD}$ is the equivalent load resistance or the output voltage divided by the load current.

To stabilize the regulator, make sure that the regulator crossover frequency is less than or equal to one-fifth of the right-half plane zero and less than or equal to one-fifteenth of the switching frequency.

The regulator loop gain is calculated using the following equation:

$$A_{VL} = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times \left|Z_{COMP}\right| \times G_{CS} \times \left|Z_{OUT}\right| \quad (14)$$

where:
$A_{VL}$ is the loop gain.
$V_{FB}$ is the feedback regulation voltage, 1.230 V.
$V_{OUT}$ is the regulated output voltage.
$V_{IN}$ is the input voltage.
$G_{MEA}$ is the error amplifier transconductance gain.
$Z_{COMP}$ is the impedance of the series RC network from COMP to GND.
$G_{CS}$ is the current sense transconductance gain (the inductor current divided by the voltage at COMP), which is internally set by the ADP1610.
$Z_{OUT}$ is the impedance of the load and output capacitor.

To determine the crossover frequency, it is important to note that at that frequency the compensation impedance ($Z_{COMP}$) is dominated by the resistor, and the output impedance ($Z_{OUT}$) is dominated by the impedance of the output capacitor. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) is simplified to

$$\left|A_{VL}\right| = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times R_{COMP} \times G_{CS} \times \frac{1}{2\pi \times f_C \times C_{OUT}} = 1 \quad (15)$$

where:
$f_C$ is the crossover frequency.
$R_{COMP}$ is the compensation resistor.

$R_{COMP}$ is calculated using the following equation:

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times V_{OUT} \times \ V_{OUT}}{V_{FB} \times V_{IN} \times G_{MEA} \times GCS} \quad (16)$$

$V_{FB}$ = 1.23, $G_{MEA}$ = 100 µS, and $G_{CS}$ = 2 S is calculated using the following equation:

$$R_{COMP} = \frac{2.55 \times 10^4 \times f_C \times C_{OUT} \times V_{OUT} \times V_{OUT}}{V_{IN}} \quad (17)$$

When the compensation resistor is known, the zero formed by the compensation capacitor and resistor is to be set to one-fourth of the crossover frequency using the following equation:

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} \quad (18)$$

where $C_{COMP}$ is the compensation capacitor.

**Table 5. Recommended External Components for Popular Input/Output Voltage Conditions**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $F_{SW}$ (MHz) | L (µH) | $C_{OUT}$ (µF) | $C_{IN}$ (µF) | R1 (kΩ) | R2 (kΩ) | $R_{COMP}$ (kΩ) | $C_{comp}$ (pF) | $I_{OUT_MAX}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 | 5 | 0.700 | 4.7 | 22 | 22 | 30.9 | 10 | 68 | 150 | 600 |
| | 5 | 1.23 | 2.7 | 10 | 22 | 30.9 | 10 | 100 | 100 | 600 |
| | 9 | 0.700 | 10 | 10 | 10 | 63.4 | 10 | 20 | 680 | 350 |
| | 9 | 1.23 | 4.7 | 4.7 | 10 | 63.4 | 10 | 47 | 150 | 350 |
| | 10 | 0.700 | 10 | 10 | 10 | 71.5 | 10 | 33 | 470 | 300 |
| | 10 | 1.23 | 4.7 | 4.7 | 10 | 71.5 | 10 | 39 | 220 | 300 |
| | 12 | 0.700 | 10 | 10 | 10 | 88.7 | 10 | 33 | 470 | 250 |
| | 12 | 1.23 | 4.7 | 10 | 10 | 88.7 | 10 | 75 | 150 | 250 |
| 5 | 9 | 0.700 | 10 | 10 | 10 | 63.4 | 10 | 24 | 470 | 450 |
| | 9 | 1.23 | 4.7 | 4.7 | 10 | 63.4 | 10 | 47 | 150 | 450 |
| | 10 | 0.700 | 10 | 10 | 10 | 71.5 | 10 | 33 | 330 | 425 |
| | 10 | 1.23 | 4.7 | 4.7 | 10 | 71.5 | 10 | 51 | 220 | 425 |
| | 12 | 0.700 | 10 | 10 | 10 | 88.7 | 10 | 33 | 330 | 350 |
| | 12 | 1.23 | 4.7 | 4.7 | 10 | 88.7 | 10 | 75 | 150 | 350 |

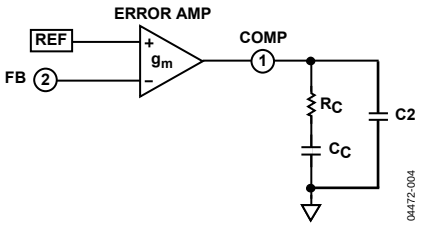



*Figure 26. Compensation Components*

The capacitor (C2) is chosen to cancel the zero introduced by output capacitance ESR. C2 is calculated using the following equation:

$$C2 = \frac{ESR \times C_{OUT}}{R_{COMP}} \quad (19)$$

For low ESR output capacitance such as with a ceramic capacitor, C2 is optional. For optimal transient performance, the $R_{COMP}$ and $C_{COMP}$ may need to be adjusted by observing the load transient response of the ADP1610. For most applications, the compensation resistor is to be in the range of 30 kΩ to 400 kΩ, and the compensation capacitor is to be in the range of 100 pF to 1.2 nF. Table 5 shows external component values for several applications.

## SOFT START CAPACITOR

The voltage at SS ramps up slowly by charging the soft start capacitor ($C_{SS}$) with an internal 3 µA current source. Table 6 listed the values for the soft start period, based on maximum output current and maximum switching frequency.

The soft start capacitor limits the rate of voltage rise on the COMP pin. This limits the peak switch current at startup. Table 6 shows a typical soft start period ($t_{SS}$) at maximum output current ($I_{OUT_MAX}$) for several conditions.

A 20 nF soft start capacitor results in negligible input current overshoot at startup and is therefore suitable for most applications. However, if an unusually large output capacitor is used, a longer soft start period is required to prevent input inrush current.

**Table 6. Typical Soft Start Period**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $C_{OUT}$ (µF) | $C_{SS}$ (nF) | $t_{SS}$ (ms) |
|---|---|---|---|---|
| 3.3 | 5 | 10 | 20 | 0.3 |
| | 5 | 10 | 100 | 2 |
| | 9 | 10 | 20 | 2.5 |
| | 9 | 10 | 100 | 8.2 |
| | 12 | 10 | 20 | 3.5 |
| | 12 | 10 | 100 | 15 |
| 5 | 9 | 10 | 20 | 0.4 |
| | 9 | 10 | 100 | 1.5 |
| | 12 | 10 | 20 | 0.62 |
| | 12 | 10 | 100 | 2 |

Conversely, if fast startup is a requirement, the soft start capacitor can be reduced or even removed, allowing the ADP1610 to start quickly, but allowing greater peak switch current (see Figure 22 to Figure 25).

## APPLICATION CIRCUITS

The circuit in Figure 27 shows the ADP1610 in a step-up configuration that can be used to generate a 10 V regulator with the following specifications: $V_{IN}$ = 2.5 V to 5.5 V, $V_{OUT}$ = 10 V, and $I_{OUT} \leq 400$ mA.

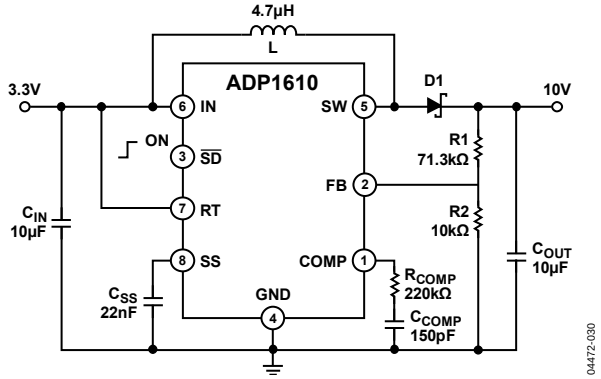



*Figure 27. 3.3 V to 10 V Step-Up Regulator*

The output is set to the desired voltage using Equation 1. To change the compensation network, see Equation 17 and Equation 18.

## DC-TO-DC STEP-UP SWITCHING CONVERTER WITH TRUE SHUTDOWN

Some battery-powered applications require very low standby current. The ADP1610 typically consumes 10 nA from the input, which makes it suitable for these applications. However, the output is connected to the input through the inductor and the rectifying diode, allowing load current draw from the input while shut down. The circuit in Figure 28 enables the ADP1610 to achieve output load disconnect at shutdown. To shut down the ADP1610 and disconnect the output from the input, drive the $\overline{SD}$ pin below 0.4 V.

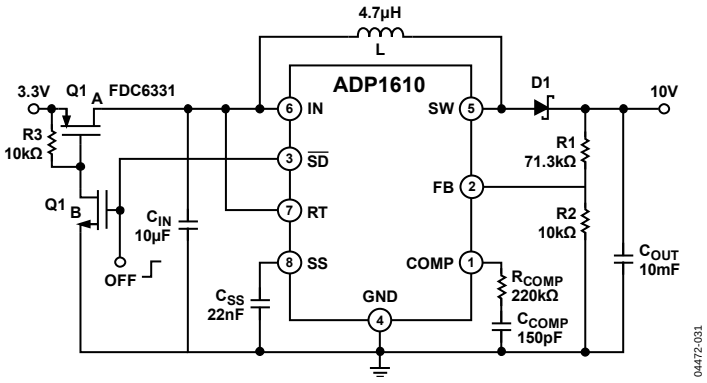



*Figure 28. Step-Up Regulator with True Shutdown*

## TFT LCD BIAS SUPPLY

Figure 29 shows a power supply circuit for TFT LCD module applications. This circuit has +10 V, −5 V, and +22 V outputs. The +10 V is generated in the step-up configuration. The −5 V and +22 V are generated by the charge-pump circuit. During the step-up operation, the SW node switches between 10 V and ground (neglecting forward drop of the diode and on resistance of the switch). When the SW node is high, C5 charges up to 10 V. C5 holds its charge and forward-biases D8 to charge C6 to −10 V. The Zener diode (D9) clamps and regulates the output to −5 V.

The VGH output is generated in a similar manner by the charge-pump capacitors, C1, C2, and C4. The output voltage is tripled and regulated down to 22 V by the Zener diode, D5.

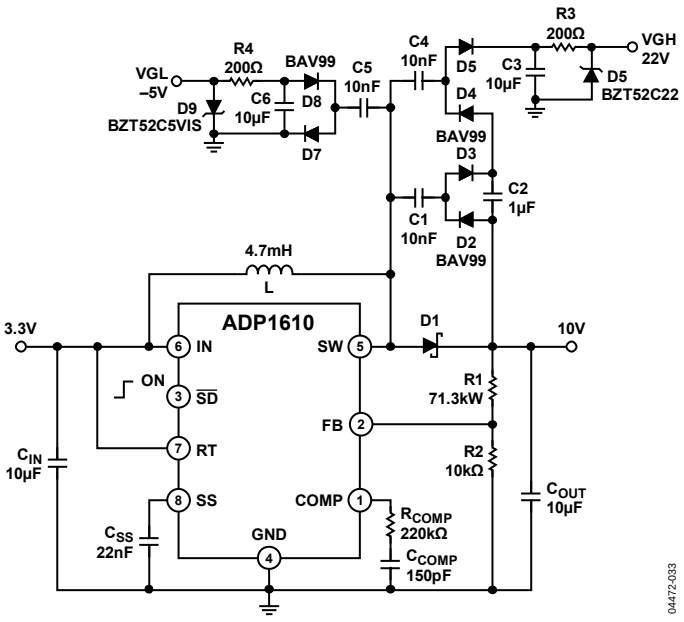



*Figure 29. TFT LCD Bias Supply*

## SEPIC POWER SUPPLY

The circuit in Figure 30 shows the ADP1610 in a single-ended primary inductance converter (SEPIC) topology. This topology is useful for an unregulated input voltage, such as a battery-powered application in which the input voltage can vary between 2.7 V to 5 V, and the regulated output voltage falls within the input voltage range.

The input and the output are dc-isolated by a coupling capacitor (C1). In steady state, the average voltage of C1 is the input voltage. When the ADP1610 switch turns on and the diode turns off, the input voltage provides energy to L1, and C1 provides energy to L2. When the ADP1610 switch turns off and the diode turns on, the energy in L1 and L2 is released to charge the output capacitor ($C_{OUT}$) and the coupling capacitor (C1) and to supply current to the load.

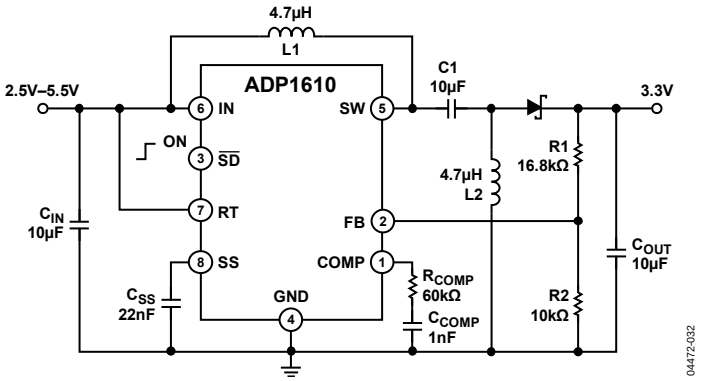



*Figure 30. 3.3 V DC-to-DC Converter*

# LAYOUT PROCEDURE

To get high efficiency, good regulation, and stability, a well-designed PCB layout is required. Where possible, use the sample application board layout as a model.

When designing PCBs the following guidelines are to be used (see Figure 2):

- The low ESR input capacitor ($C_{IN}$) is to be kept close to IN and GND.
- The high current path from $C_{IN}$ through the inductor L1 to SW and PGND is to be kept as short as possible.
- The high current path from $C_{IN}$ through L1, the rectifier D1, and the output capacitor $C_{OUT}$ is to be kept as short as possible.
- High current traces are to be kept as short and as wide as possible.
- The feedback resistors are to be placed as close to the FB pin as possible to prevent noise pickup.
- The compensation components are to be placed as close as possible to COMP.
- To prevent radiated noise injection, high impedance traces are not to be routed near any node connected to SW or near the inductor.

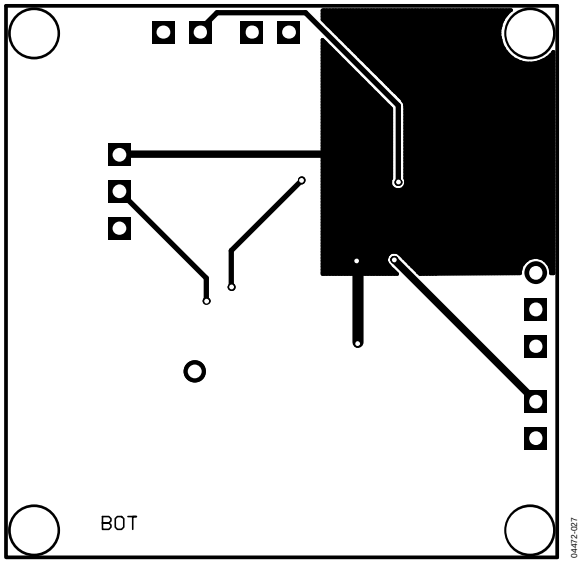



*Figure 31. Sample Application Board (Bottom Layer)*

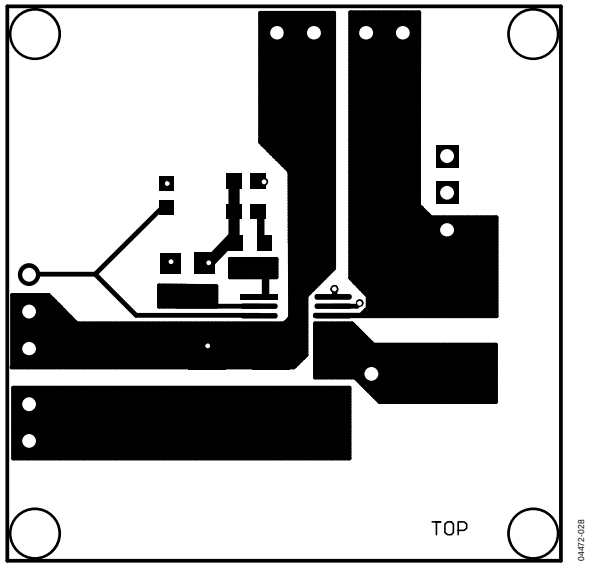



*Figure 32. Sample Application Board (Top Layer)*

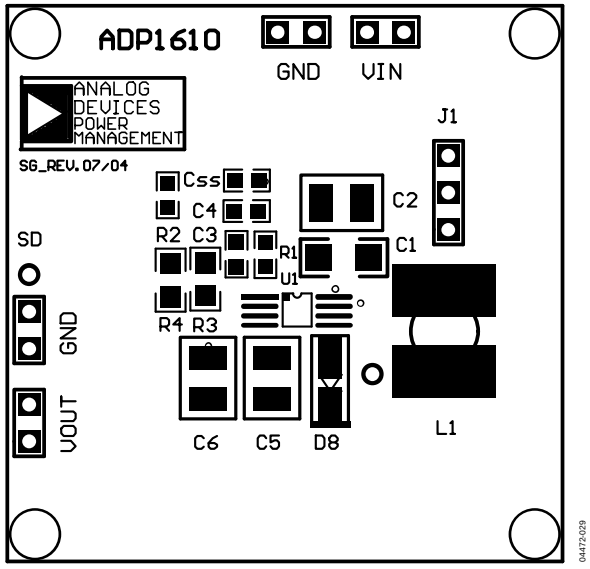
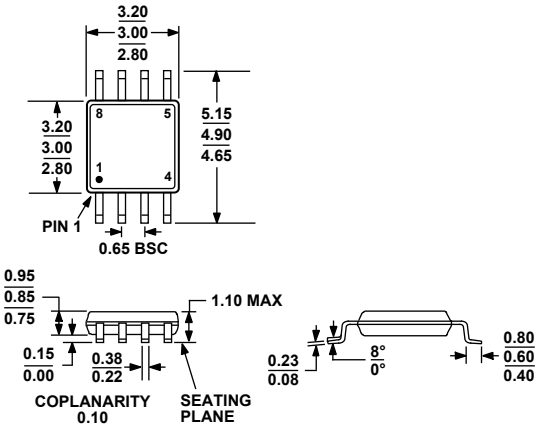



*Figure 33. Sample Application Board (Silkscreen Layer)*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-187-AA

*Figure 34. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADP1610ARMZ-R7[1] | −40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | P03 |
| ADP1610-EVALZ[1] | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES

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