Integrated 500 mA Load Switch with Quad Signal Switch

Data Sheet

ADP1190

FEATURES

- Low input voltage range: 1.4 V to 3.6 V
- Power switch: low RDS_{ON} of 60 mΩ at 3.6 V, with active discharge
- 4 normally open SPST signal switches: RDS_{ON} of 2 Ω at 1.8 V with active pull-down on one side
- 500 mA continuous operating current
- Built-in level shift for control logic that can be operated by 1.2 V logic
- Ultralow shutdown current: <0.7 µA
- Ultrasmall 1.2 mm × 1.6 mm × 0.5 mm, 12-ball, 0.4 mm pitch WLCSP

APPLICATIONS

- Mobile phones
- SIM card disconnect switches
- Digital cameras and audio devices
- Portable and battery-powered equipment

FUNCTIONAL BLOCK DIAGRAM

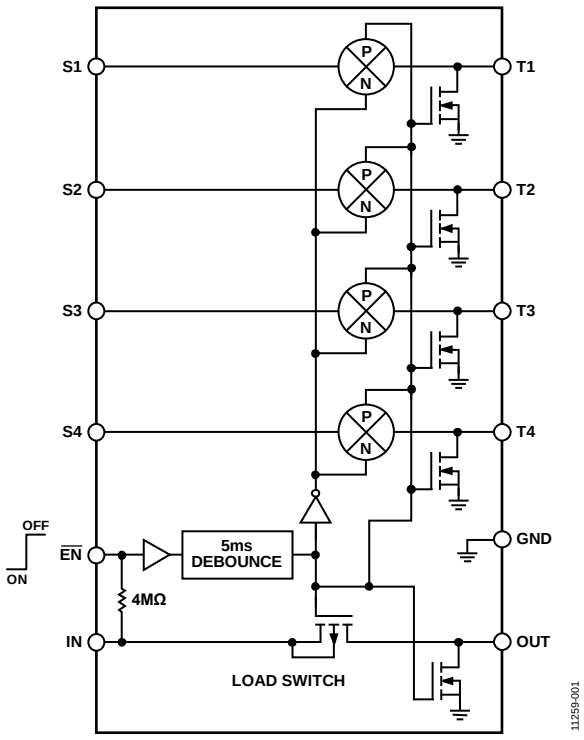

Figure 1.

GENERAL DESCRIPTION

The ADP1190 is an integrated high-side load switch with four signal switches, designed for operation from 1.4 V to 3.6 V. This load switch provides power domain isolation for extended power battery life. The load switch is a low on-resistance P-channel MOSFET that supports up to 500 mA of continuous load current and minimizes power loss. Integrated with the load switch are four normally open 2 Ω SPST signal switches.

Aside from its excellent operating performance, the ADP1190 occupies minimal printed circuit board (PCB) space with an area less than 1.92 mm^2 and a height of 0.50 mm. The ADP1190 is available in an ultrasmall 1.2 mm × 1.6 mm, 12-ball, 0.4 mm pitch WLCSP.

Rev. 0 Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2013 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Revision History 2
Specifications 3
Timing Diagram 3
Absolute Maximum Ratings 4
Thermal Data 4
Thermal Resistance 4
ESD Caution 4
Pin Configuration and Function Descriptions 5
Typical Performance Characteristics 6
Theory of Operation 9
Application Block Diagram 10
Outline Dimensions 11
Ordering Guide 11

REVISION HISTORY

4/13—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{LOAD} = 200 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.4		3.6	V
$\overline{EN}$ INPUT						
$\overline{EN}$ Input Threshold	V_{EN_TH}	1.4 V < V_{IN} < 1.8 V, T_J = −40°C to +85°C (active low)	0.35		1.2	V
		1.8 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +85°C (active low)	0.45		1.2	V
Logic High Voltage	V_{IH}	1.4 V ≤ V_{IN} ≤ 3.6 V	1.2			V
Logic Low Voltage	V_{IL}	1.4 V ≤ V_{IN} ≤ 3.6 V (chip enable)			0.35	V
$\overline{EN}$ Input Pull-Up Resistance	R_{EN}			4		MΩ
CURRENT						
Ground Current[1]	I_{GND}	OUT open, T_J = −40°C to +85°C			2	µA
Shutdown Current	I_{OFF}	$\overline{EN}$ = V_{IN} or open		0.7		µA
		$\overline{EN}$ = V_{IN} or open, T_J = −40°C to +85°C			2	µA
Analog Switch Off Current	I_{A_OFF}	Into S1, $\overline{EN}$ = V_{IN} or open		0.4		µA
LOAD SWITCH V_{IN} TO V_{OUT} RESISTANCE	RDS_{ON}					
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, $\overline{EN}$ = 1.5 V		60		mΩ
		V_{IN} = 2.5 V, I_{LOAD} = 200 mA, $\overline{EN}$ = 1.5 V		80		mΩ
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, $\overline{EN}$ = 1.5 V, T_J = −40°C to +85°C		100	170	mΩ
SIGNAL SWITCH RESISTANCE	RDS_{ON}	Maximum value of analog input sweep				
		V_{IN} = 3.6 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		0.6		Ω
		V_{IN} = 2.5 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		1		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		2.0		Ω
RDS Flatness		V_{IN} = 3.6 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		0.5		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		1		Ω
OUTPUT DISCHARGE RESISTANCE	R_{DIS}	On load switch output and each analog switch output, T1, T2, T3, and T4		215		Ω
−3 dB BANDWIDTH	BW_{3dB}	V_{IN} = 3.6 V, R_{LOAD} = 50 Ω, C_{LOAD} = 5 pF, see Figure 23		50		MHz
V_{OUT} TIME						
Turn-On Delay Time	t_{ON_DLY}	I_{LOAD} = 200 mA, $\overline{EN}$ = GND, C_{LOAD} = 0. 1 µF		5		ms
Turn-Off Delay Time	t_{OFF_DLY}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, $\overline{EN}$ = 1.5 V, C_{LOAD} = 0.1 µF		4		µs

[1] Ground current includes $\overline{EN}$ pull-down current.

TIMING DIAGRAM

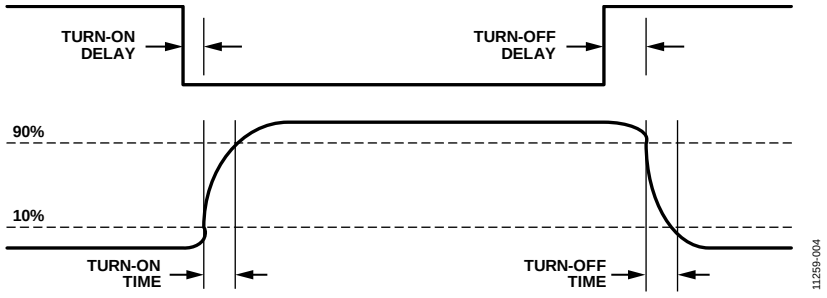

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to +4.0 V
OUT to GND	−0.3 V to V_{IN}
Sx to GND	−0.3 V to +4.0 V
Tx to GND	−0.3 V to +4.0 V
$\overline{EN}$ to GND	−0.3 V to +4.0 V
Continuous Load Switch Current	
T_A = 25°C	±1 A
T_A = 85°C	±500 mA
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP1190 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *Wafer Level Chip Scale Package*, available at www.analog.com.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
12-Ball WLCSP	130	29.2	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

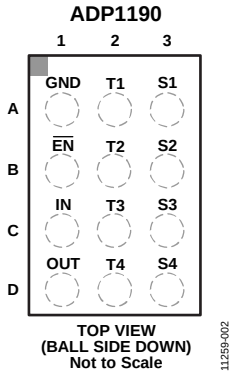

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GND	Ground.
B1	$\overline{EN}$	Enable Input, Active Low.
C1	IN	Input Voltage.
D1	OUT	Load Switch Output Voltage.
A2	T1	Channel 1 Analog Switch. Connect to the SIM card socket (has active discharge).
B2	T2	Channel 2 Analog Switch. Connect to the SIM card socket (has active discharge).
C2	T3	Channel 3 Analog Switch. Connect to the SIM card socket (has active discharge).
D2	T4	Channel 4 Analog Switch. Connect to the SIM card socket (has active discharge).
A3	S1	Channel 1 Analog Switch. Connect to the microcontroller.
B3	S2	Channel 2 Analog Switch. Connect to the microcontroller.
C3	S3	Channel 3 Analog Switch. Connect to the microcontroller.
D3	S4	Channel 4 Analog Switch. Connect to the microcontroller.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

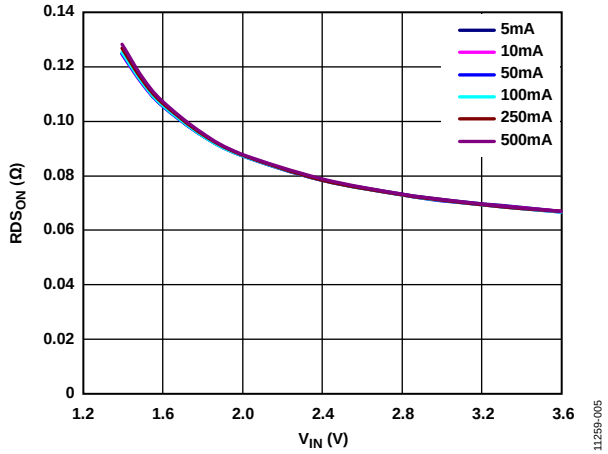

Figure 4. Load Switch RDS_{ON} vs. Input Voltage (V_{IN}), Different Load Currents

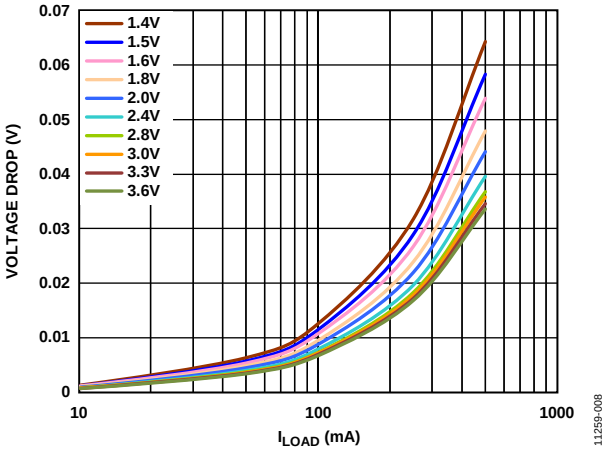

Figure 7. Load Switch Voltage Drop vs. Load Current, Different Input Voltages

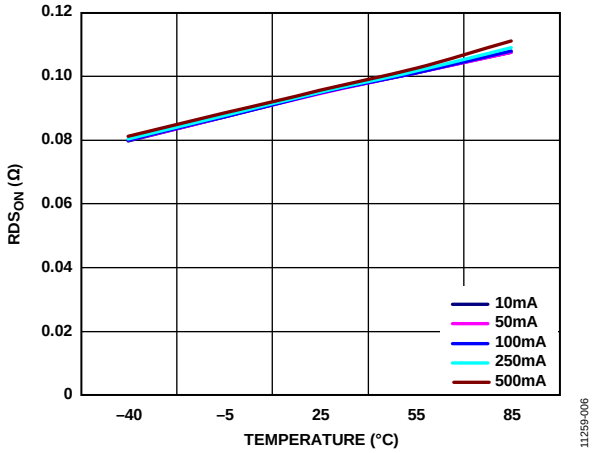

Figure 5. Load Switch RDS_{ON} vs. Temperature, Different Load Currents, V_{IN} = 1.8 V

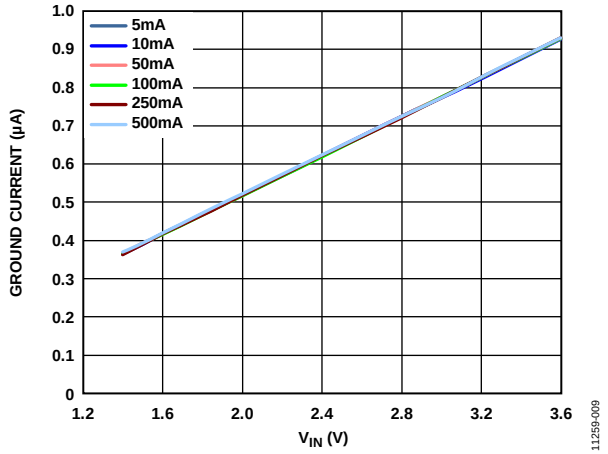

Figure 8. Ground Current vs. Input Voltage, Different Load Currents

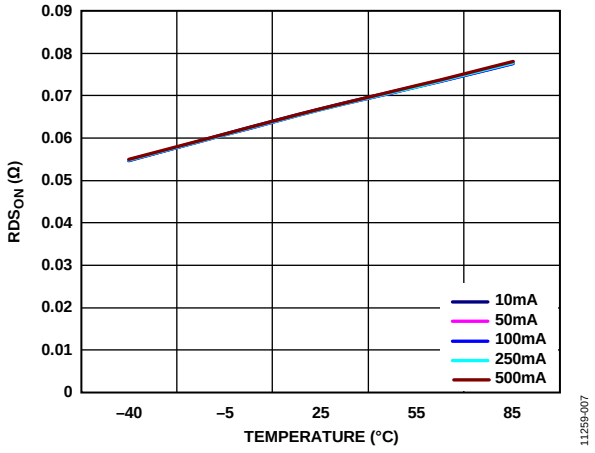

Figure 6. Load Switch RDS_{ON} vs. Temperature, Different Load Currents, V_{IN} = 3.6 V

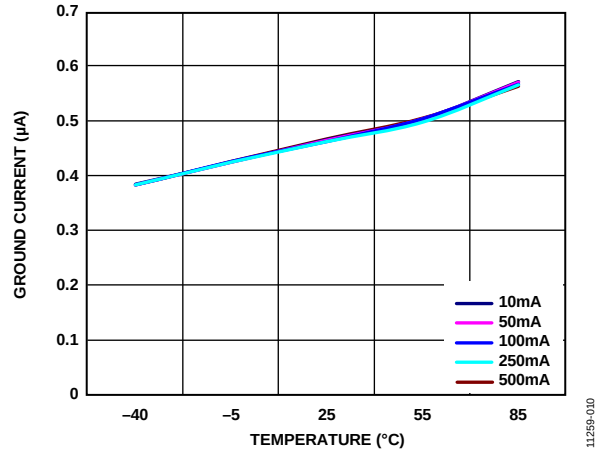

Figure 9. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 1.8 V

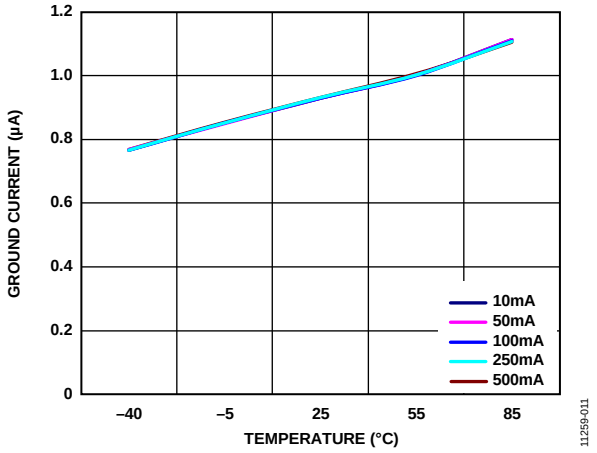

Figure 10. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 3.6 V

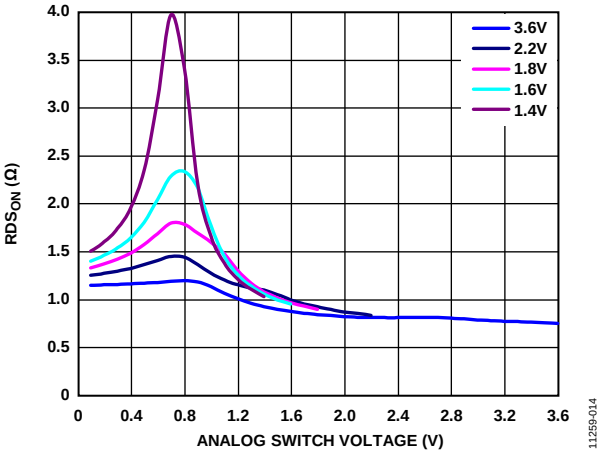

Figure 13. Signal Switch RDS_{ON} vs. Analog Switch Voltage

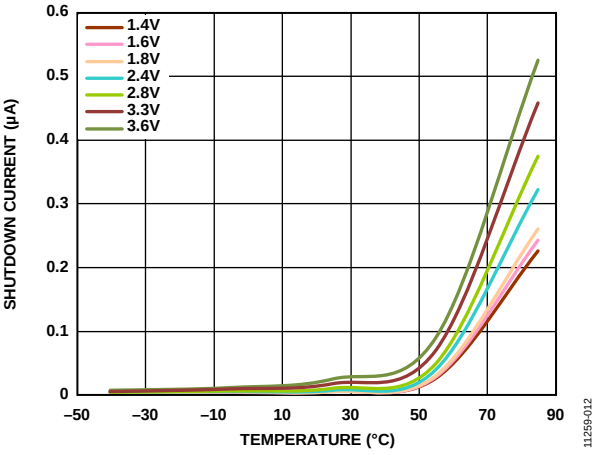

Figure 11. Shutdown Current vs. Temperature, Different Input Voltages

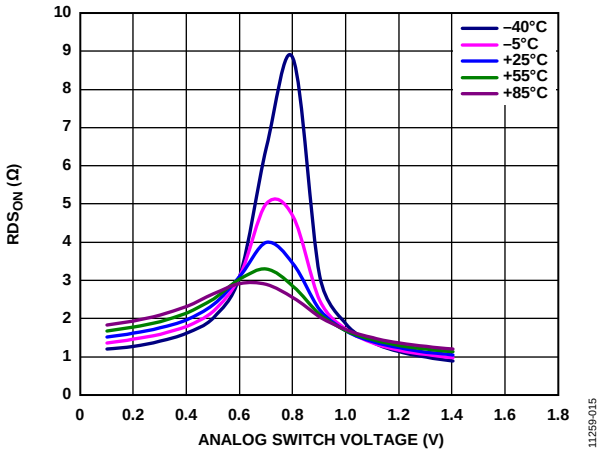

Figure 14. Signal Switch RDS_{ON} vs. Analog Switch Voltage and Temperature, V_{IN} = 1.4 V

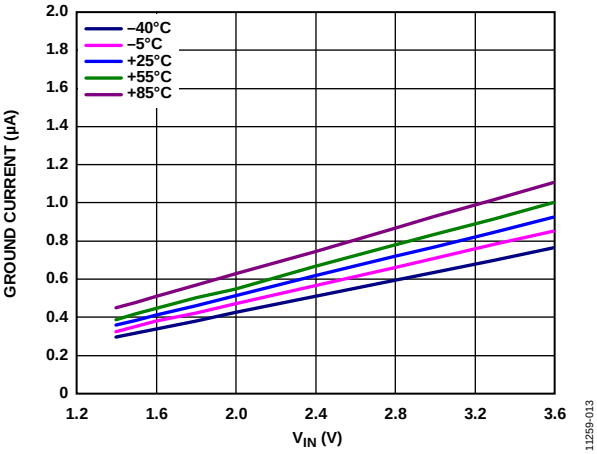

Figure 12. No Load Ground Current vs. Input Voltage and Temperature

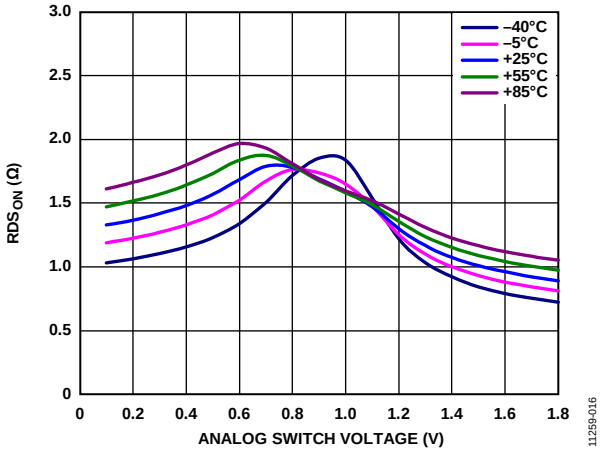

Figure 15. Signal Switch RDS_{ON} vs. Analog Switch Voltage and Temperature, V_{IN} = 1.8 V

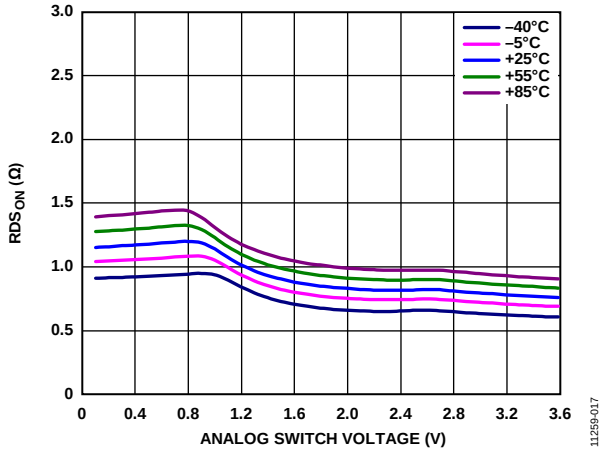

Figure 16. Signal Switch RDS_{ON} vs. Analog Switch Voltage and Temperature, V_{IN} = 3.6 V

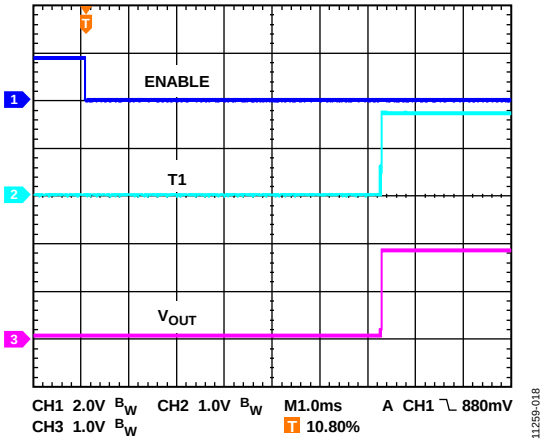

Figure 17. Typical Turn-On Delay Time, V_{IN} = 1.8 V, 50 mA Load

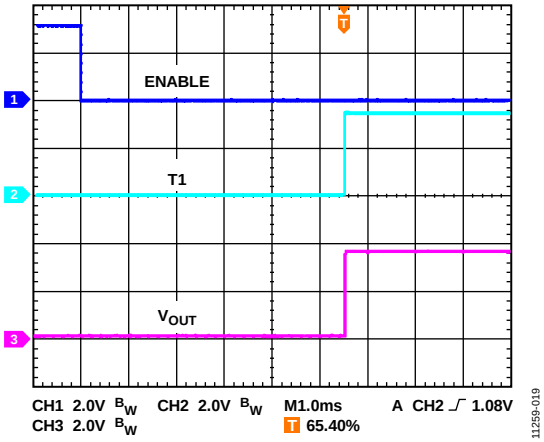

Figure 18. Typical Turn-On Delay Time, V_{IN} = 3.6 V, 100 mA Load

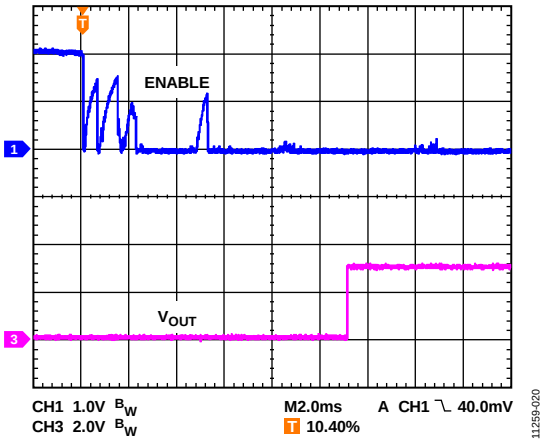

Figure 19. Enable Debounce Behavior, V_{IN} = 1.8 V

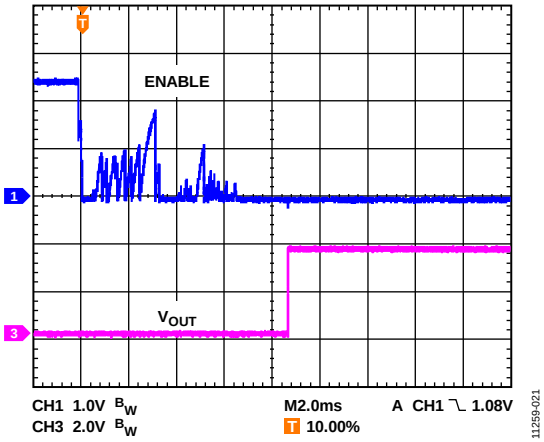

Figure 20. Enable Debounce Behavior, V_{IN} = 3.6 V

THEORY OF OPERATION

The ADP1190 is a high-side load switch integrated with four signal switches. The load switch and signal switches are turned on by a low signal on the $\overline{EN}$ pin. A 4 MΩ pull-up resistor on this pin allows it to be driven by an open-collector or mechanical switch. When the part is disabled, the T1 to T4 pins are actively pulled down with a nominal resistance of 215 Ω. There is a 5 ms debounce counter on $\overline{EN}$ for use with a mechanical $\overline{EN}$ switch. That is, $\overline{EN}$ must be held low for 5 ms before the part is enabled. If $\overline{EN}$ transitions high before this timeout, the counter is reset and starts a new 5 ms count.

The signal path is controlled by a PMOS/NMOS transmission gate with an on resistance of 2 Ω. Break-before-make logic control ensures that the active pull-down is off before the signal path is enabled.

In addition to these features, the ADP1190 occupies minimal printed circuit board (PCB) space with an area less than 1.92 mm^2 and a height of 0.50 mm. The ADP1190 is available in an ultrasmall 1.2 mm × 1.6 mm, 12-ball, 0.4 mm pitch WLCSP.

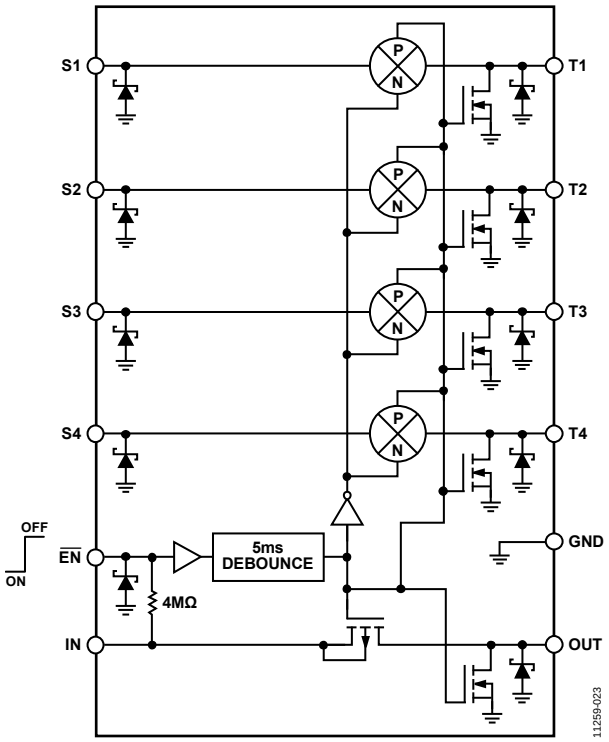

Figure 21. Block Diagram with ESD Protection Devices

APPLICATION BLOCK DIAGRAM

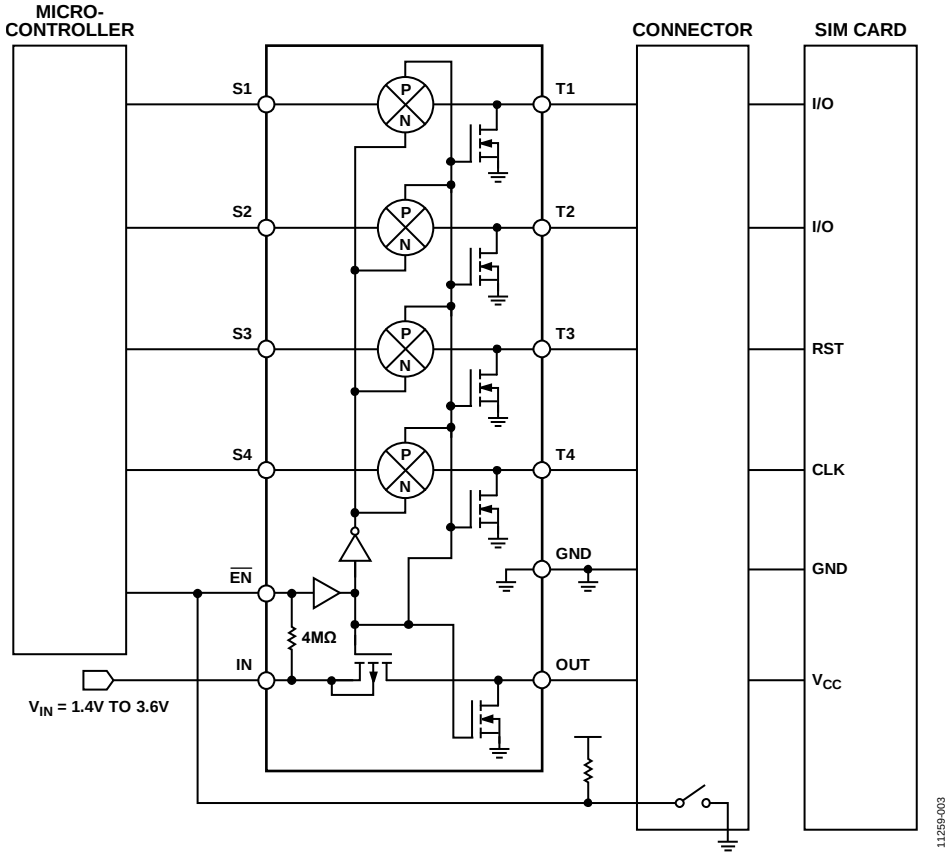

Figure 22. Typical Application

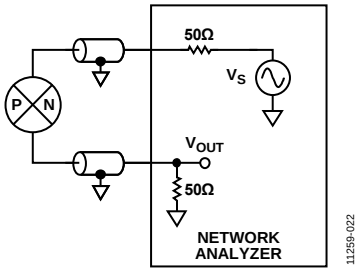

Figure 23. Bandwidth Measurement Setup

OUTLINE DIMENSIONS

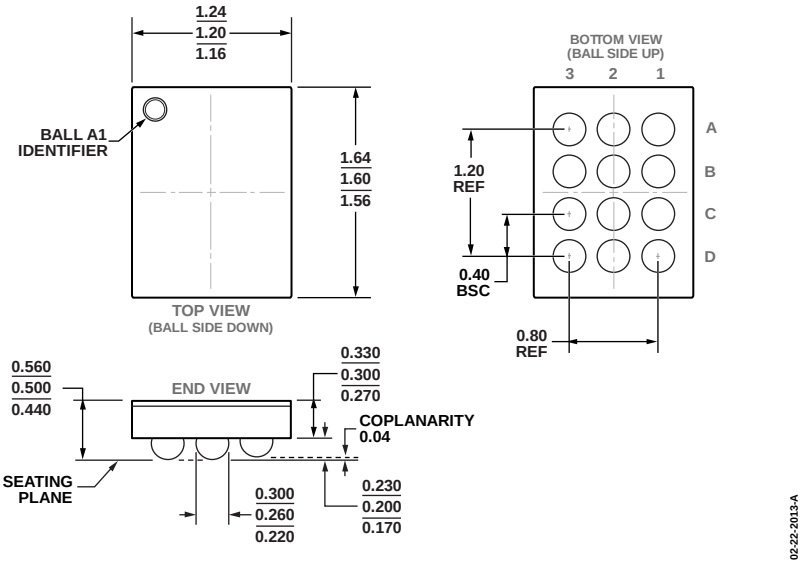

Figure 24. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP1190ACBZ-R7	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	CB-12-10	LNE

[1] Z = RoHS Compliant Part.

NOTES

©2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D11259-0-4/13(0)