10.7 Gbps Electro-Absorption Modulator Driver

Preliminary Technical Data

ADN2849

FEATURES

Data Rates up to 10.709Gb/s
Typical Rise/Fall Time 27ps
Power Dissipation 900mW (at 2V swing, 1V offset)
Programmable Modulation Voltage up to 3V
Programmable Bias Offset Voltage up to 2V
Voltage-input control for offset, modulation
Cross Point Adjust Range 30%- 85%
Selectable Data Retiming
PECL/CML Data & Clock Inputs
50Ω on Chip Data & Clock Terminations
Modulation Ebnable/Disable
$|S_{11}|$<-10dB , $|S_{22}|$<-8dB at 10GHz
Positive or negative 5.2 or 5.0V single supply operation
Available in dice and 4x4mm 24 Lead LFCSP package

PRODUCT DESCRIPTION

The ADN2849 is a low power 10.7Gbps driver for electro-absorption modulator (EAM) applications. The modulation voltage is programmable via an external voltage up to a maximum swing of 3V when driving 50Ω. The bias offset voltage and output eye cross point are also programmable. On-chip 50Ω resistor is provided for back termination of the output. The ADN2849 is driven by AC coupled differential CML level data and has selectable data retiming to remove jitter from data input signal. The modulation voltage can be enabled or disabled by driving the MOD_ENB pin with the proper logic levels. It can operate with positive or negative (5.2V or 5.0V) supply voltage.

The ADN284949 is available in a compact 4x4mm plastic package or dice format.

APPLICATIONS

SONET OC-192 Optical Transmitters
SDH STM-64 Optical Transmitters
10Gb Ethernet IEEE802.3
XFP/X2/XENPACK/MSA-300 Optical Modules

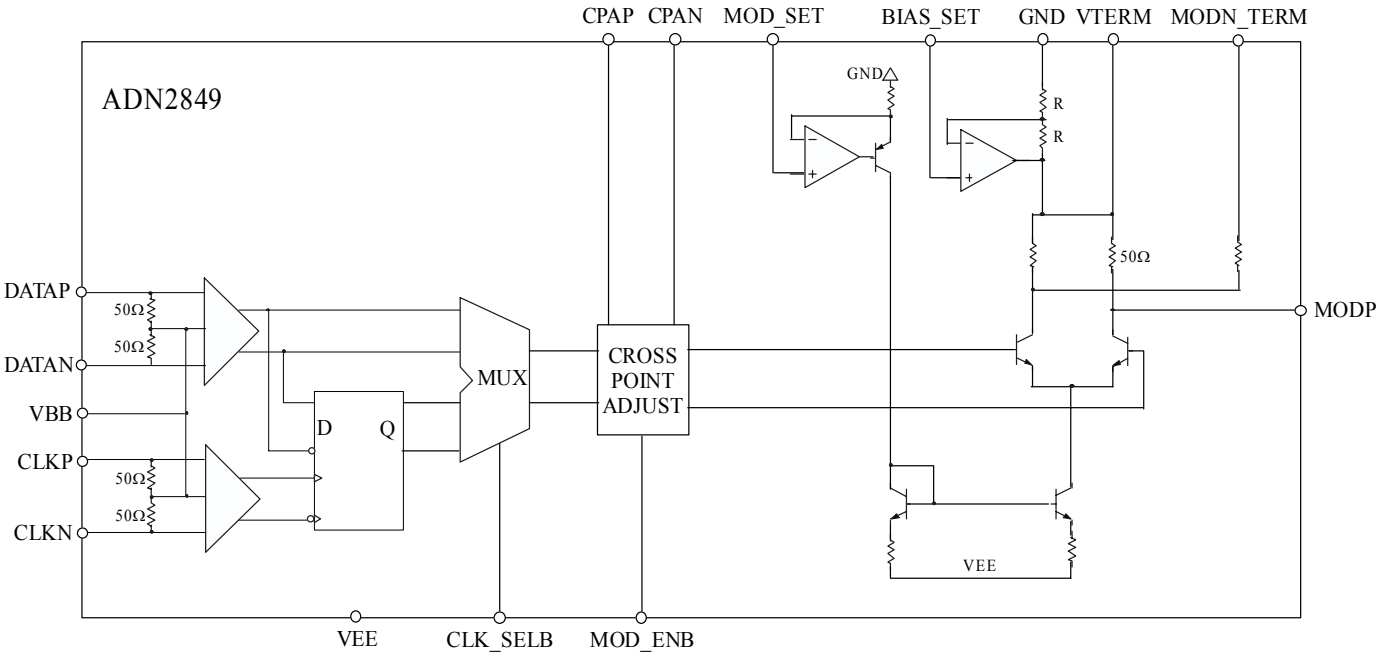


Figure 1. Functional Block Diagram

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Specifications

(Electrical Specifications (VEE=VEE_{MIN} to VEE_{MAX}. All specifications T_{min} to T_{max}, Z_L=50Ω unless otherwise noted. Typical values specified at 25^{0}C)

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
Bias Offset Voltage(MODP)					
Bias offset voltage	-0.25		-2.0	V	Note 1
BIAS_SET voltage to bias offset voltage gain	0.9		1.1	V/V	T_a=25^{0}C, VEE=-5.2V
Bias offset voltage drift over temperature and VEE	-5		5	%	
Modulation Voltage(MODP)					
Modulation voltage swing	0.6		3.0	V	Note1
MOD_SET voltage to modulation voltage swing gain	1.5		1.9	V/v	T_a=25^{0}C, VEE=-5.2V
Modulation voltage drift over temperature and VEE	-5		5	%	
Back termination resistance	40		60	Ω	
Rise time (20% - 80%)		27	36	ps	
Fall time (20% - 80%)		27	36	ps	
Random jitter			0.75	ps RMS	
Total jitter			10	ps_{p-p}	
Cross point adjust range	30		85	%	
Cross point drift over temperature and VEE	-5		5	%	
Minimum output voltage(single ended)	VEE+1.7			V	Note1
$\|S_{22}\|$		-8		dB	At 10GHz
Modulation enable time			100	ns	
Modulation disable time			100	ns	
Data Inputs (DATAP, DATAN)					
Differential Input voltage	600		1600	mV_{p-p}	
Termination resistance	40		60	Ω	
Setup time (see figure 2)	25			ps	CLK_SELB='0'
Hold time (see figure 2)	25			ps	CLK_SELB='0'
$\|S_{11}\|$		-10		DB	At 10GHz
Clock Inputs (CLKP, CLKN)					
Differential Input voltage	600		1600	mV_{p-p}	
Termination resistance	40		60	Ω	
$\|S_{11}\|$		-10		dB	At 10GHz
Cross point adjust (CPAN, CPAP)					
Input voltage range	-0.85		-1.85	V	
CPAP, CPAN differential voltage			0.6	V_{p-p}	
Input current	85		115	μA	
Logic Inputs (MOD_ENB, CLK_SELB)					
V_{IH}	VEE+2			V	
V_{IL}			VEE+0.8	V	
I_{IL}			-400	μA	V_I=VEE+0.4V
I_{IH}			20	μA	V_I=VEE+2.4V
			200	μA	V_I=0V
Supply					
VEE	-4.75	-5.2	-5.5	V	IMOD=0
I_{EE}		52		mA	$V_{MODP/MODN}$=0

Notes:
Minimum supply voltage and minimum output voltage determine maximum output swing and maximum bias offset that can be achieved concurrently.
Measured using the characterization circuit shown in figure 3.

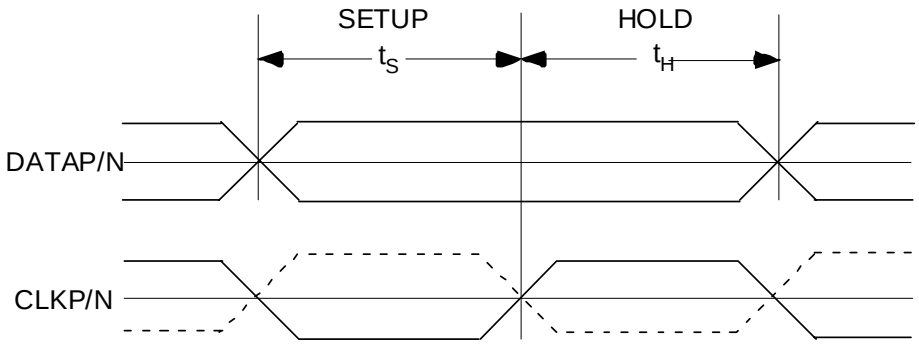


Figure 2. Setup and hold time

TBD

Figure 3. High-speed characterization circuit

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min	Max	Units	Conditions
VEE to GND	TBD	TBD	V	
VBB to GND	TBD	TBD	V	
DATAP, DATAN to GND	TBD	TBD	V	
CLKP, CLKN to GND	TBD	TBD	V	
CPAP, CPAN to GND	TBD	TBD	V	
MOD_SET to GND	TBD	TBD	V	
BIAS_SET to GND	TBD	TBD	V	
MOD_ENB to GND	TBD	TBD	V	
CLK_SELB to GND	TBD	TBD	V	
Staorage temperature range	-60	+150	^{0}C	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

PACKAGE THERMAL SPECIFICATIONS

Table 3.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS/COMMENTS
$\theta_{J\text{-}TOP}$	TBD	TBD	TBD	^{0}C/W	Thermal resistance from junction to top of package
$\theta_{J\text{-}PAD}$	TBD	TBD	TBD	^{0}C/W	Thermal resistance from junction to bottom of exposed pad

ORDERING GUIDE

Table 4.

Model	Temperature range	Package description
ADN2849ACP	-40^{0}C to +85^{0}C	24 Lead LFCSP
ADN2849ACP-RL	-40^{0}C to +85^{0}C	24 Lead LFCSP
ADN2849ACP-RL7	-40^{0}C to +85^{0}C	24 Lead LFCSP
ADN2849SURF	-40^{0}C to +85^{0}C	Bare die

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS (T_A=25^{0}C, VEE=-5.2V)

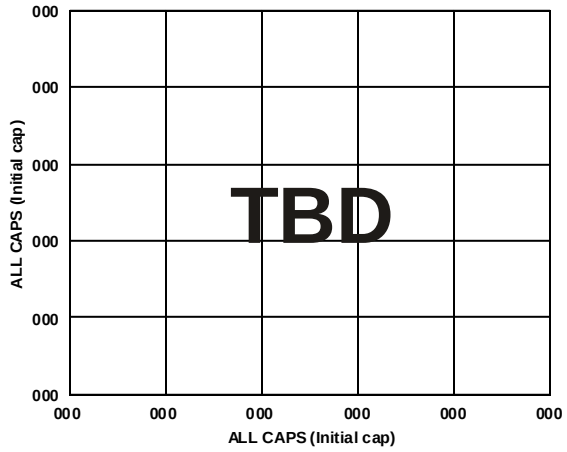


Figure 4. Rise time vs. Swing

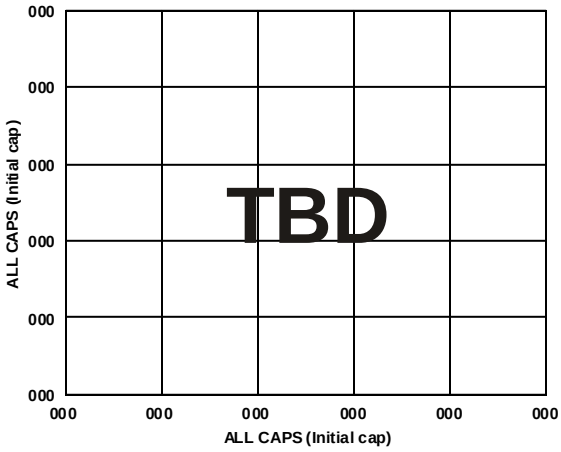


Figure 7. Total jitter vs. Swing

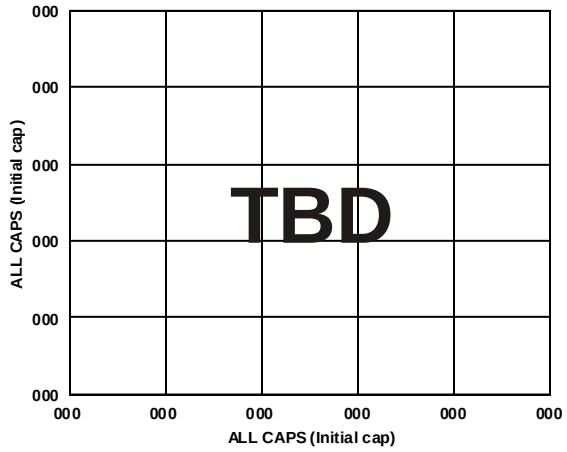


Figure 5. Fall time vs. Swing

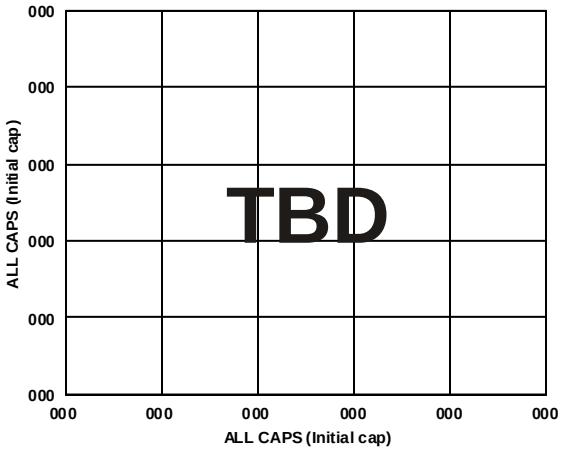


Figure 8. Cross point vs. differential voltage at CPAP/CPAN pins

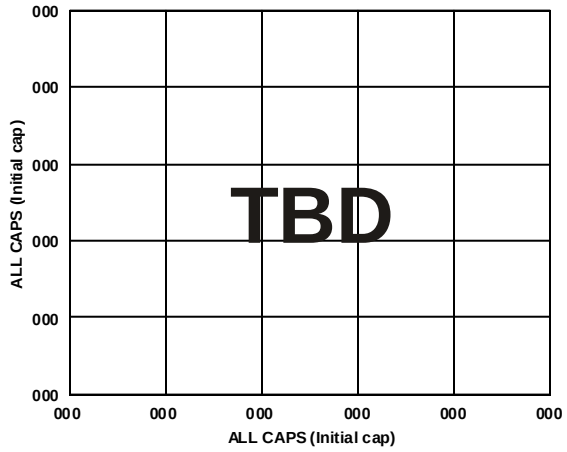


Figure 6. Random jitter vs. Swing

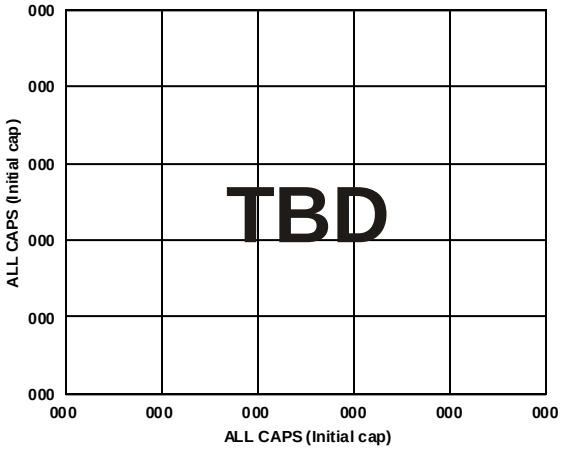


Figure 9. Differential S11 vs. frequency

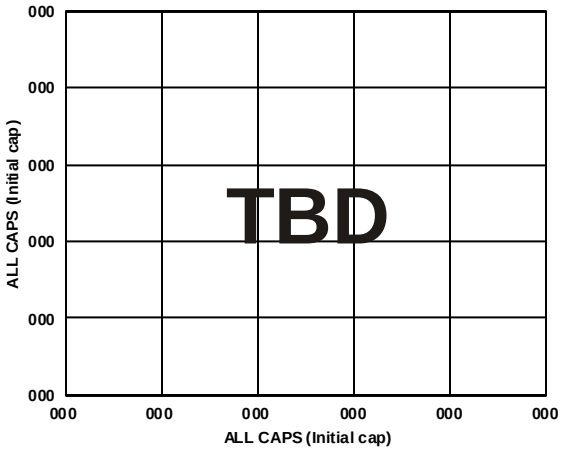


Figure 10. Single-ended S22 vs. frequency

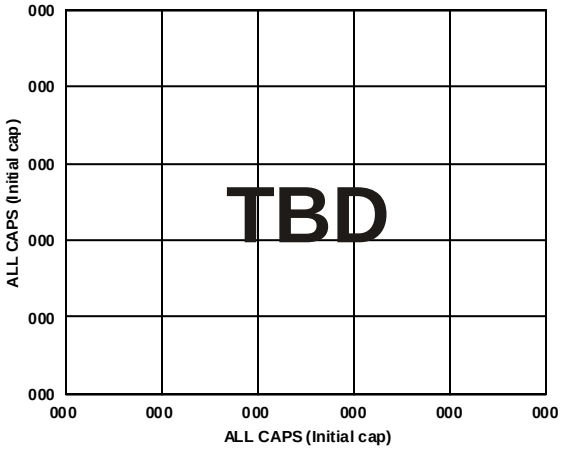


Figure 21. Total supply current vs. Swing with retiming disabled

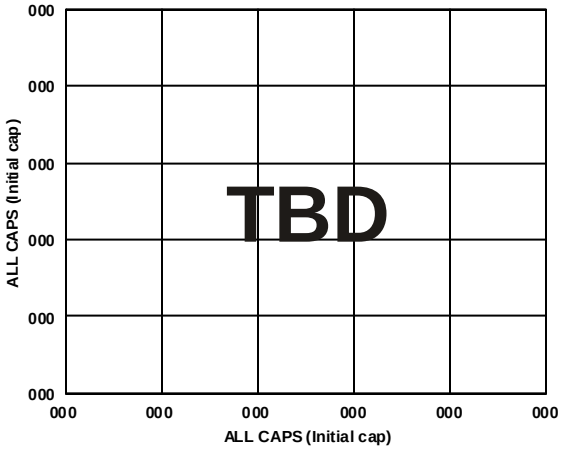


Figure 12. Total supply current vs. Swing with retiming enabled

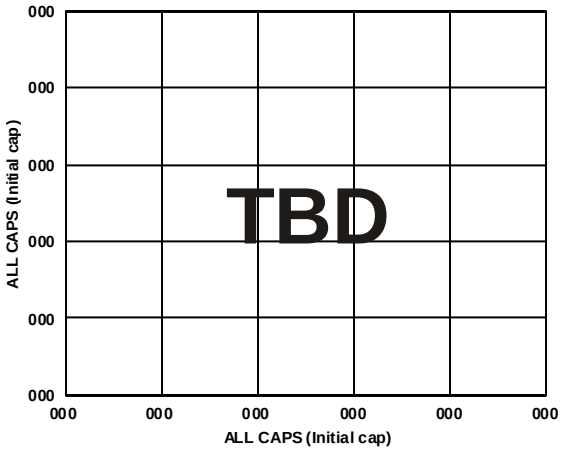


Figure 13. Electrical eye diagram

(2.5V swing, 0.5V offset, PRBS31 at 10.7Gbps)

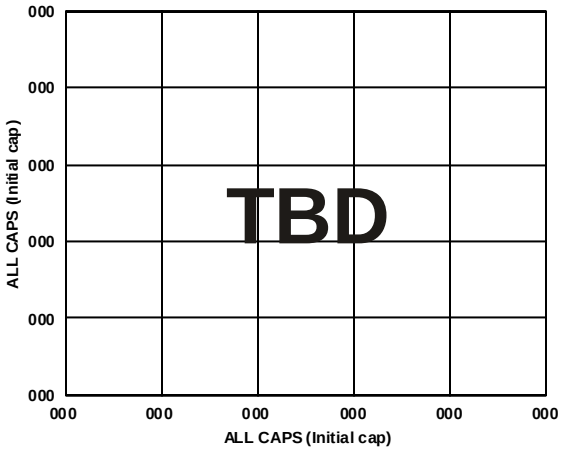


Figure 14. Optical eye diagram using the FLD5F20NP EML

(Pav=0dBm, ER=10dB, PRBS31 pattern at 9.95328Gbps, SONET OC192 mask test)

PIN CONFIGURATION AND FUNCTION DESCRIPTION

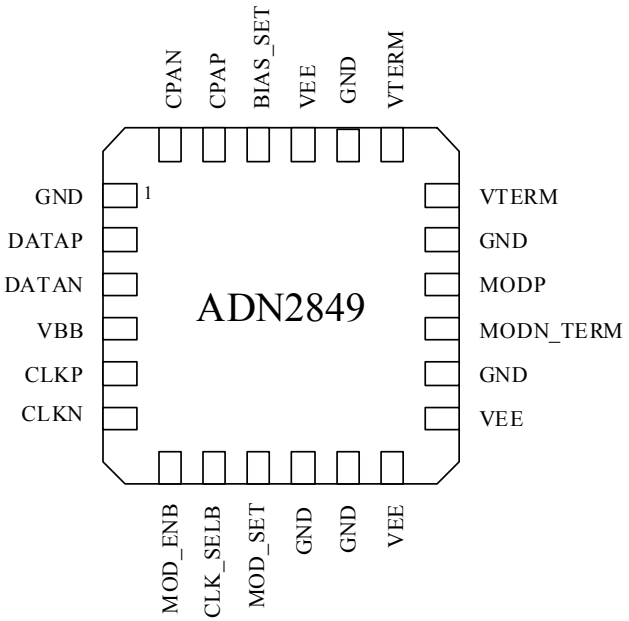


Figure 15. Pin configuration

Note: There is a n exposed pad on the bottom of the package that must be connected to the most negative supply rail of the ADN2849

Table 5.

Pin number	Mnemonic	Description
1, 10, 11, 14,17, 20	GND	Positive power supply
2	DATAP	AC coupled CML data, positive differential terminal
3	DATAN	AC coupled CML data, negative differential terminal
4	VBB	CML termination resistor
5	CLKP	AC coupled CML clock, positive differential terminal
6	CLKN	AC coupled CML clock, negative differential terminal
7	MOD_ENB	Modulation enable logic input
8	CLK_SELB	Retiming select logic input
9	MOD_SET	Modulation voltage set input
12, 13, 21	VEE	Negative power supply
15	MODN_TERM	Termination resistor for MODN
16	MODP	Positive modulation voltage output
18, 19	VTERM	Back termination voltage output
22	BIAS_SET	Bias offset voltage set input
23	CPAP	Cross point adjust positive control input
24	CPAN	Cross point adjust negative control input
Exposed Pad	Pad	Connect to the most negative supply rail of the ADN2849

PAD CONFIGURATION AND FUNCTION DESCRIPTION

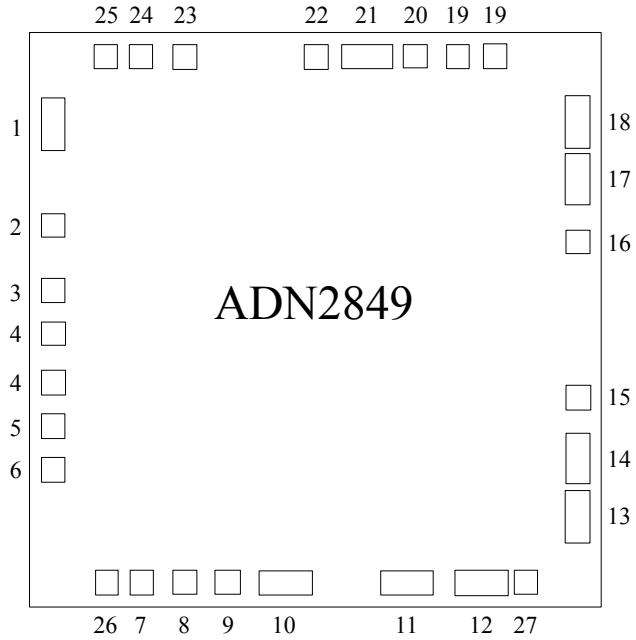


Figure 16. Pad configuration

(Die size 2.05×2.05mm, single bond pad size 84×84μm with 76×76μm glass opening, double bond pad size 184×84μmwith 176×76μm)

Notes:
1. The metallization photograph and the die pad coordinates appear at the end of this document.
2.The pads that have the same number must be bonded together.
3. The back side of the die must be connected to the most negative supply rail of the ADN2849

Table 6.

Pad number	Mnemonic	Description
1, 10, 11, 14,17, 20, 25, 26, 27	GND	Positive power supply
2	DATAP	AC coupled CML data, positive differential terminal
3	DATAN	AC coupled CML data, negative differential terminal
4	VBB	CML termination resistor
5	CLKP	AC coupled CML clock, positive differential terminal
6	CLKN	AC coupled CML clock, negative differential terminal
7	MOD_ENB	Modulation enable logic input
8	CLK_SELB	Retiming select logic input
9	MOD_SET	Modulation voltage set input
12, 13, 21	VEE	Negative power supply
15	MODN_TERM	Termination resistor for MODN
16	MODP	Positive modulation voltage output
18, 19	VTERM	Back termination voltage output
22	BIAS_SET	Bias offset voltage set input
23	CPAP	Cross point adjust positive control input
24	CPAN	Cross point adjust negative control input

THEORY OF OPERATION

GENERAL

Figure 17 shows a typical EA modulator characteristic. Vm represents the voltage across the modulator and Pout represents the optical output power. For small voltages across the modulator it is in its high transmission state. As the voltage becomes more negative, the modulator becomes less transparent to the laser light. Fig. 17 also shows a typical drive signal for an EA modulator. It consists of a modulation signal with a swing Vs, and a bias offset voltage Vb

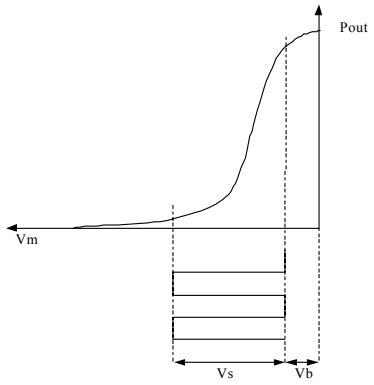


Figure 17. Typical transfer function of an EA modulator

As shown in the functional block diagram (figure 1), the ADN2849 consists of an input stage for data signals, a cross point adjust block and the output stage that generates the bias offset and modulation voltages. The retiming option allows the user to reduce the jitter by applying a reference clock to the clock inputs of the ADN2849. The cross point adjust block pre-distorts the data signal applied to the output stage in order to compensate for the non-linear transfer function of the EA modulator as shown in figure 17. The modulation and the bias offset voltage can be programmed via external DC voltages applied to the ADN2849. These voltages are converted to currents internally and applied to the output stage. The single-ended output stage provides both the bias offset and modulation voltages at the same pin (MODP) without the need of any external components. The ADN2849 can operate with positive or negative (5.0V or 5.2V) supply voltage.

INPUT STAGE

The input stage of the ADN2849 gains the data and clock signals applied to the DATAP, DATAN and CLKP, CLKN pins respectively to a level that ensures proper operation of the ADN2849's output stage. The data and clock inputs are PECL/CML compatible and can accept input signal swings in the range of 600mV to 1600mV peak-to peak differential. The equivalent circuit for the data and clock input pins is shown in figure 18.

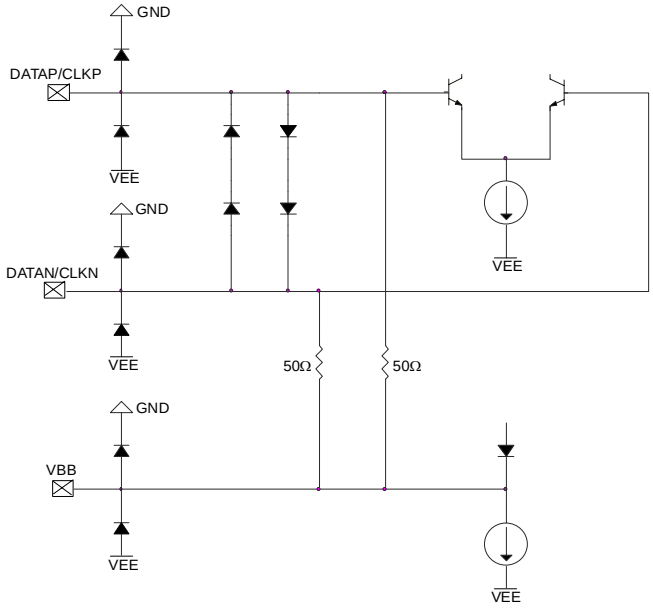


Figure 18. Equivalent circuit for the data and clock input pins

The data and clock input pins are internally terminated with a 100Ω differential termination resistor to minimize signal reflections at the input pins that could otherwise lead to degradation in the output eye diagram. The ADN2849 input pins must be AC-coupled with the signal source to eliminate the need of matching between the common mode voltages of the data signal source and the inputs stage of the driver. Also, the common mode terminal of the internal termination resistors (VBB) must be externally decoupled. Figure 19 shows the recommended connection between the data/signal source and the ADN2849 input pins.

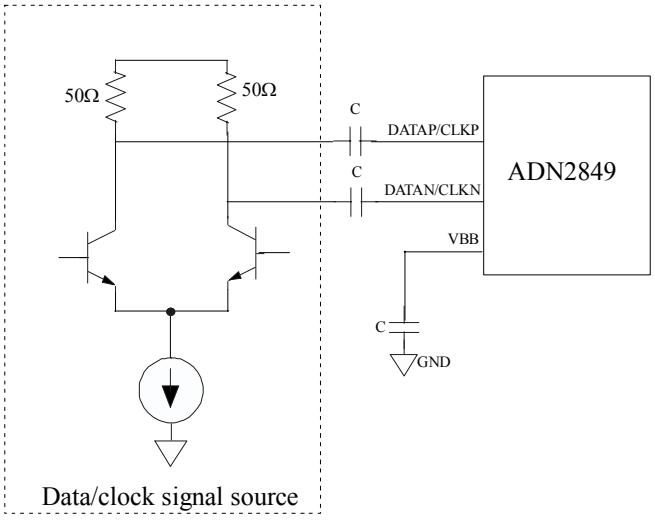


Figure 19. AC-coupling the data/clock signal source to the ADN2849 input pins

The capacitors used AC-coupling and the decoupling of the VBB pin must have an impedance less than 50Ω over the required operating frequency range. Generally this is achieved using values from 10nF to 100nF.

The retiming feature of the ADN2849 allows the user to remove the data dependent jitter present on the DATAP and DATAN pins by applying the data and clock signals to the ADN2849's internal latch. The retiming feature can be enabled or disabled depending on the logic level applied to the CLK_SELB pin as described in table 7. Note that any jitter present on the CLKP and CLKN pins is added to the output.

Table 7.

CLK_SELB logic level	Retiming function
High	Disabled
Low	Enabled

If the retiming feature is disabled the CLKP and CLKN inputs can be left floating.

The CLK_SELB is a 5V TTL and CMOS compatible digital input. Its equivalent circuit is shown in figure 20.

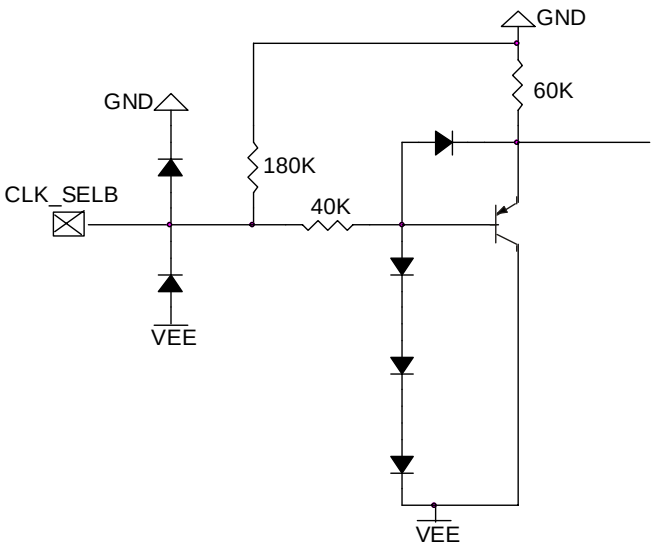


Figure 20. Equivalent circuit of the CLK_SELB pin

CROSS POINT ADJUST

The cross point adjust function allows the user to move the eye crossing level in the modulation voltage to compensate for asymmetry in the EA modulator electrical-to- optical transfer function. Figure 21 shows an example on how the cross point adjust can compensate the asymmetry of the EA modulator transfer function. The 50% cross point in the optical eye can be obtained in this case by moving the cross point of the signal applied to the EA modulator away from the 50% point.

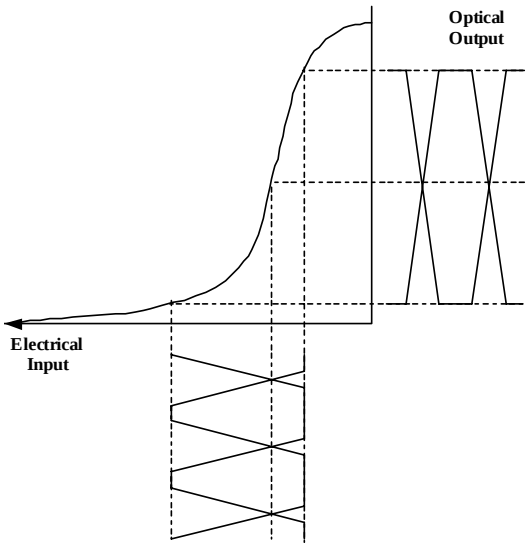


Figure 21. Cross point adjust compensation

The cross point is controlled by the differential voltage applied to the CPAP and CPAN pins. The equivalent circuit of the CPAP and CPAN pins is shown in figure 22.

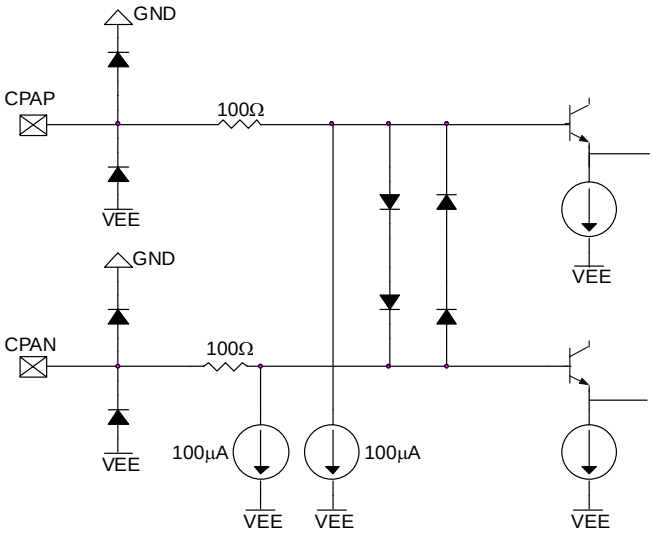


Figure 22. Equivalent circuit of the CPAP and CPAN pins

The single-ended voltage at CPAP and CPAN pins must be within the –0.8V to-1.85V range for proper operation of the cross point adjust block. The cross point will be controlled by the differential voltage obtained from the single-ended voltages applied to CPAP and CPAN pins. A simple implementation of a cross point adjust circuit is shown in figure 23 where a 20KΩ potentiometer generates the required differential voltage within the specified input voltage range.

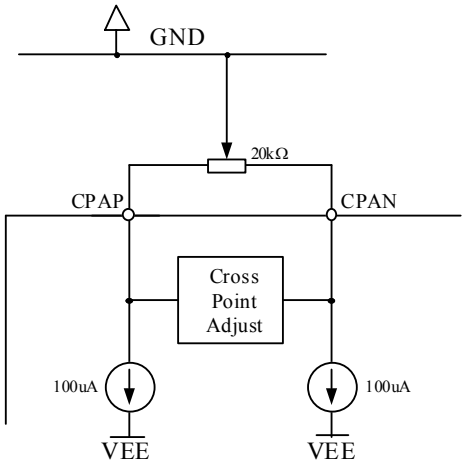


Figure 23. Cross point adjust control circuit

An alternative implementation is to use a voltage DAC and a single-ended to differential conversion amplifier such as the AD138 that will allow digital control of the cross point. When designing the circuitry that will drive the voltages at the CPAP and CPAN pins the user should take in account that each pin is sinking 100μA. If the cross point adjust feature is not required both the CPAP and CPAN pins should be connected to GND. This will automatically set the cross point to 50%. Once the cross point adjust has been calibrated under nominal conditions it has very low drift over temperature and supply voltage variations.

MODULATION ENABLE

The modulation voltage generated by the ADN2849 can be enabled or disabled under the control of the MOD_ENB pin. When the modulation is disabled, the input data is ignored and the voltage at the output of the ADN2849 will place the EA modulator in a high absorption (low transparency) state. The relationship between the logic state of the MOD_ENB input and the modulation voltage is described in table 8.

Table 8.

MOD_ENB logic level	Modulation voltage
Low	Enabled
High	Disabled

The MOD_ENB pin is a 5V TTL and CMOS compatible logic input. Its equivalent circuit of the MOD_ENB pin is shown in figure 24.

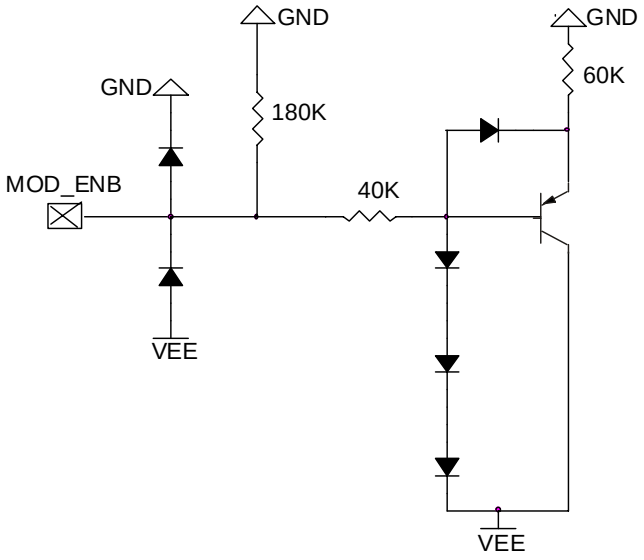


Figure 24. Equivalent circuit of the MOD_ENB pin

OUTPUT STAGE

The output stage of the ADN2849 can provide up to 2V bias offset and up to 3V modulation voltage across a single-ended 50Ω load. Both the bias offset and the modulation voltage are made available at a single pin (MODN) eliminating the need for external bias inductors as shown in figure 25.

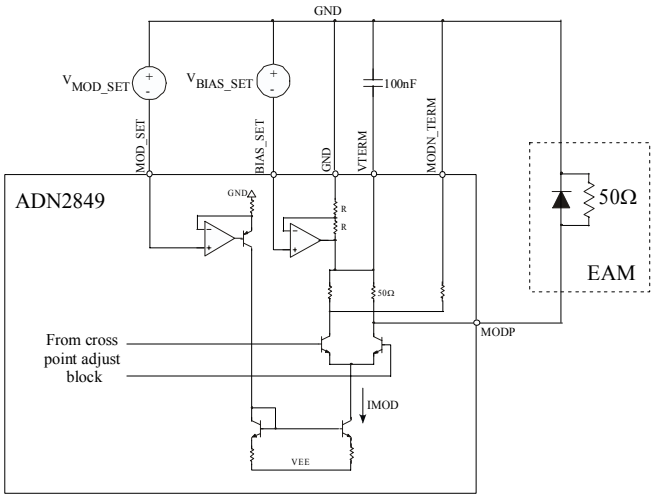


Figure 25. Output stage of the ADN2849

Modulation voltage

The modulation voltage is established by switching the modulation current through the parallel combination of the modulator terminating impedance (50Ω) and the 50Ω back-termination resistor on the ADN2849. The modulation set voltage applied to the MOD_SET pin is converted into current (IMOD) using a voltage-to-current converter which forces a voltage equal to V_{MOD_SET} across an internal fixed resistor. For IMOD range of 24mA to 120mA, the MOD_SET voltage ranges from 340mV to 1.7V. With its maximum modulation current of 120mA, the ADN2849 is capable of generating a 3V modulation voltage across the equivalent load resistance (25Ω). The equivalent circuit of the MOD_SET pin is shown in figure 26.

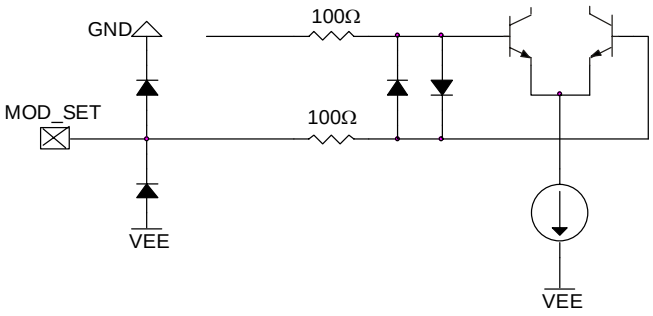


Figure 26. Equivalent circuit of the MOD_SET pin

Bias offset voltage

The bias offset voltage is set by adjusting the voltage between the BIAS_SET pin and GND. An internal operational amplifier sets the termination voltage for the internal 50Ω output back-termination resistors (VTERM) by gaining up the BIAS_SET voltage by two. This gain of two cancels out the attenuation of the dividing network formed by the 50Ω back- termination resistor from the ADN2849 output and the 50Ω load termination, providing a nominal gain of one from the BIAS_SET input to the bias offset voltage available at the output of the ADN2849 (MODP pin). For proper operation, an external low ESR 100nF decoupling capacitor is required between the VTERM pin and GND to prevent transient disturbances on this node. The equivalent circuits of the BIAS_SET, MODP, MODN_TERM and VTERM pins are shown in figure27.

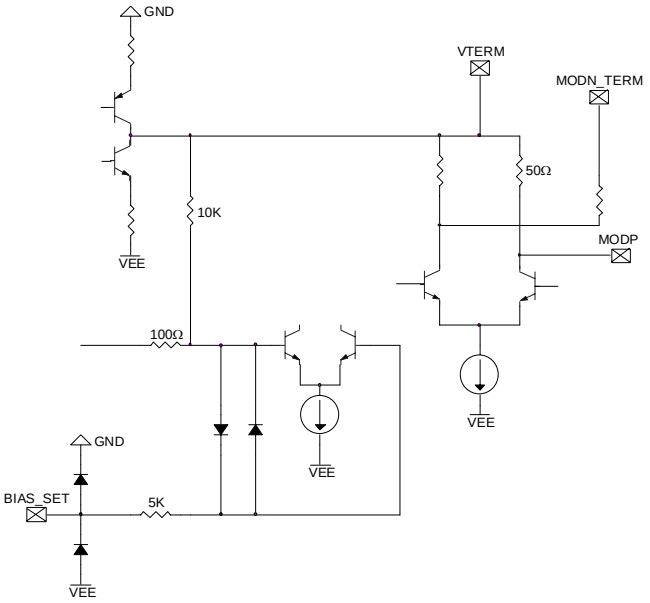


Figure 27. Equivalent circuit of the BIAS_SET, MODP, MODN_TERM and VTERM pins

During factory calibration of the optical transmitter, the user adjusts the BIAS_SET and MOD_SET voltages to achieve the desired bias offset and modulation voltages. This adjustment calibrates out BIAS_SET to bias offset voltage and MOD_SET to modulation voltage gain variations in the ADN2849 due to resistor process variations and the offset of the internal amplifiers. The drift in the bias offset and modulation voltages over temperature and supply voltage variations is very low once it has been calibrated under nominal conditions.

Headroom calculations

The ADN2849 is capable of delivering up to 2V bias offset and up to 3V modulation voltage on a 50Ω single-ended load. However, these values for the bias offset and modulation voltages cannot be obtained at the same time due to headroom constraints. The minimum supply voltage and the MODP minimum output voltage specifications determine the maximum modulation and bias offset voltages that can be achieved concurrently. In order to guarantee proper operation of the ADN2849, the bias offset and modulation voltages must satisfy the following condition:

$$V_{Modulation} + V_{Bias\,Offset} \le |VEE| - V_{MODP\,min}$$

Where,

$V_{Modulation}$ = the required modulation voltage

$V_{Bias\ Offset}$ = the required bias offset voltage

VEE = the supply voltage

$V_{MODPmin}$ = the minimum voltage at the MODP pin (see table 1)

POWER DISSIPATION

The power dissipated by the ADN2849 is a function of the supply voltage and the level of bias offset and modulation voltages required. Figure 28 shows the power dissipation of the ADN2849 vs. modulation voltage for different bias offset voltages. To ensure long-term reliable operation, the junction temperature of the ADN2849 must not exceed 125^0C.

For improved heat dissipation the module's case can be used as heat sink as shown in figure 29. A compact optical module is a complex thermal environment, and calculations of device junction temperature using the package $\theta_{J\text{-}A}$ (Junction-to-Ambient thermal resistance) do not yield accurate results.

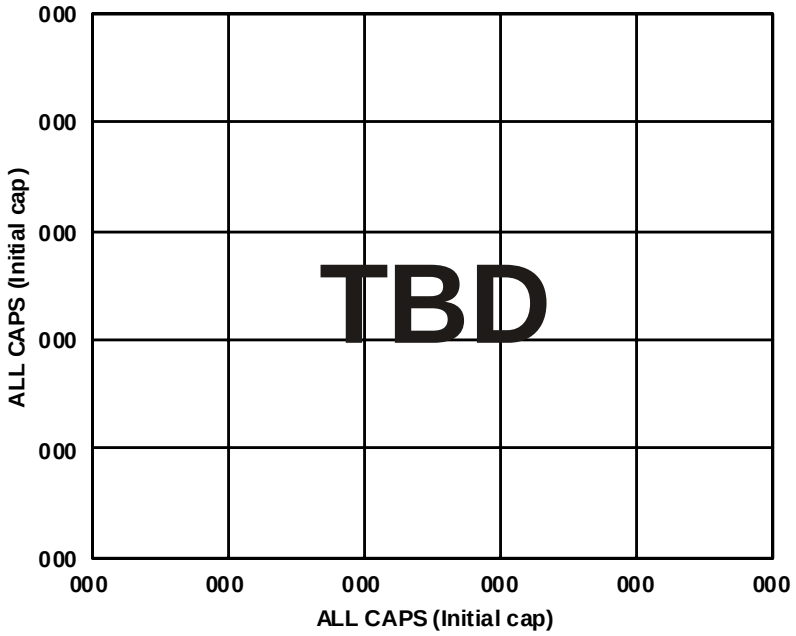


Figure 28. Power dissipation of the ADN2849 vs. bias offset and modulation voltage

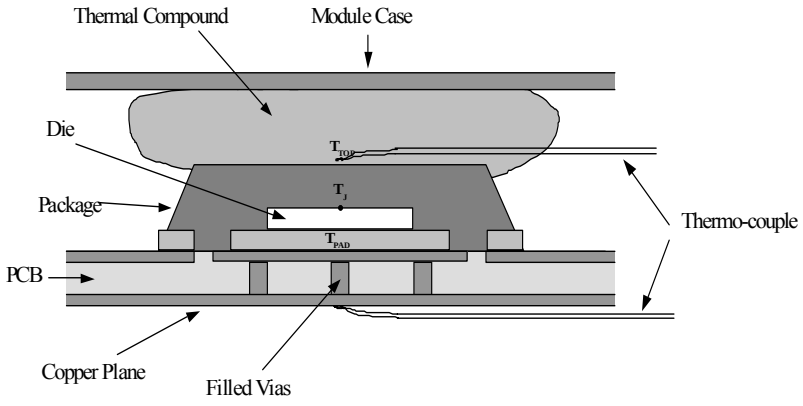


Figure 29. Typical optical module structure

The following procedure can be used to estimate the IC junction temperature.

T_{TOP} = Temperature at top of package in ^{0}C.

T_{PAD} = Temperature at package exposed paddle in ^{0}C.

T_J = IC junction temperature in ^{0}C.

P = Power disipation in W.

$\theta_{J\text{-}TOP}$ = Thermal resistance from IC junction to package top.

$\theta_{J\text{-}PAD}$ = Thermal resistance from IC junction to package exposed pad.

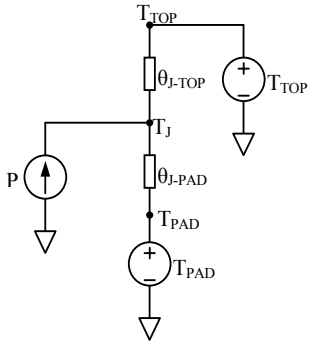


Fig. 32. Electrical model for thermal calculations

T_{TOP} and T_{PAD} can be determined by measuring the temperature at points inside the module, as shown in fig. 30. The thermocouples should be positioned so as to obtain an accurate measurement of the package top and paddle temperatures. Using this model the junction temperature can be calculated using the formula:

$$T_J = \frac{P \times (\theta_{J-PAD} \times \theta_{J-TOP}) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

Where $\theta_{J\text{-}TOP}$ and $\theta_{J\text{-}PAD}$ are given in table 3 and P is the power dissipated by the ADN2849 obtained from the graph shown in figure 28.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 31 shows the typical application circuit for the ADN2849. Applying DC voltages to the BIAS_SET and MOD_SET pins can control the Modulation and bias offset voltages. The data signal source must be connected to the DATAP and DATAN pins using 50Ω impedance transmission lines. If a reference clock signal is available, the retiming option can be enabled using the CLK_SELB input. Note that the connection between the clock signal source and the CLKP and CLKN pins must be made using 50Ω transmission lines. The cross point can be adjusted using the potentiometer R3. The modulation voltage can be enabled or disabled using the MOD_ENB pin.

The ADN2849 can operate with positive or negative (5.0V or 5.2V) supply voltage. Care should be taken to connect the GND pins to the positive rail of the supply voltage while the VEE and the exposed pad to the negative rail of the supply voltage.

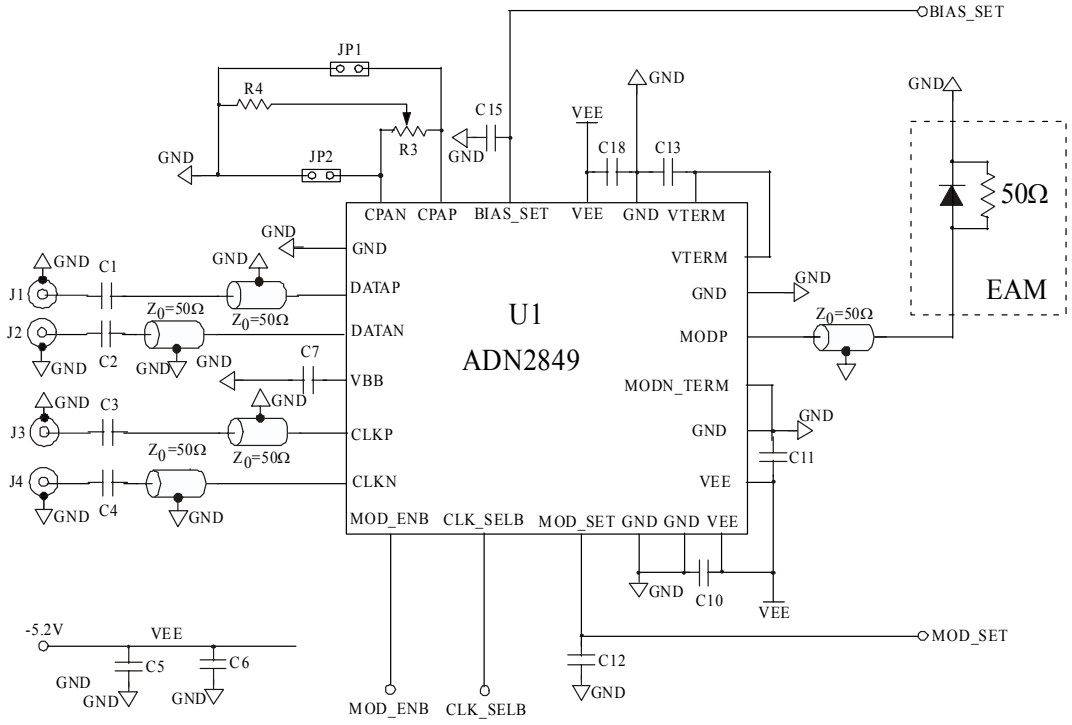


Figure 31. Typical ADN2849 application circuit

PCB LAYOUT GUIDELINES

Due to the high frequencies at which the ADN2849 operates, care should be taken when designing the PCB layout in order to obtain optimum performance. It is recommended to use controlled impedance transmission lines for the high-speed signal paths The length of the transmission lines must be kept to a minimum to reduce losses and pattern dependant jitter. All the VEE and GND pins must be connected to solid copper planes using low inductance connections. When the connections are made through vias, multiple vias can be connected in parallel to reduce the parasitic inductance. The VTERM, VBB, MODN_TERM and VEE pins must be locally decoupled with high quality capacitors. If proper decoupling cannot be achieved using a single capacitor, the user can use multiple capacitors in parallel for each GND pin. A 20µF tantalum capacitor must be used as general decoupling capacitor for the entire module The exposed pad should be connected to the most negative rail of the supply voltage using filled vias so that solder does not leak through the vias during reflow. Using filled vias under the package greatly enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

DESIGN EXAMPLE

This section describes a design example that covers the followings:

- Headroom calculation for the required bias offset and modulation voltages
- Required voltage range at the BIAS_SET and MOD_SET pins to generate the required bias offset and modulation voltages

This design example assumes a -5.2V supply voltage, 0.5V bias offset voltage and 2V modulation voltage.

Headroom calculations

In order to operate properly, the bias offset and modulation voltages must satisfy the following condition:

$$V_{Modulation} + V_{Bias\,Offset} \le |VEE| - V_{MODP\,min}$$

Assuming that $V_{MODPmin}$=1.7V (see table1), the above condition became:

$$2.5V \le 5.2 - 1.7 = 3.5V$$

BIAS_SET voltage range

The voltage range at the BIAS_SET pin to generate 0.5V bias offset voltage at the MODP pin can be calculated using the BIAS_SET voltage to bias offset voltage gain specification from table1 using the formulae:

$$V_{BIAS_SET\,min} = \frac{V_{BIAS\ OFFSET}}{K_{max}}$$

$$V_{BIAS_SET\,max} = \frac{V_{BIAS\ OFFSET}}{K_{min}}$$

Where K_{min} and K_{max} are the minimum and maximum values of the BIAS_SET voltage to offset bias voltage gain from table1.

Substituting the values the BIAS_SET voltage range is 0.45V to 0.55V.

MOD_SET voltage range

The voltage range at the MOD_SET pin to generate 2V bias offset voltage at the MODP pin can be calculated using the MOD_SET voltage to bias offset voltage gain specification from table1 using the formulae:

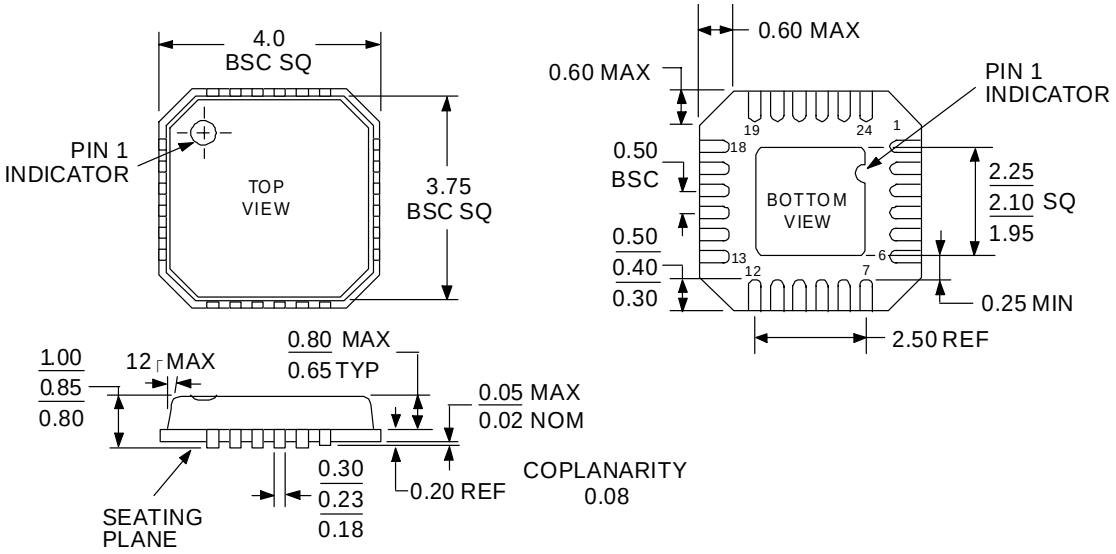
$$V_{MOD_SET\,min} = \frac{V_{MODULATION}}{K_{max}}$$

$$V_{MOD_SET\,max} = \frac{V_{MODULATION}}{K_{min}}$$

Where K_{min} and K_{max} are the minimum and maximum values of the MOD_SET voltage to offset bias voltage gain from table1.

Substituting the values the MOD_SET voltage range is 1.05V to 1.33V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

Figure 32. 24-Lead Lead Frame Chip Scale Package (LFCSP) 4mm×4mm Body (CP-24)

Dimensions shown in millimeters

PR04323-0-9/04(PrG)

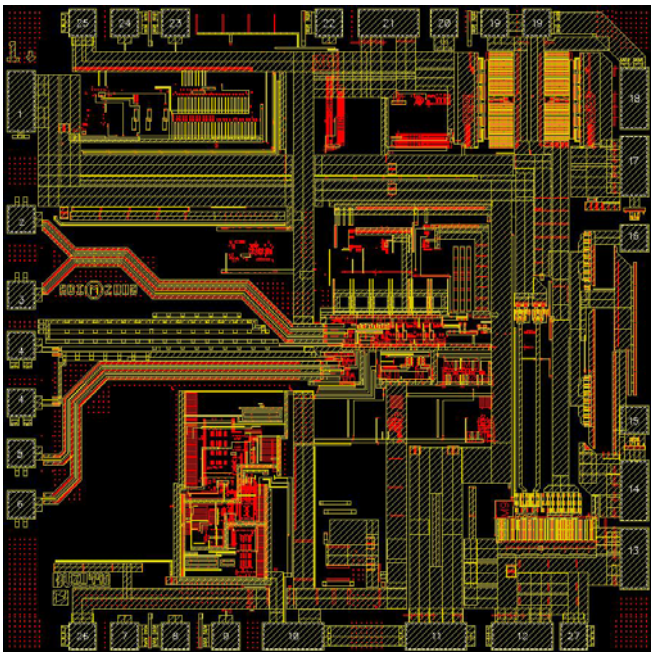


Figure 33. ADN2849 metallization photograph

Table 9. Die pad coordinates

Pad Number	X(µm)	Y(µm)
1	-920.50	685.00
2	-920.50	331.55
3	-920.50	103.05
4	-920.50	-48.75
4	-920.50	-220.15
5	-920.50	-371.95
6	-920.50	-525.55
7	-609.10	-920.50
8	-457.30	-920.50
9	-305.50	-920.50
10	-103.70	-920.50
11	324.85	-920.50
12	584.00	-920.50
13	920.50	-688.20
14	920.50	-484.20
15	920.50	-271.10
16	920.50	274.50
17	920.50	490.00
18	920.50	694.00
19	628.00	920.50
19	501.10	920.50
20	349.30	920.50
21	182.40	920.50
22	3.50	920.50
23	-457.30	920.50
24	-609.10	920.50
25	-736.00	920.50
26	-736.00	-920.50
27	738.00	-920.50

Note: The coordinates are measured between the center of the die and the center of the pad.